

LCFC Confidential


G Project M/B Schematics Document

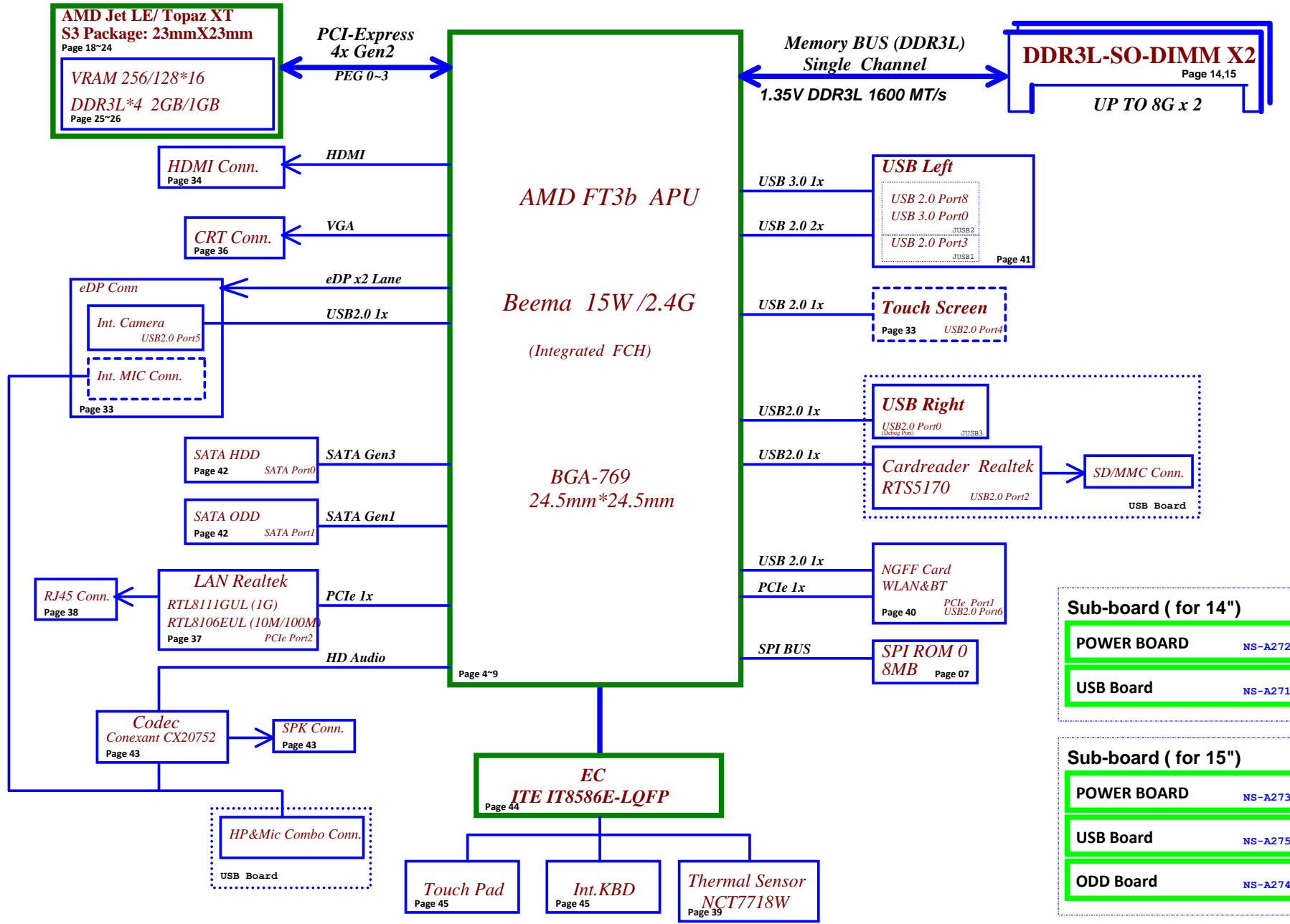
AMD FT3B Beema SOC with DDRIIL

AMD JET-LE

2014-1-3

REV: 0.3

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/15	Deciphered Date	2013/08/15	Cover Page		
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Voltage Rails (O --> Means ON , X --> Means OFF)

State	power plane	B+	+5VALW +3VALW +3VL	+1.35V (+VSYSMEN)	+1.8VALW +0.95VALW	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.675VS +APU_CORE +APU_CORE_NB +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0		O	O	O	O	O
S3		O	O	O	O	X
S5 S4/AC		O	O	X	X	X
S5 S4/ Battery only		O	X	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID need to be update!

BOARD Config.	GPIOxx	GPIOxx	GPIOxx	Function
	0	0	0	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
EHCI		0	RIGHT USB (2.0)
		1	N/A
		2	Card Reader
		3	LEFT USB (2.0)
		4	Touch Screen
		5	Camera
		6	Blue Tooth
xHCI		0	N/A
		1	LEFT USB (3.0)
		8	N/A
		9	N/A

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU ID part
8106EUL@	8106EUL LAN part
8111GUL@	8111GUL LAN part
GIGA@	Giga LAN Part
TS@	Touch Screen part
ZODD@	Zero Power ODD part
AOAC@	AOAC support part
HDT@	HDT Debug part
Kabini@	Kabini APU part
SDV@	SDV PWR part
S2G@	X76 SAMSUNG 2G
M2G@	X76 MICRON 2G
H2G@	X76 HYNIX 2G
S1G@	X76 SAMSUNG 1G
M1G@	X76 MICRON 1G
H1G@	X76 HYNIX 2G

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	IT8586E +3VALW	X	X	X	X APU_SIC APU_SID	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VS_VGA	X	IT8586E +3VS	X	X	V	V APU_SIC APU_SID	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X	APU +3VS	X

PCIE PORT LIST

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	
	1	GPU
	2	
	3	

VRAM

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Battery	0X16	Thermal Sensor	1001_100xb
Charger	0001_0010 b	GPU	0x41(default)
		APU Thermal Diode	TBU

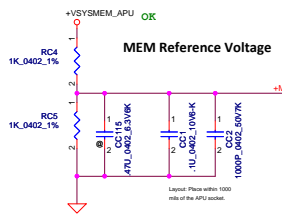
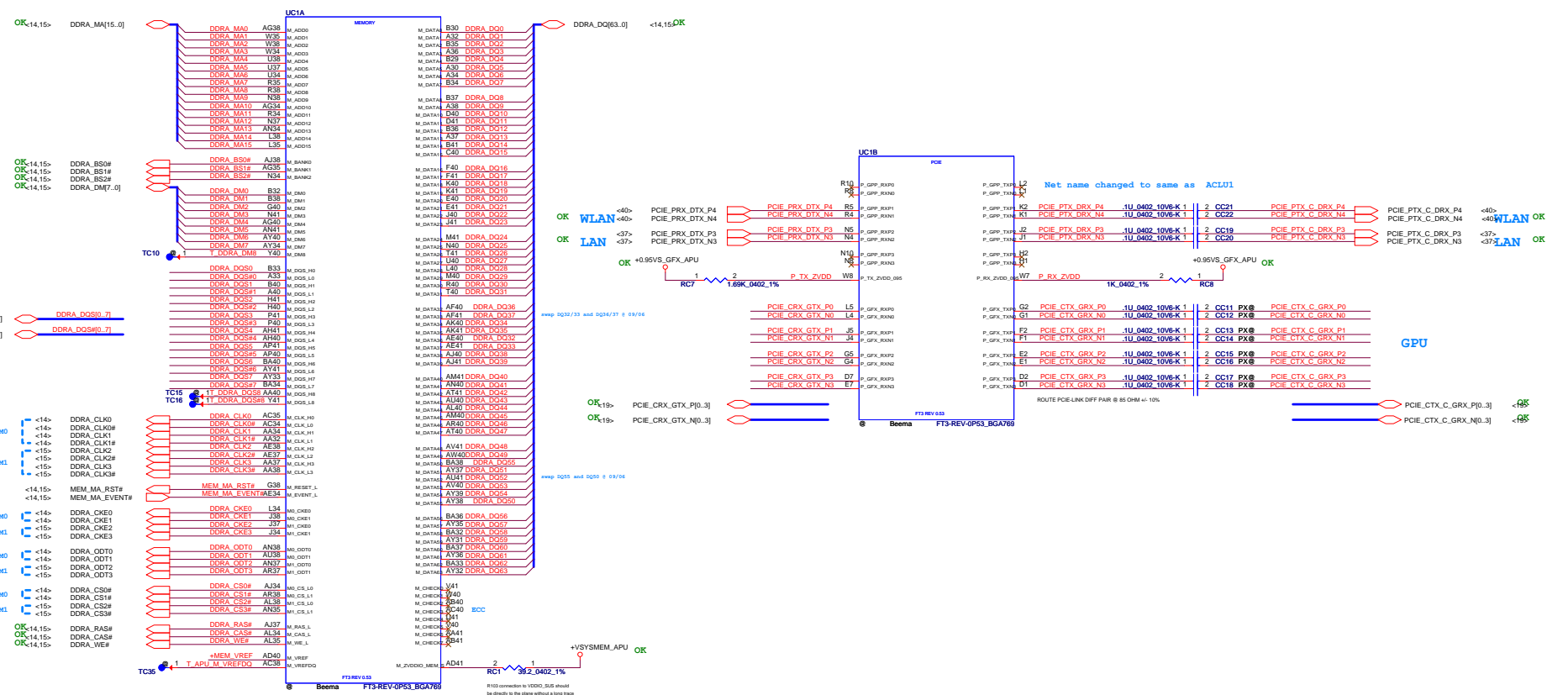
APU SM Bus address

Device	Address
DDR DIMMA	1001_000Xb
DDR DIMMB	1001_010Xb
WLAN	RSVD

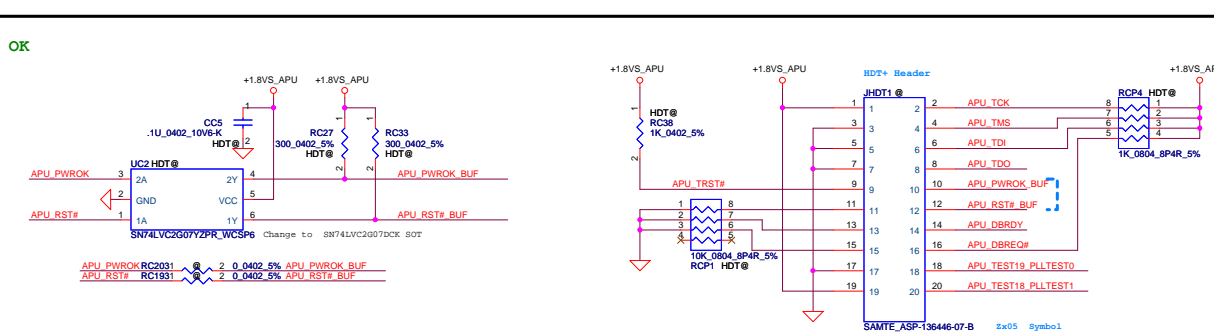
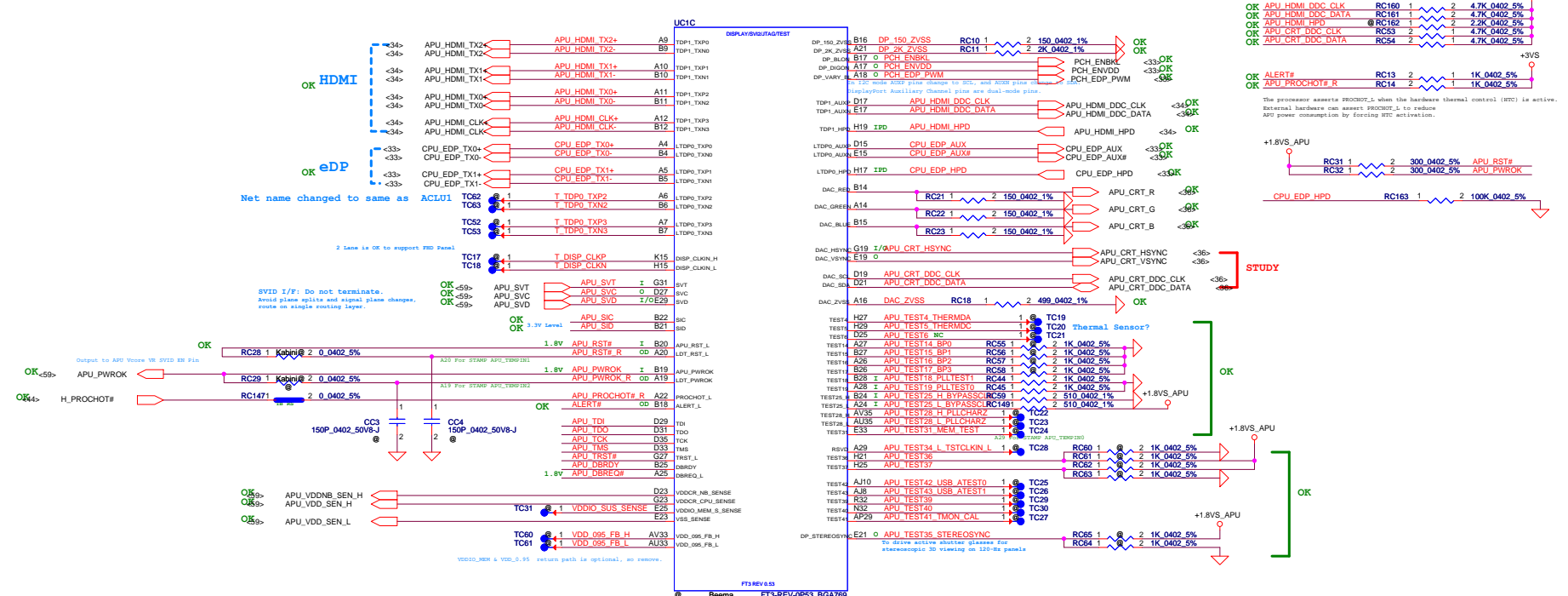
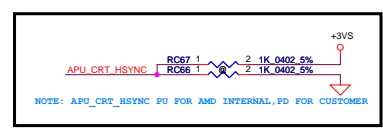
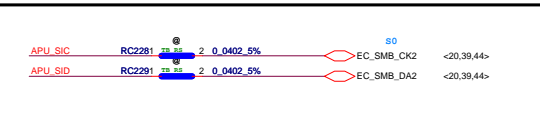
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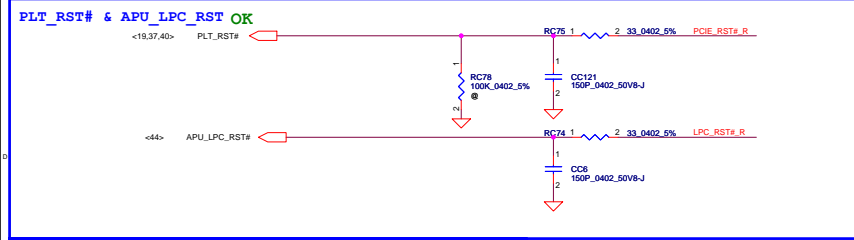
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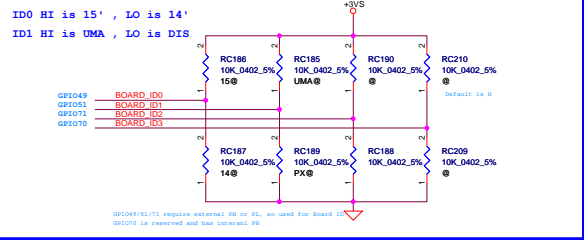
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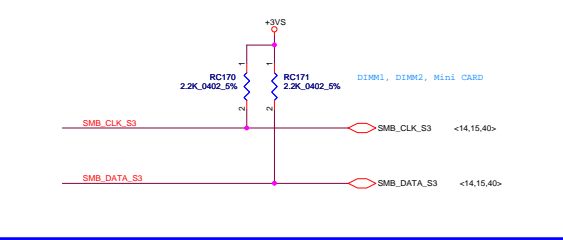
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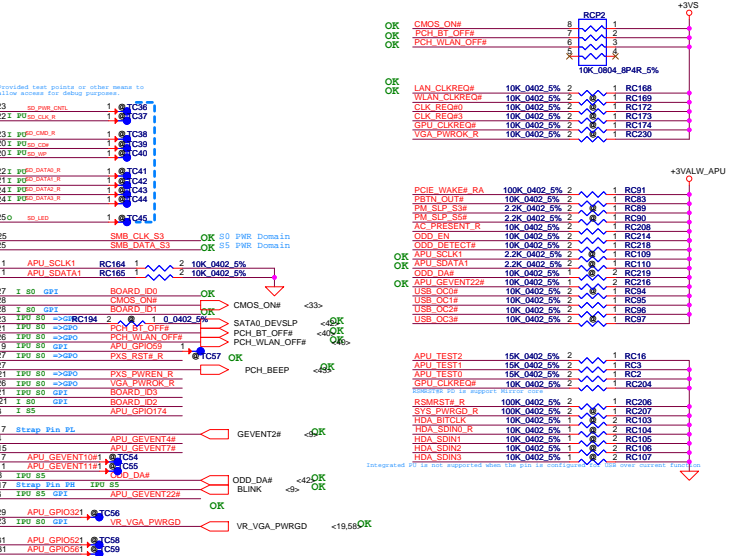
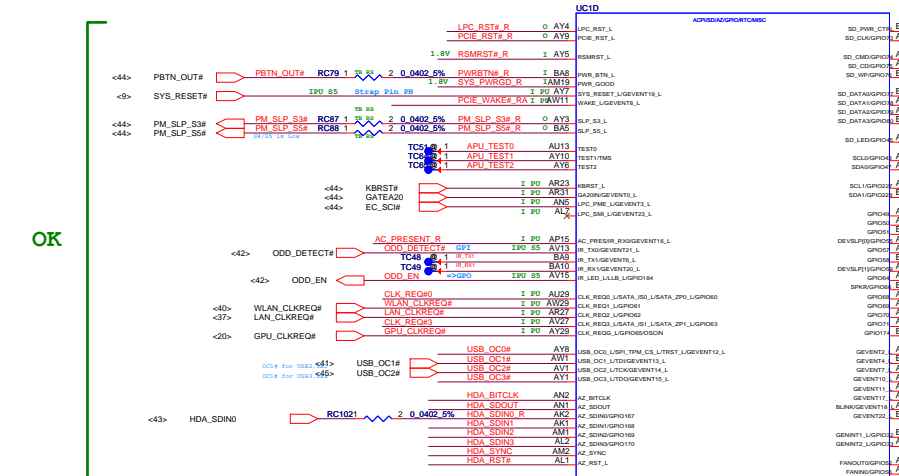
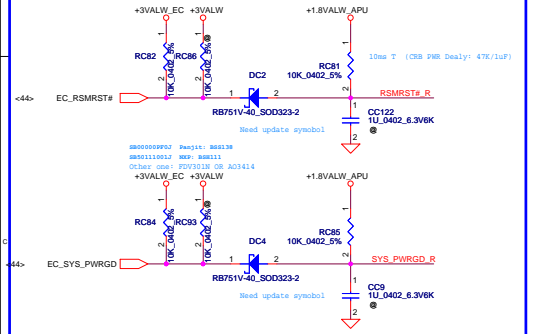
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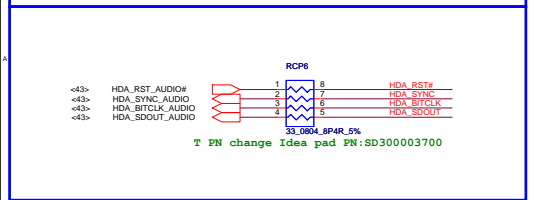
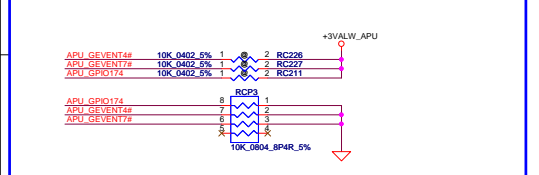
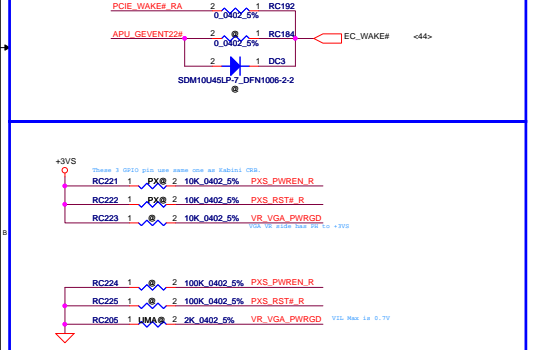
SMB_CLK_S3 OK



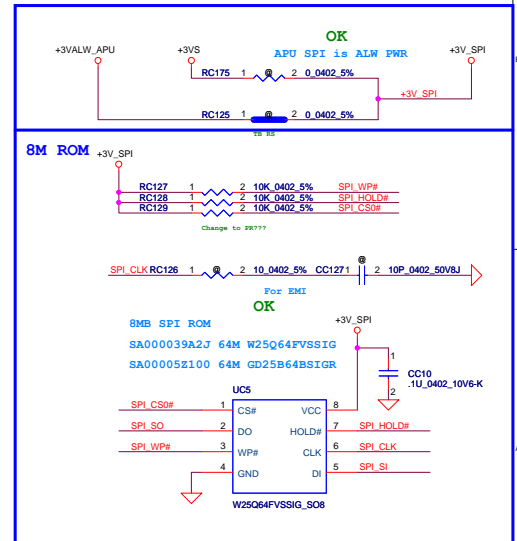
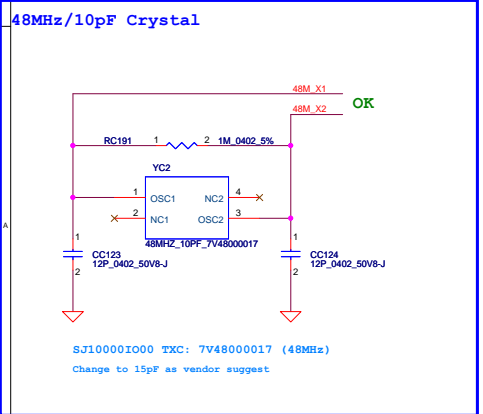
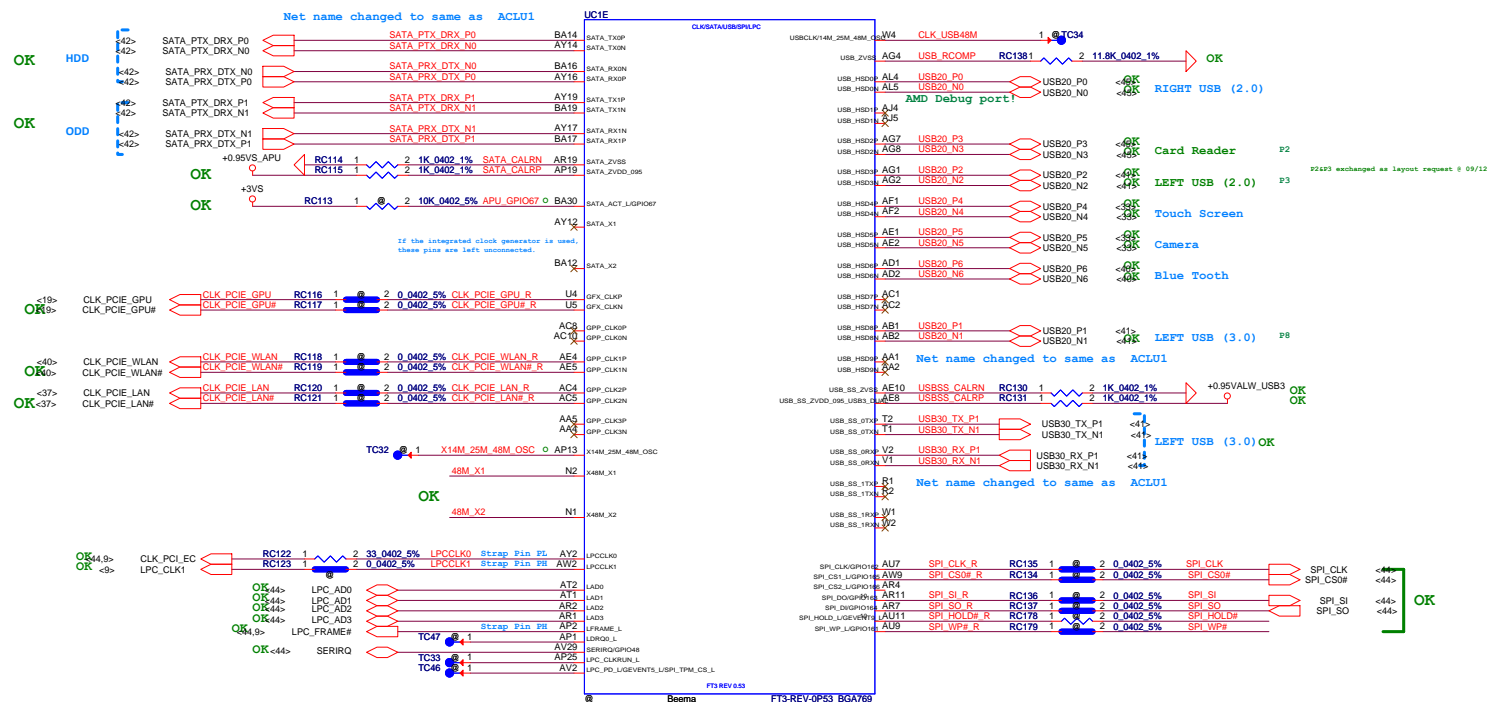
RSRST# OK



EC_WAKE# OK



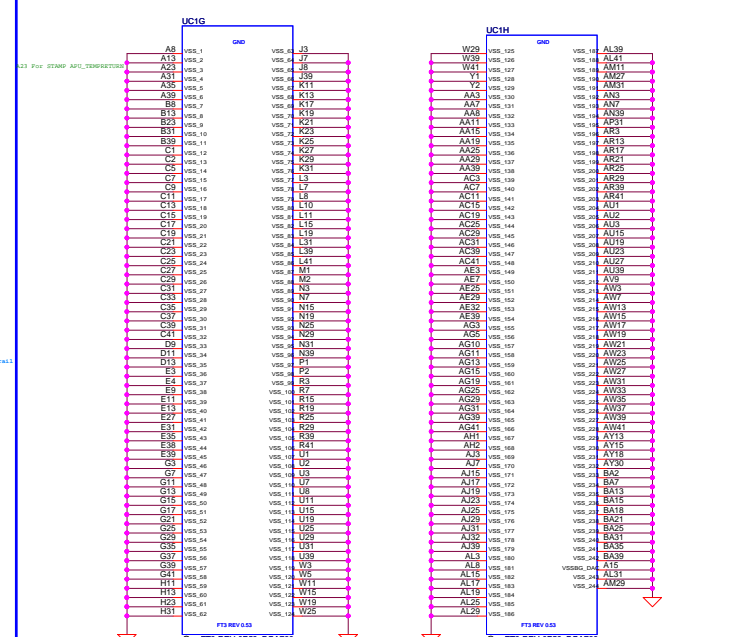
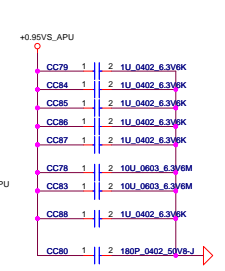
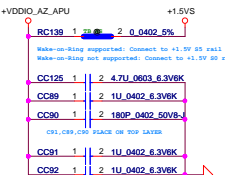
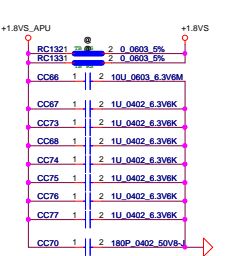
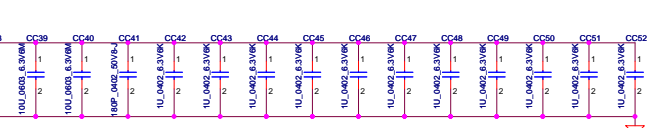
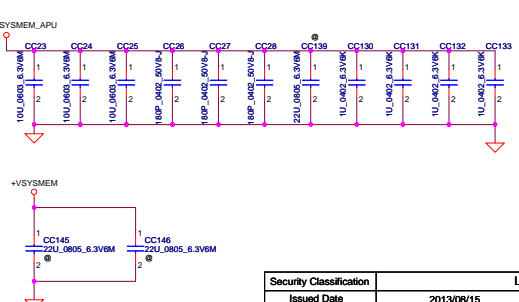
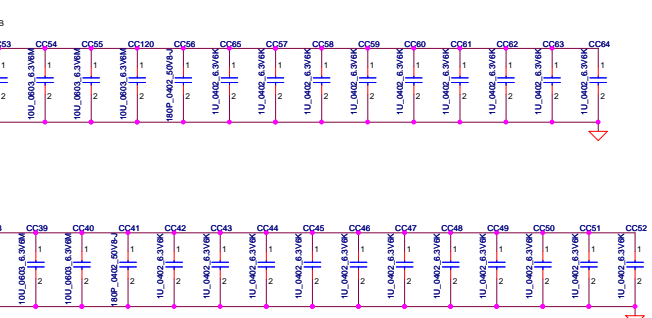
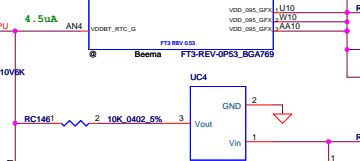
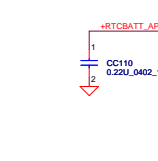
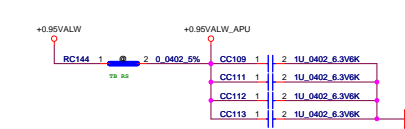
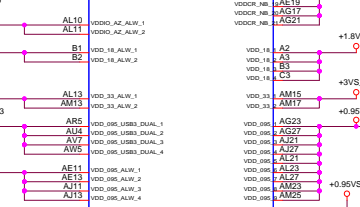
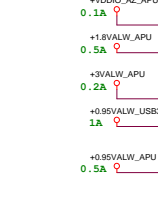
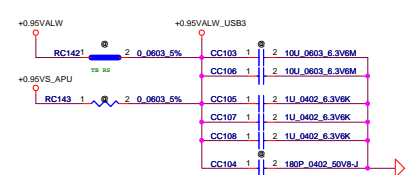
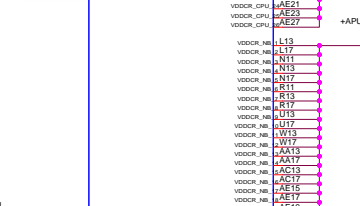
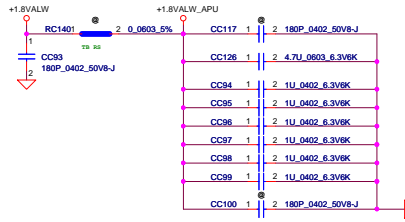
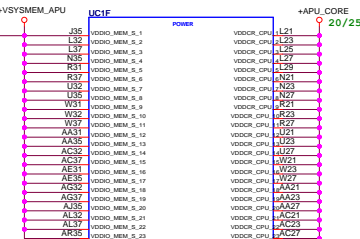
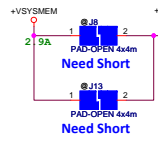
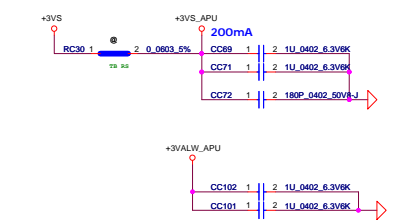
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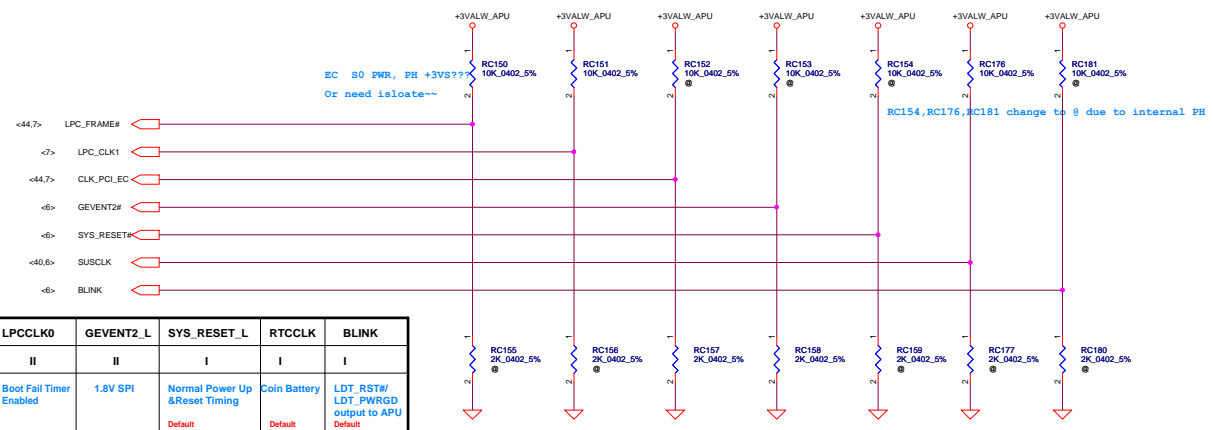


All RLC follow CRB, need double check with DG.



SA000063Q00 BCD: AP2138N-1.5TRG1
 SA000063000 ANPEC: AP1510215AITRG

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STRAP PINS

Signal	LFRAME_L	LPCCCLK1	LPCCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	1.8V SPI	Normal Power Up & Reset Timing Default	Coin Battery Default	LDT_RST#/LDT_PWRGD output to APU Default
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled Default	3.3V SPI Default	Reserved	Direct DC	Reserved

Type I straps become valid immediately after capture with the rising edge of RSMRST_L.
 Type II straps become valid after PWR_GOOD is asserted.
 All Strap pins must be configured with either external pull-up or pull-down resistors.

5

4

3

2

1

D

D

C


C

B

B

A

A

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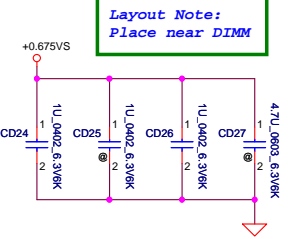
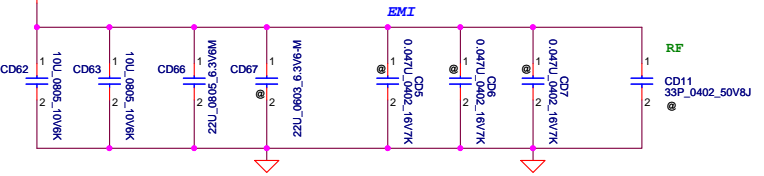
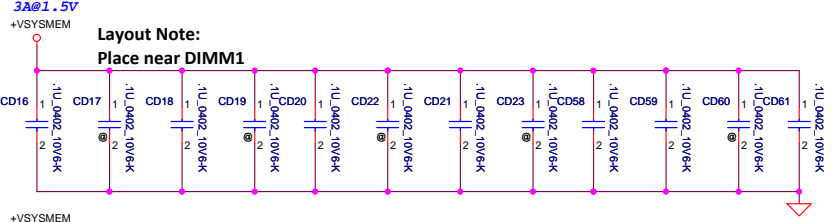
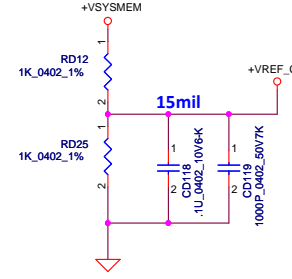
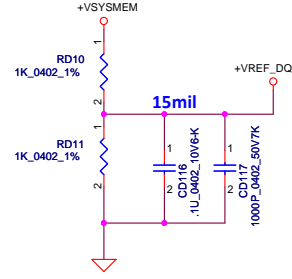
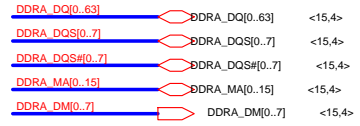
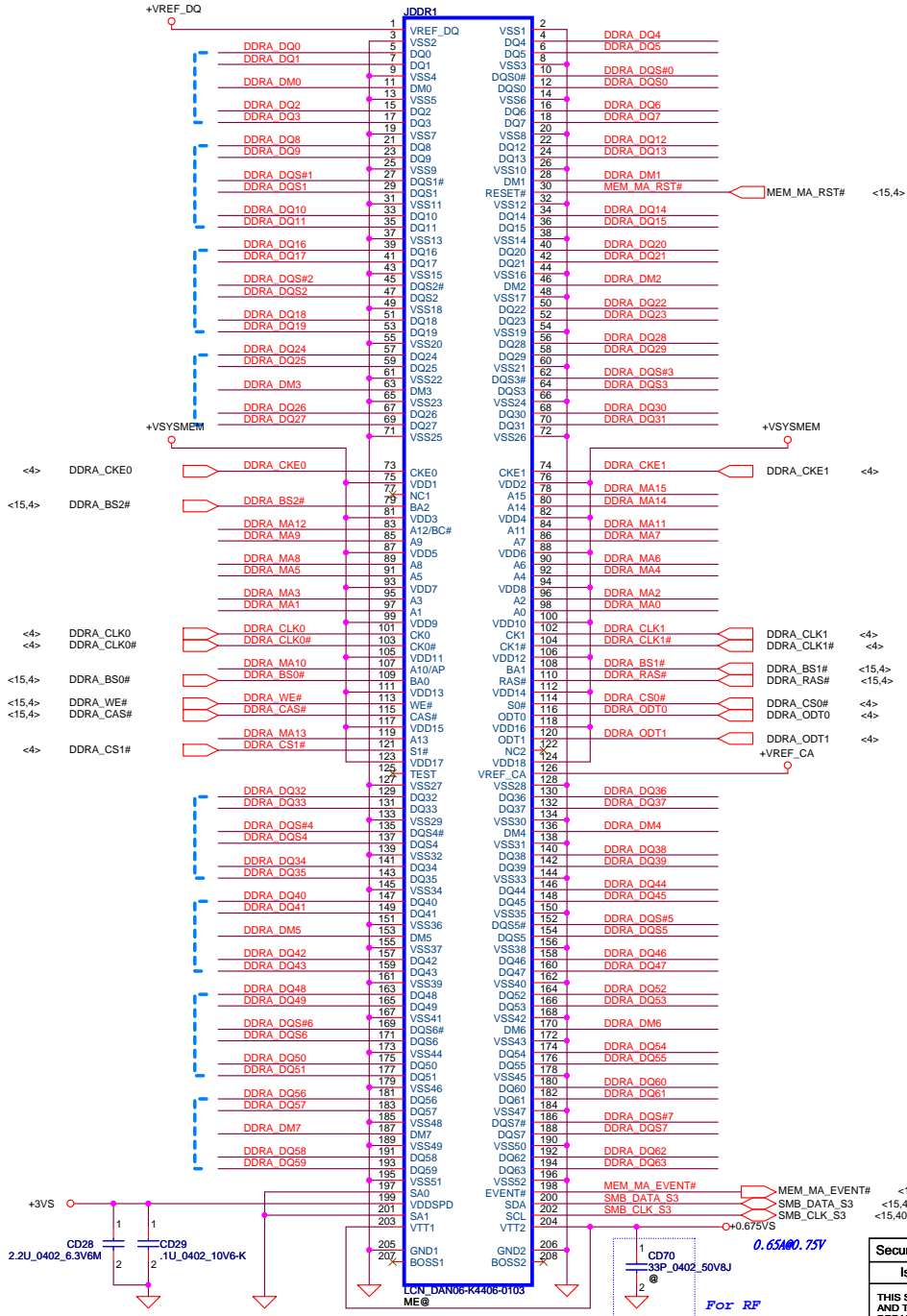
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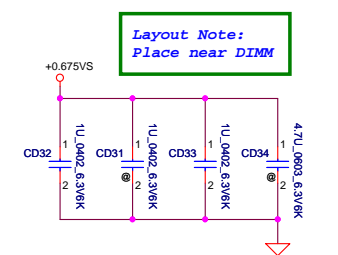
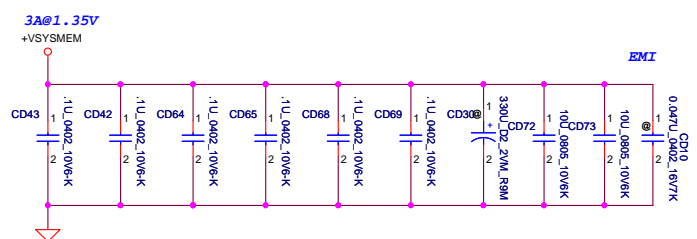
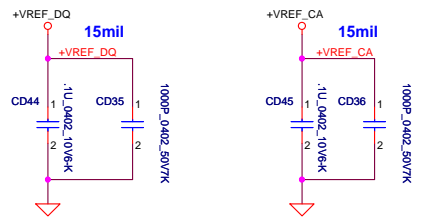
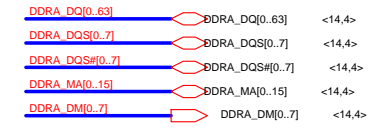
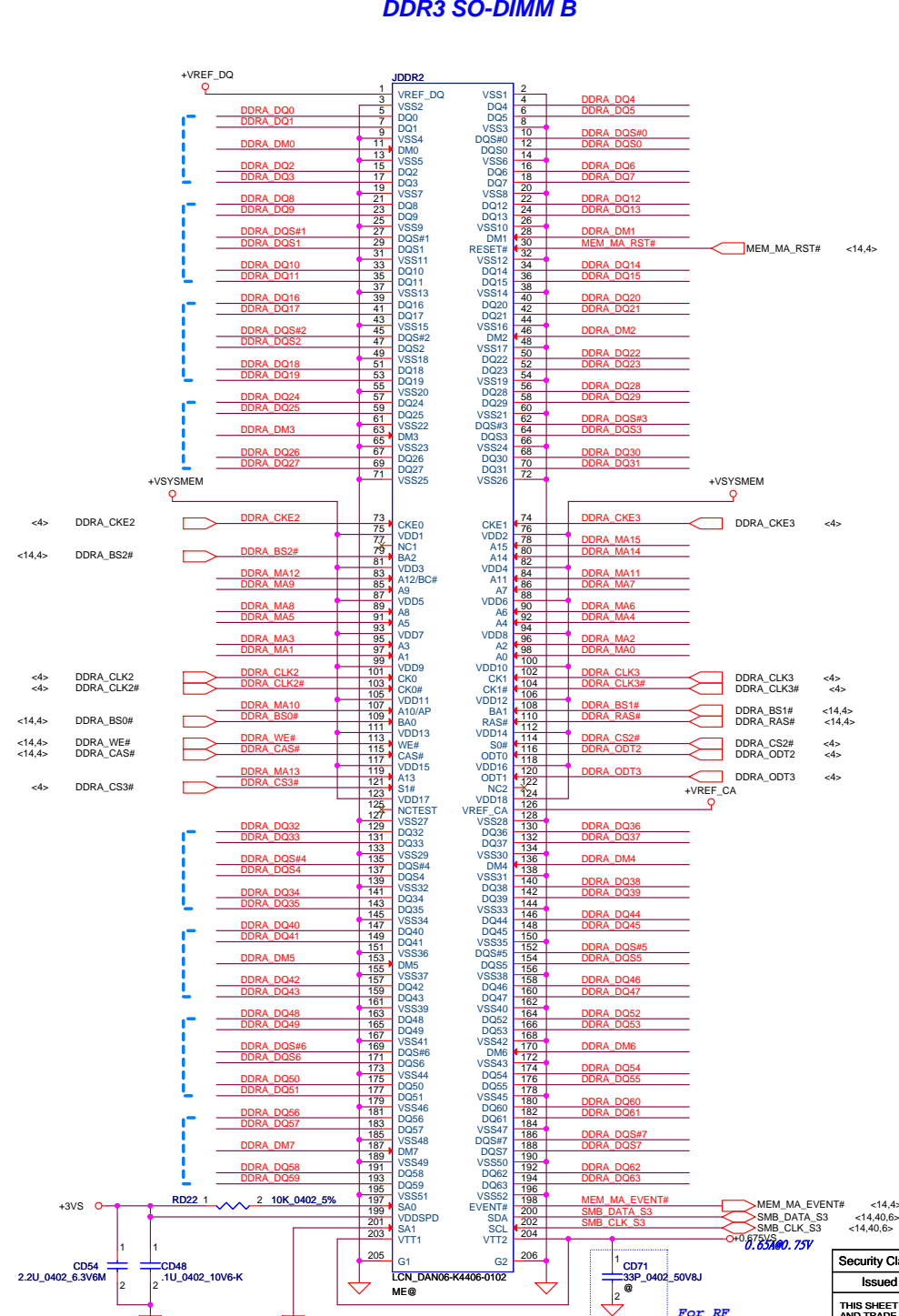
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DDR3 SO-DIMM A



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			Sheet 14 of 60

DDR3 SO-DIMM B




Layout Note:
Place near DIMM

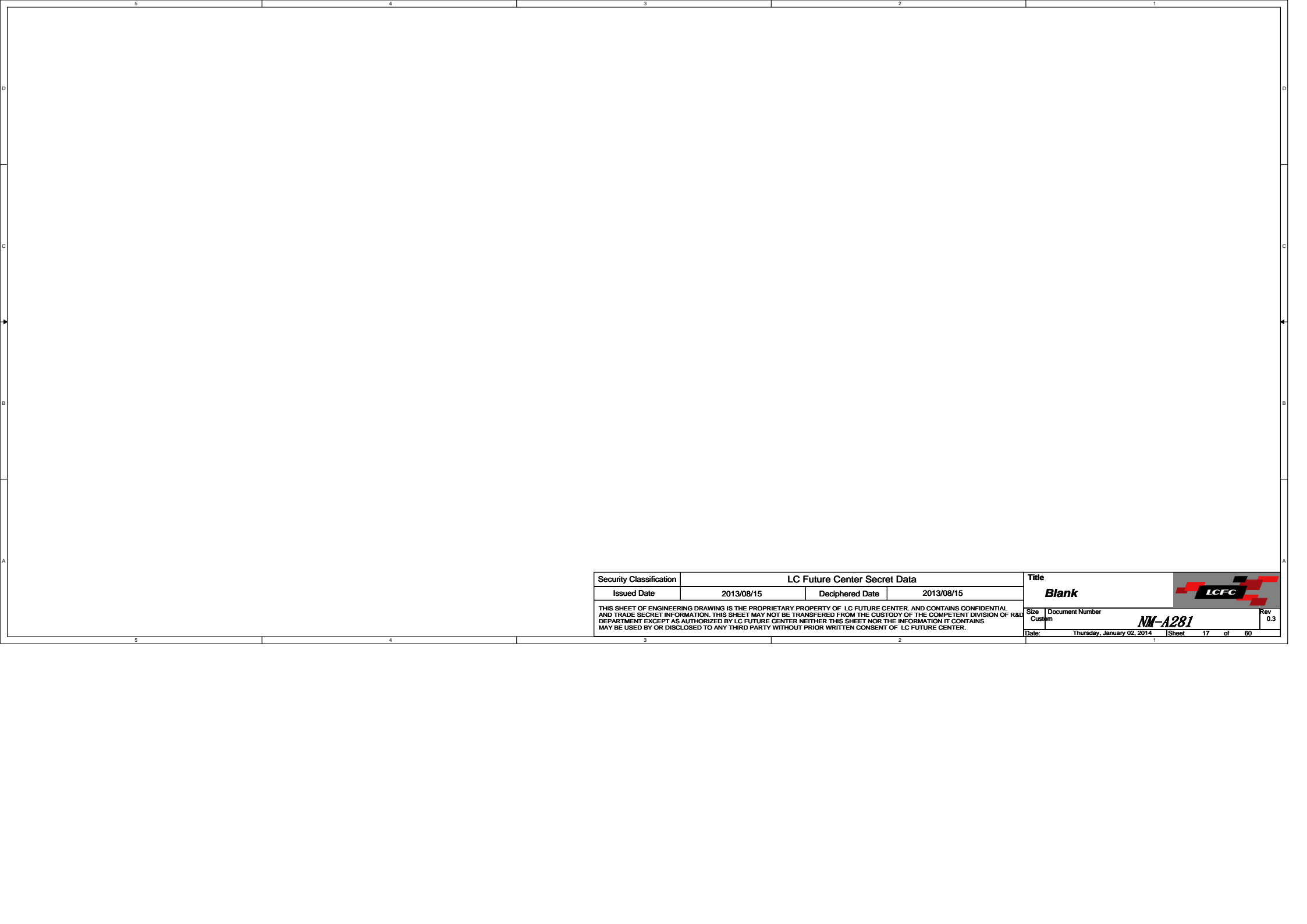
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Issued Date	2013/08/15	Deciphered Date
		2013/08/15


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VGA Note list need to be update!

Power-Up/Down Sequence

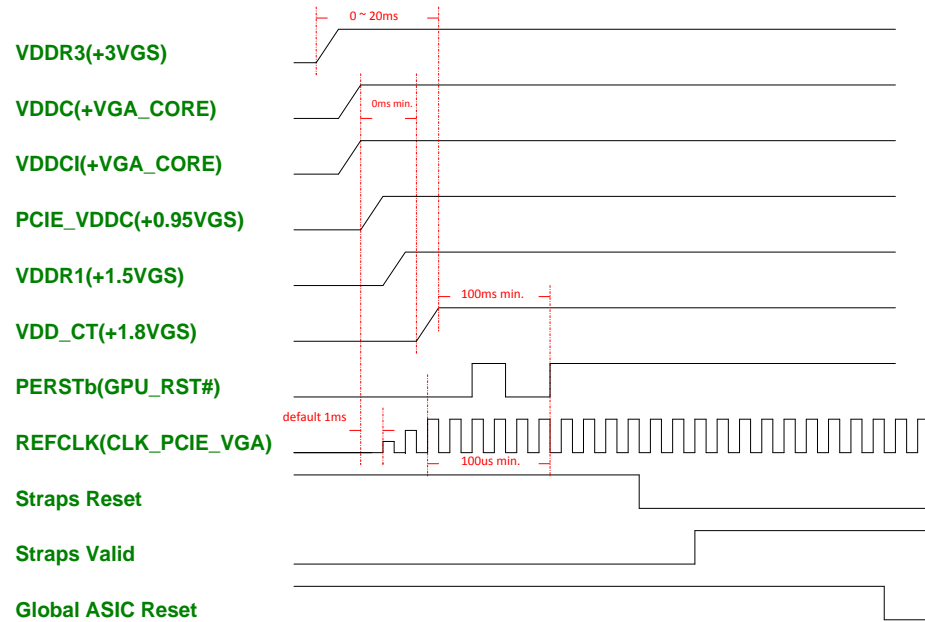
"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

For power down, reversing the ramp-up sequence is recommended.

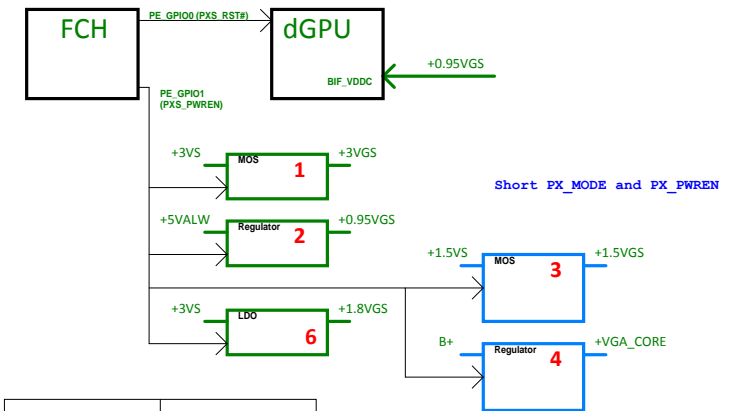


Without BACO option :

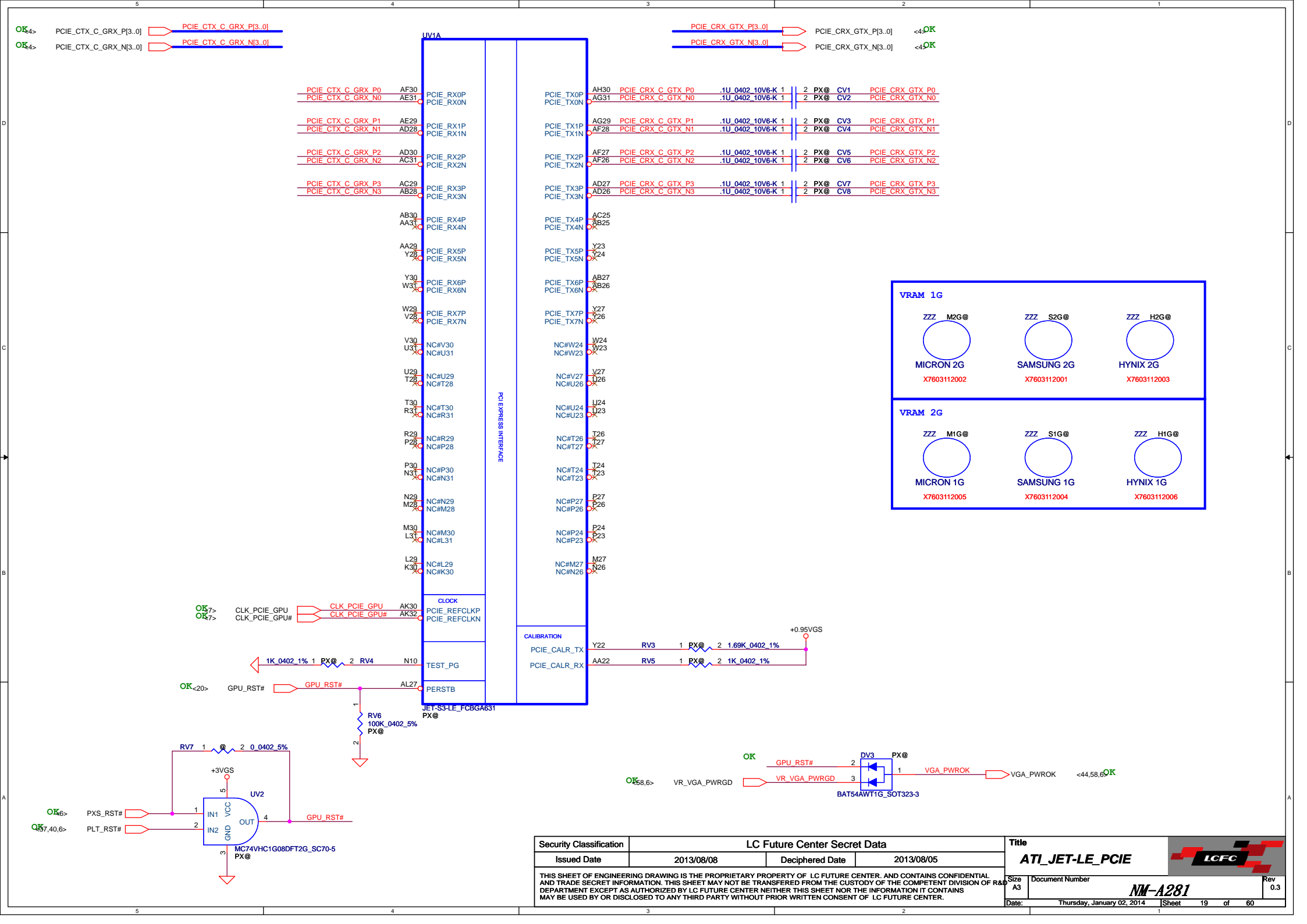
PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
 PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDR, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1D1	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

PX5.5

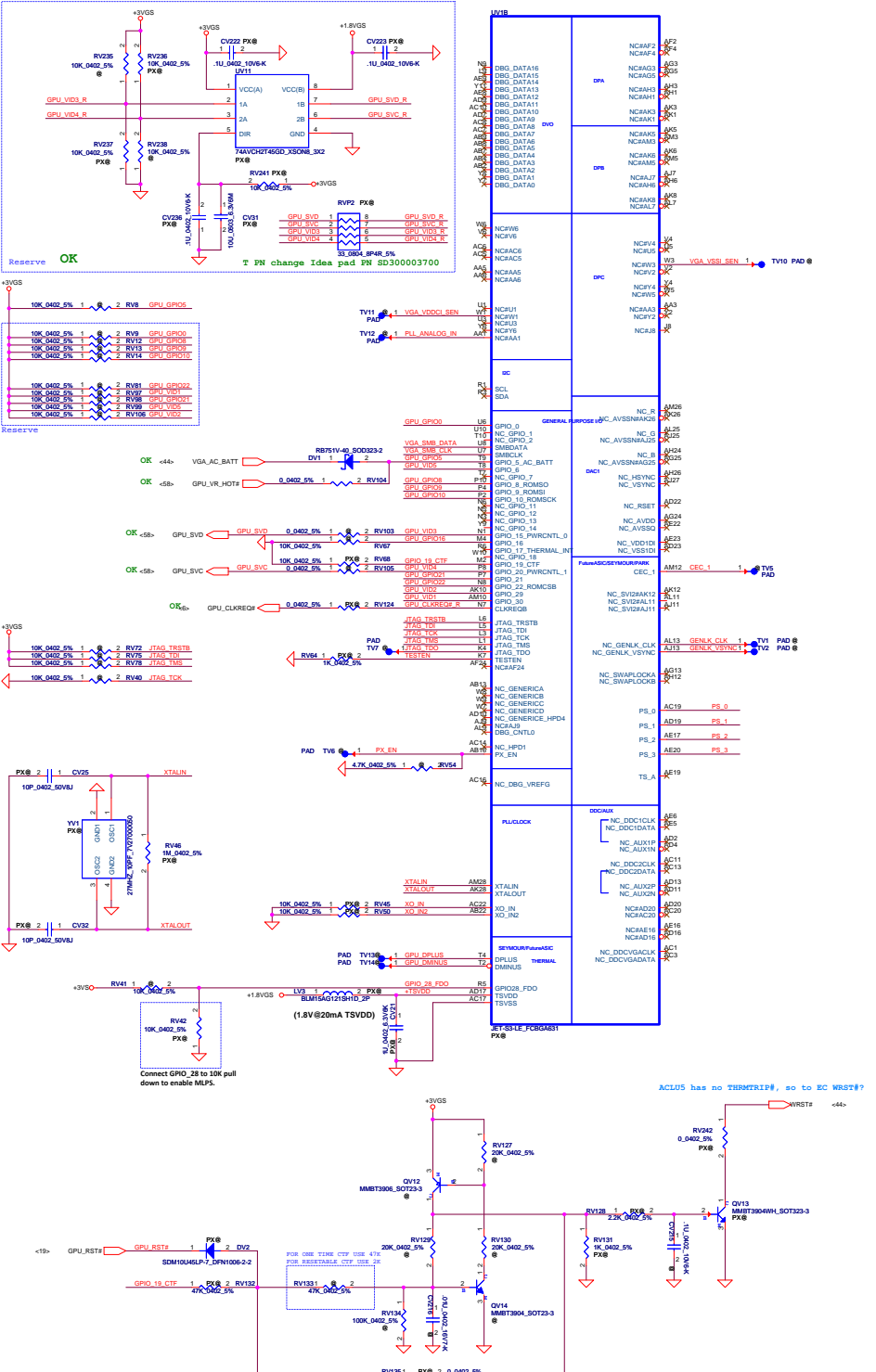


Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192



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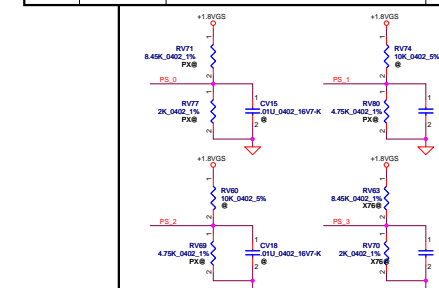
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ATI_JET-LE_PCIE	
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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

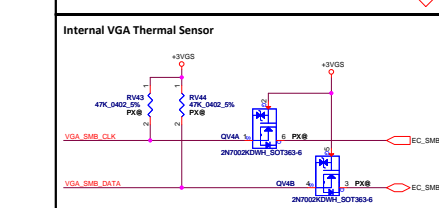
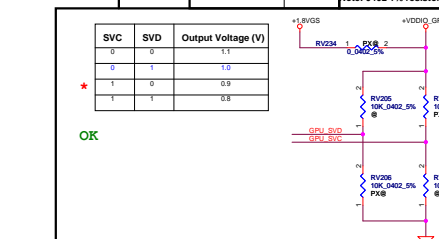
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[2]	ROM_CONFIG[1]	Define the primary memory capacity size when STRAP_BIOS_ROM_EN = 0.	100 = 256MB
PS_0[3]	ROM_CONFIG[2]		
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[6]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	X
PS_1[1]	STRAP_BIF_CLK_PMLEN	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	0 = Not support
PS_1[2]	STRAP_BIF_CLK_PMLEN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter half swing is enabled. 1 = The transmitter full swing is enabled.	1
PS_1[5]	STRAP_TX_DEEMPHLEN	0 = Tx deemphases disabled. 1 = Tx deemphases enabled.	1 = Enable
PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capability enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap options such as for memory ID	X
PS_3[2]	BOARD_CONFIG[1]	10 = Hynix IG 11 = Micron IG 12 = Samsung IG	
PS_3[3]	BOARD_CONFIG[2]	00 = Samsung IG 01 = Samsung IG	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be generated for the OS and user. (Combine with PS_0[6])	X
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	111 = No usable endpoints. 101 = One usable endpoint. 100 = Two usable endpoints. 011 = Three usable endpoints. 010 = Four usable endpoints. 001 = Five usable endpoints. 000 = Six usable endpoints. 000 = All endpoints are usable.	



MLPS	Bit				BOM			
	5	4	3	2	1	R_pu (Ω)	R_pd (Ω)	C (nF)
PS_0 [5:1]	1	1	0	0	1	RV71=8.45k	RV77=2k	CV15=NC
PS_1 [5:1]	1	1	0	0	0	RV74=NC	RV90=4.75k	CV16=NC
PS_2 [5:1]	1	1	0	0	0	RV77=4.75k	RV97=4.75k	CV18=NC
PS_3 [5:1]	1	1	0	0	0	RV99=NC	RV98=4.75k	CV19=NC
PS_3 [5:1]	1	1	X	X	X	RV60=X76	RV69=X76	CV16=X76
PS_3 [5:1]	1	1	X	X	X	RV60=X76	RV69=X76	CV16=X76

R_pu (Ω)	R_pd (Ω)	Bits [5:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4900	011
4530	4900	100
680	50	3240 5620
82	51	3400 10000
10	10	4750 NC 111

Note: 0402 1% resistors are required



UV1F

NC_VARY_BL
NC_DIGON

AB11
AB12

NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P
NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P

AL15
AK14
AH16
AJ15

NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P
NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P

AL17
AK16
AH18
AJ17

NC_TXOUT_L3P
NC_TXOUT_L3N

AL19
AK18

TMDP

NC_UPHYAB_TMDPB_TX0N
NC_UPHYAB_TMDPB_TX0P
NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P

AH20
AJ19
AL21
AK20


NC_UPHYAB_TMDPB_TX2N
NC_UPHYAB_TMDPB_TX2P
NC_UPHYAB_TMDPB_TX3N
NC_UPHYAB_TMDPB_TX3P

AH22
AJ21
AL23
AK22

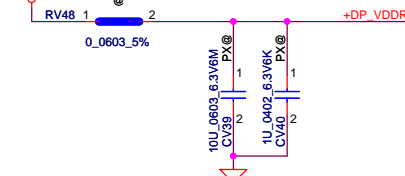
NC_TXOUT_U3P
NC_TXOUT_U3N

AK24
AJ23

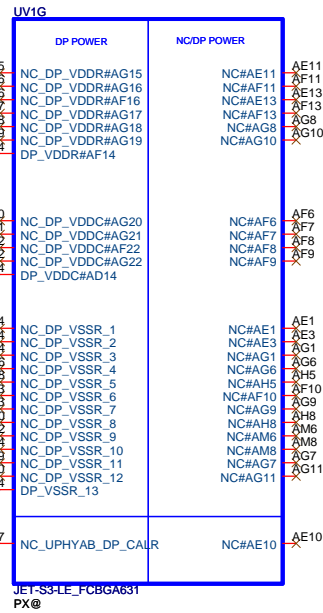
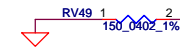
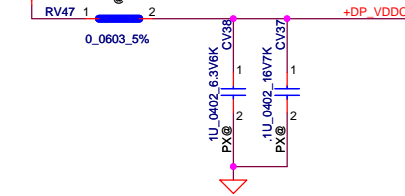
JET-SS-LE_FCBGA631
PX@

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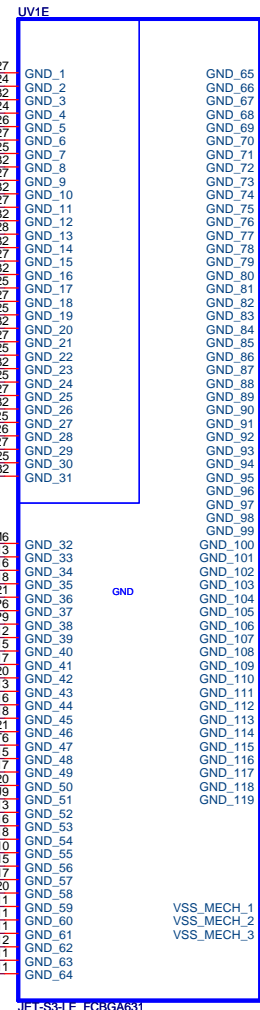
+1.8VGS @ (1.8V@425mA DP_VDDR)



+0.95VGS @ (0.95V@560mA DP_VDDC)



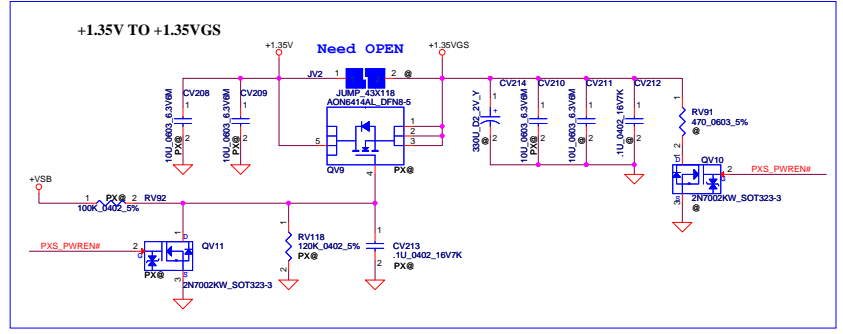
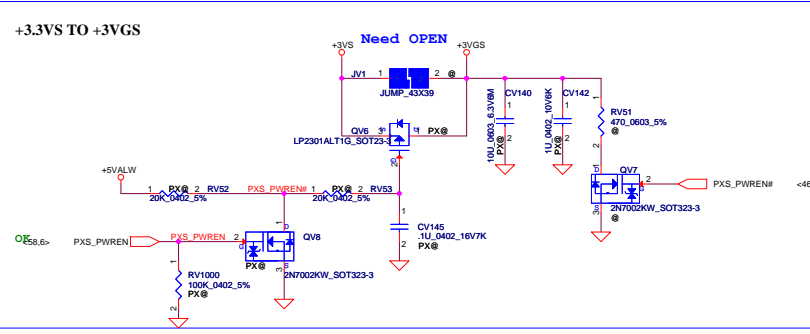
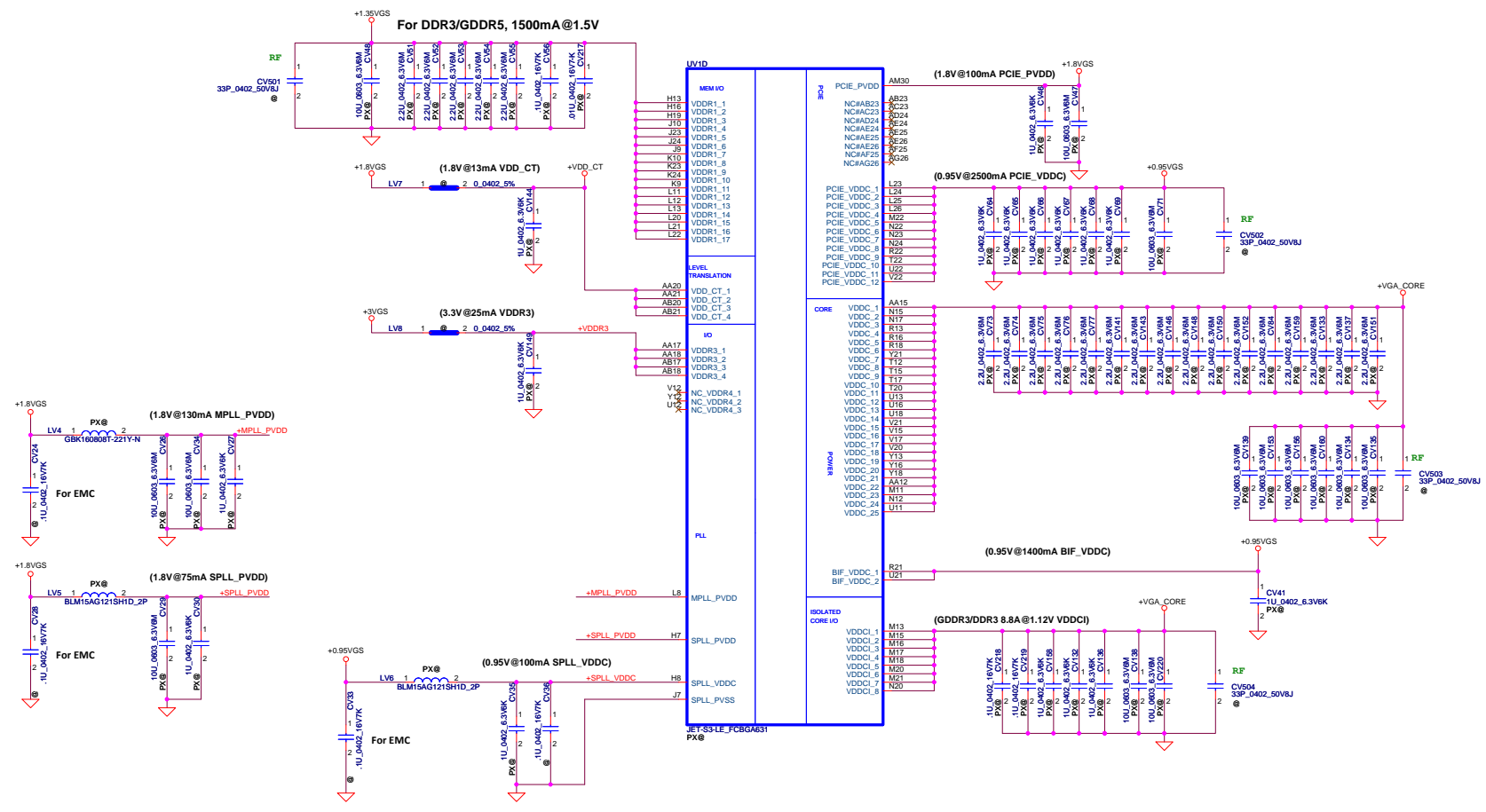
JET-S3-LE_FCBGA831 PX@



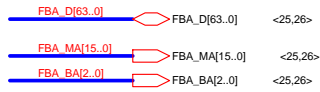
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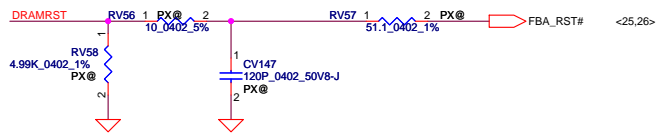
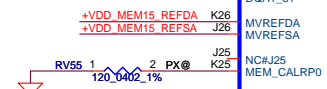
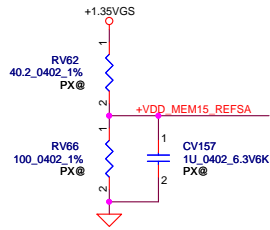
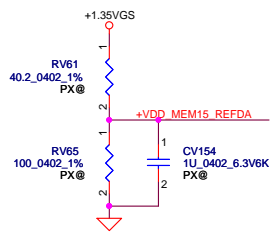
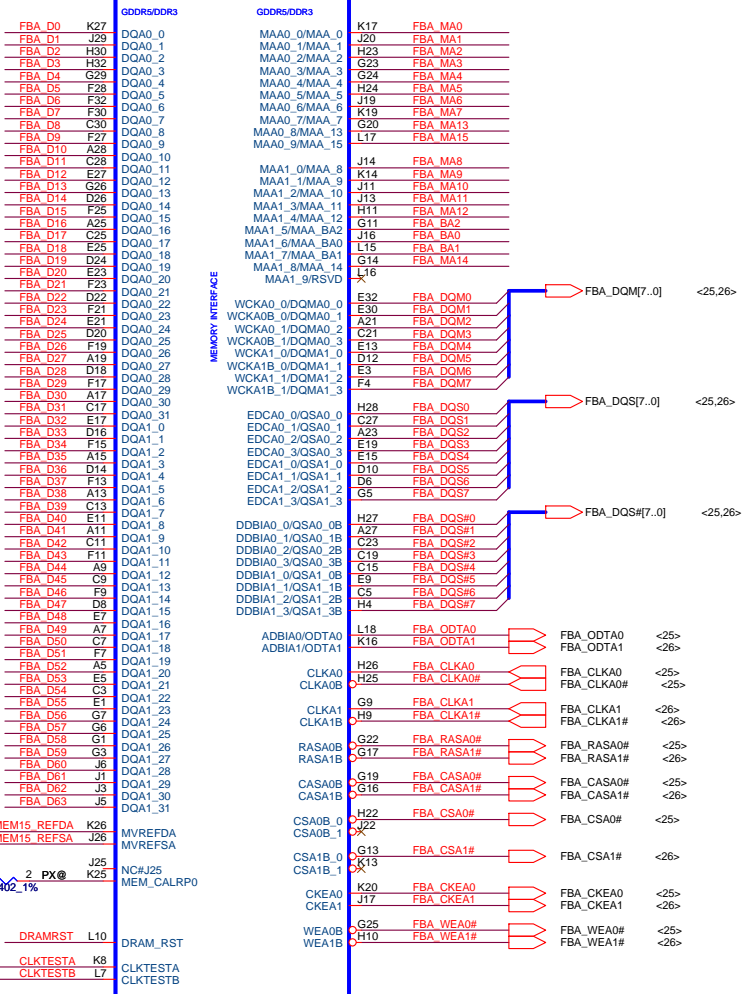
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UVIC

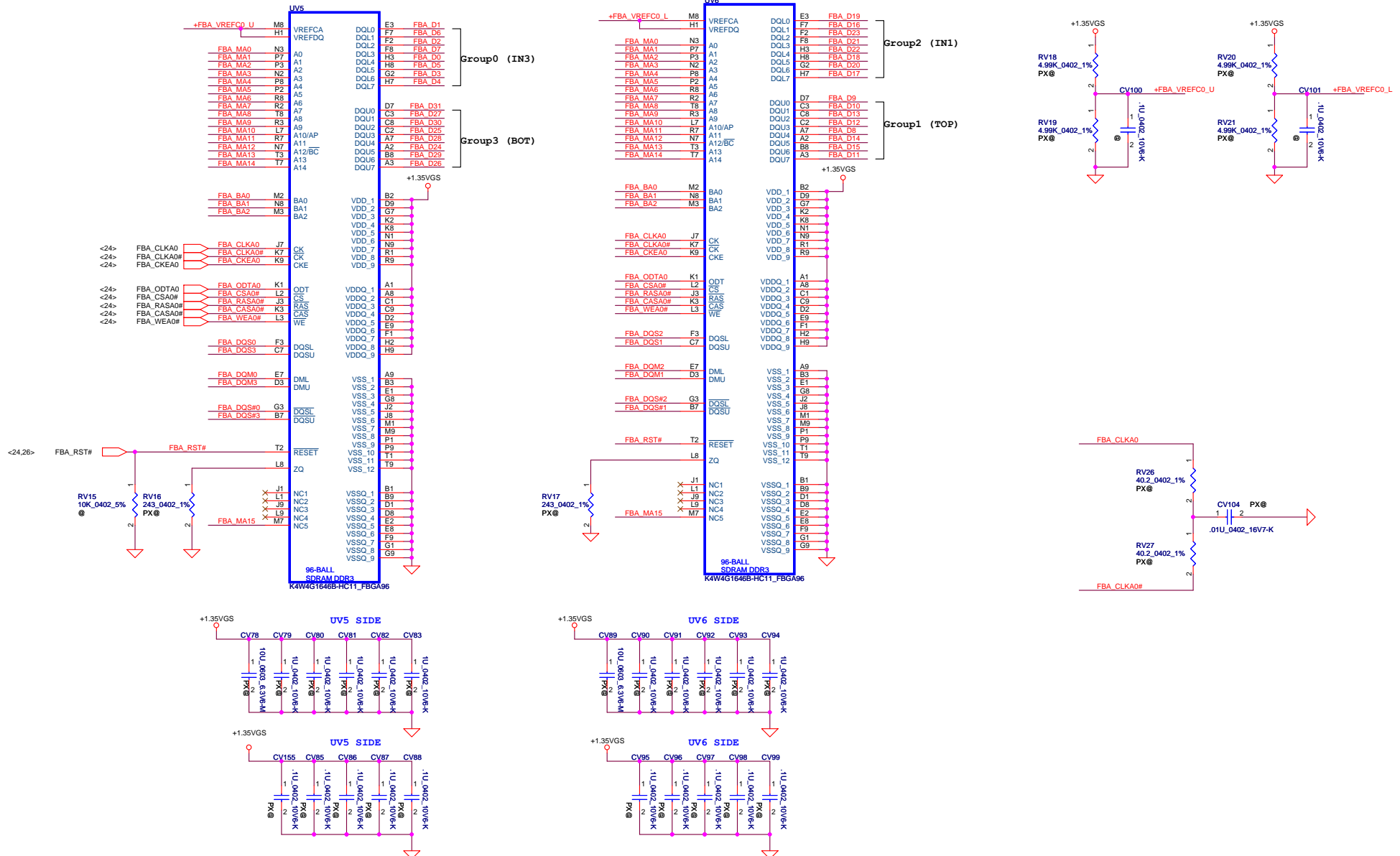


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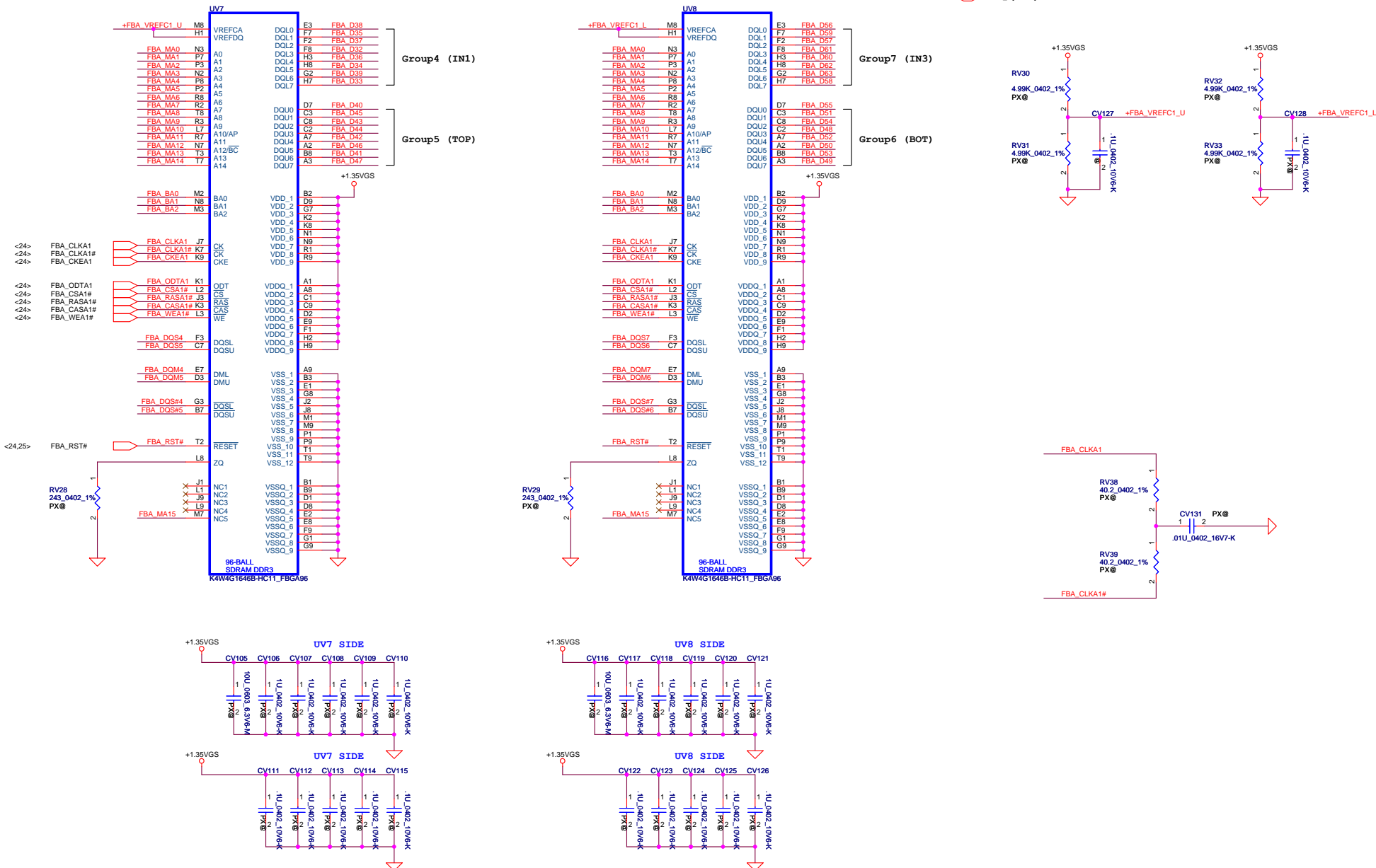
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- FBA_BA[2..0] <24,26>
- FBA_DQS[3..0] <24>
- FBA_DQM[3..0] <24>
- FBA_DQS# [3..0] <24>
- FBA_D[31..0] <24>

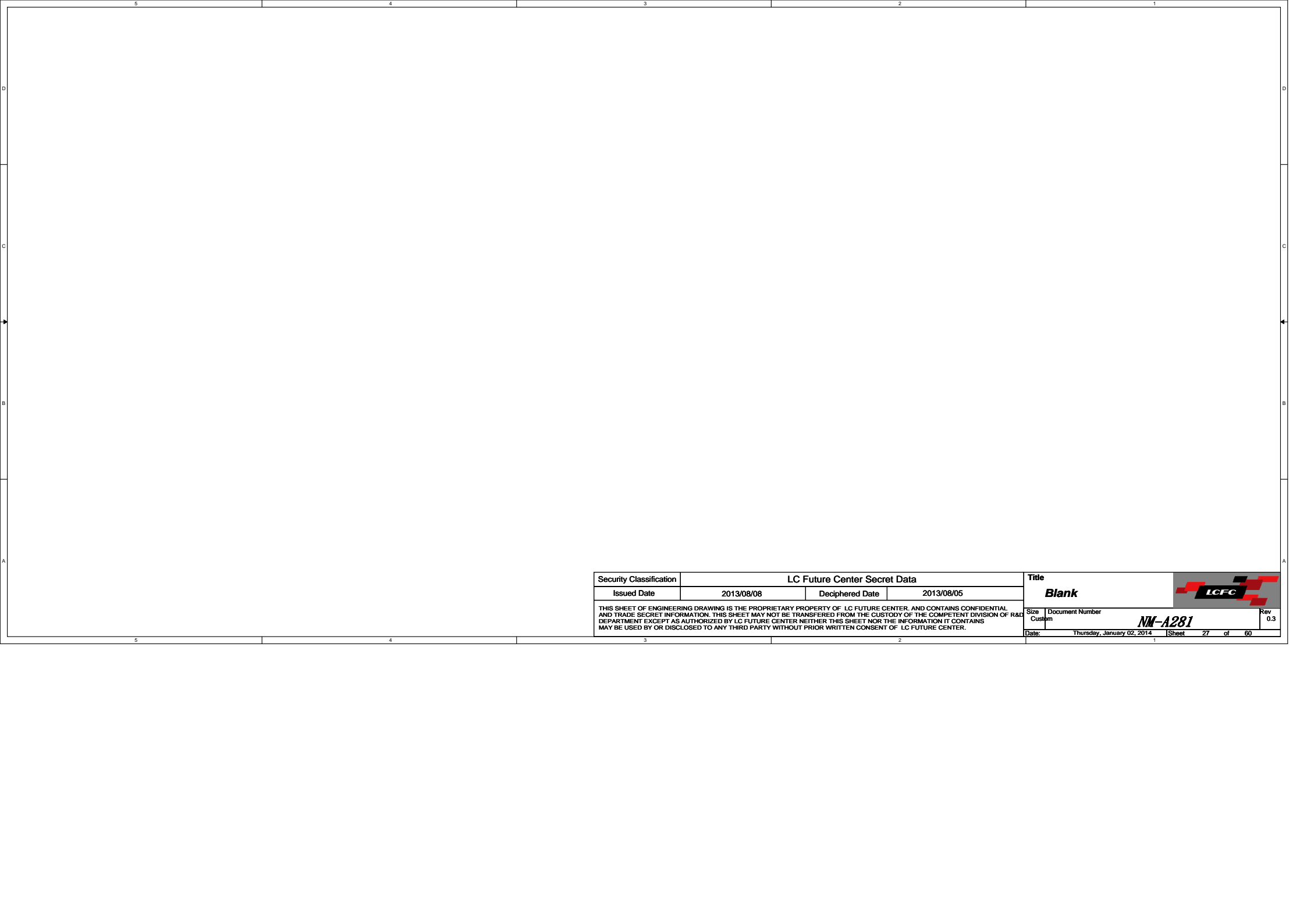
ACLU5 swap the VRAM Data @ 08/26
 VRAM 8 pcs change to 4 pcs @ 09/26




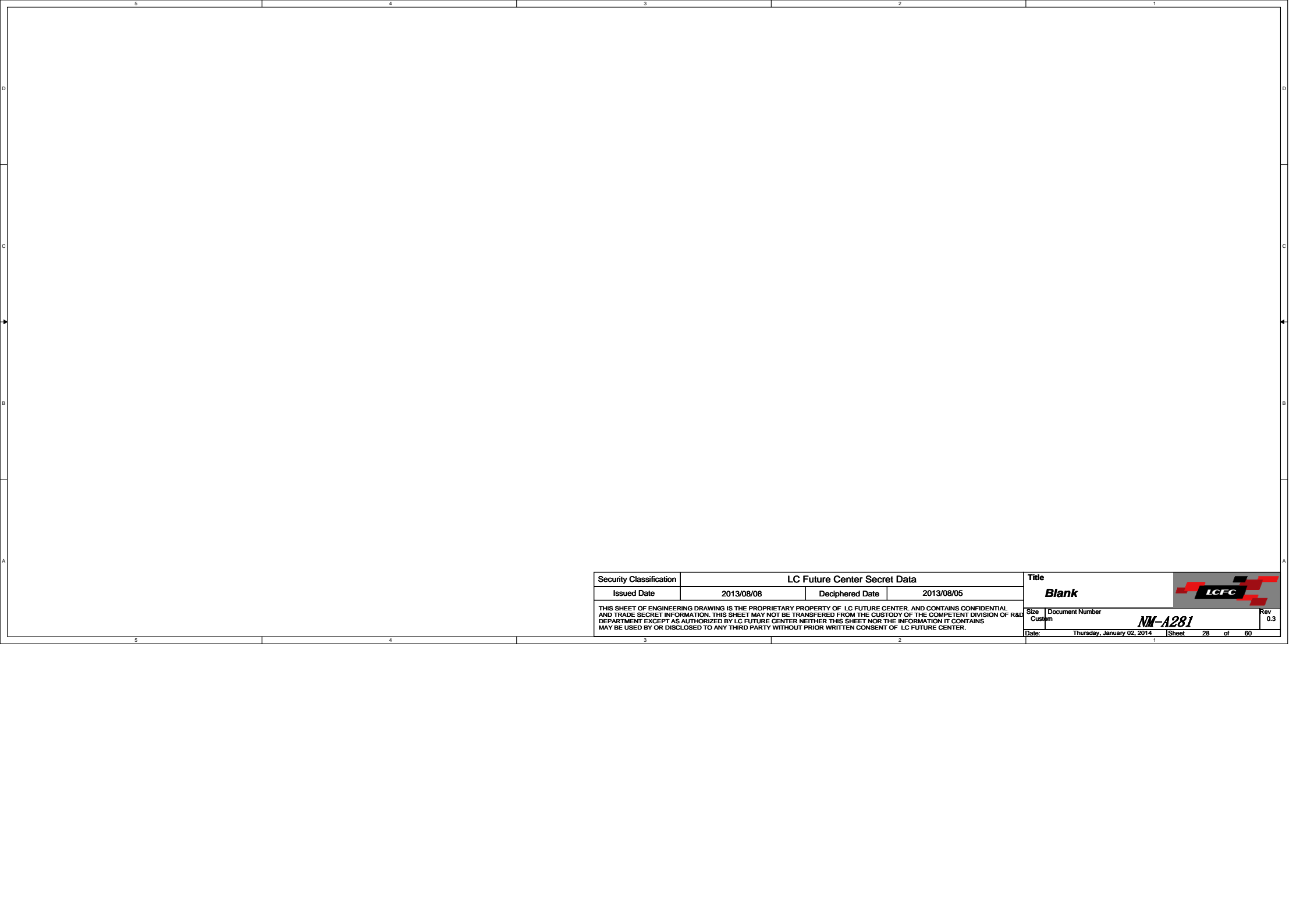
Memory Partition A - Upper 32 bits




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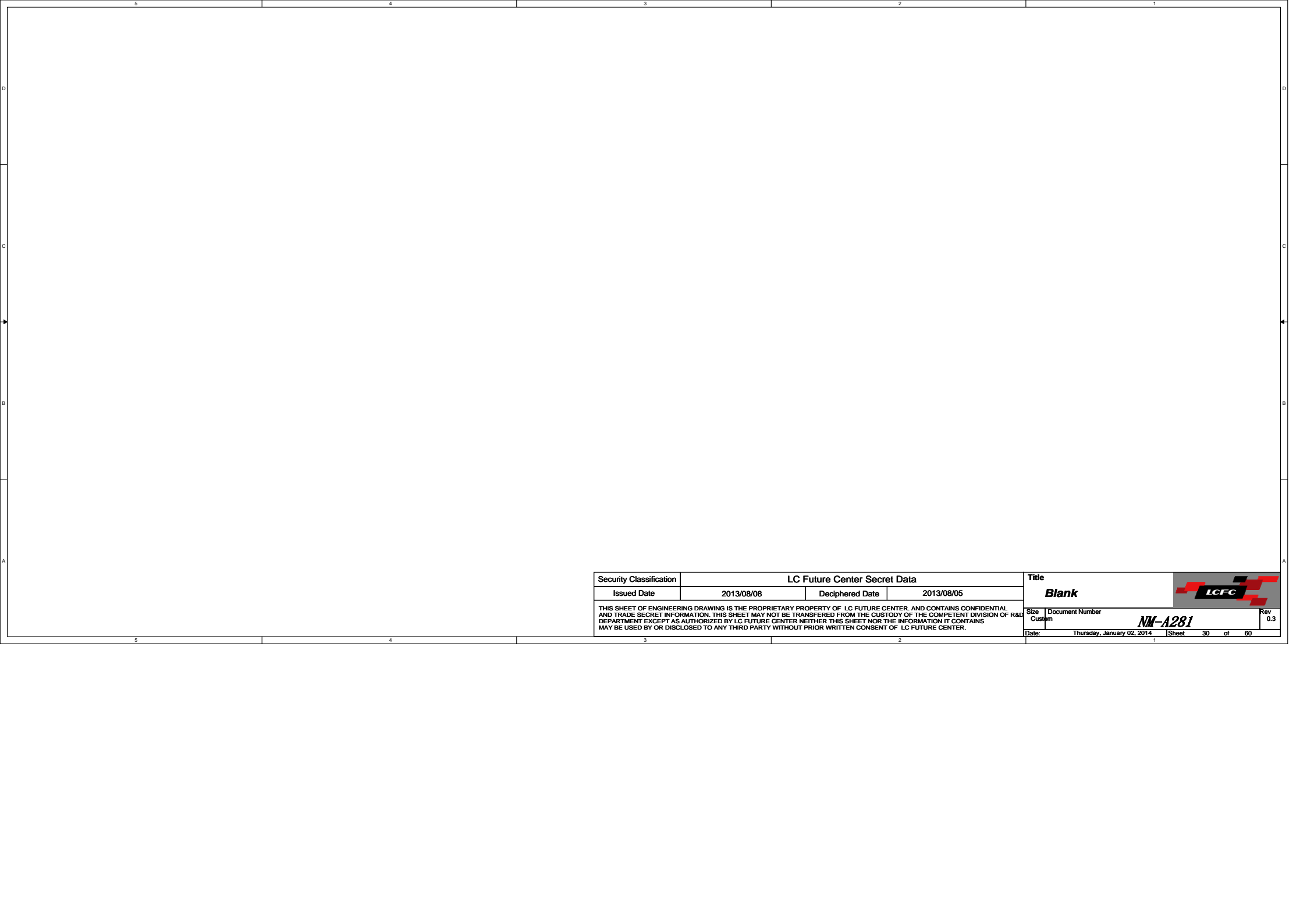



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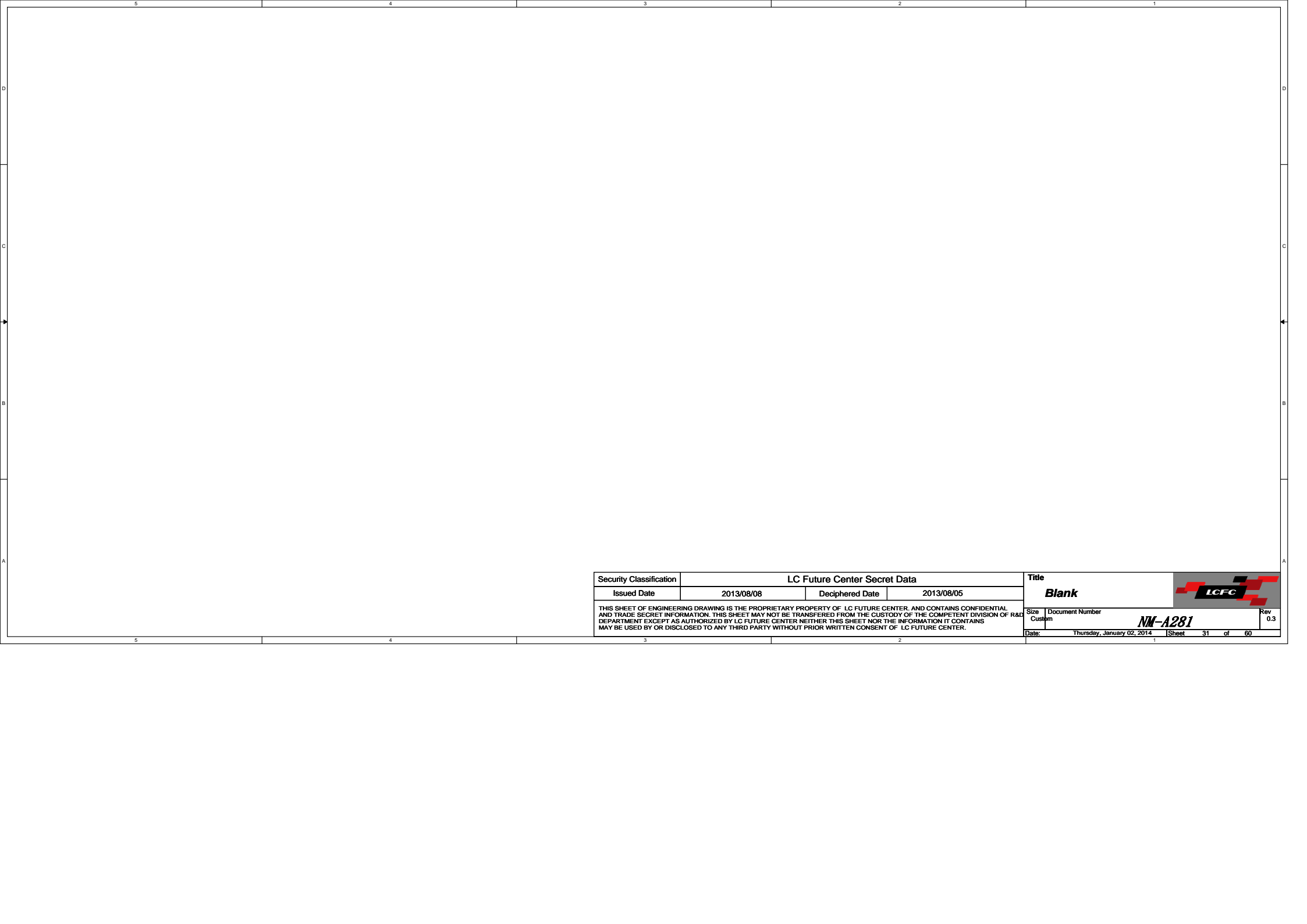



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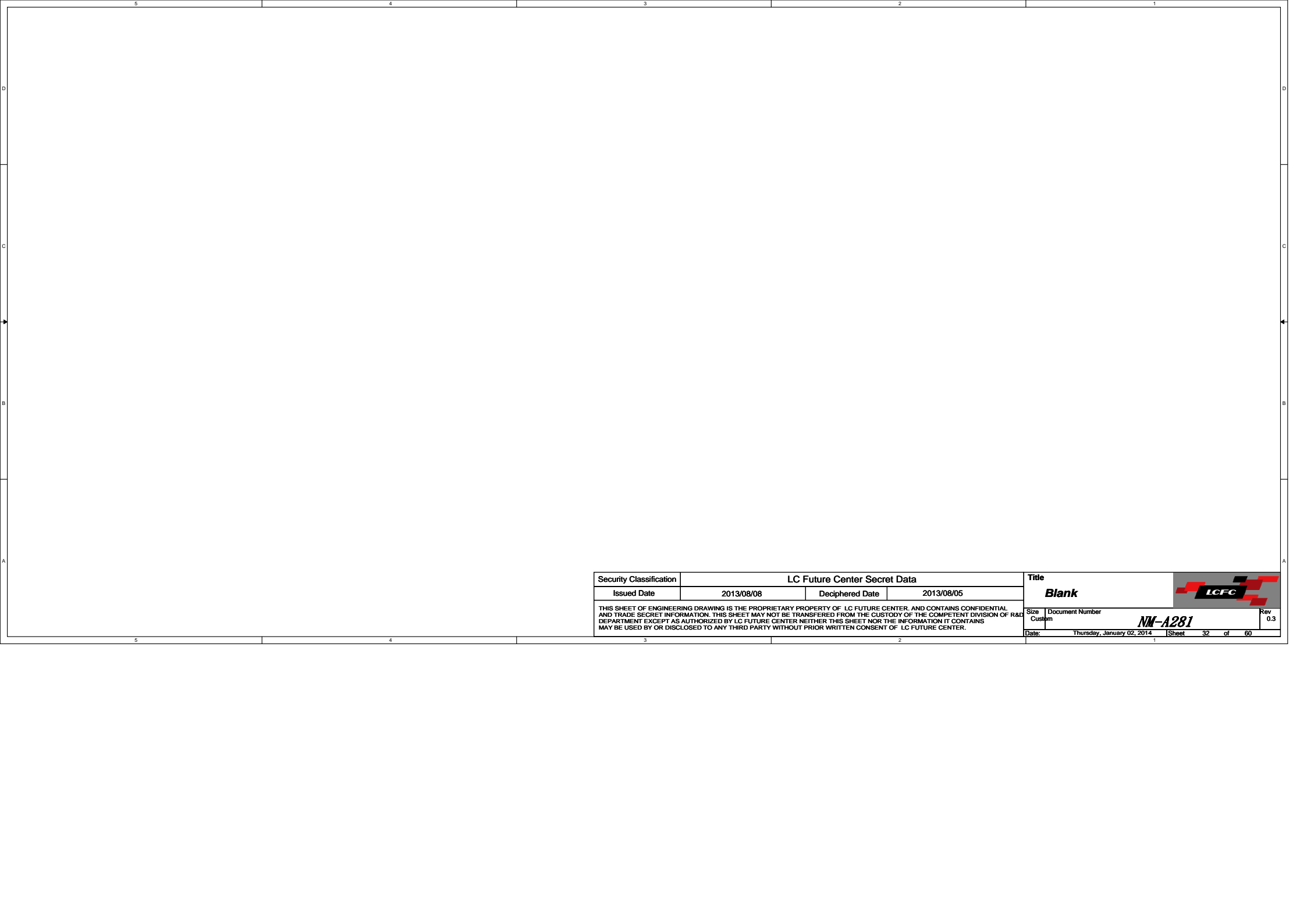
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				Date: Thursday, January 02, 2014	Rev 0.3
				Sheet 30 of 60	

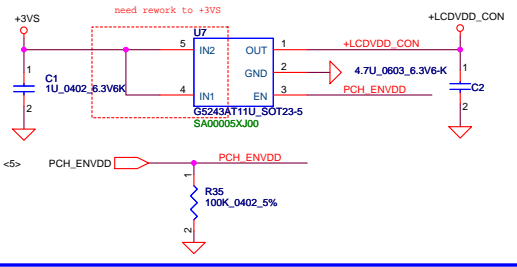


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Blank	
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				Date: Thursday, January 02, 2014	Rev 0.3
				Sheet 31 of 60	

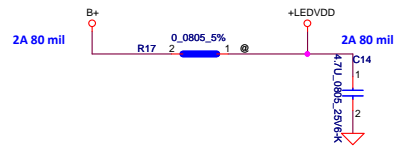


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Blank	
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				Date: Thursday, January 02, 2014	Rev 0.3
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LCD POWER CIRCUIT OK

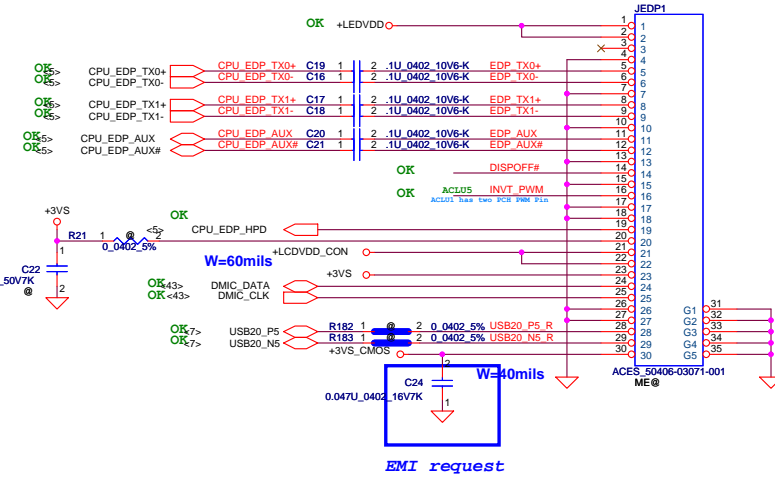
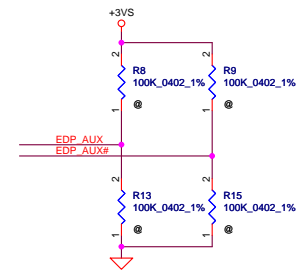
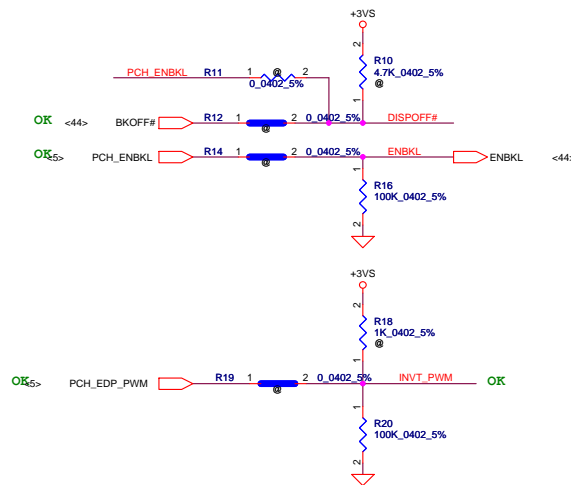
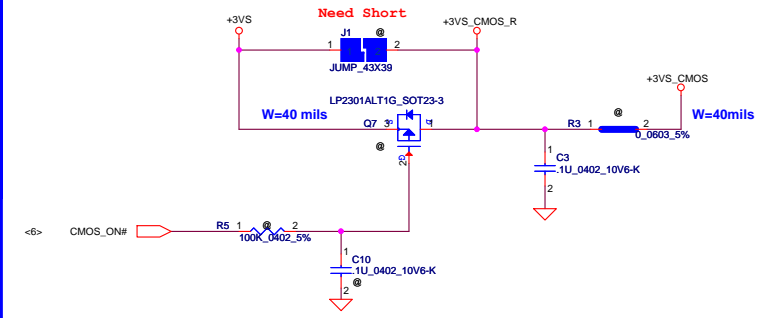


B+ to +LEDVDD POWER OK

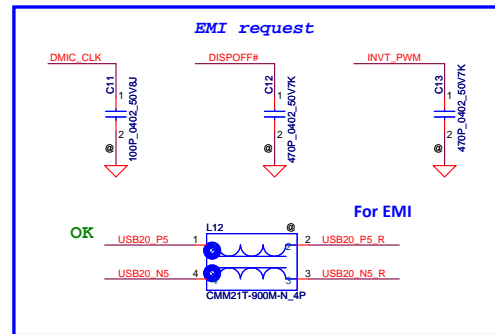
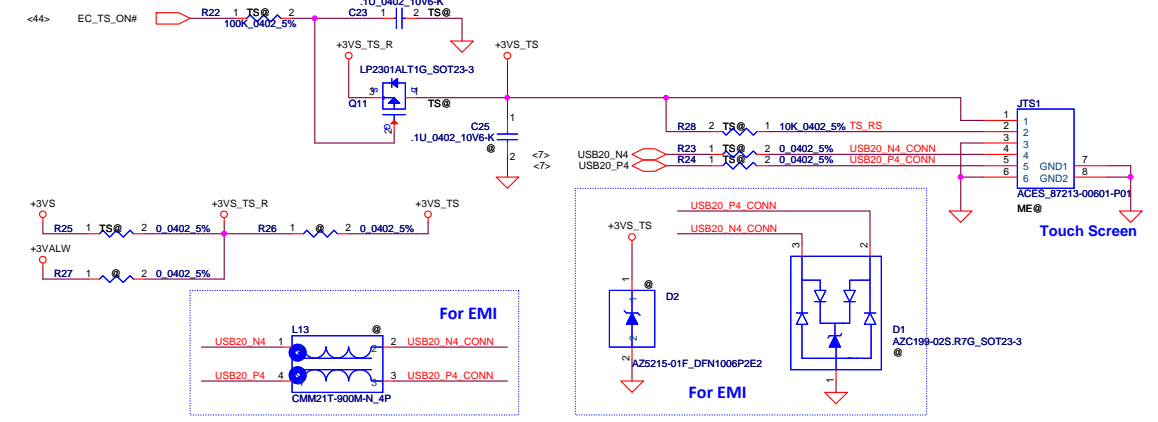


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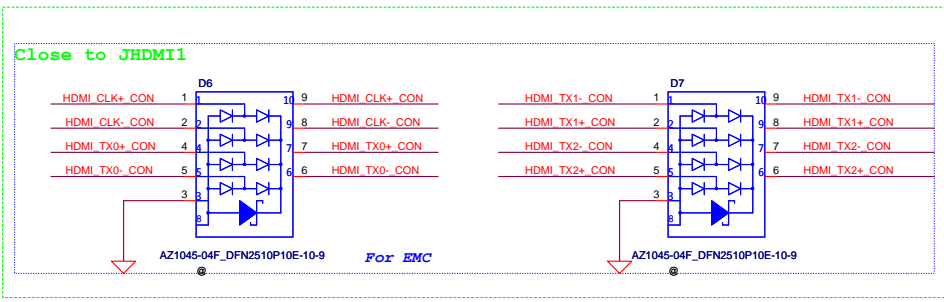
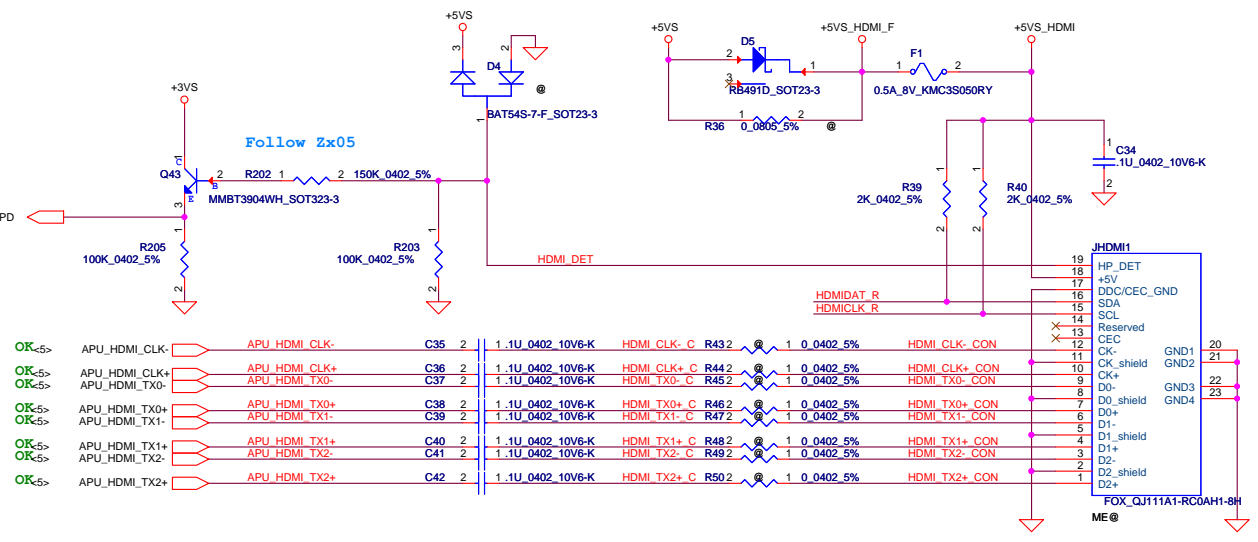
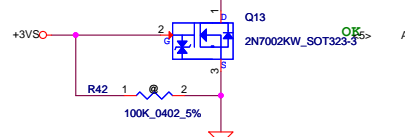
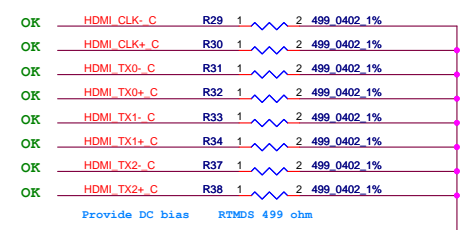
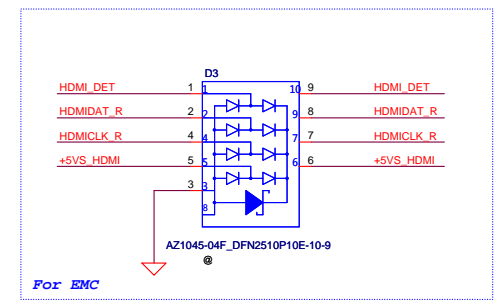
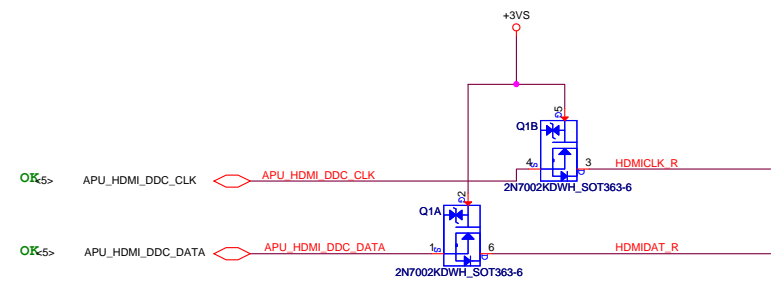
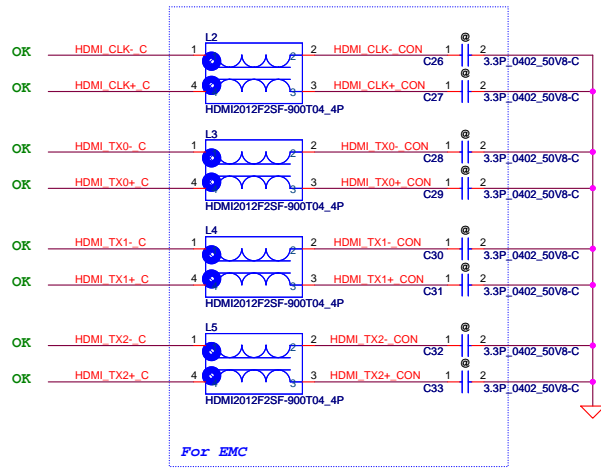
CMOS Camera



Touch Screen OK



Security Classification	LC Future Center Secret Data		Title	eDP/ CMOS/Touch screen
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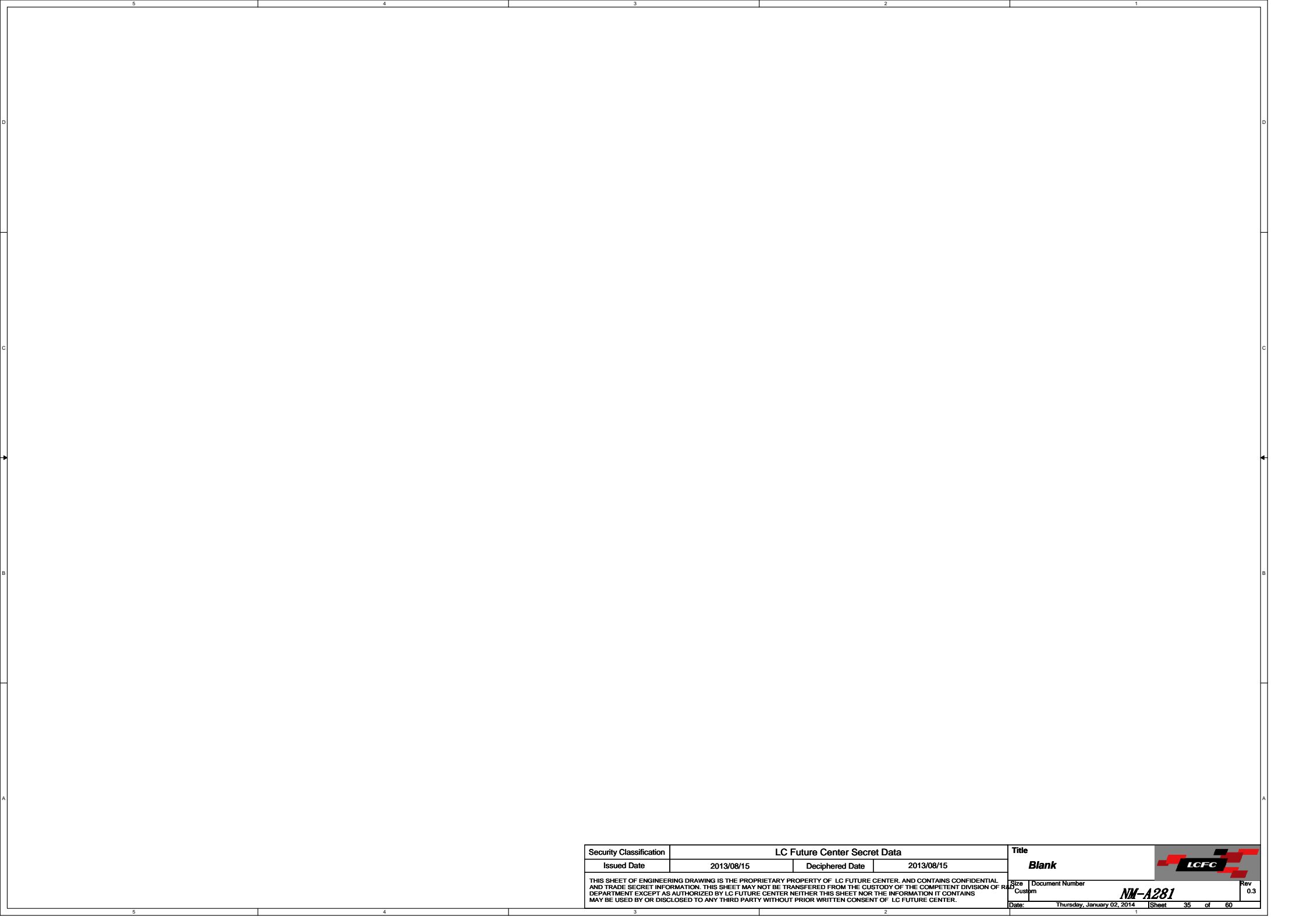



Security Classification				LC Future Center Secret Data				Title	
Issued Date		2013/08/15		Deciphered Date		2013/08/15		HDMI_CONN	
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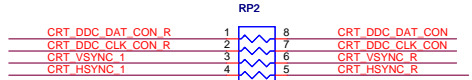
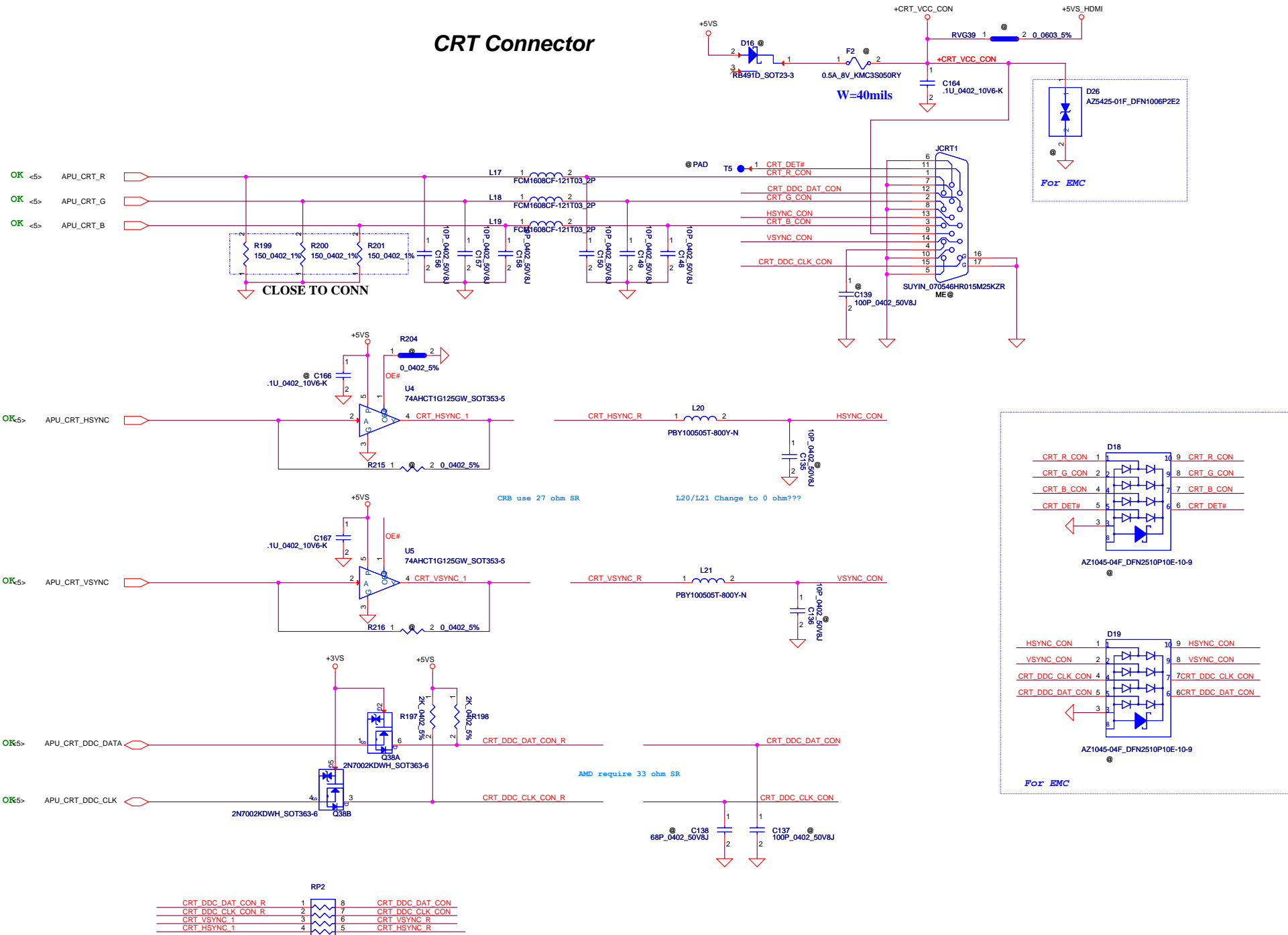
NM-A281

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CRT Connector



T PN change Idea pad PN SD300003700

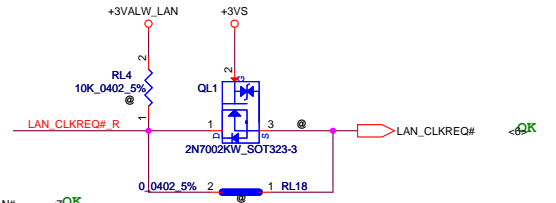
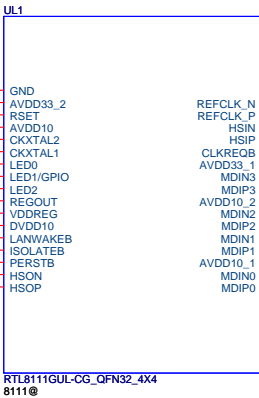
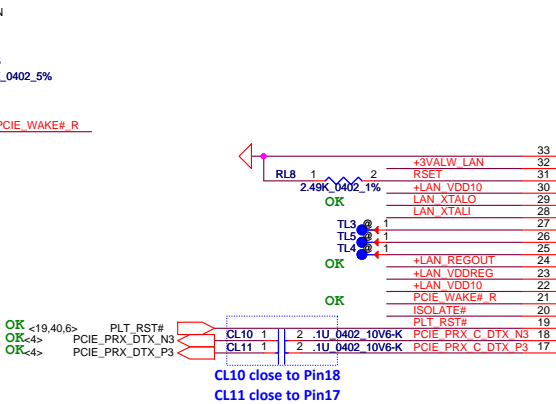
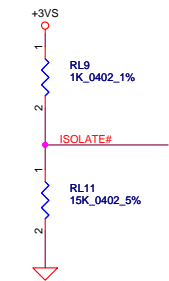
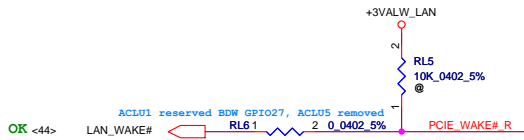
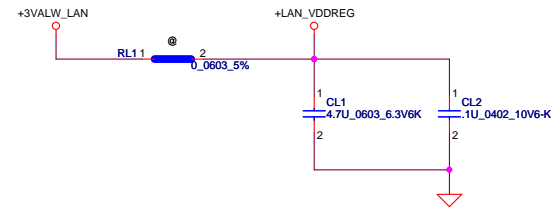
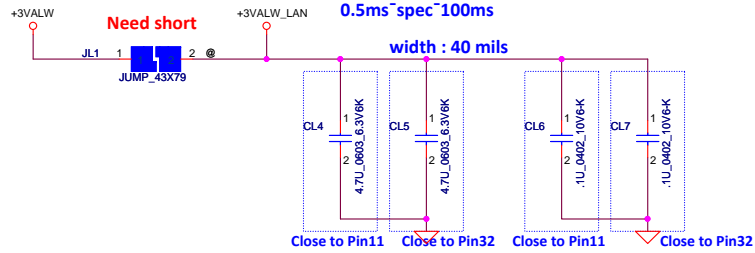
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Issued Date	2013/08/15	Deciphered Date
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CRT	Custom	NM-A281	0.3
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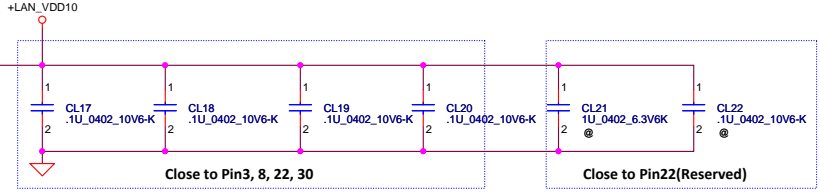
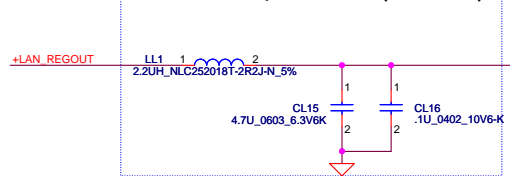


+3VALW TO +3VALW_LAN

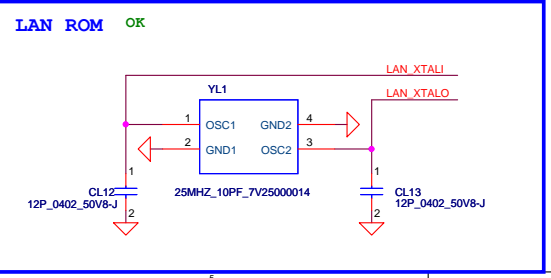
**+3VALW_LAN rising time (10%~90%):
0.5ms spec~100ms**



For RTL8111GUL/RTL8106EUL (SWR mode)

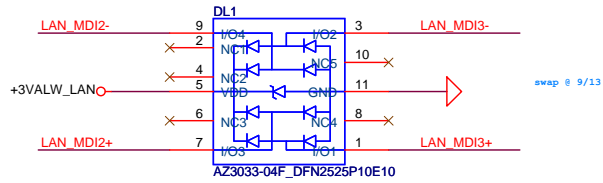


Layout Note: LL1 must be within 200mil to Pin36,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

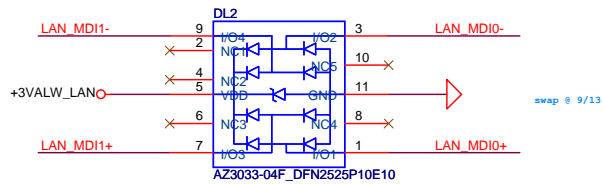


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Issued Date		2013/08/08		Deciphered Date		2013/08/05		LAN_RTL8111GUL/RTL8106E LCFC	
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Size Custom	Document Number		Date				Thursday, January 02, 2014		Rev 0.3
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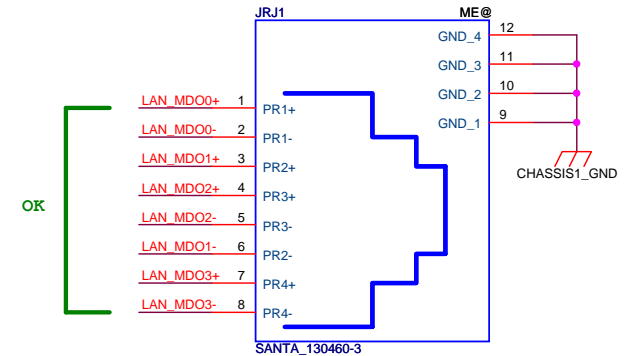
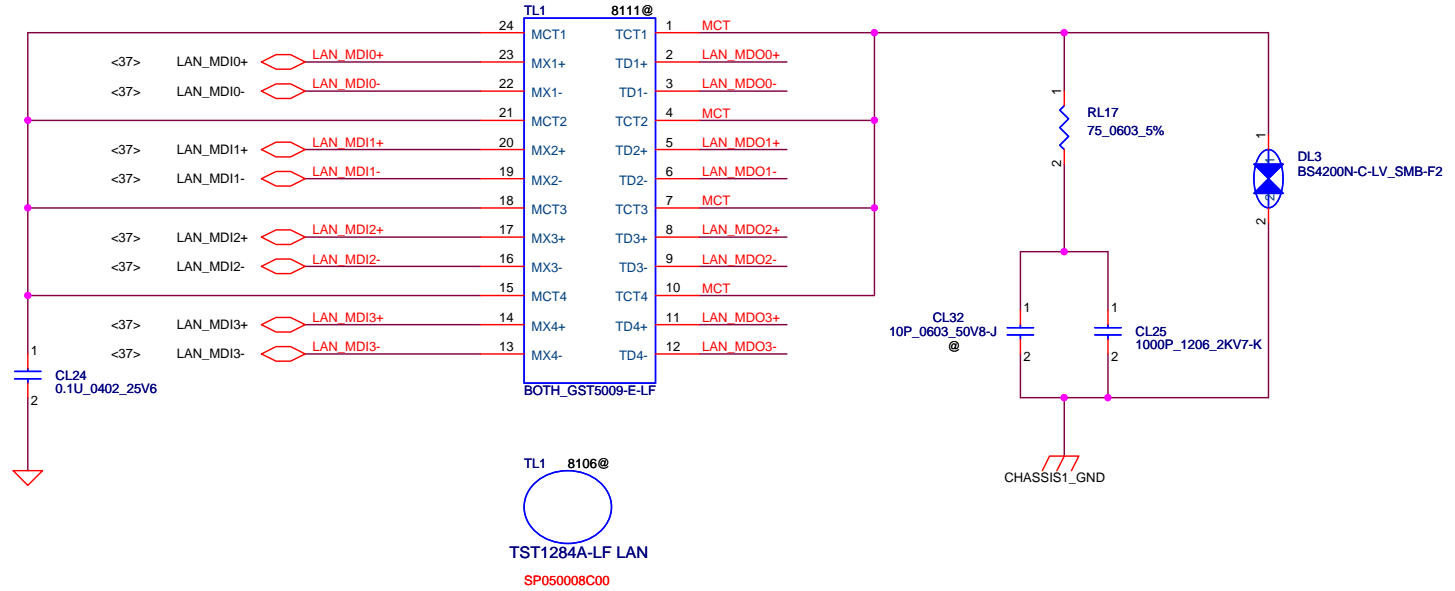
DL1/DL2
1'S PN:SC30003M00



Place Close to TL1

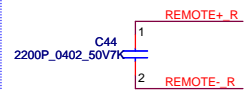


Place Close to TL2



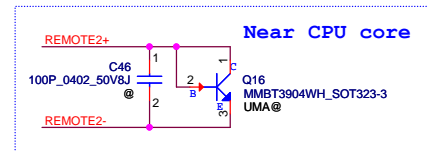
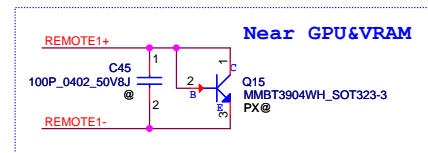
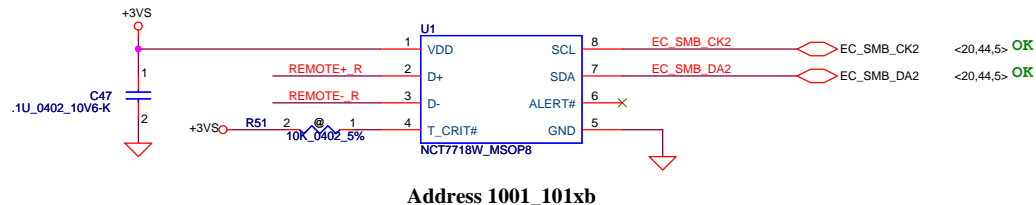
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_Transformer	
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Close to U1



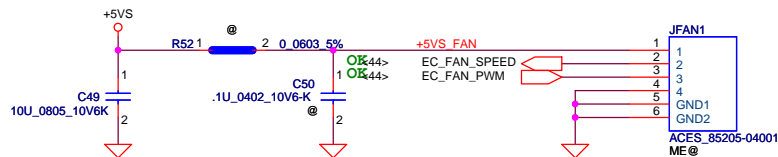
SMSC thermal sensor placed near DIMM

OK



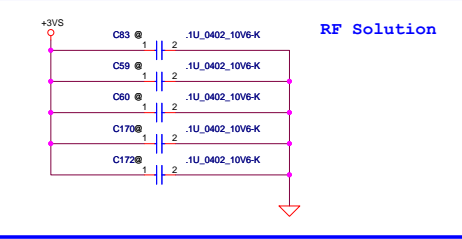
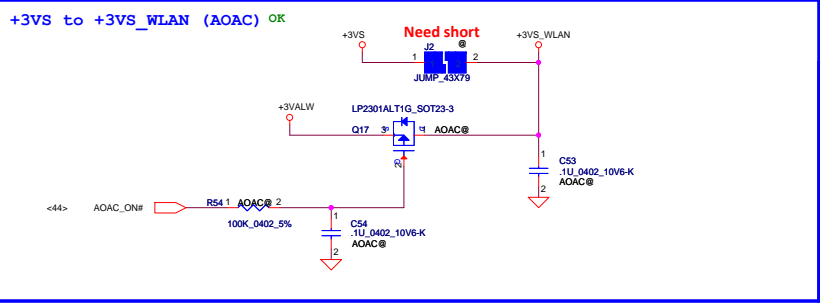
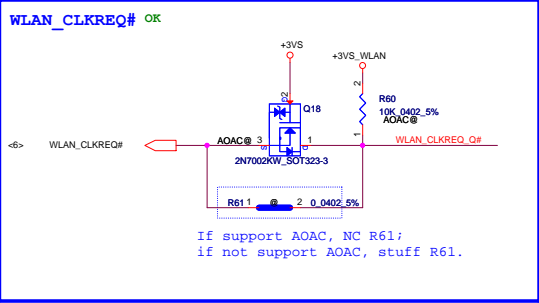
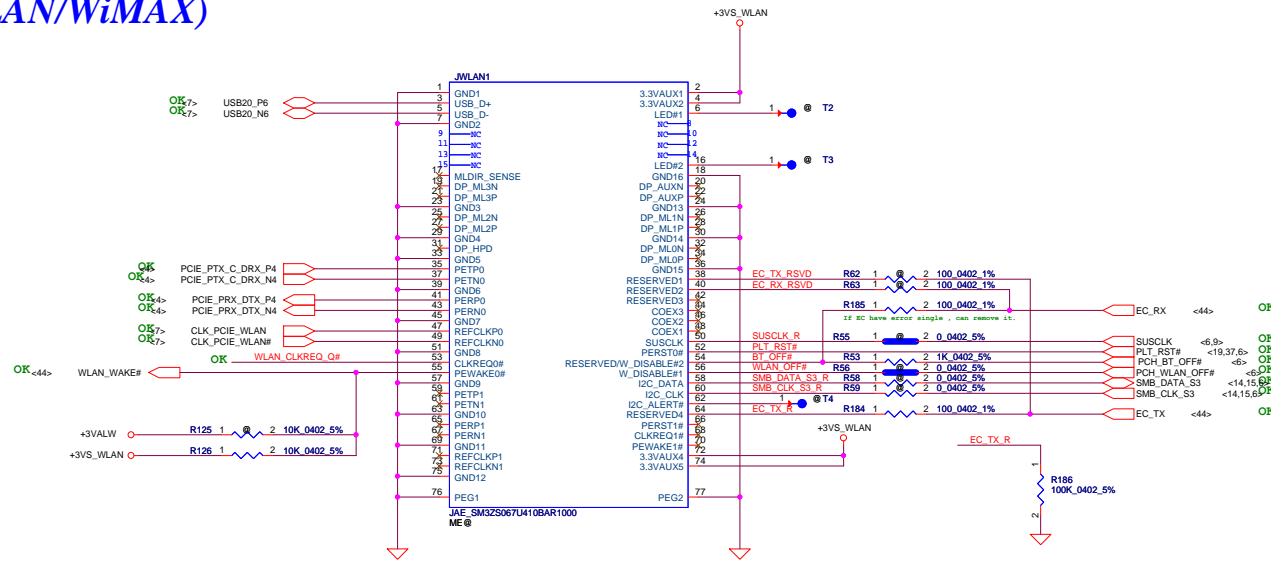
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn



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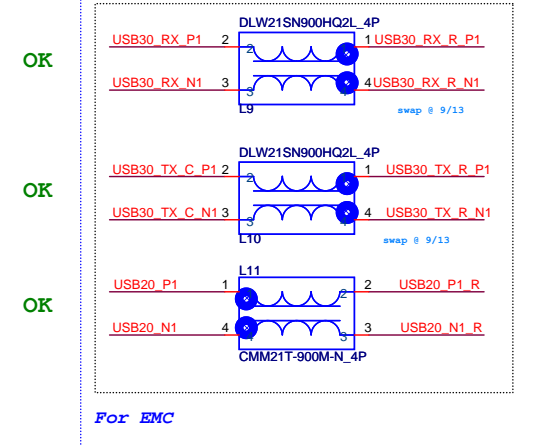
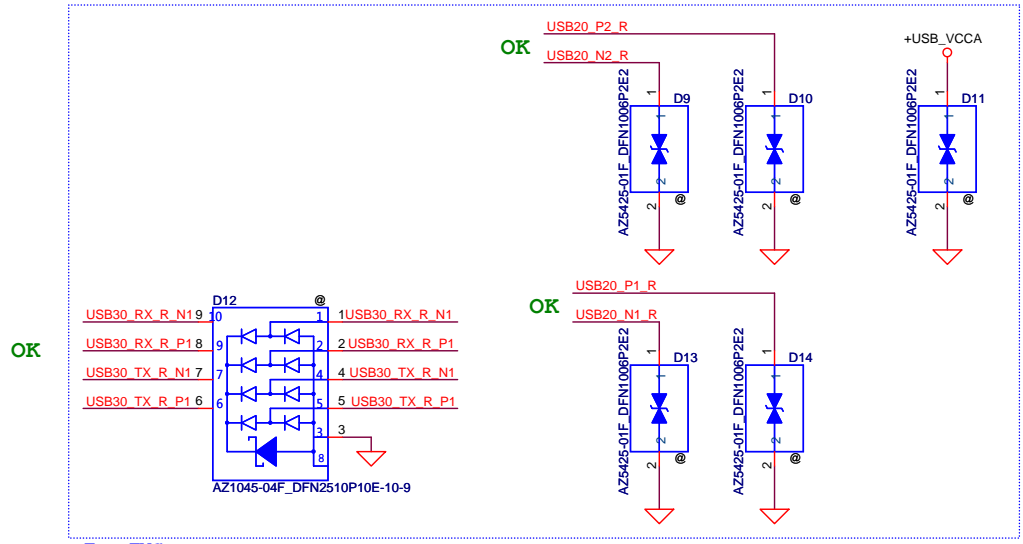
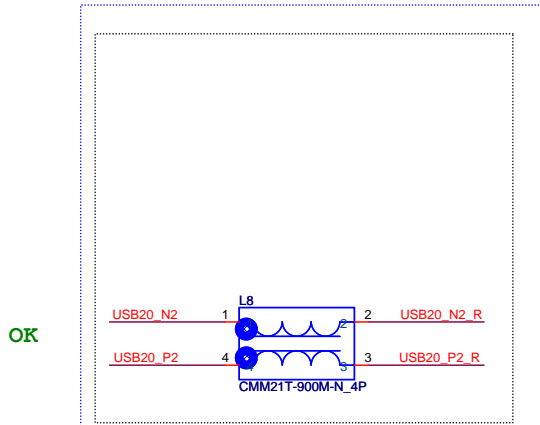
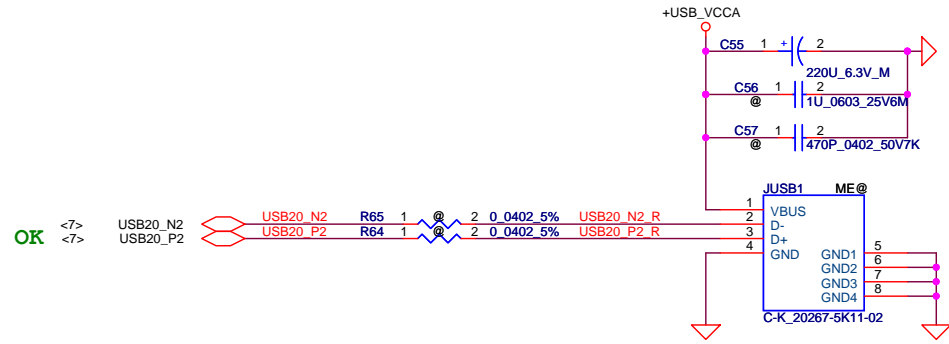
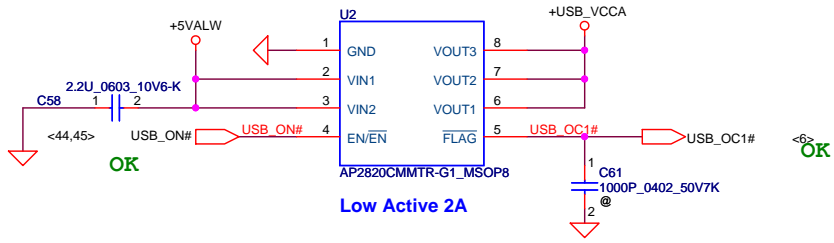
Mini-Express Card(WLAN/WiMAX)



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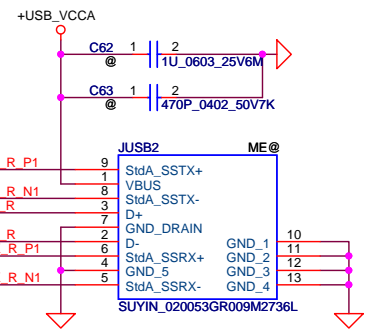
Title	NGFF WLAN	
Size	Document Number	Rev
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LEFT SIDE USB3.0 PORT X2



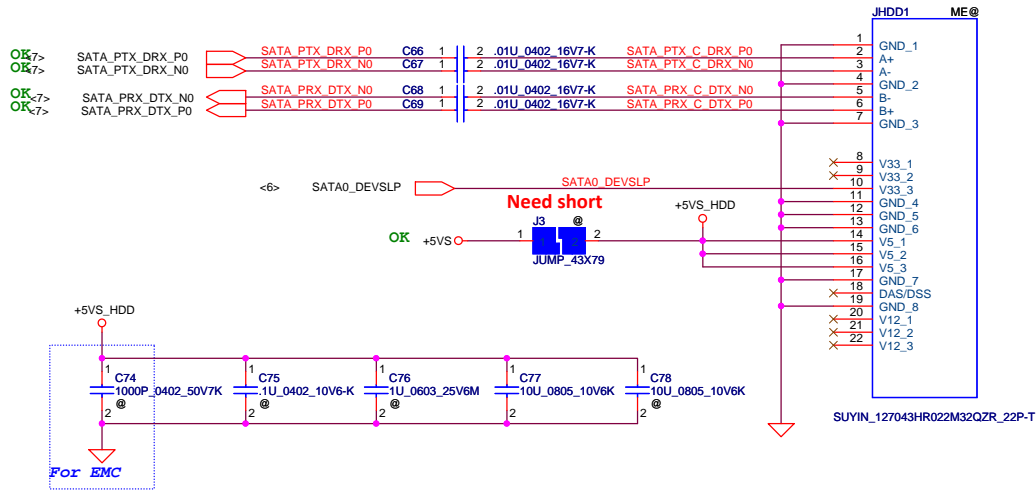
For EMC

OK	<7>	USB30_TX_P1	USB30_TX_P1	C64	1	2	.1U 0402 10V6-K	USB30_TX_C_P1	R68	1	2	0 0402 5%	USB30_TX_R_P1
OK	<7>	USB30_TX_N1	USB30_TX_N1	C65	1	2	.1U 0402 10V6-K	USB30_TX_C_N1	R69	1	2	0 0402 5%	USB30_TX_R_N1
OK	<7>	USB20_P1	USB20_P1						R70	1	2	0 0402 5%	USB20_P1_R
OK	<7>	USB20_N1	USB20_N1						R71	1	2	0 0402 5%	USB20_N1_R
OK	<7>	USB30_RX_P1	USB30_RX_P1						R72	1	2	0 0402 5%	USB30_RX_R_P1
OK	<7>	USB30_RX_N1	USB30_RX_N1						R73	1	2	0 0402 5%	USB30_RX_R_N1

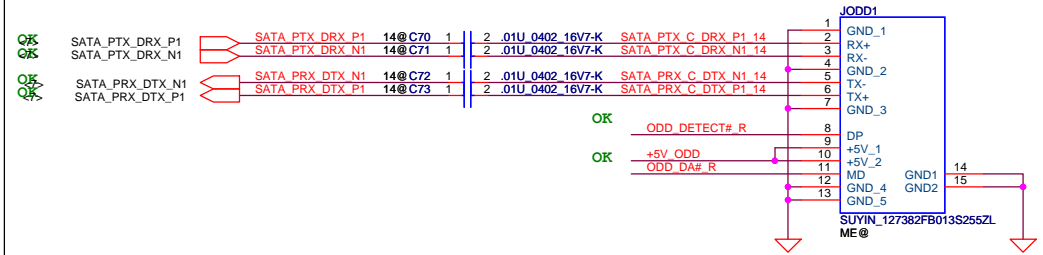


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Issued Date		2013/08/08		Deciphered Date		2013/08/05		USB2.0/USB3.0 PORT (LEFT)					
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Size	Document Number	Rev								Date			
Custom	NM-A281	0.3								Thursday, January 02, 2014			
										Sheet	41	of	60

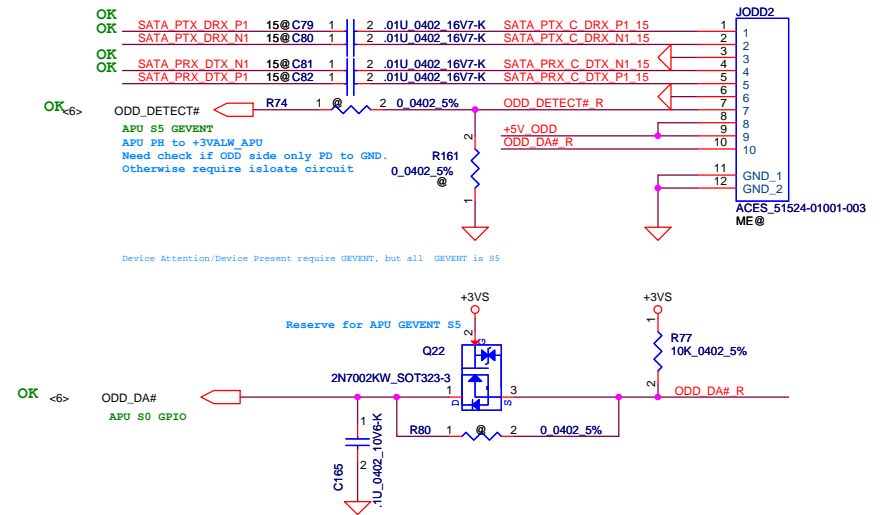
SATA HDD Conn.



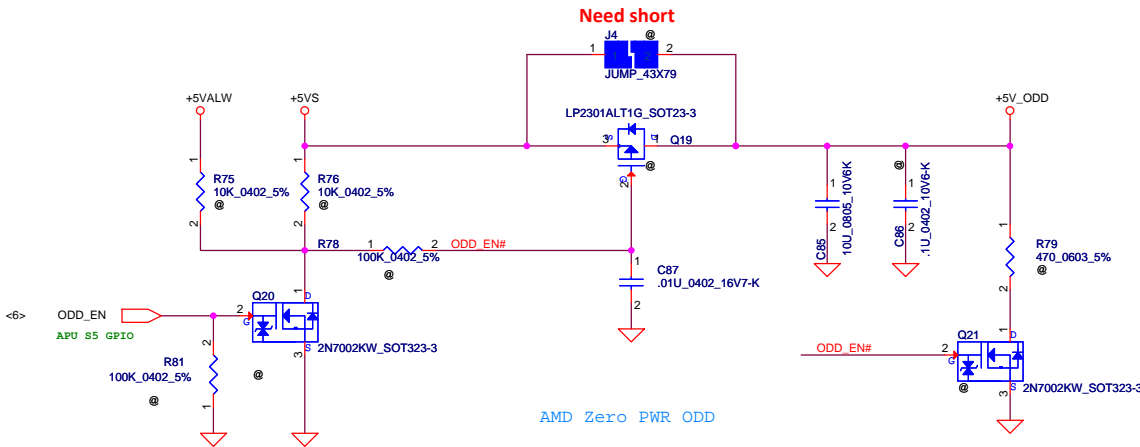
FOR 14" SATA ODD Conn.



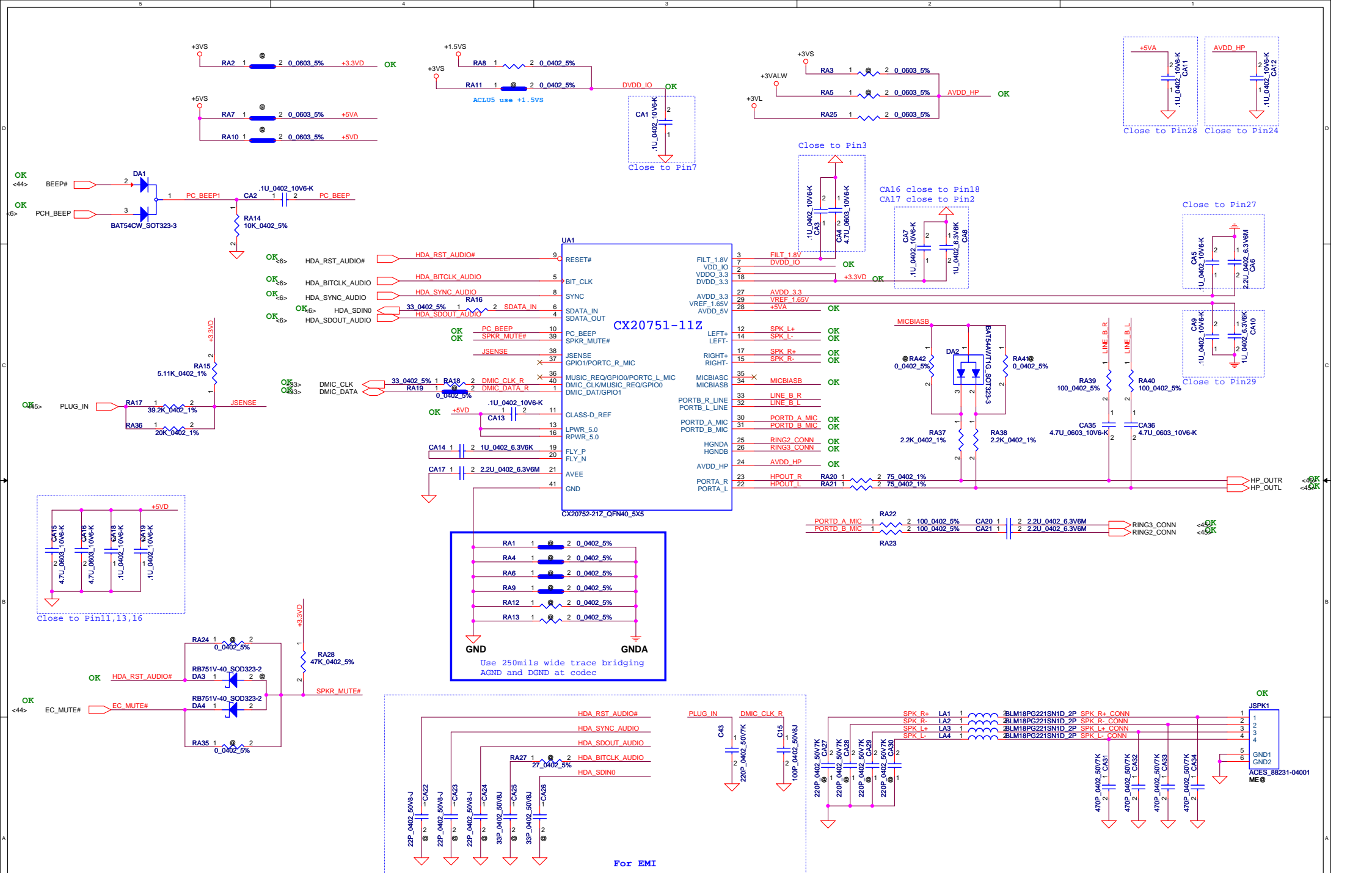
FOR 15" SATA ODD FFC Conn



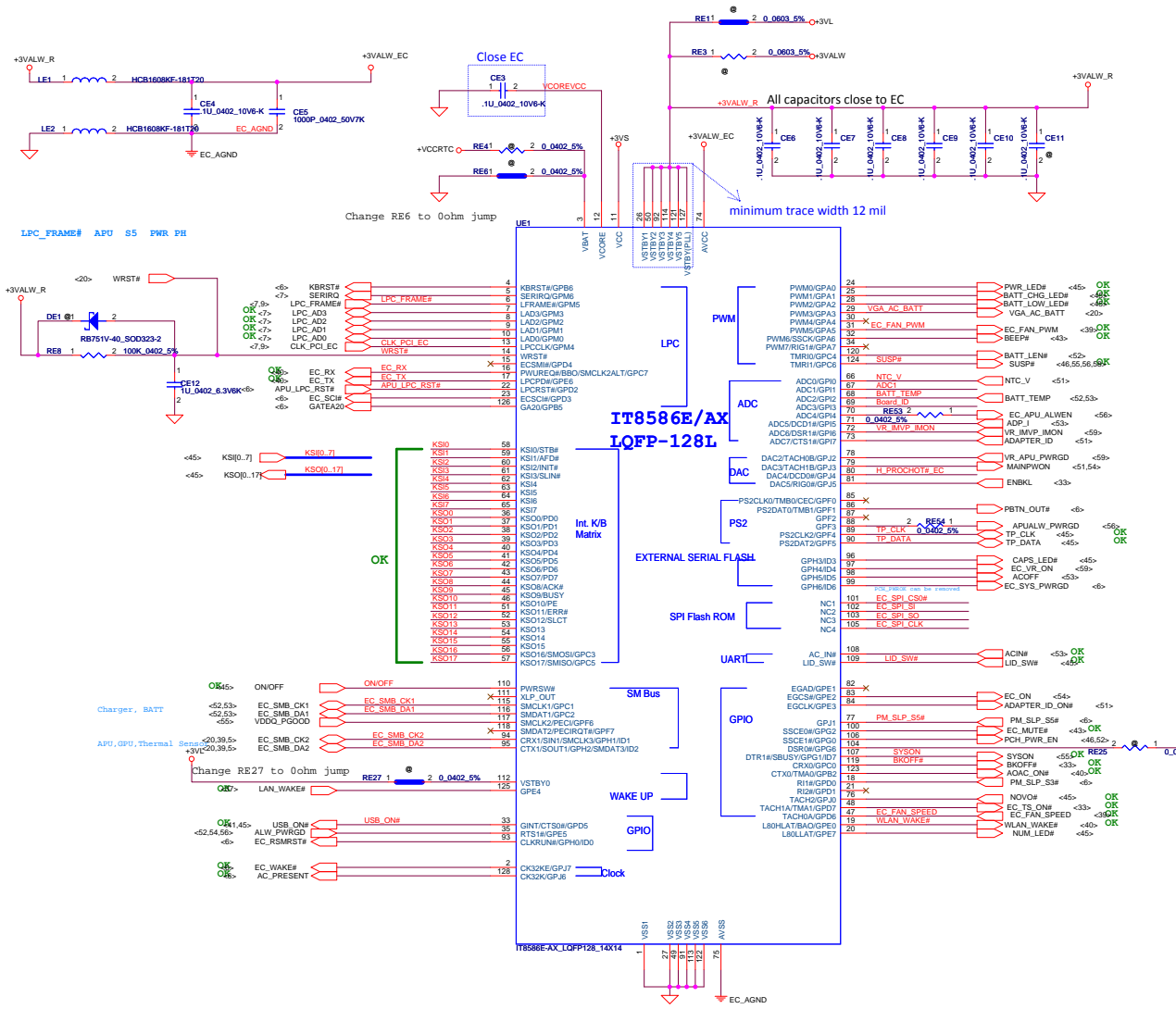
+5VS to +5V_ODD OK



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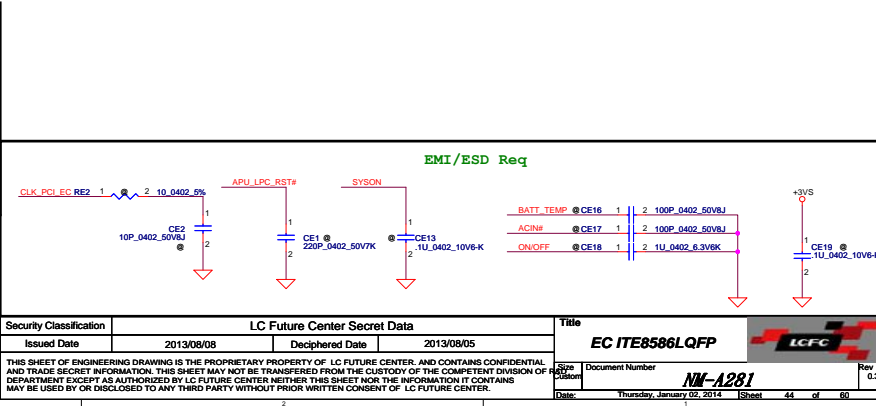
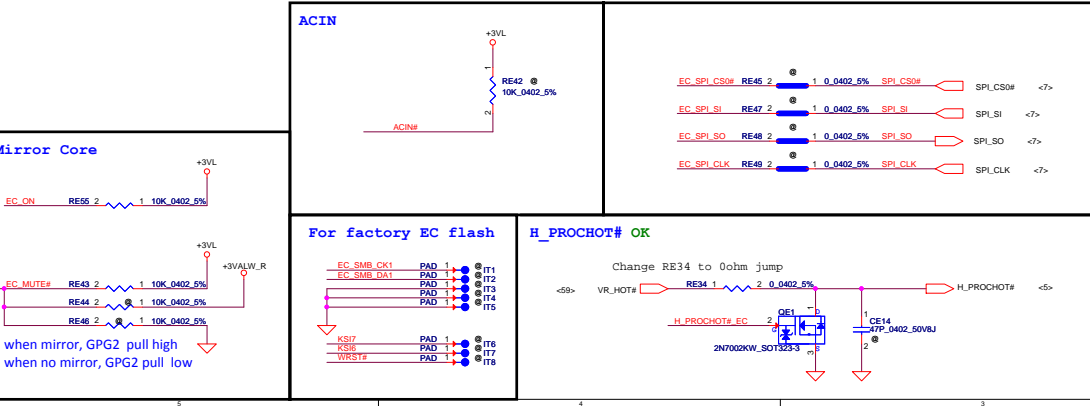


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Title	Codec_CX20752		Rev
Size	Document Number	NM-A281	
Date:	Thursday, January 02, 2014	Sheet	43 of 60

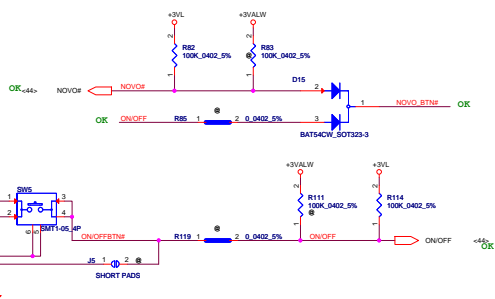


BORAD ID Config

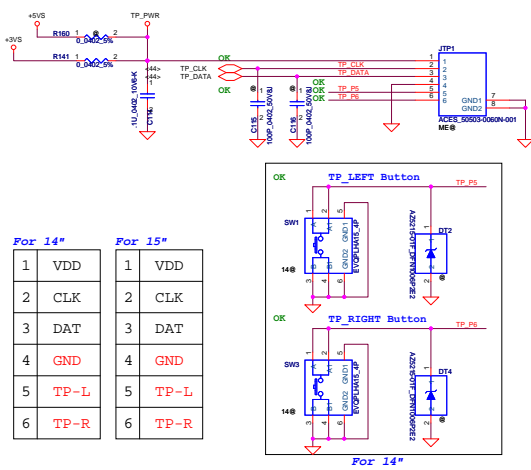
Board ID	RE34	V _{AD_BTD} min	V _{AD_BTD} typ	V _{AD_BTD} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



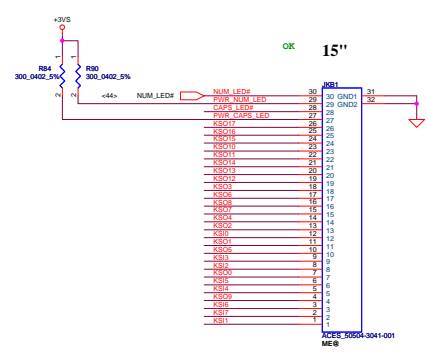
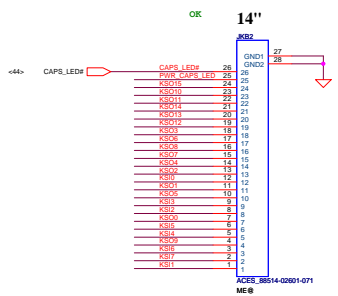
ON/OFF switch



TP/B Connector

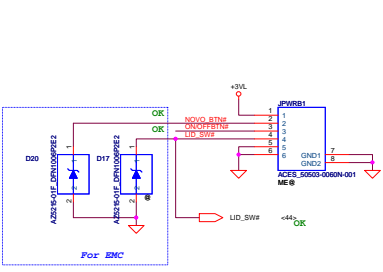


K/B Connector



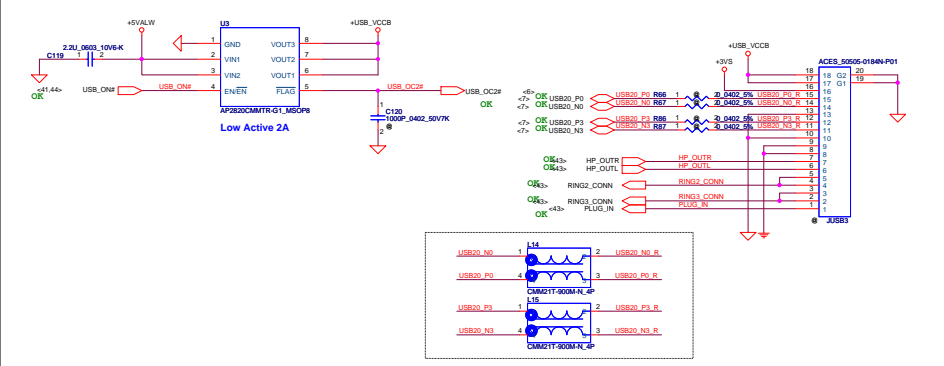
	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS14_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS04_15
KB_14	KS04_14	KS01_15
KB_15	KS07_14	KS04_15
KB_16	KS08_14	KS01_14
KB_17	KS06_14	KS01_15
KB_18	KS03_14	KS05_15
KB_19	KS02_14	KS06_15
KB_20	KS03_14	KS07_15
KB_21	KS04_14	KB_LED_PWR_15
KB_22	KS01_14	CAPS_LED#_15
KB_23	KS01_14	VDD_15
KB_24	KS01_14	NUM_LEDS_15

PWR/B Connector

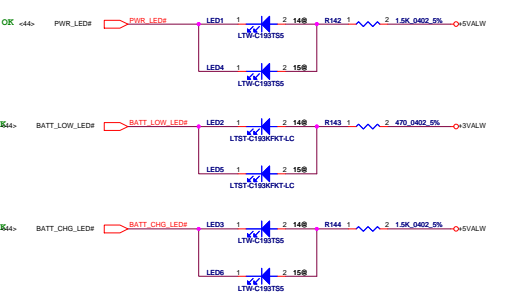



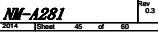
USB I/O Connector

Right Side USB2.0 Port X 1 (USB/B)

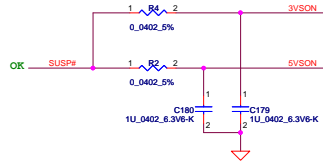


LED

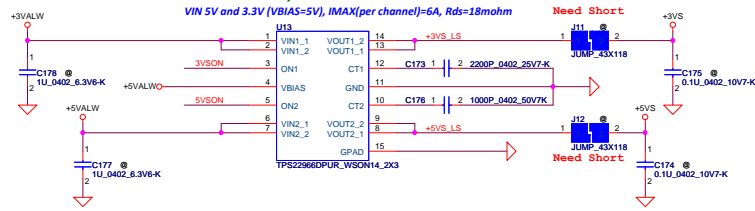


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Size	Document Number		Rev				
Sheet	Thursday, January 02, 2014		Issue		45 of 60		

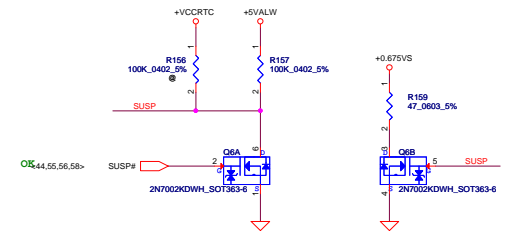
Load Switch
+5VALW To +5VS OK
+3VALW To +3VS



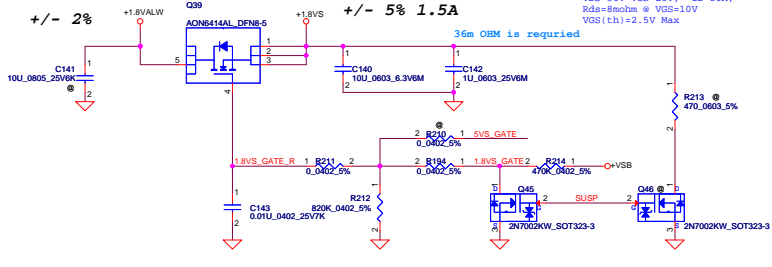
+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms



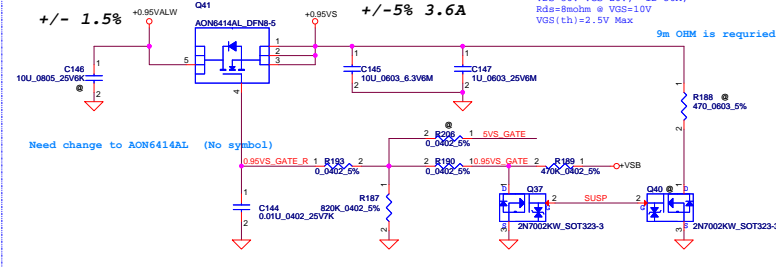
For DisCharge



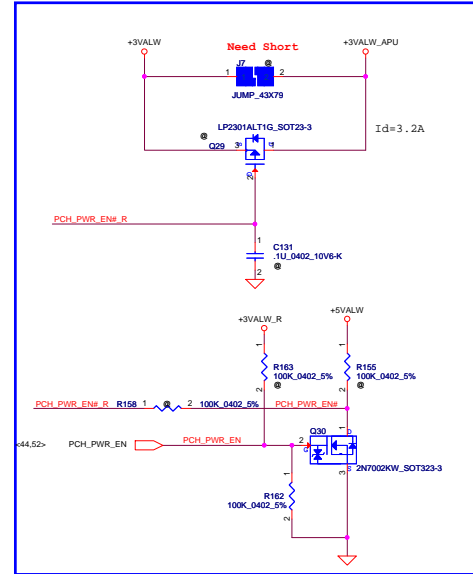
+1.8VALW to +1.8VS



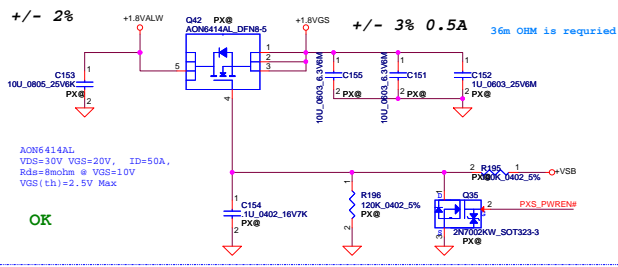
+0.95VALW to +0.95VS



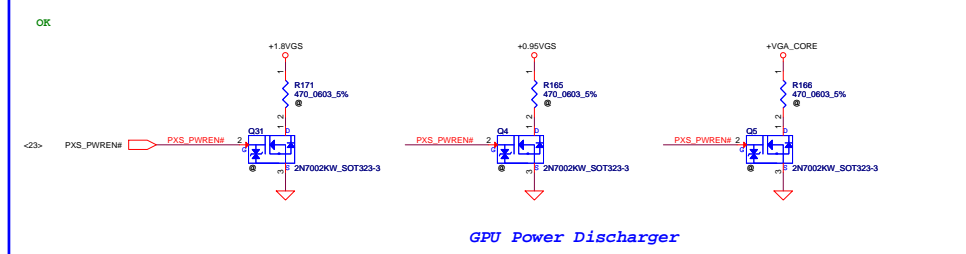
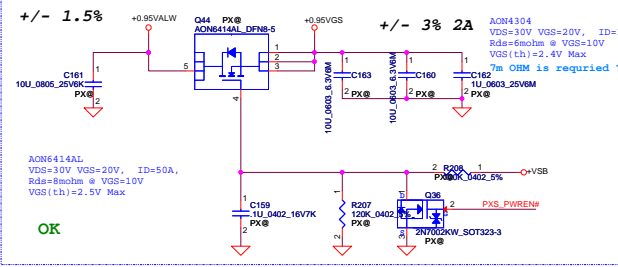
Need check all the EN pin and PWR Sequence.



+1.8VALW to +1.8VGS Reserve for GPU/APU share +1.8V



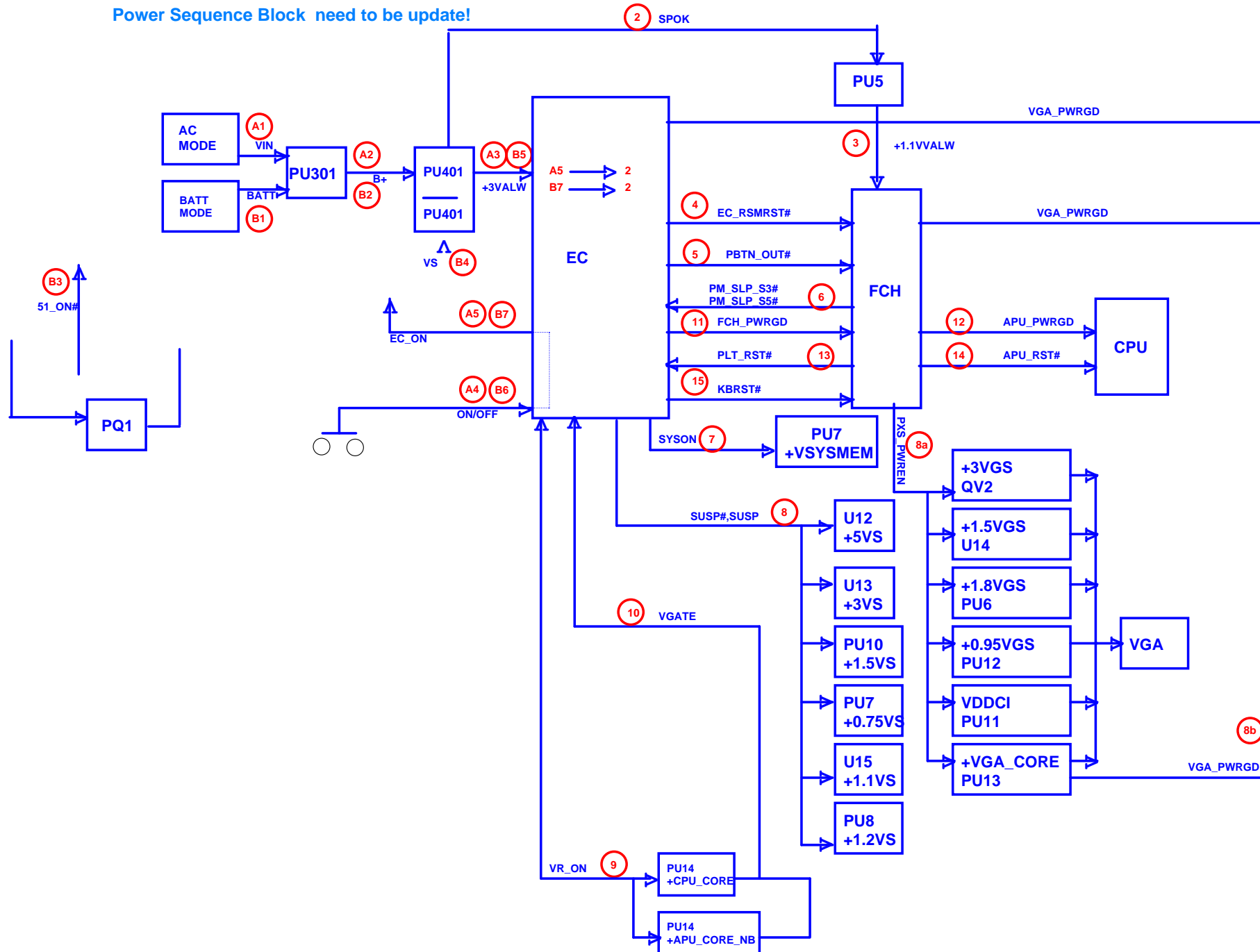
+0.95VALW to +0.95VGS Reserve for GPU/APU share +0.95V



GPU Power Discharge

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Document Number	Revision		Rev
	NM-A281		0.3
Date	Thursday, January 03, 2014	Sheet	46 of 60

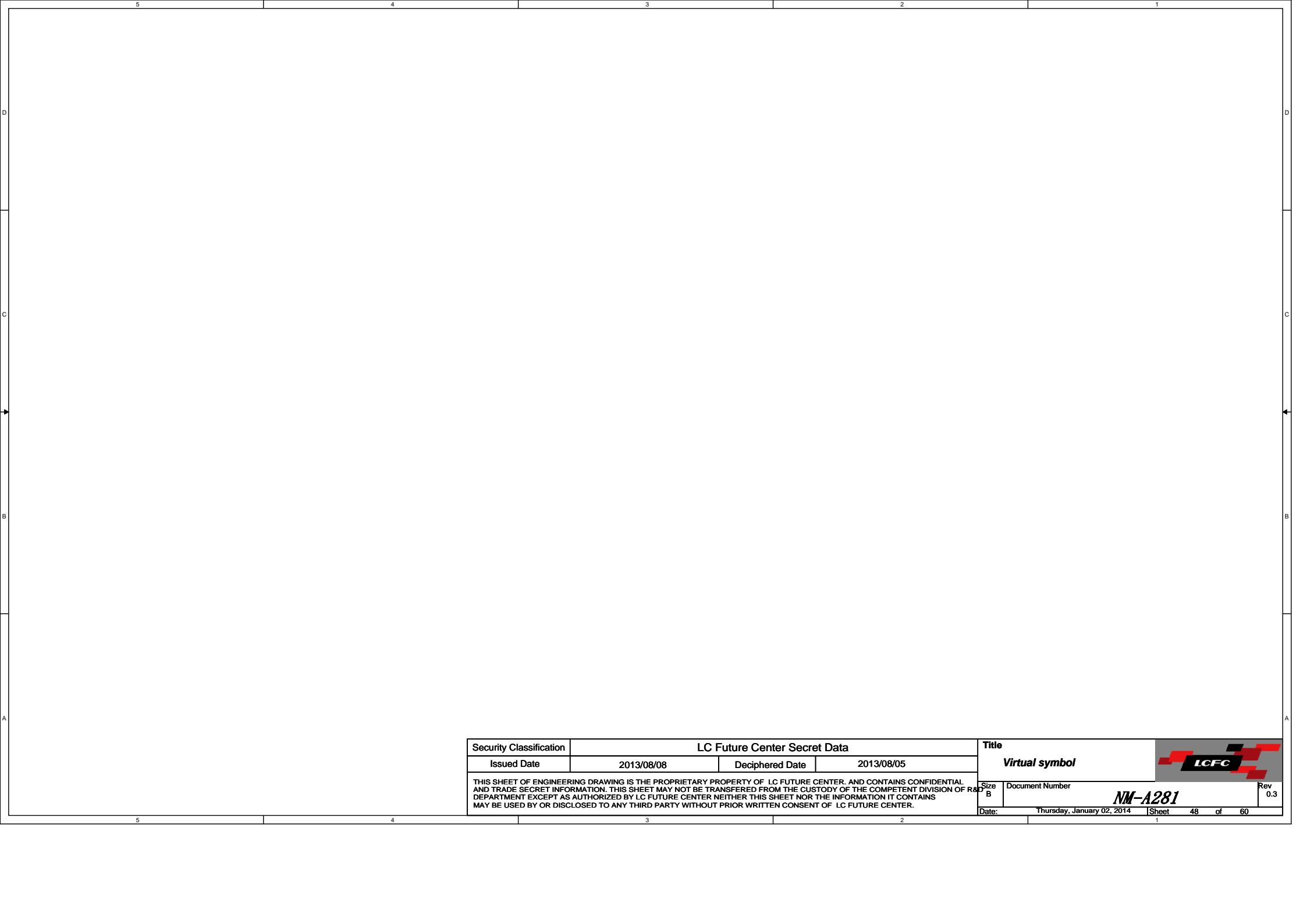
Power Sequence Block need to be update!




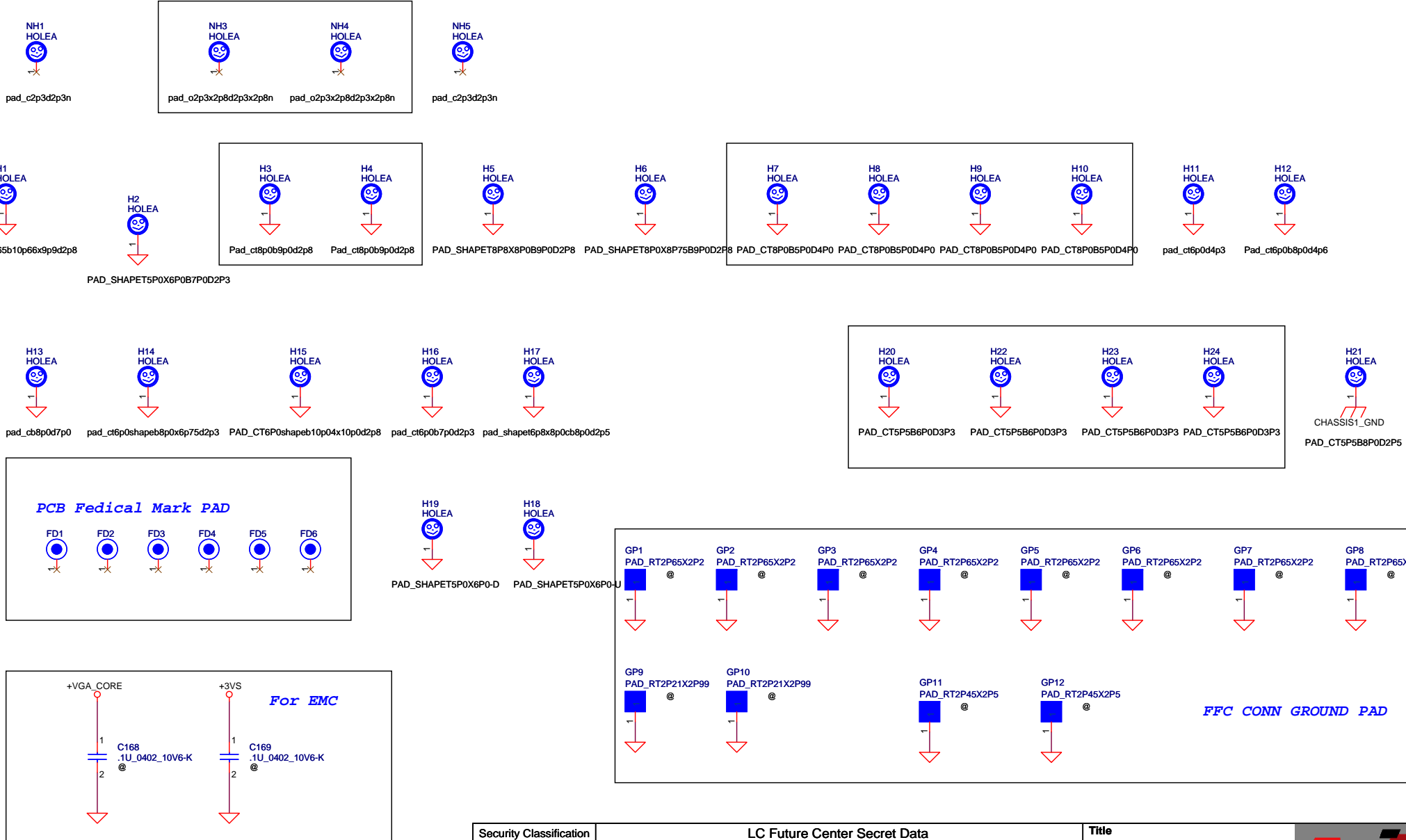
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Title	Power sequence Block	Rev	0.3
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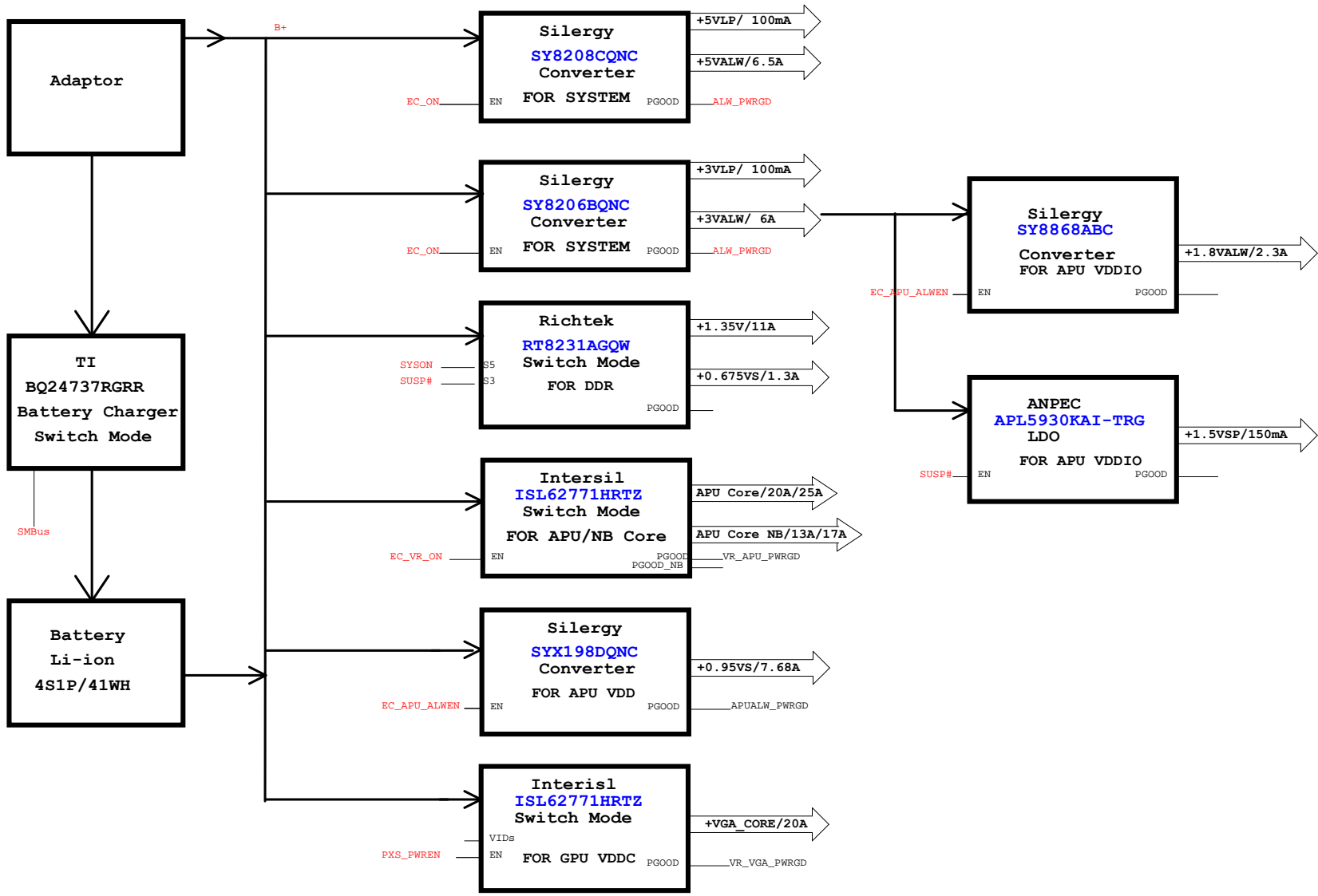


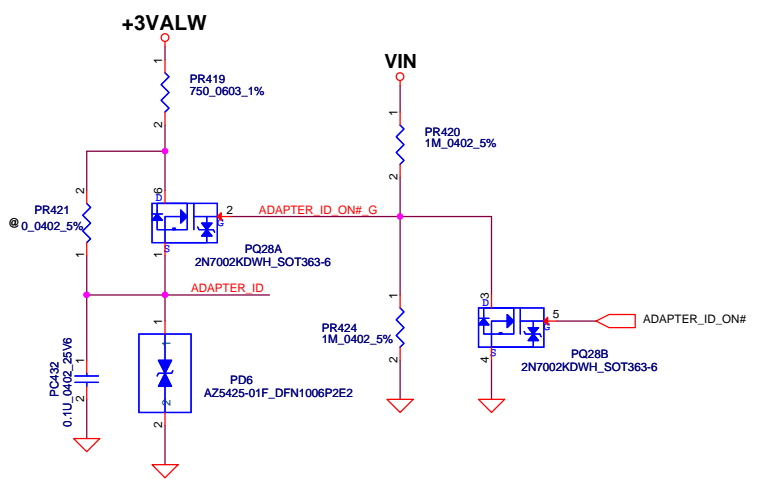
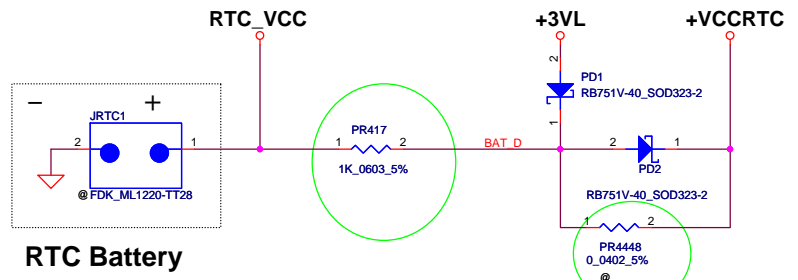
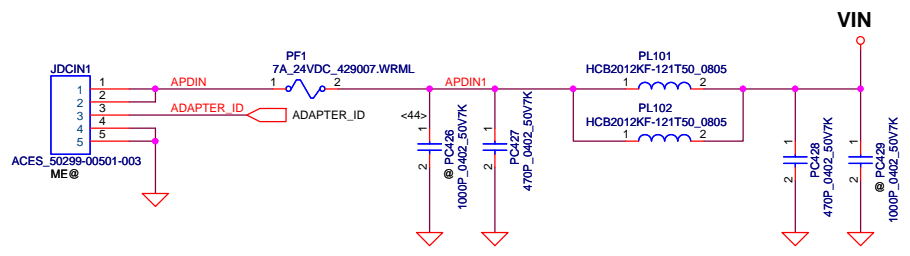


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				Date: Thursday, January 02, 2014	Rev 0.3
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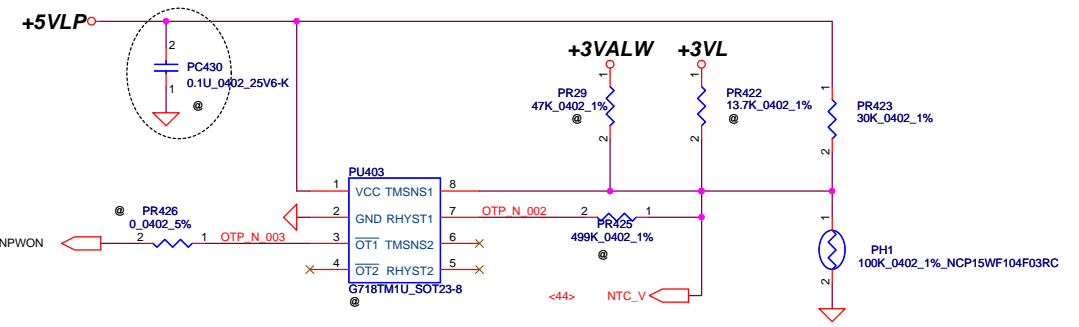


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				NM-A281	0.3
				Date: Thursday, January 02, 2014	Sheet 49 of 60

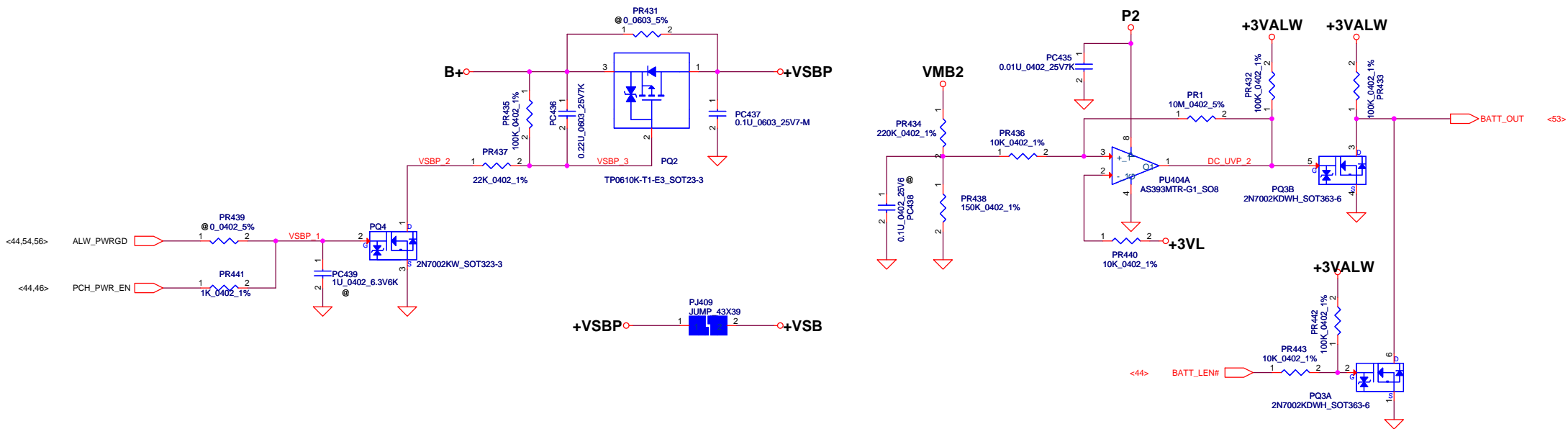
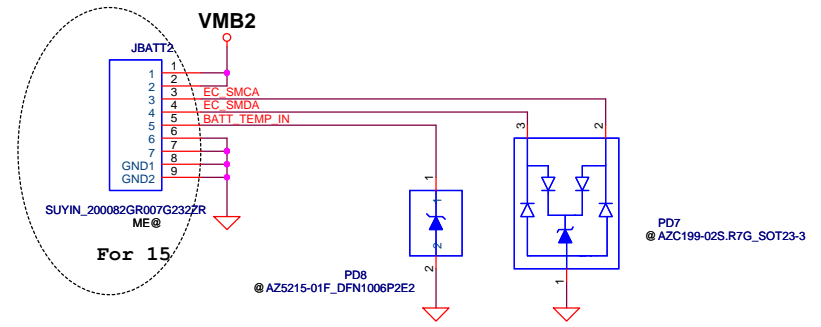
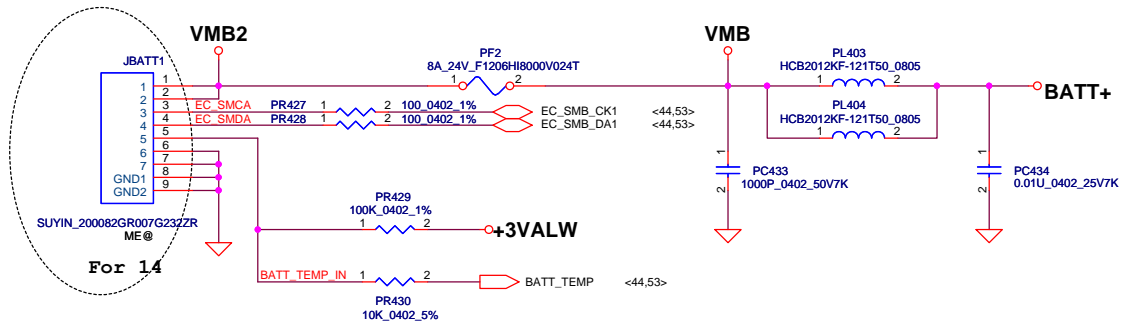




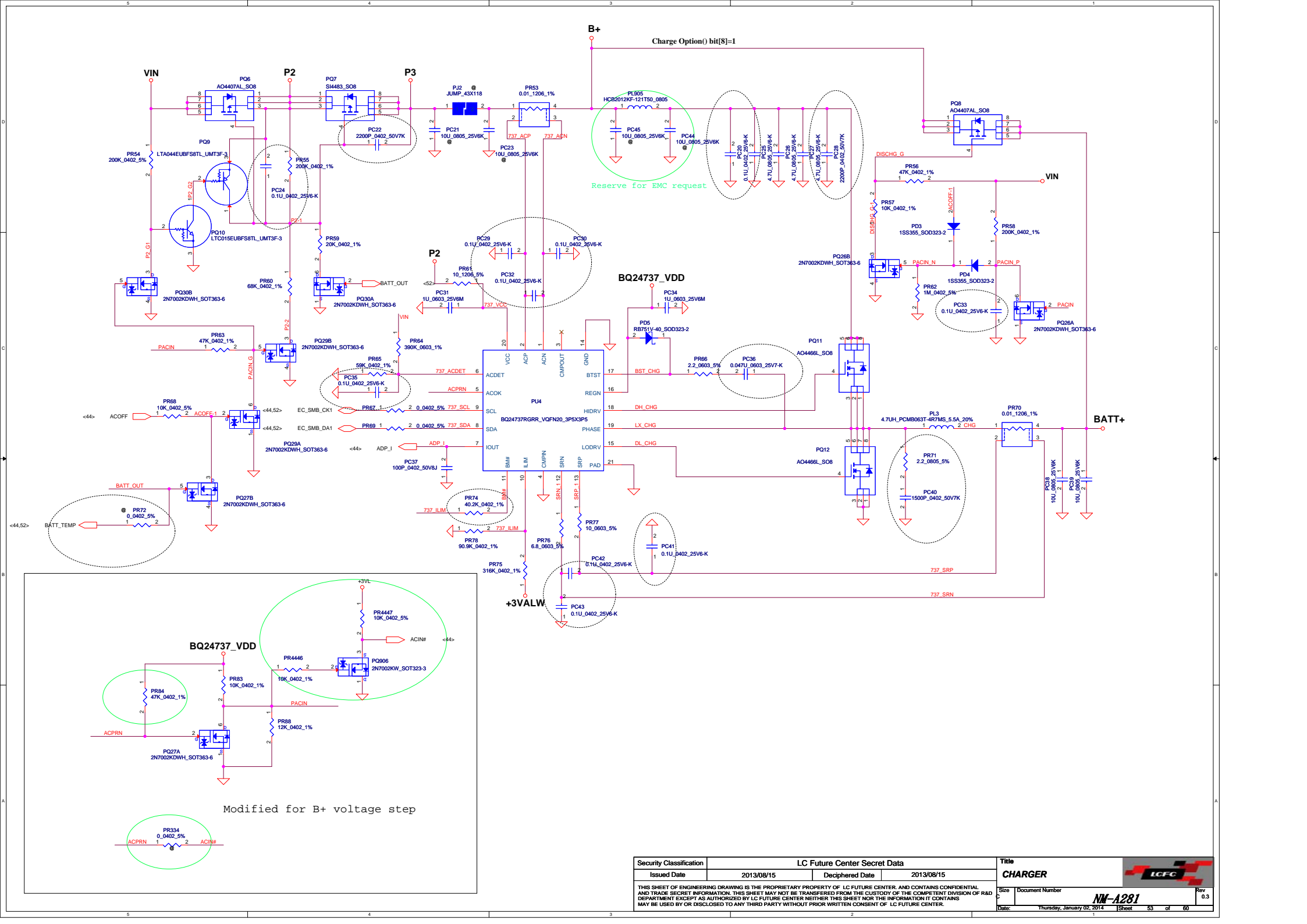
PH1 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C



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Size	Custom	Document Number	NM-A281		Rev
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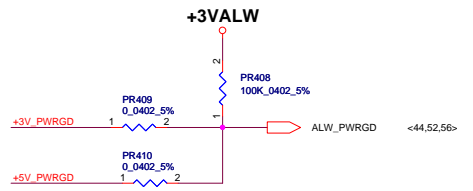
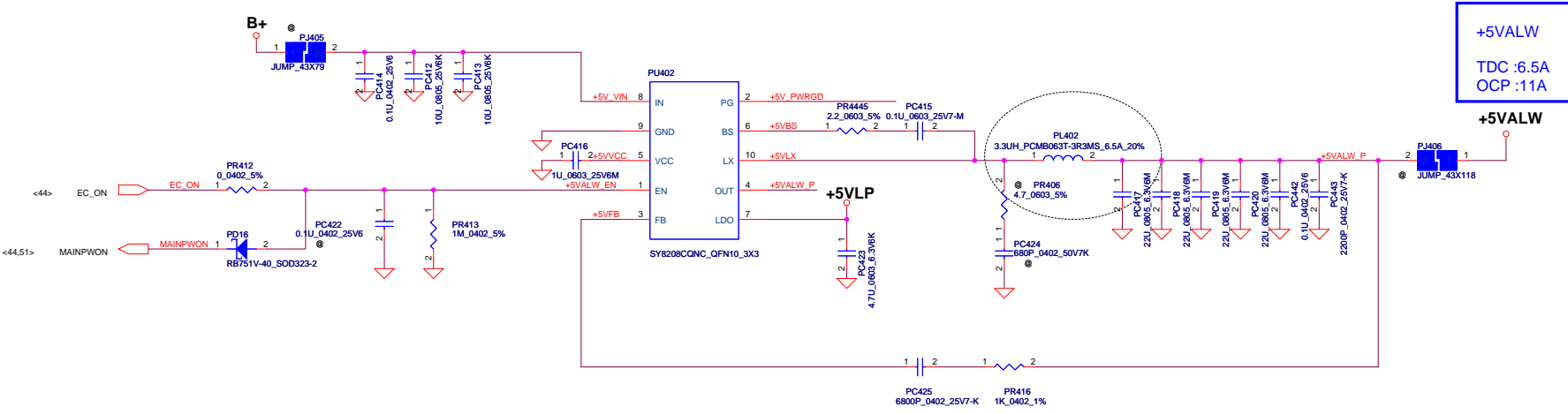
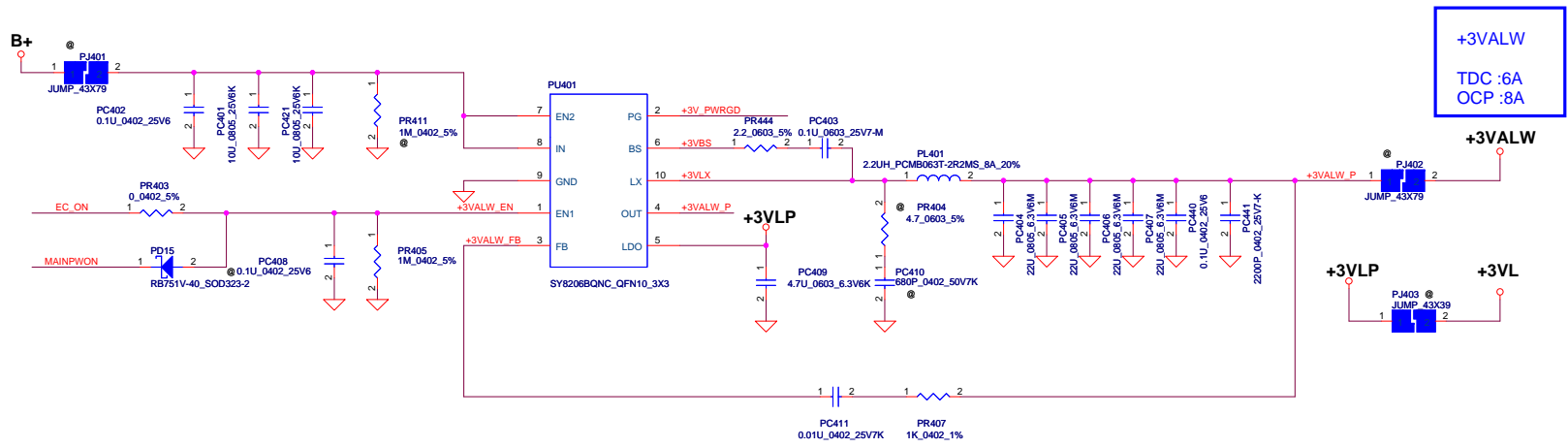


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Size	Document Number	Date		Rev	
Custom	NM-A281	Thursday, January 02, 2014		0.3	
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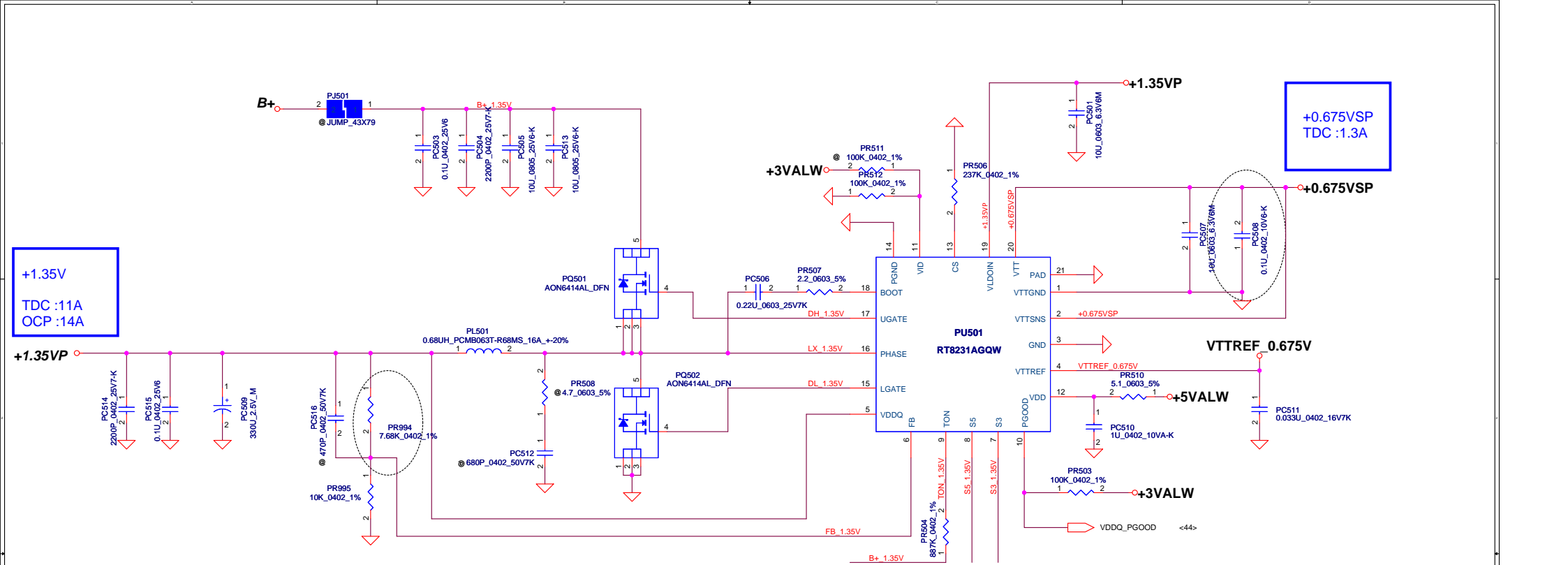


Modified for B+ voltage step

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Size	Document Number	Rev		0.3
Date:	Thursday, January 02, 2014	Sheet	53	of 60

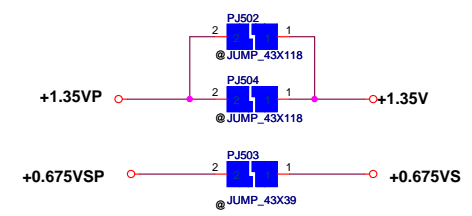
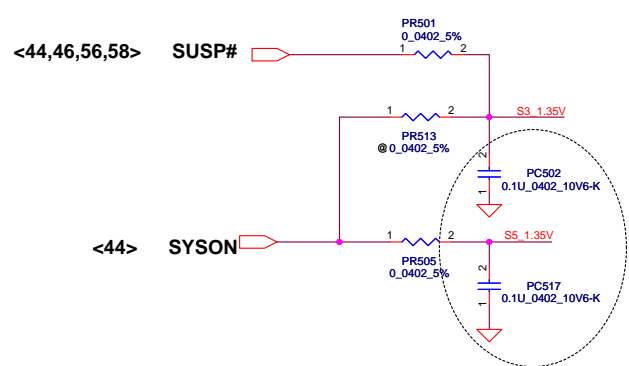


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+1.35V
TDC :11A
OCP :14A

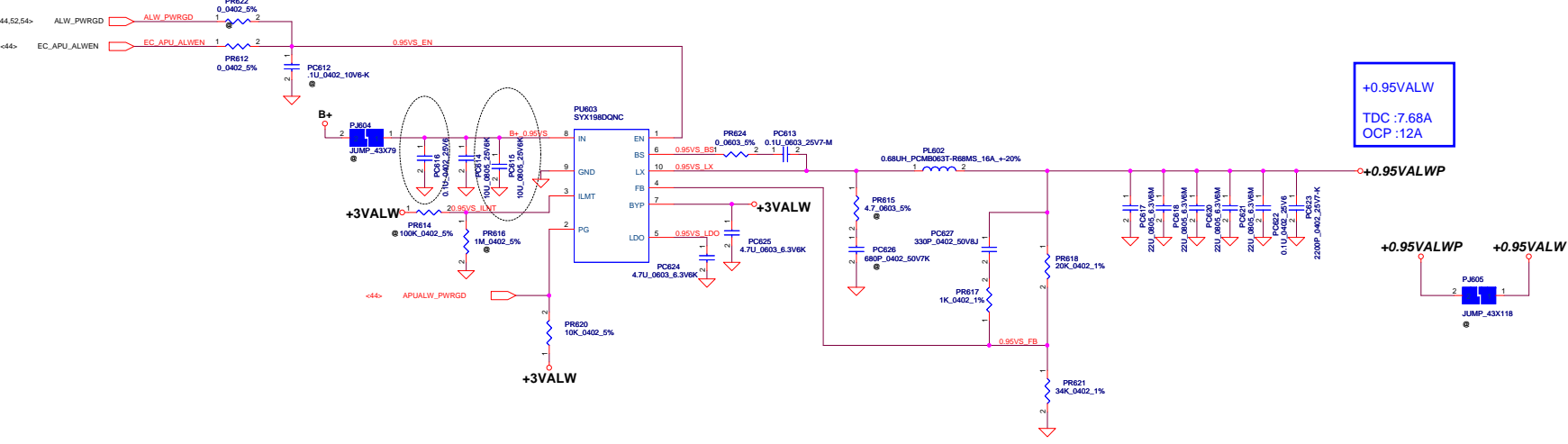
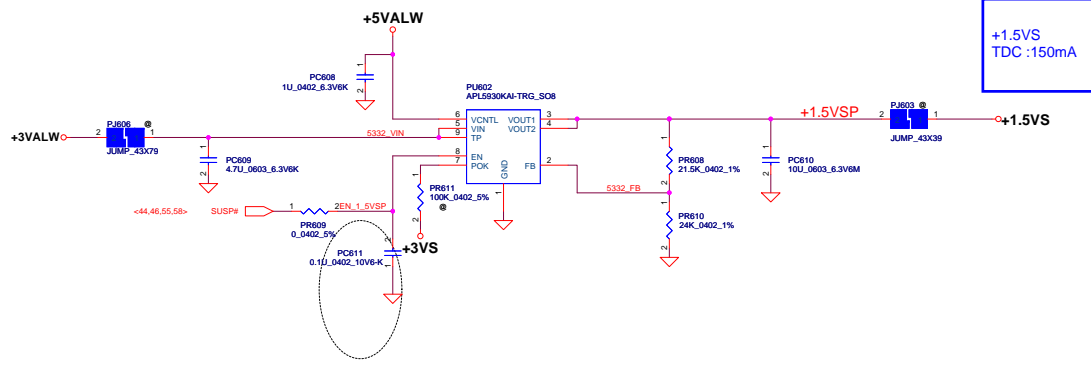
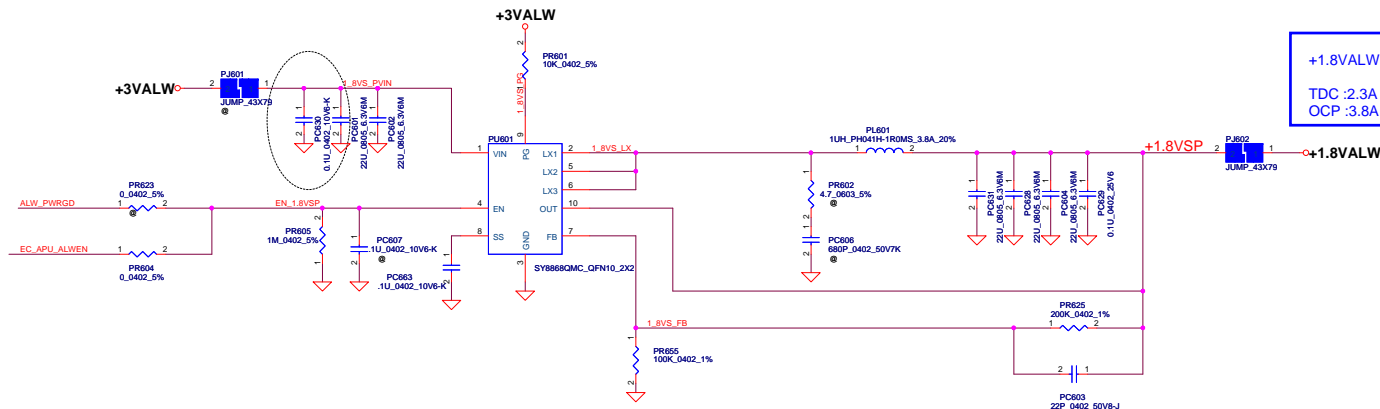
+0.675VSP
TDC :1.3A



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Title	1.35VS/+0.675VS		
Size	Document Number	NW-1281	
Rev	0.3	Date:	Thursday, January 02, 2014
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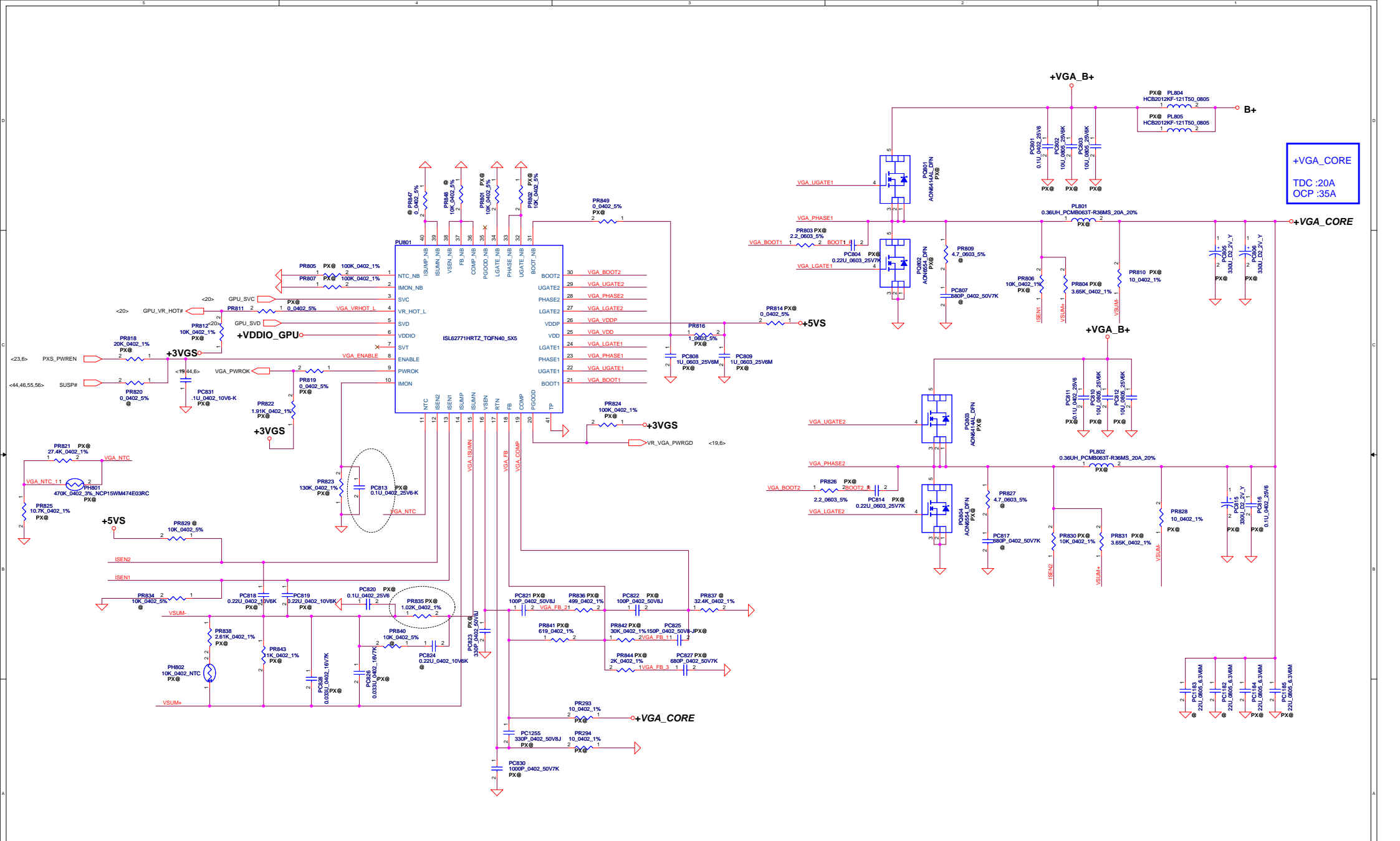


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			NM-A281
			Rev 0.3
			Date: Thursday, January 02, 2014 Sheet 56 of 60



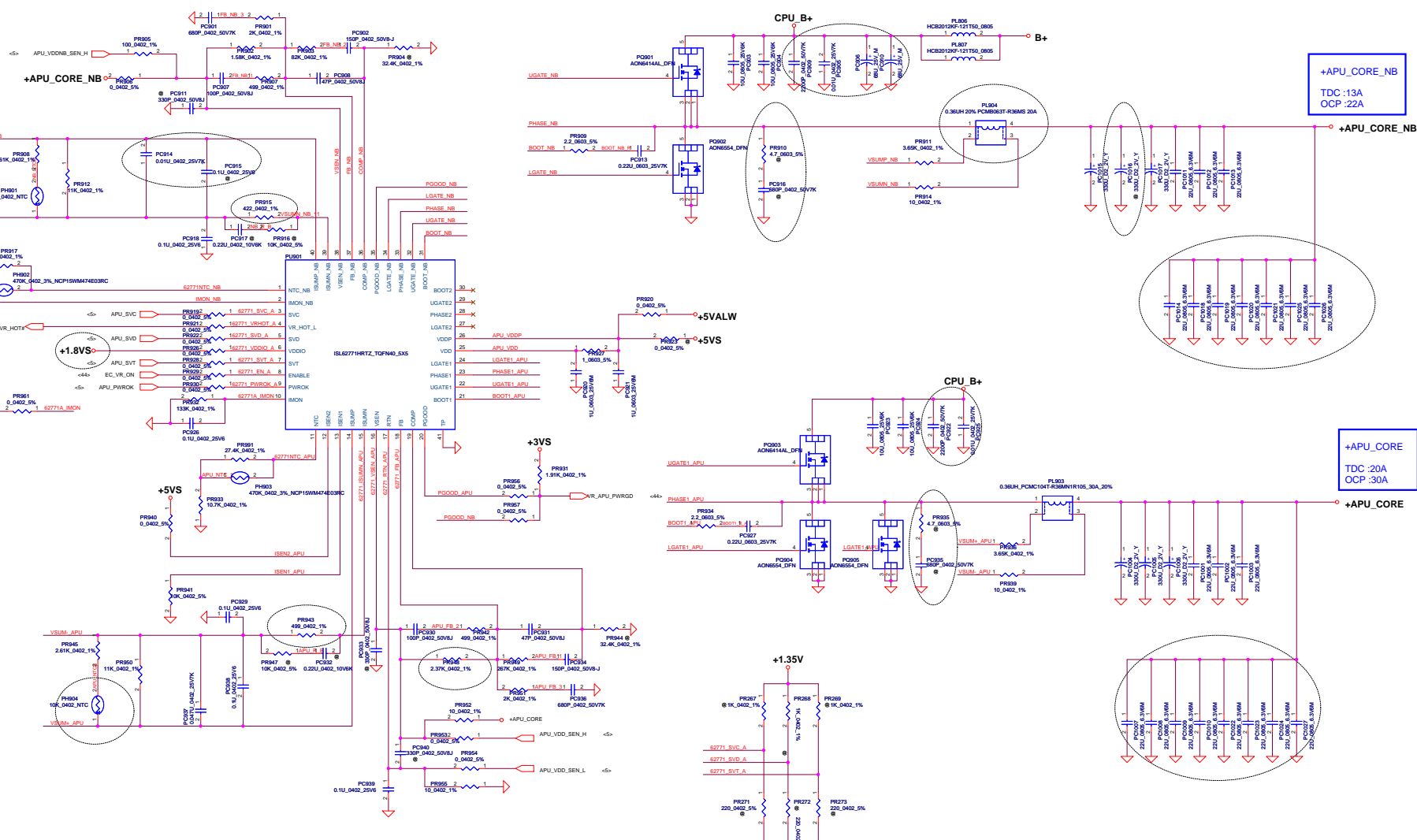


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						Custom	NM-A281	0.3
						Date:	Thursday, January 02, 2014	Sheet 57 of 60



+VGA_CORE
TDC :20A
OCP :35A

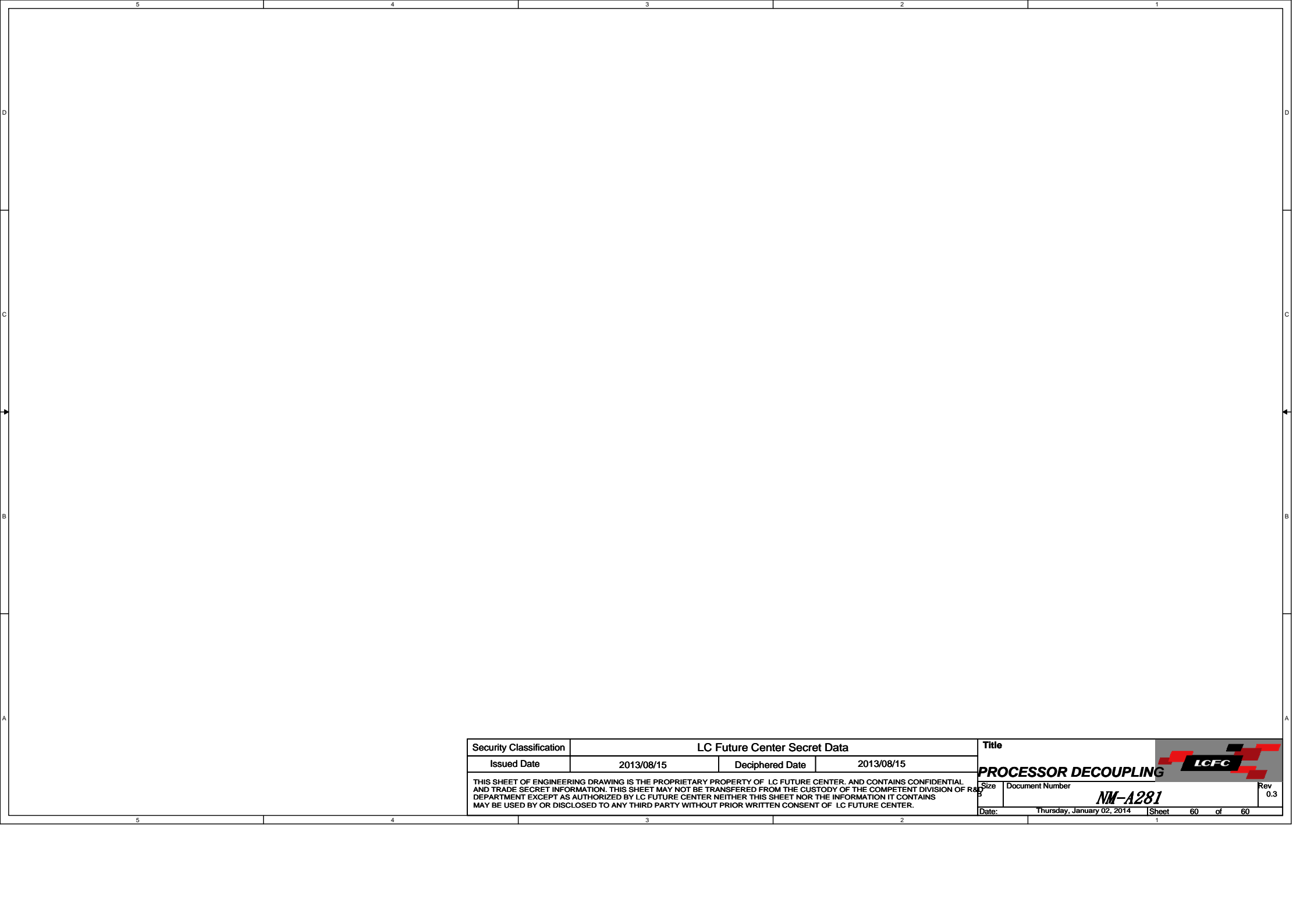
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PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	PWR_CPU Core	
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				Document Number	0.3
				Date:	Thursday, January 02, 2014
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