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# LCFC Confidential

## EG521/EG522 MB Schematics Document

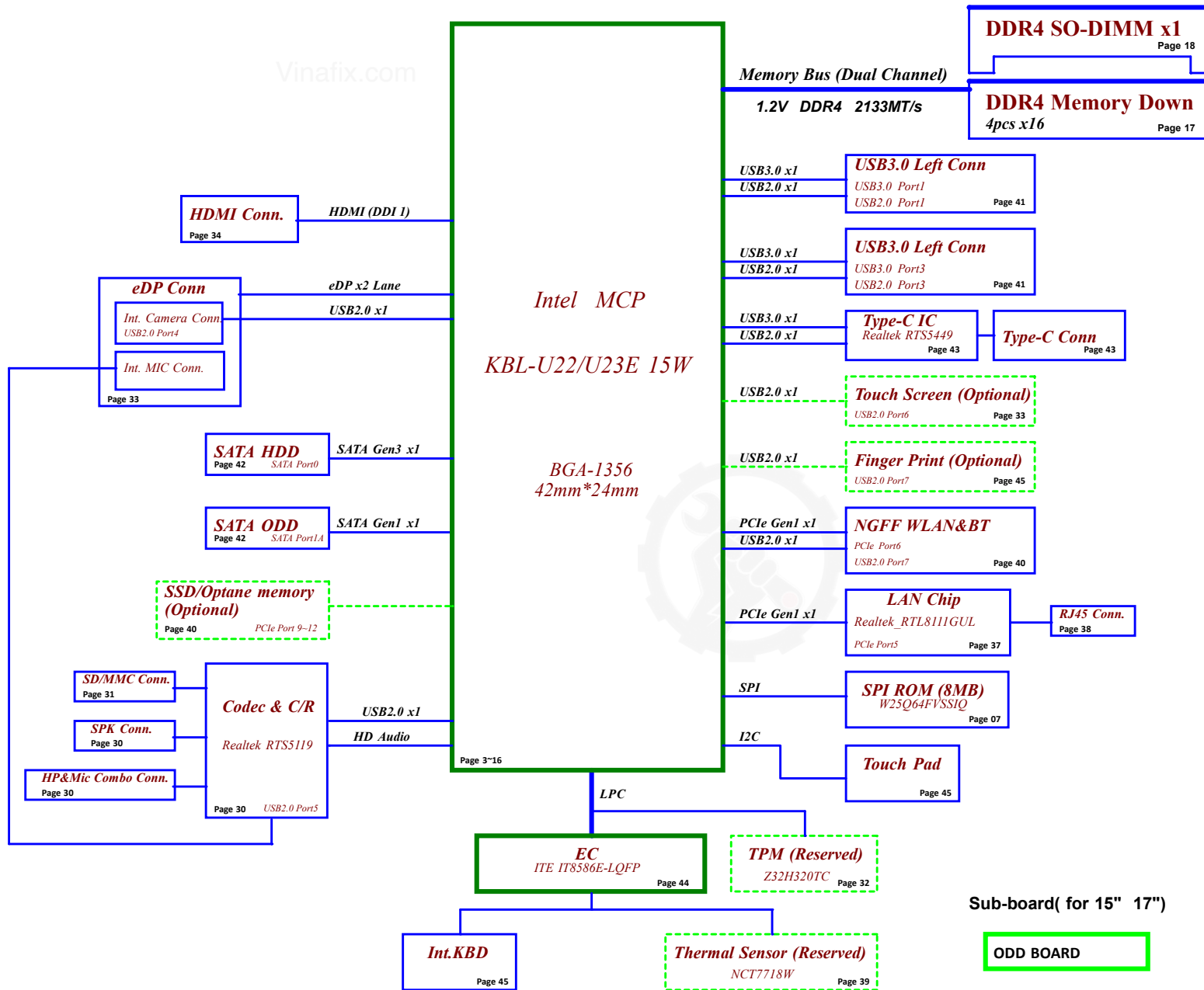
Kabylake-U42 with DDR4

2017-04-25

REV: 0.2

Security Classification	LC Future Center Secret Data		Title		
Issued Date	2015/08/20	Deciphered Date	2016/08/20		Cover Page
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**Voltage Rails ( 0 --> Means ON , X --> Means OFF )**

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4 AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIe	1~4 X4 PCIe DGPU
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9~12 X4 PCIe Optane Memory
	0 HDD
	1A ODD
SATA	1B used as PCIe
	2 used as PCIe

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAM rank part
DUALRANK@	For dual VRAM rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

**SMBUS Control Table**

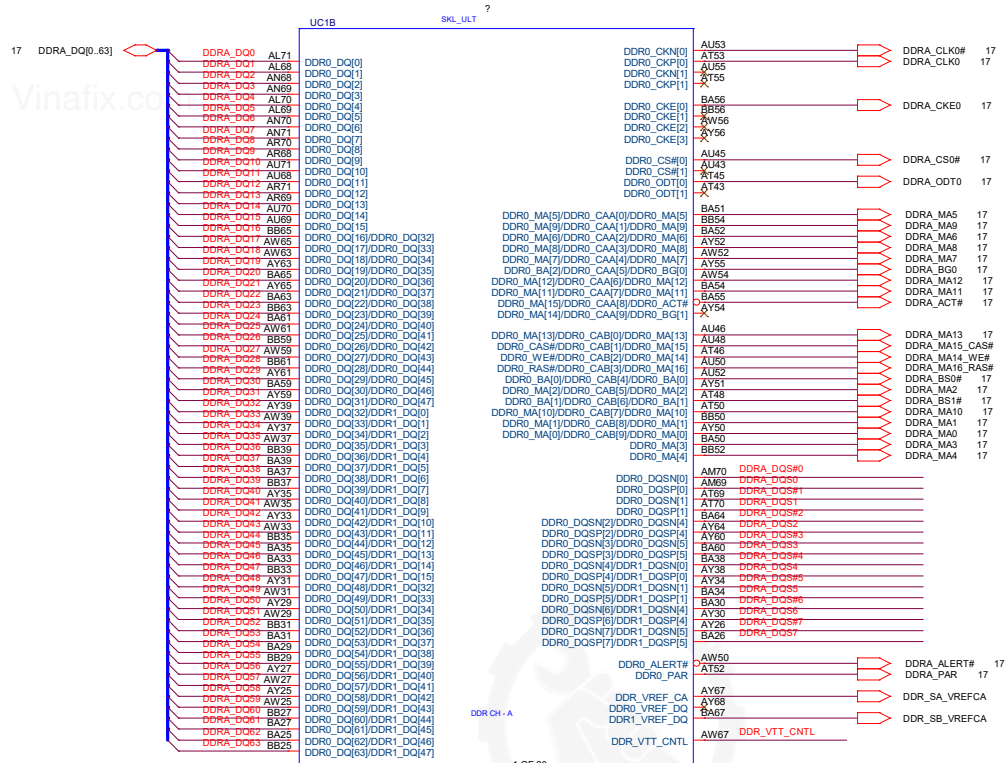
	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

**EC SMBus1 address      EC SMBus2 address      EC SMBus3 address      PCH SM Bus address**

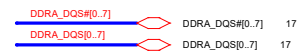
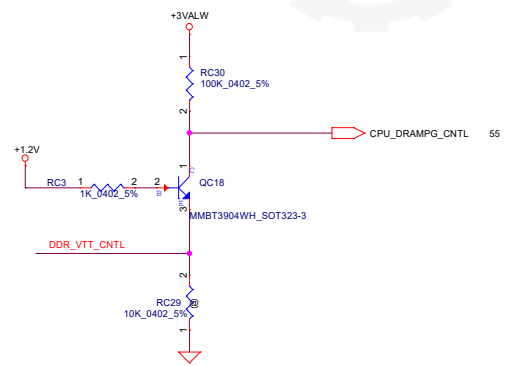
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update			Wlan	Reserved

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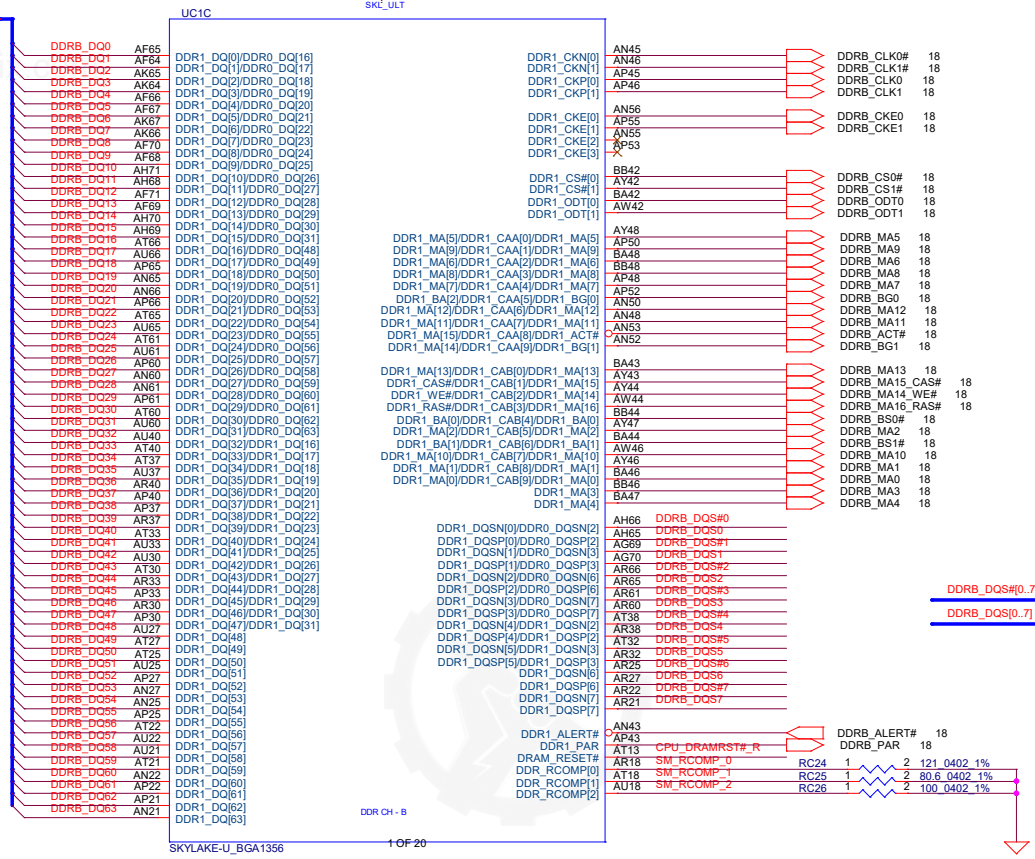
SKYLAKE-U\_BGA1356  
REV = 1



SMVREF  
WIDTH: 2.0MIL  
SPACING: 2.0MIL

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18 DDRB\_DQ[0..63]



UC1C

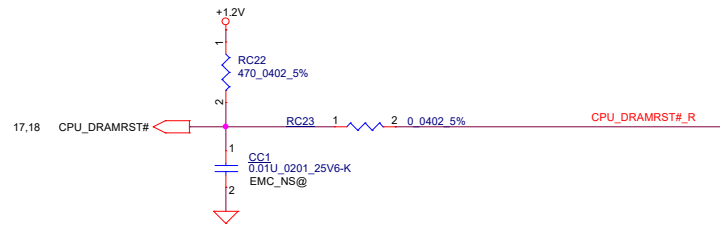
SKL\_ULT

DDR CH - B

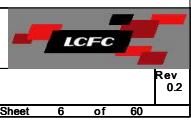
SKYLAKE-U BGA1356

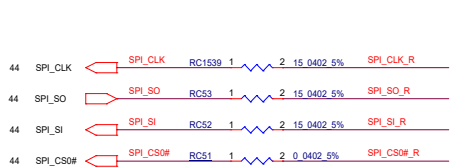
REV = 1

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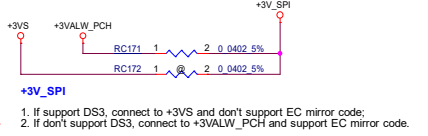
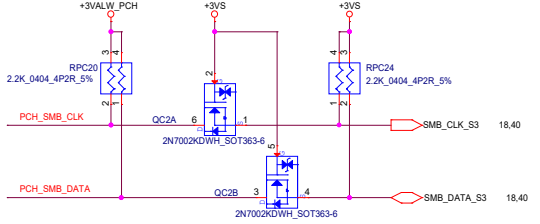
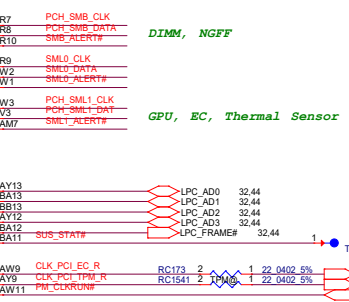
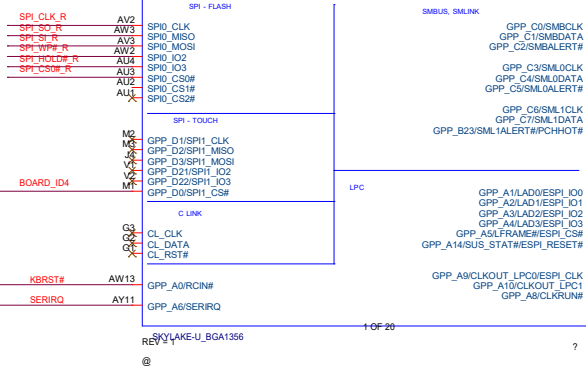


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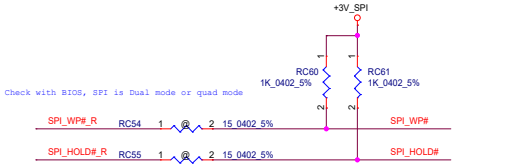
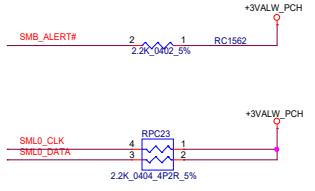
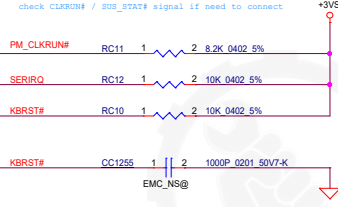




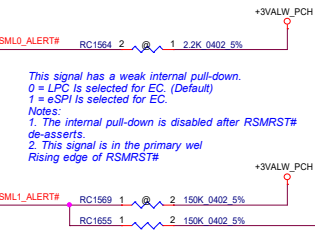
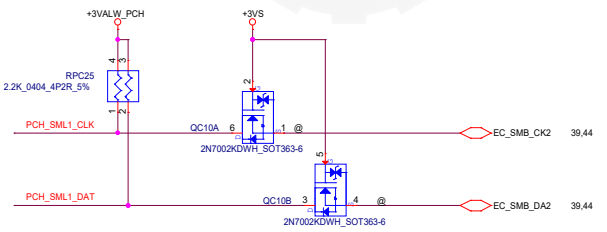
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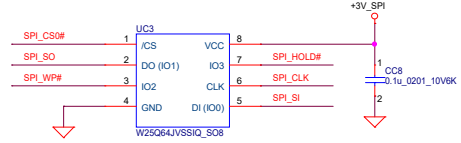
- 1. If support DS3, connect to +3VS and don't support EC mirror code;
- 2. If don't support DS3, connect to +3VALW\_PCH and support EC mirror code.



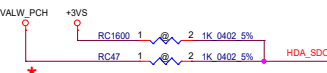
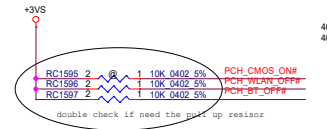
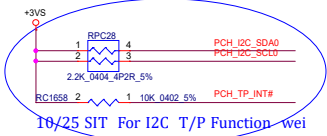
Check with B108, SPI is Dual mode or quad mode



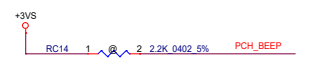
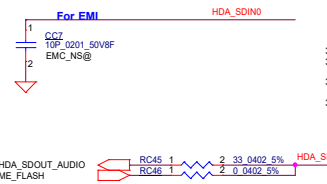
This signal has a weak internal pull-down.  
 0 = LPC Is selected for EC. (Default)  
 1 = eSPI Is selected for EC.  
 Notes:  
 1. The internal pull-down is disabled after RSMRST# de-asserts  
 2. This signal is in the primary well  
 Rising edge of RSMRST#  
 To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST#. (Refer to WW52\_MOW)



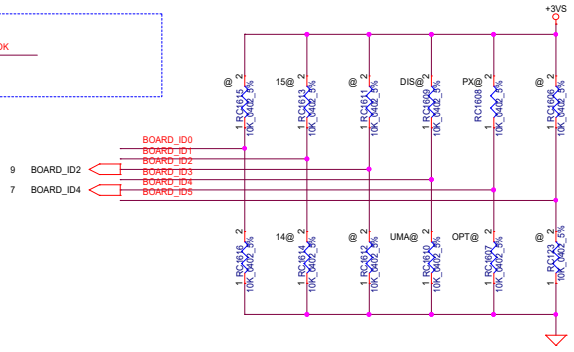
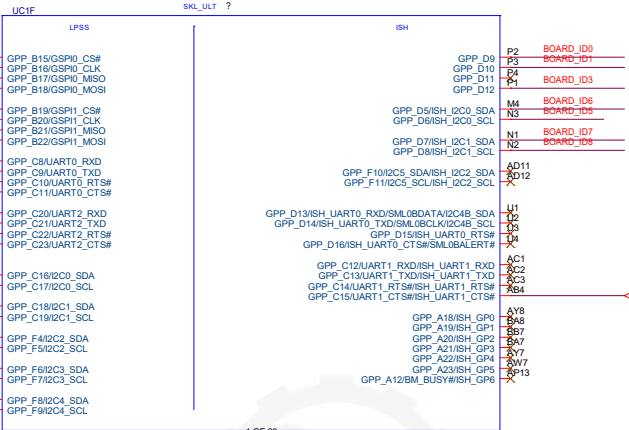
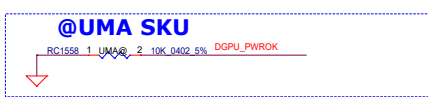
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	MCP (MISC, JTAG, SPI, LPC, SML1, SML0)
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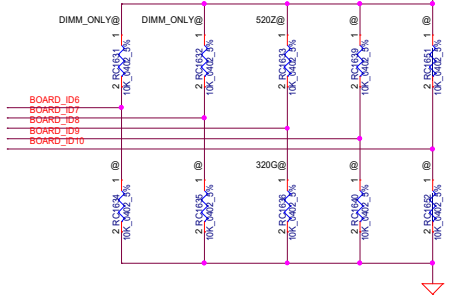
**HDA\_SDO** This signal has a weak internal pull-down.  
 0 = Enable security measures defined in the Flash Descriptor.  
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0 MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1 MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) 1 = LPC	0	Rising edge of PCH_PWROK



Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1614
	01 15"	RC1616 RC1613
	10 17"	RC1615 RC1614
	11 Reserved	RC1615 RC1613
Board_ID2	0 Reserved	RC1612
	1 Reserved	RC1611
Board_ID3	0 UMA	RC1610
	1 DIS	RC1609
Board_ID4	0 NV GPU	RC1607
	1 AMD GPU	RC1608
Board_ID5	0 Reserved	RC123
	1 Reserved	RC1606

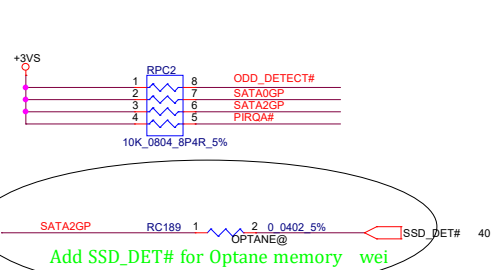
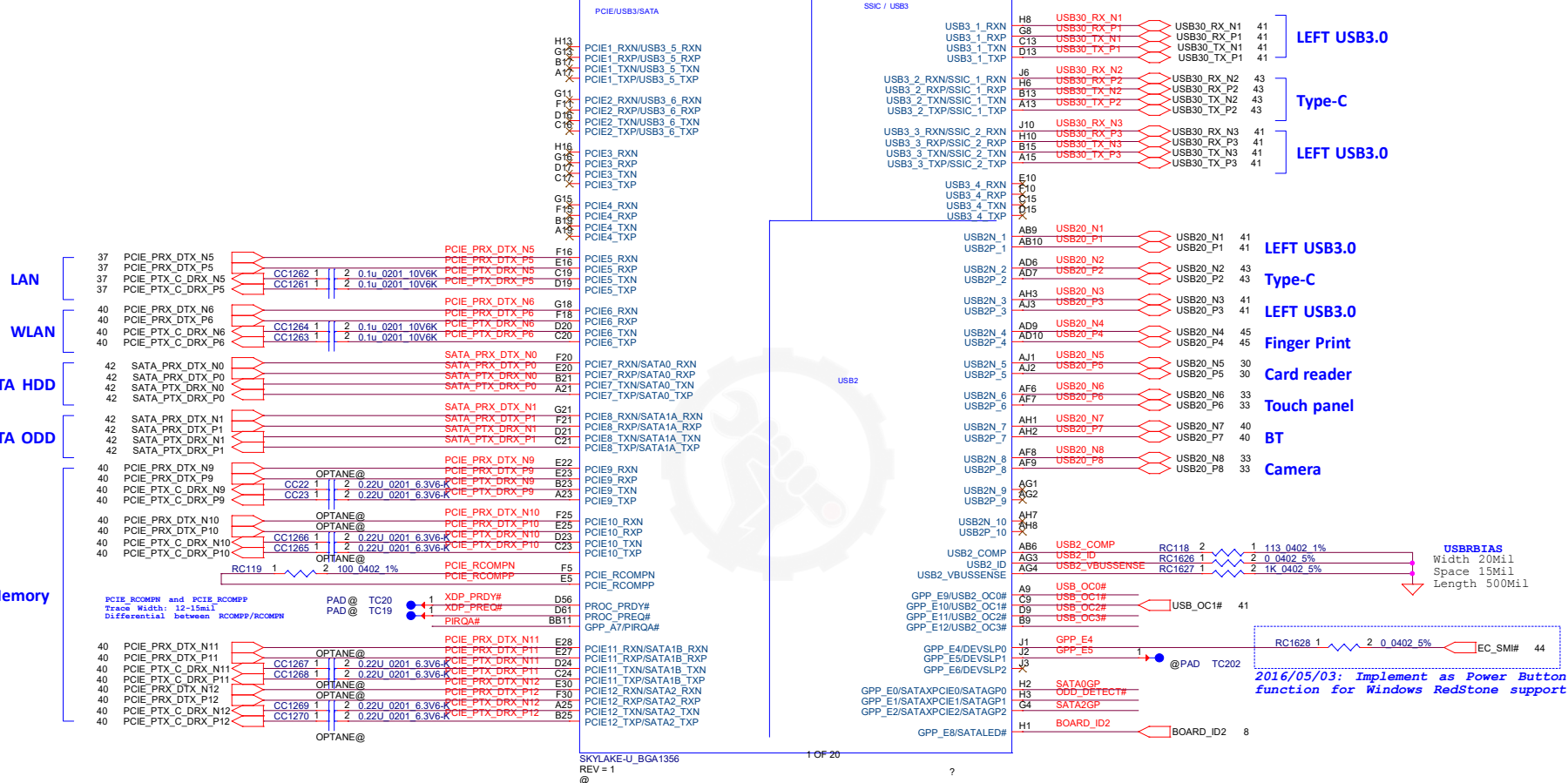


Board ID	Description	Stuff R
Board ID [6,7]	00 Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01 Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10 Micron 8Gb 2400 MT/s	RC1631 RC1635
	11 SO-DIMM Only	RC1631 RC1632
Board_ID8	0 320G	RC1636
	1 520Z	RC1633
Board_ID9	0 Reserved	RC1640
	1 Reserved	RC1639
Board_ID10	0 Reserved	RC1652
	1 Reserved	RC1651

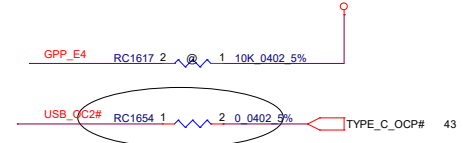


UC1H

SKL\_UL1 ?



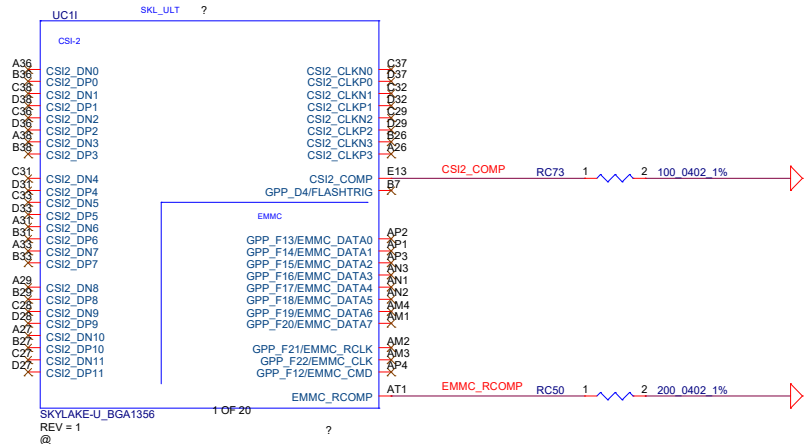
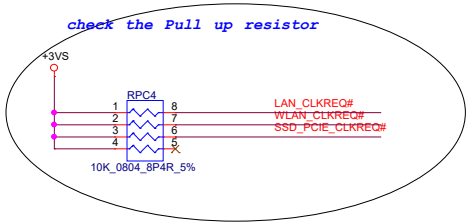
Add SSD\_DET# for Optane memory wei



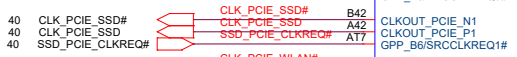
8/24 Reserve TYPE\_C\_OCP# to CPU USB\_OC2# wei

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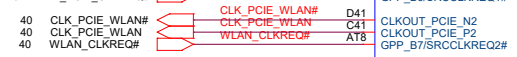
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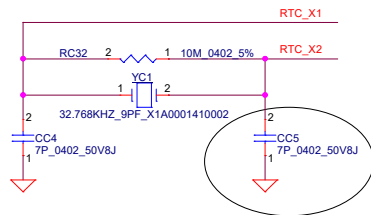
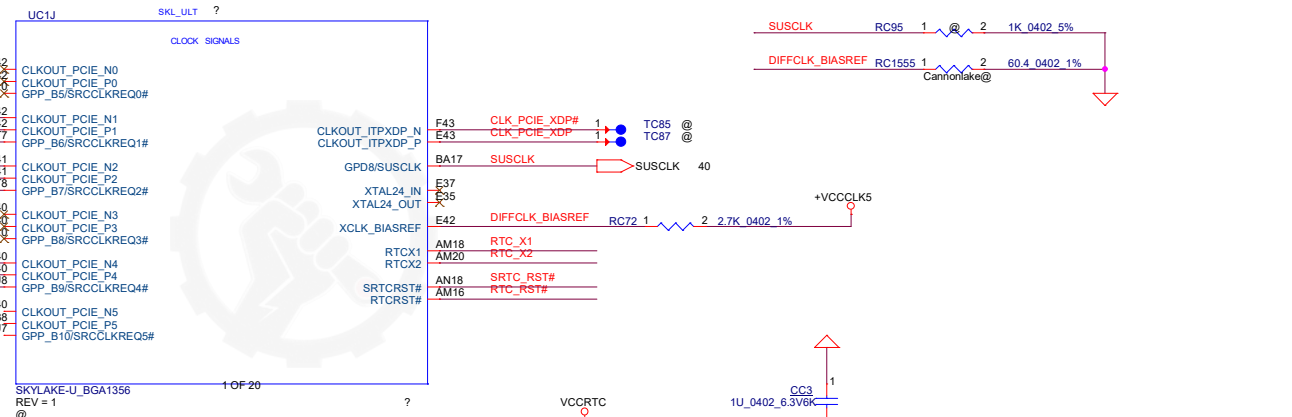
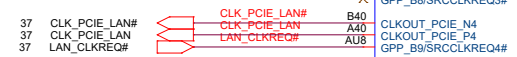
Optane memory



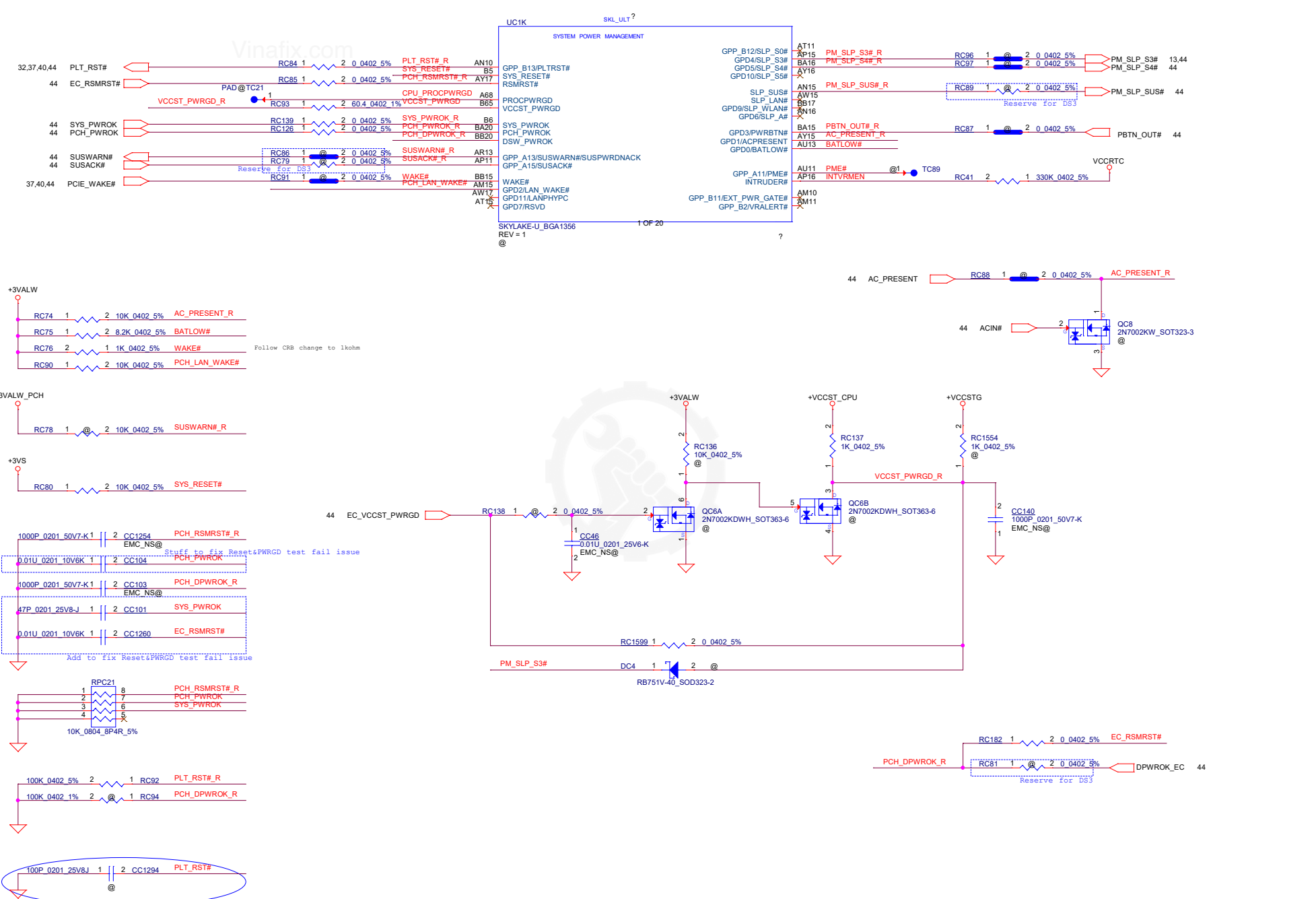
PCIE CLK5 WLAN



PCIE CLK4 LAN



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Follow CRB change to 1kohm

Stuff to fix Reset&PWRGD test fail issue

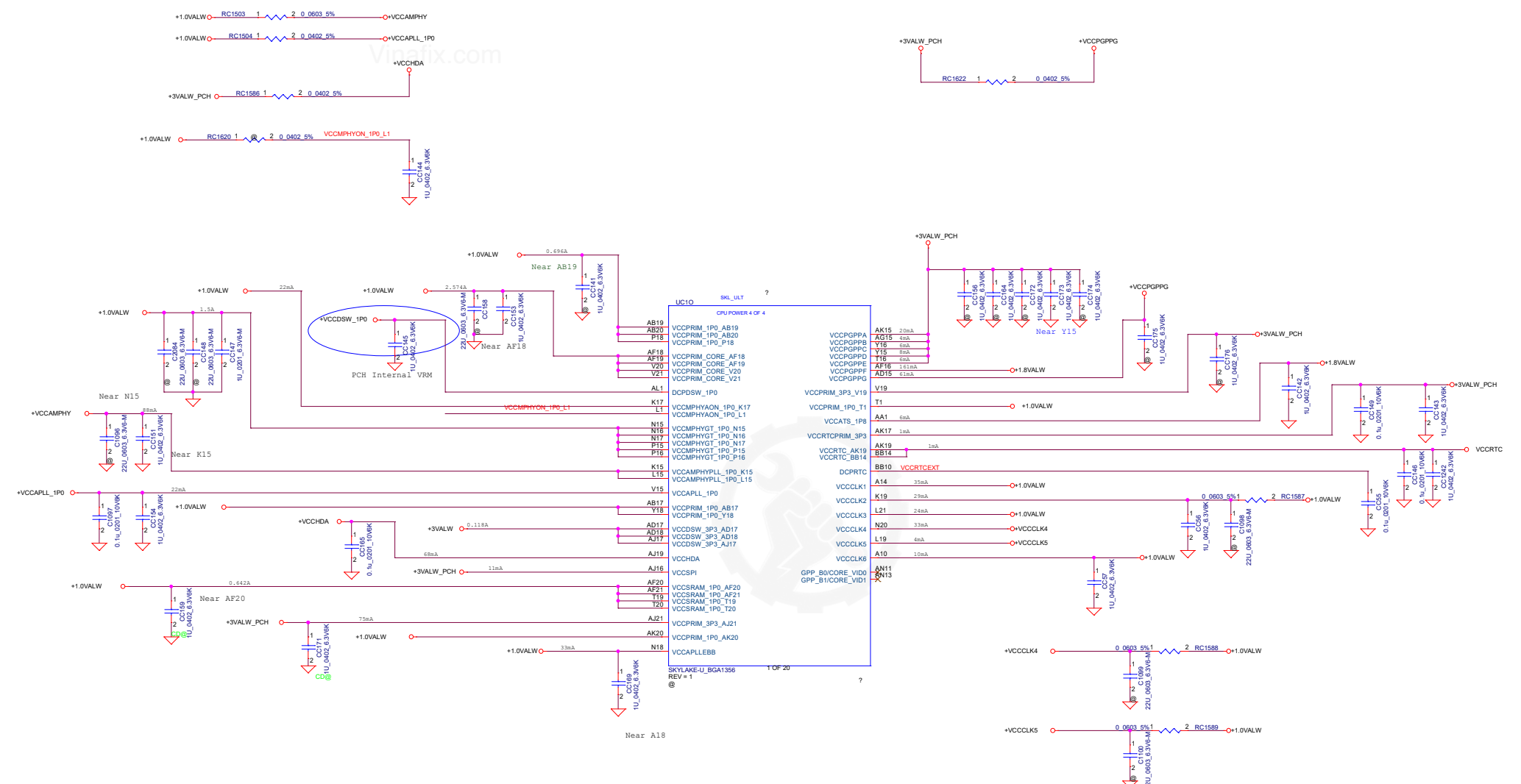
Add to fix Reset&PWRGD test fail issue

10/25 SIT Add to fix PLT\_RST# glitch issue wei

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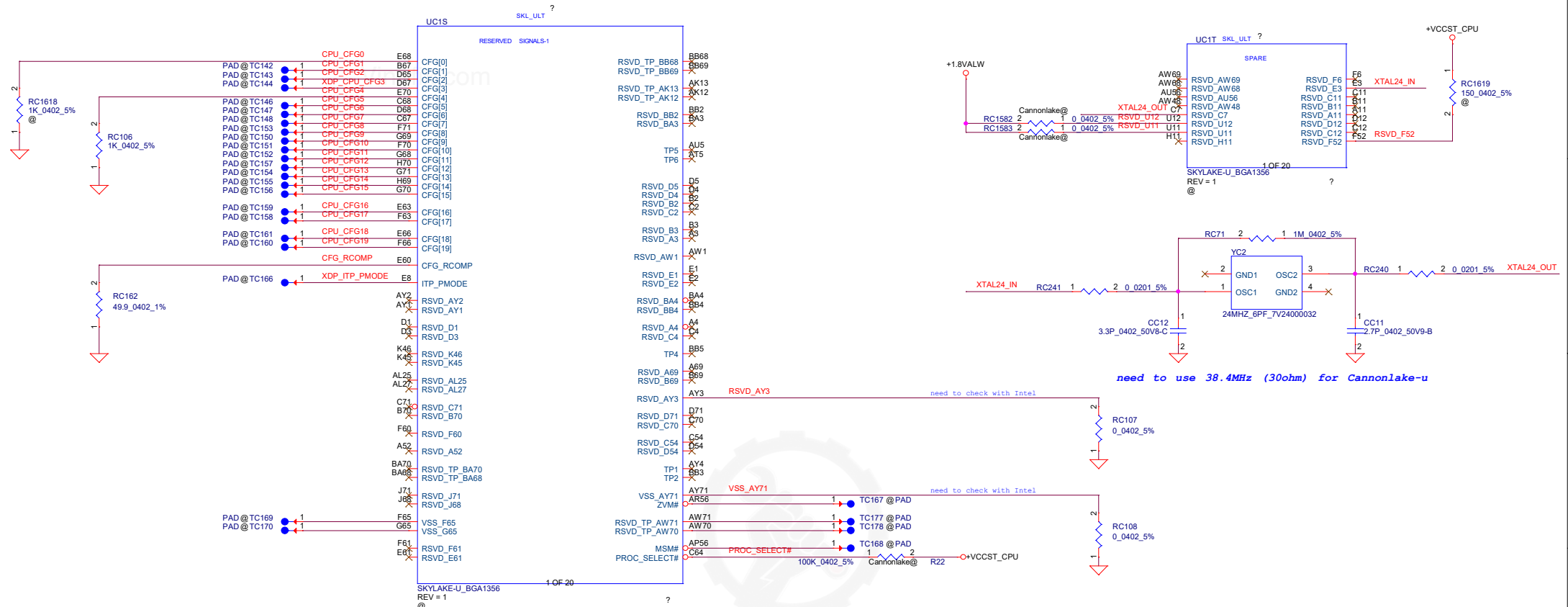






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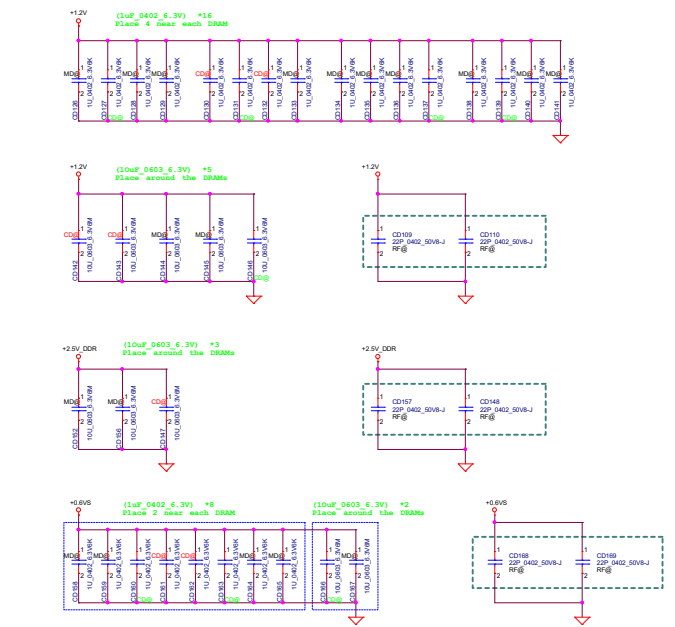
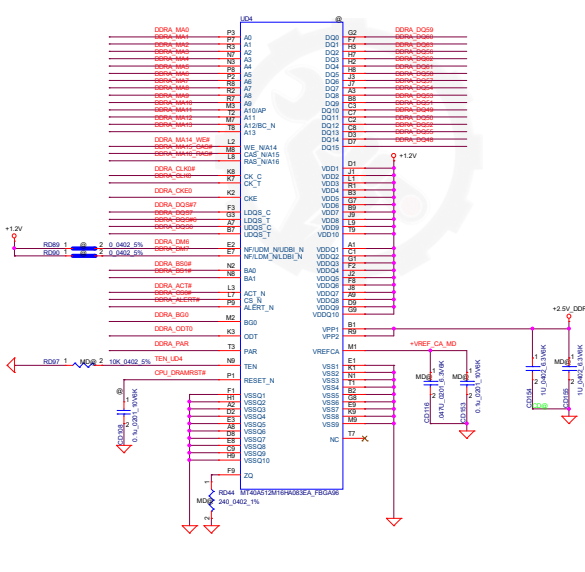
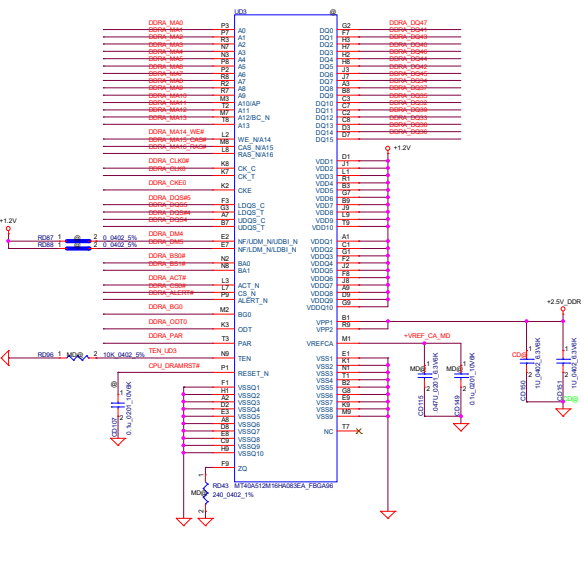
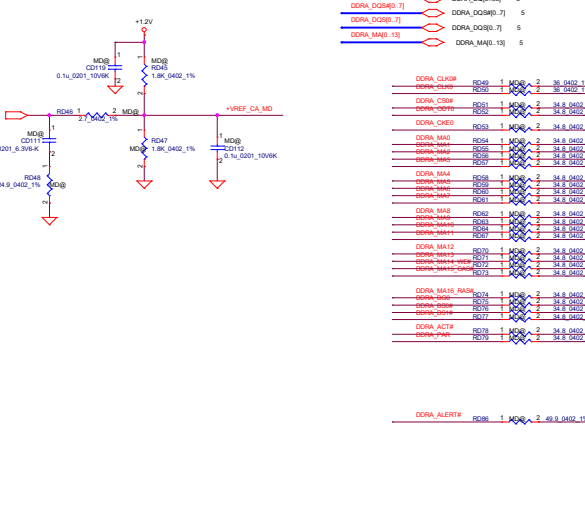
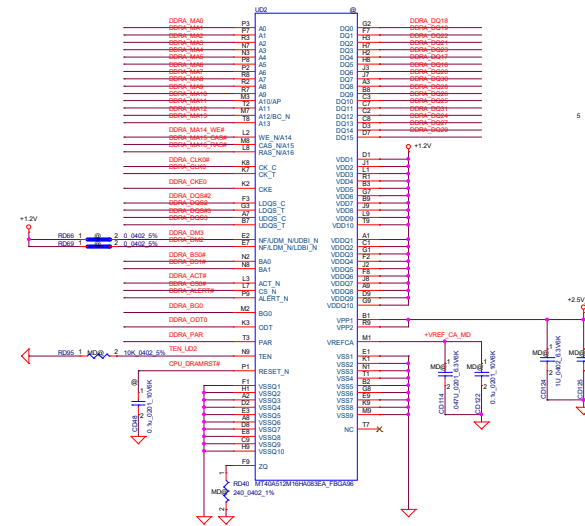
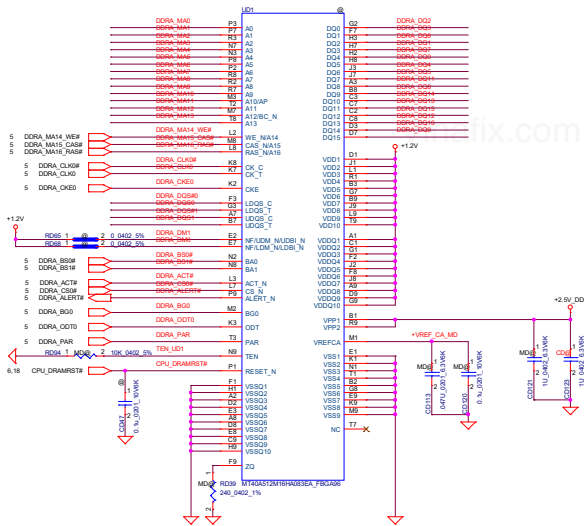
Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled *	1

Security Classification	LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date
		2016/08/20

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MCP (CFG,RESERVED)		
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Custom	EG521	0.2
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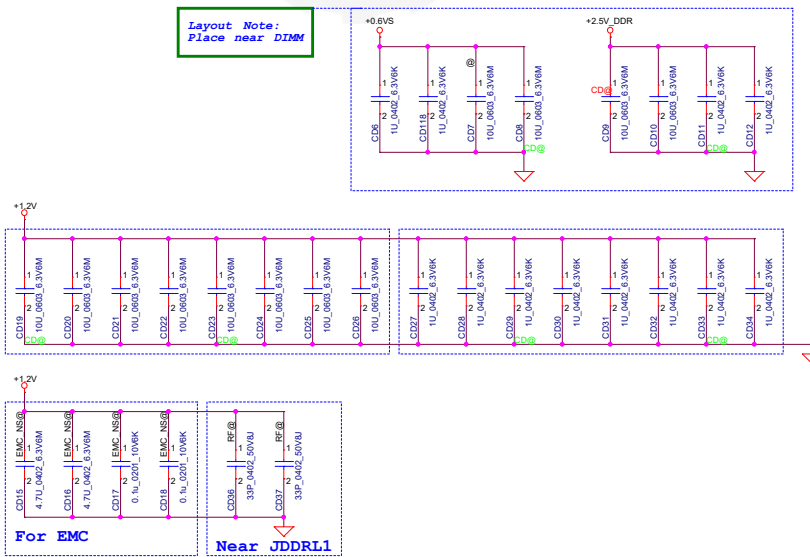
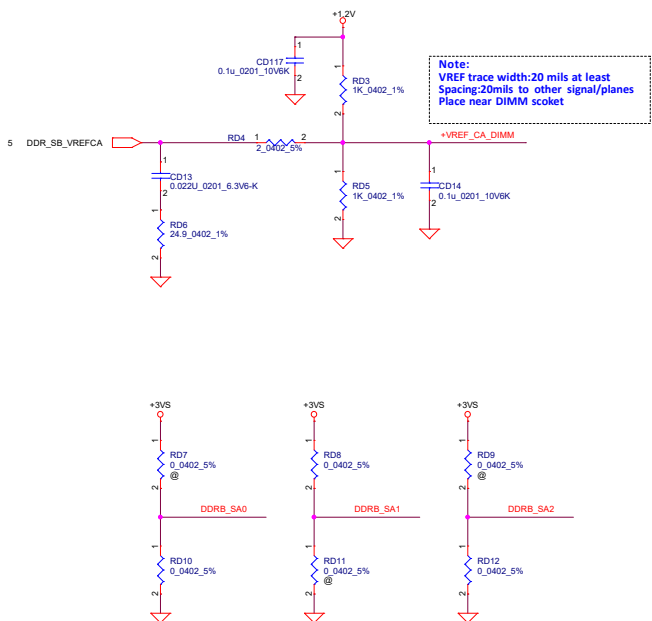
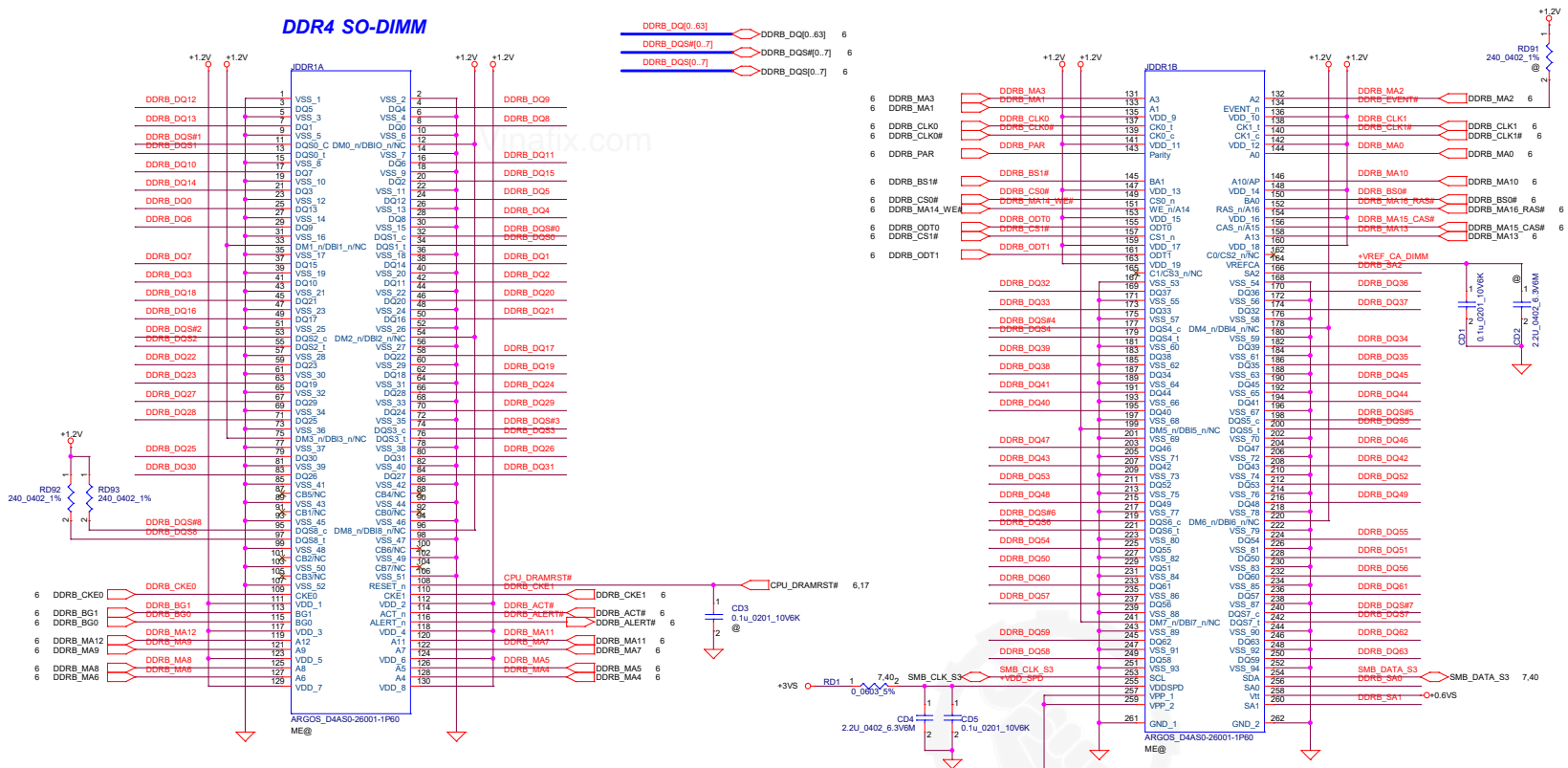




- DDR4\_DQ0\_08
- DDR4\_DQ0\_07
- DDR4\_DQ0\_06
- DDR4\_DQ0\_05
- DDR4\_DQ0\_04
- DDR4\_DQ0\_03
- DDR4\_DQ0\_02
- DDR4\_DQ0\_01
- DDR4\_DQ0\_00

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File Name	Document Number	Revision	Rev
DDR4	EG523	0.2	0.2
Date	Issued Date	Revised	By
	2018/12/14		

# DDR4 SO-DIMM




SPD Address = 2H

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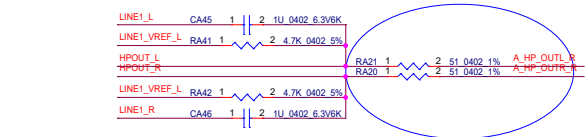
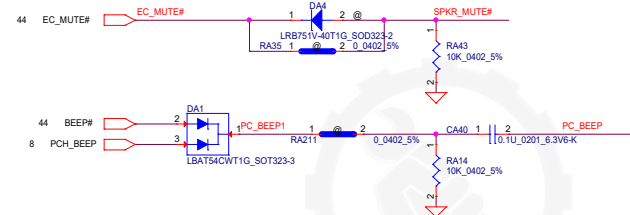
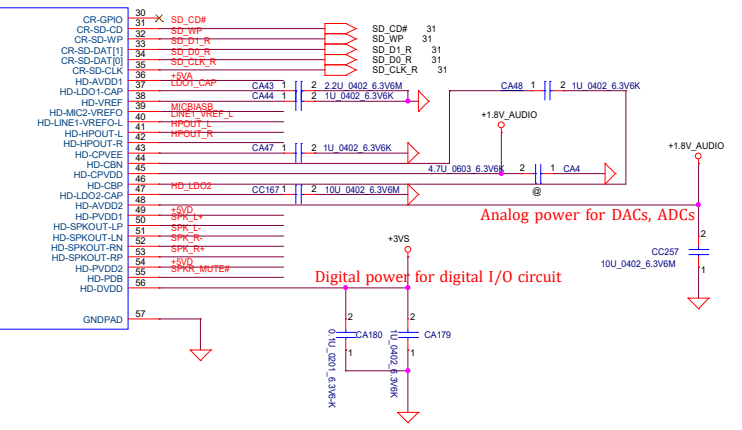
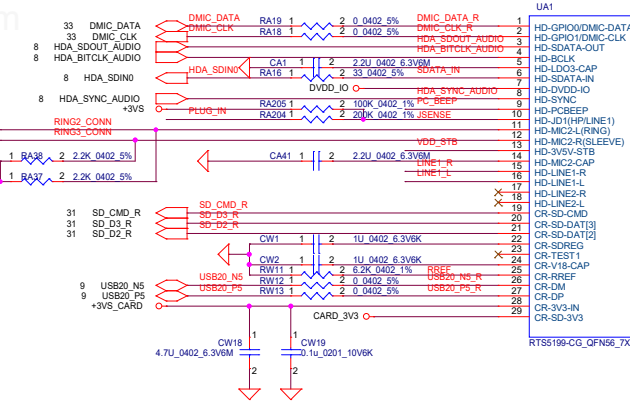
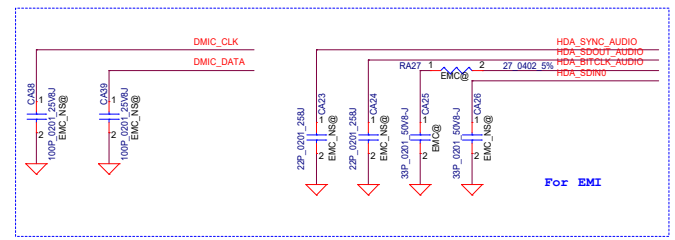
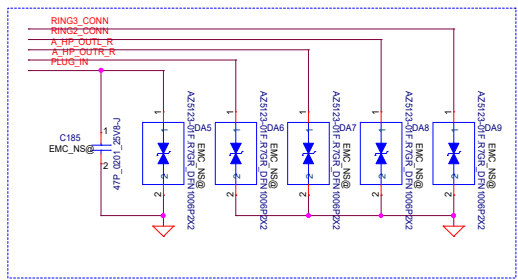
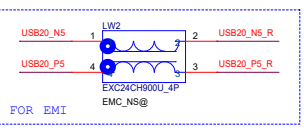
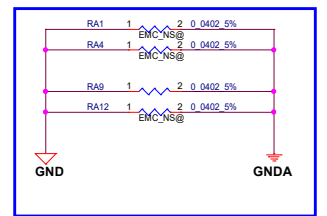
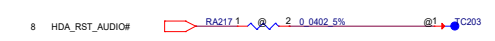
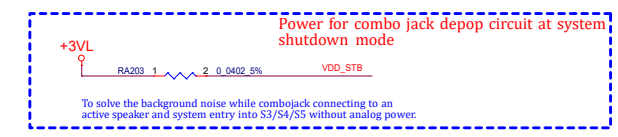
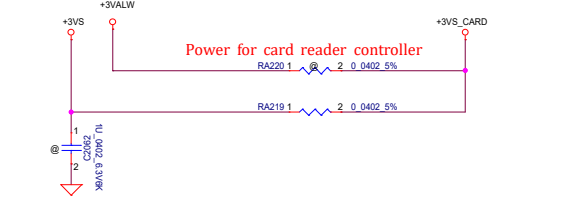
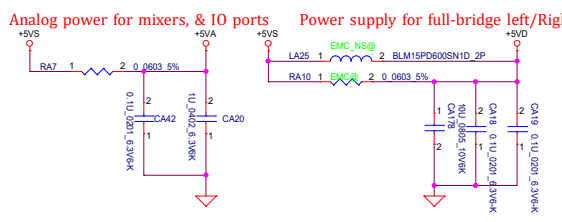
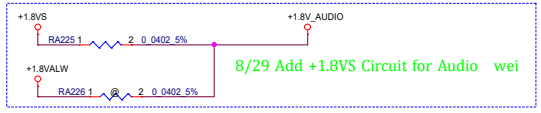
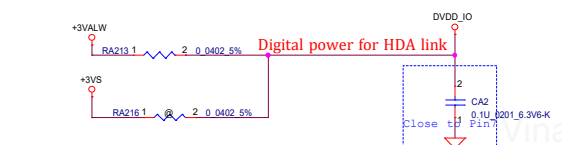


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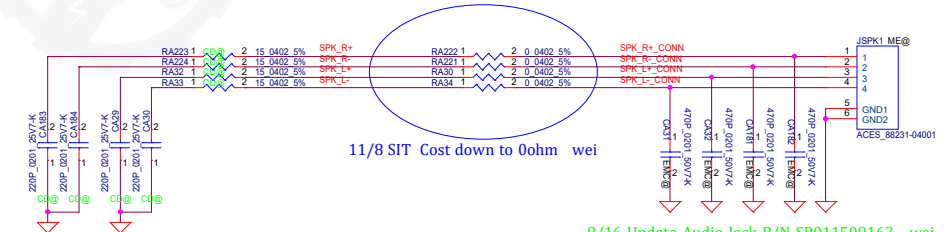
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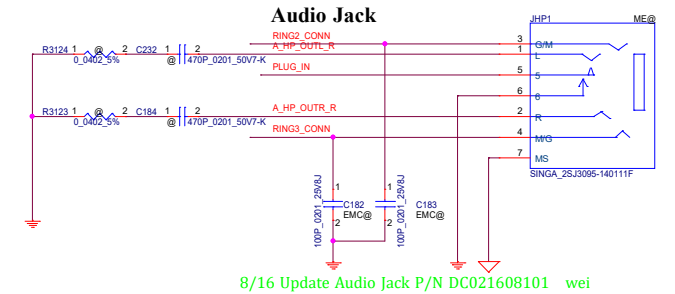
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11/8 SIT Vendor suggestion form 47 ohm change to 51om wei

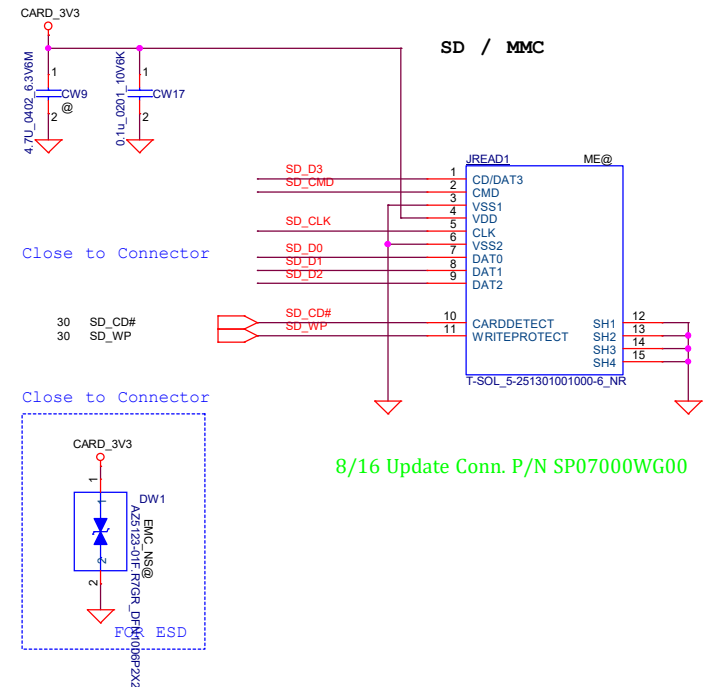
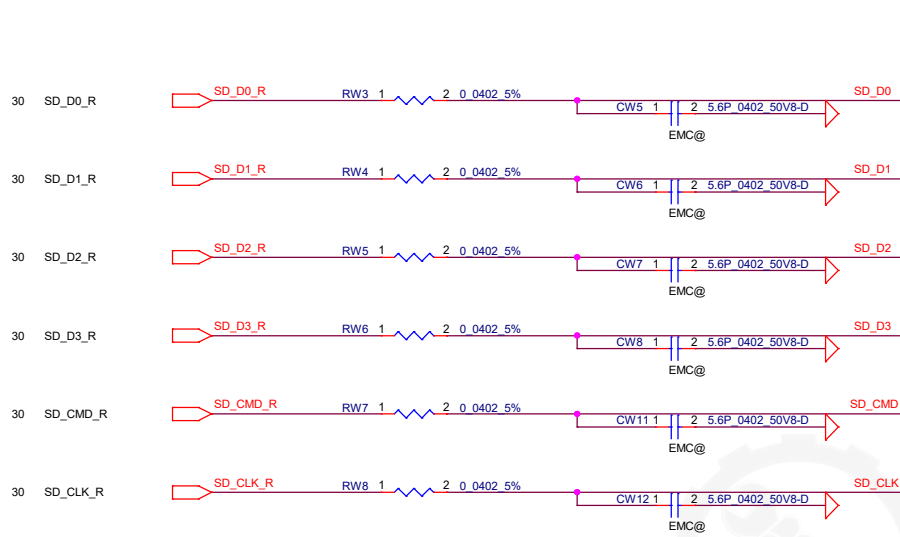


8/16 Update Audio Jack P/N SP011509163 wei



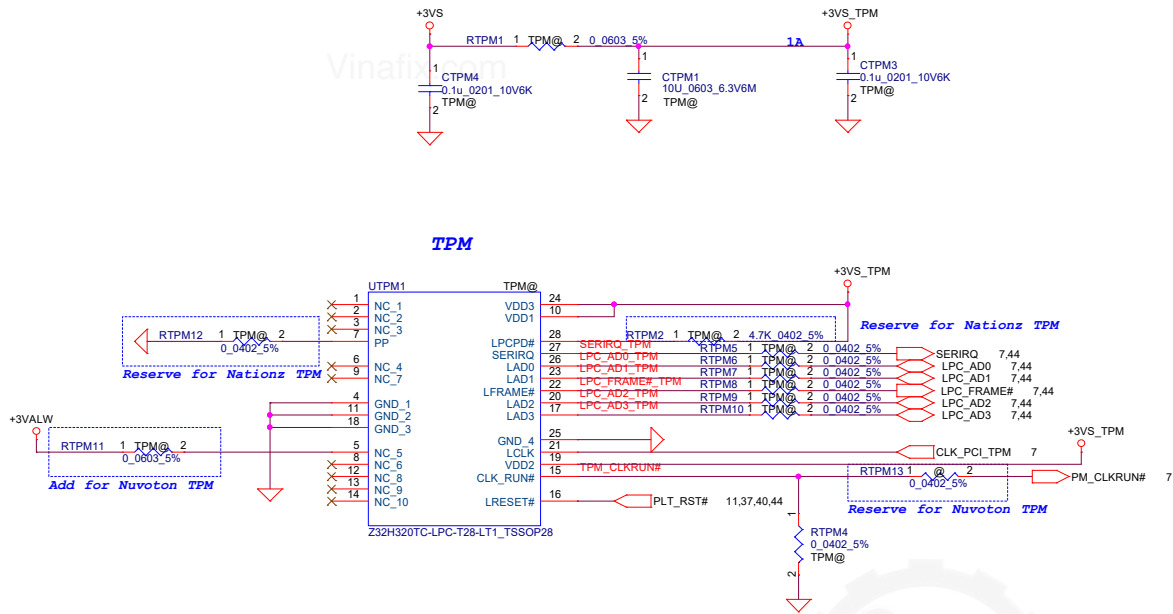
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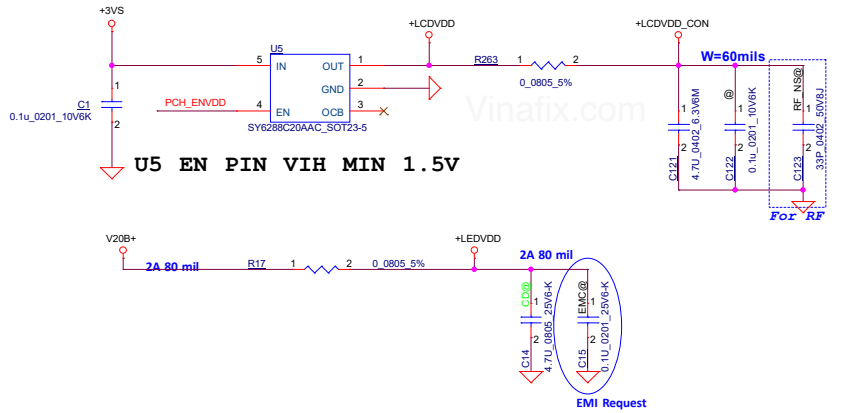
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RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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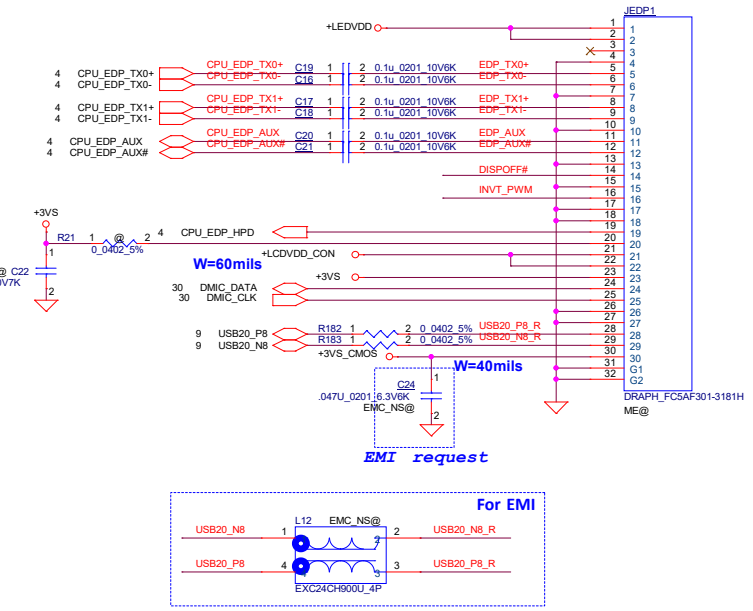
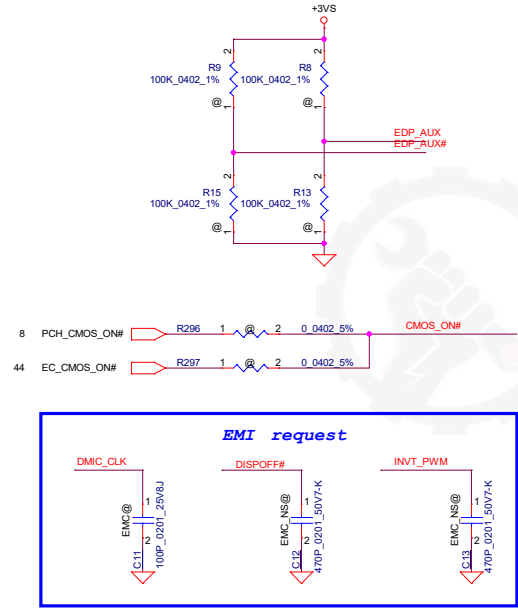
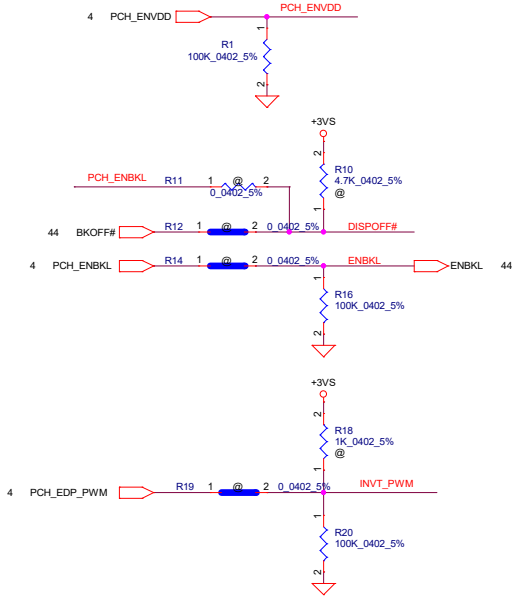
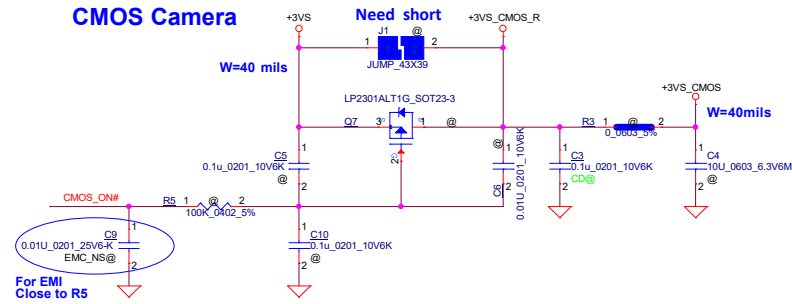
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Custom	EG521	0.2
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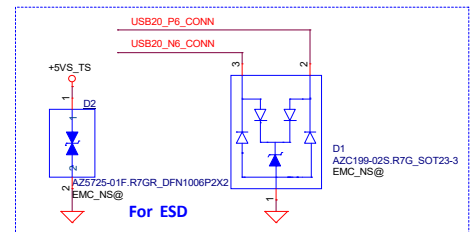
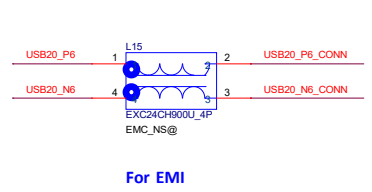
### LCD POWER CIRCUIT



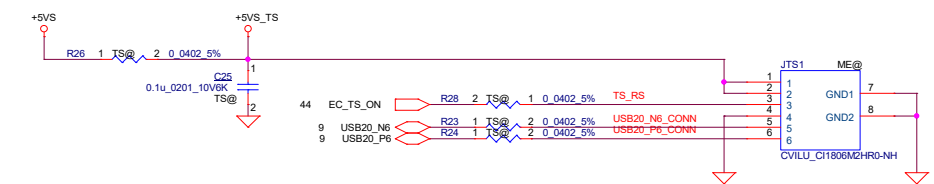
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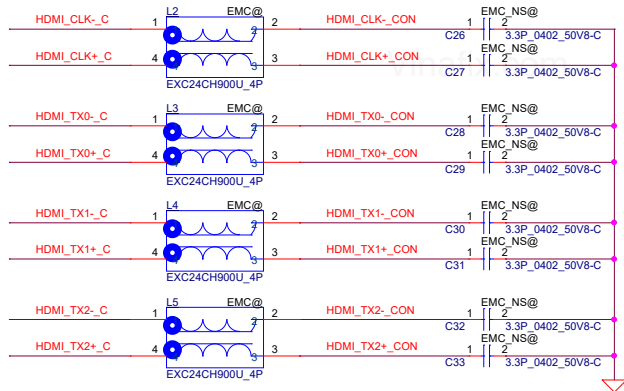
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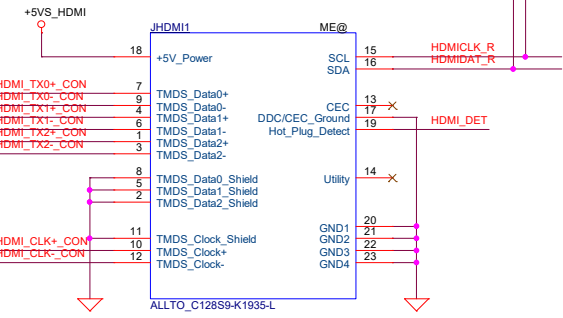
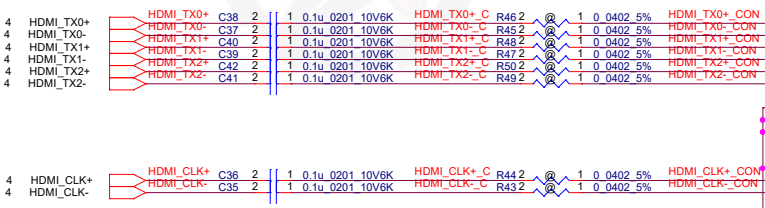
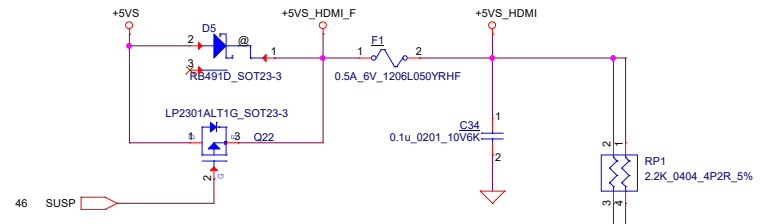
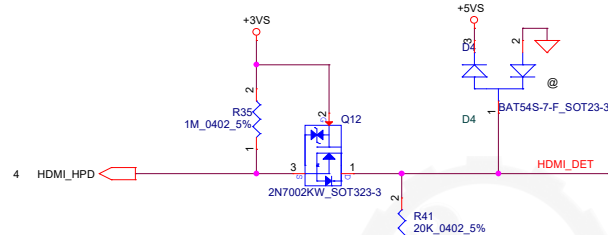
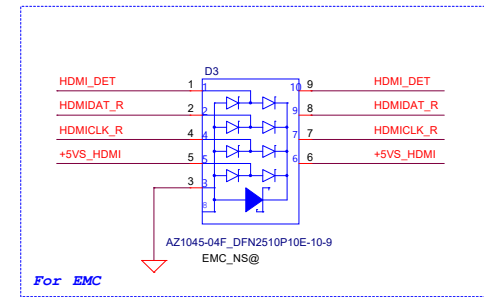
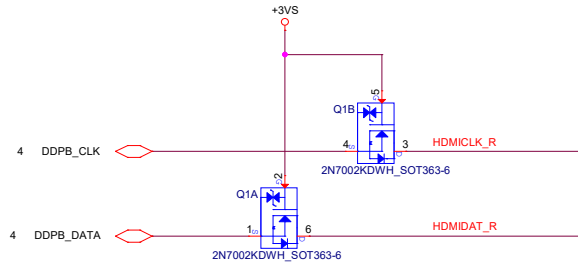
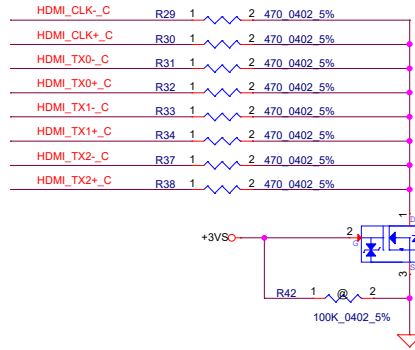
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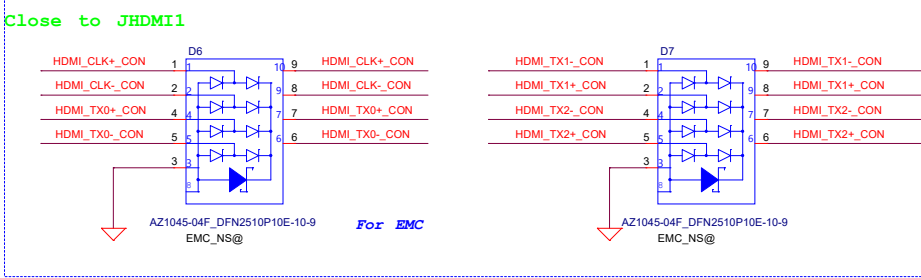
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For EMC



8/16 Update HDMIConn. P/N DC021608081 wei




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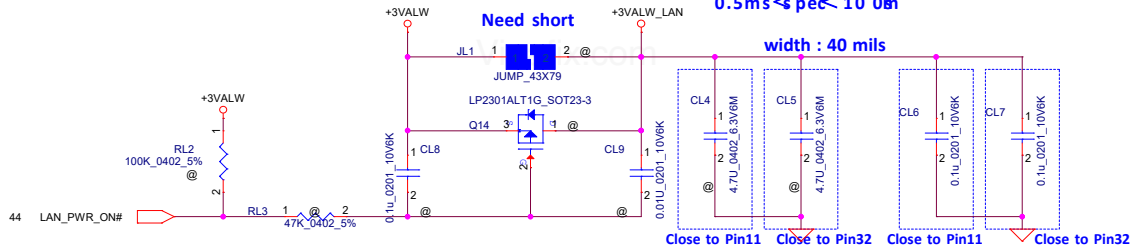
Security Classification	LC Future Center Secret Data			Title		
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				Custom	<b>EG521</b>	0.2
				Date:	Tuesday, April 25, 2017	Sheet 36 of 60

**+3VALW TO +3VALW\_LAN**

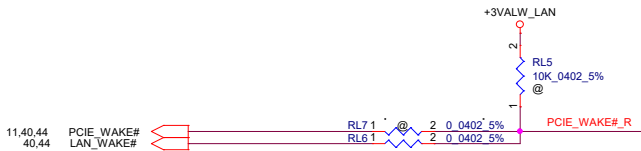
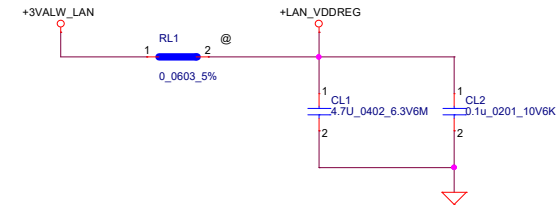
**+3VALW\_LAN rising time (10%~90%)**  
**0.5ms <= t\_rise <= 100ns**

**Need short**

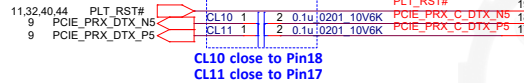
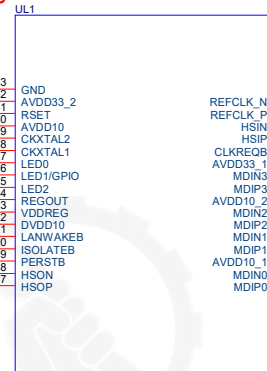
**width : 40 mils**



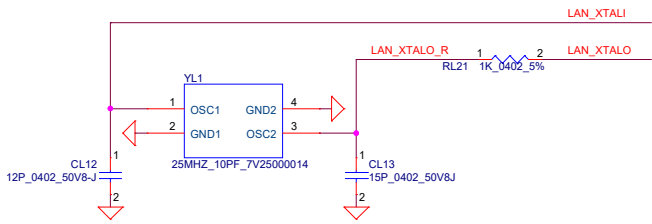
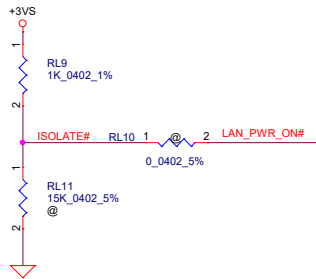
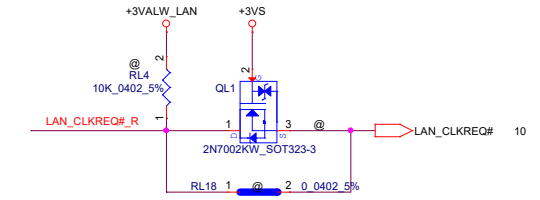
Close to Pin11    Close to Pin32    Close to Pin11    Close to Pin32



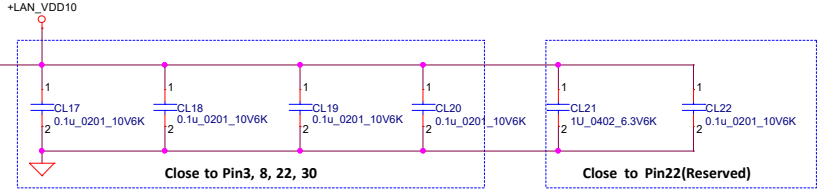
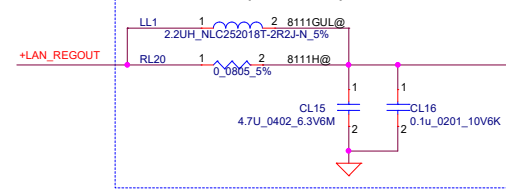
**manual change the Codec PN to RTL8111GUL-CG**



CL10 close to Pin18  
 CL11 close to Pin17



**For RTL8111GUL(SWR mode, reserved)**  
**For RTL8111H (LDO mode)**

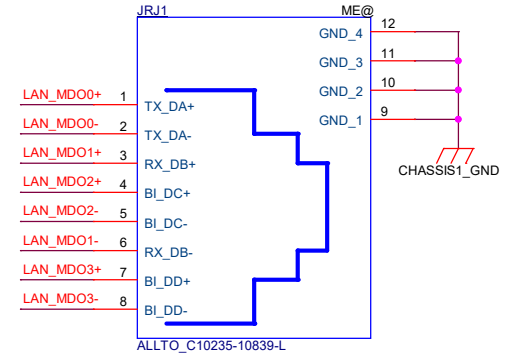
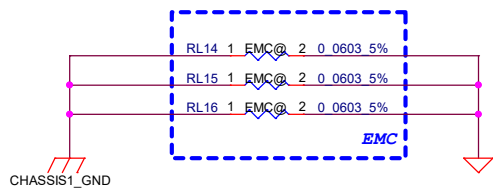
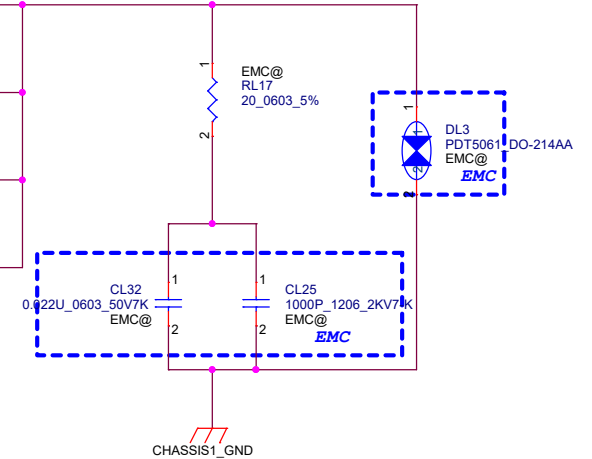
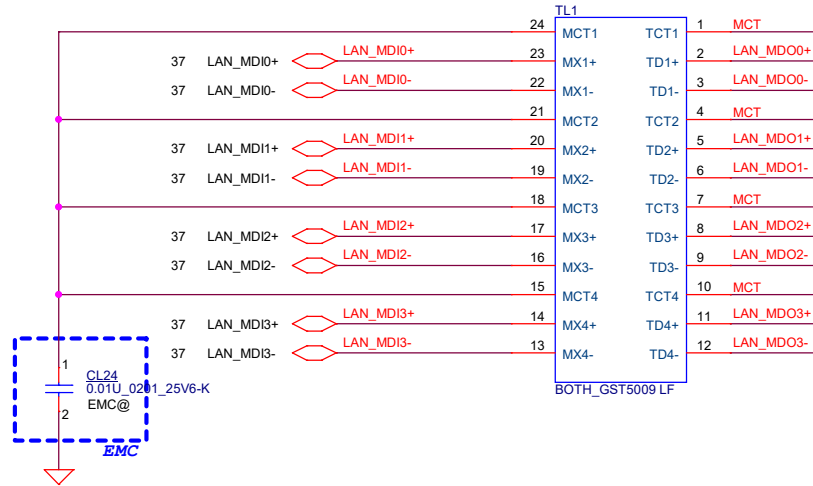
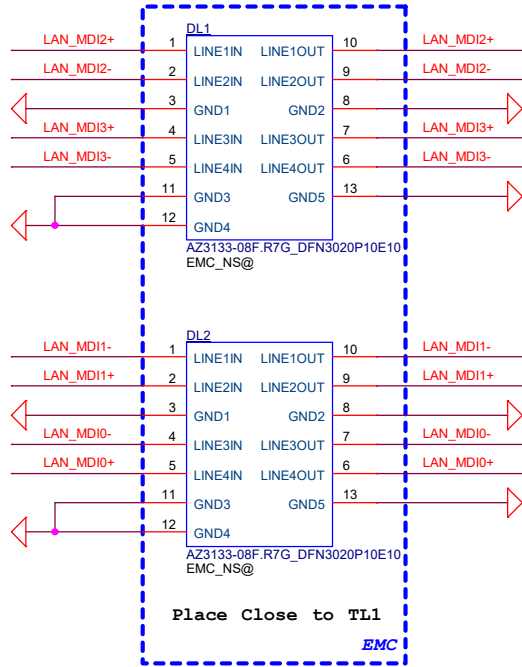


Layout Note: LL1 must be within 200mil to Pin24,  
 CL15,CL16 must be within 200mil to LL1  
 +LAN\_REGOUT: Width =60mil

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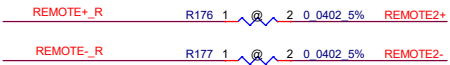
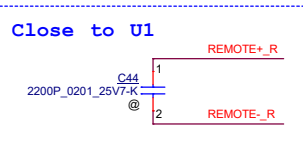
DL1/DL2  
1'S PN:SC300003M00

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8/16 Update RJ45 P/N DC021608091 wei

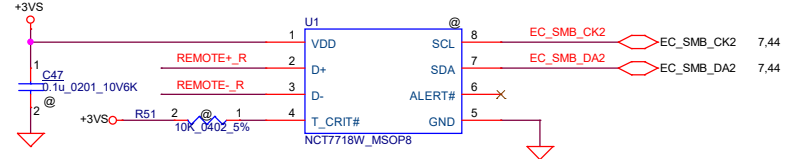
Security Classification	LC Future Center Secret Data		Title		
Issued Date	2015/08/20	Deciphered Date	2016/08/20		LAN_Transformer
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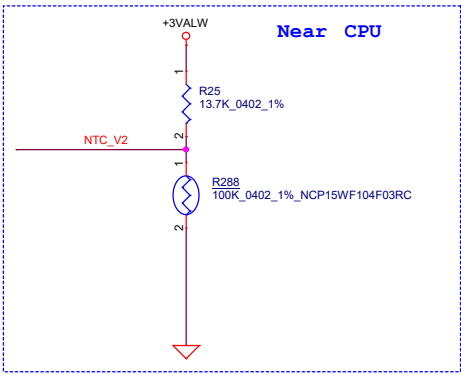
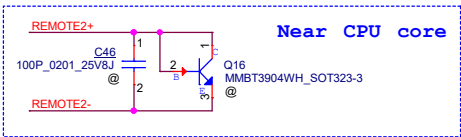
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REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

**SMSC thermal sensor placed near DIMM**

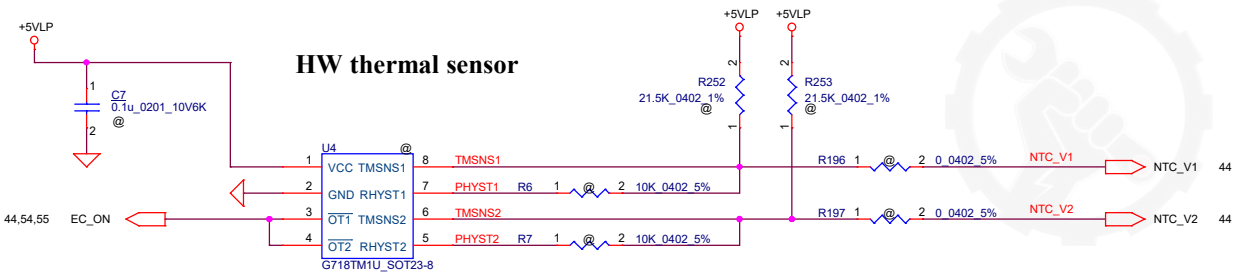


Address 1001\_101xb

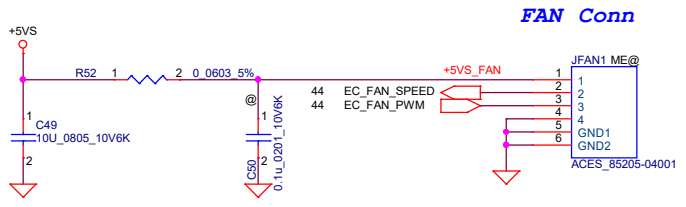


for layout optimized, change the EC\_AGND to GND

**HW thermal sensor**

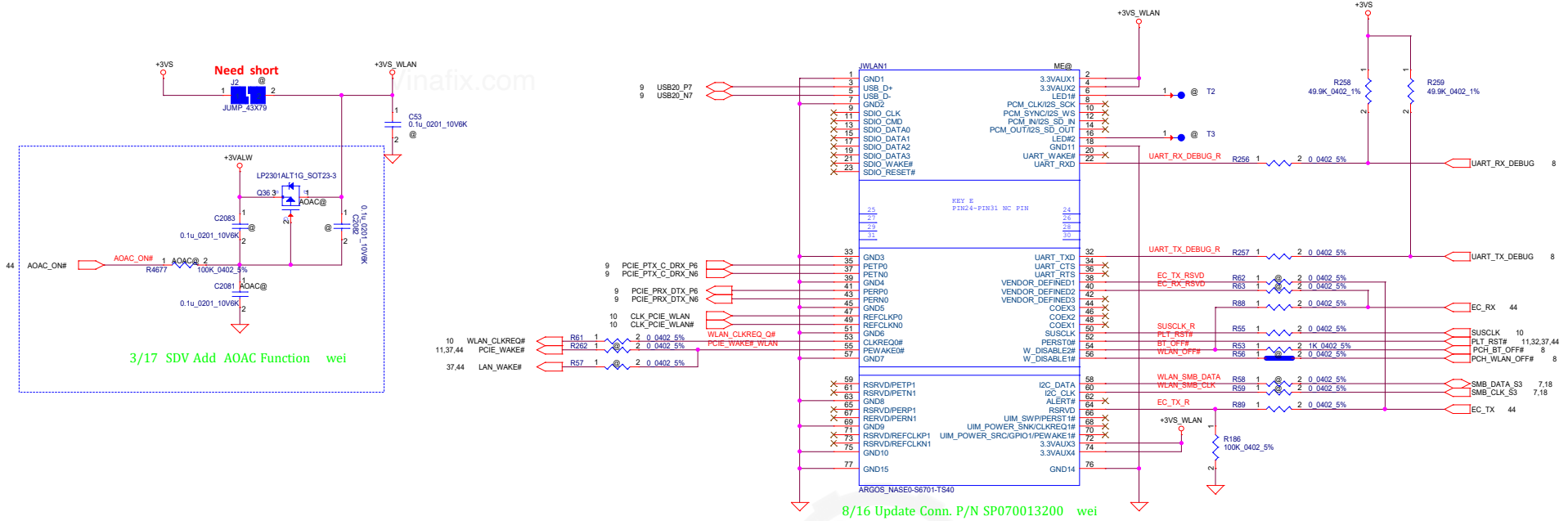


over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C

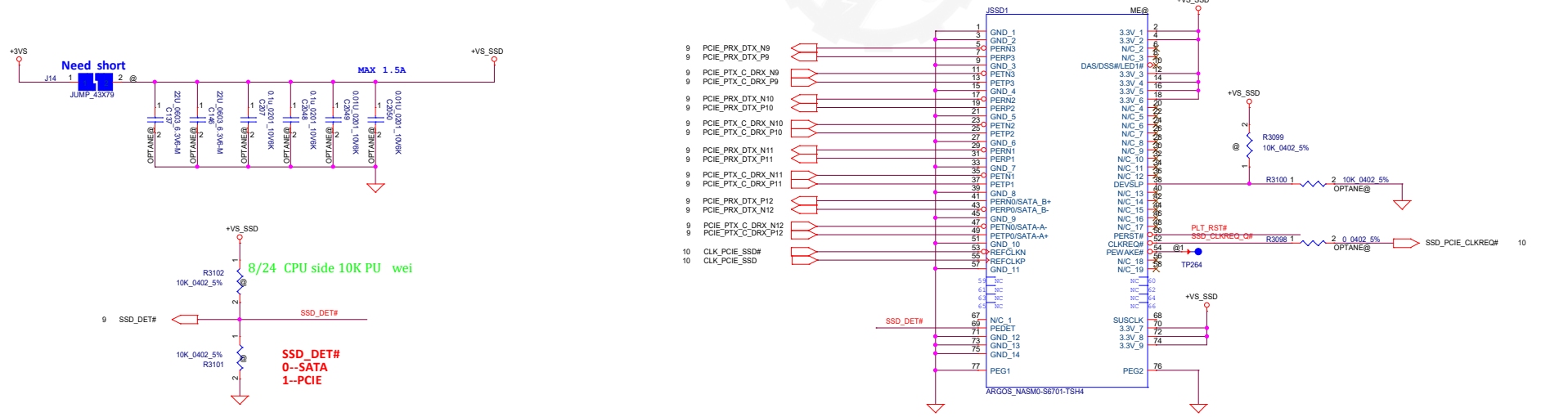


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Thermal sensor/FAN Conn <b>LCFC</b>			
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# Mini-Express Card(WLAN/WiMAX)



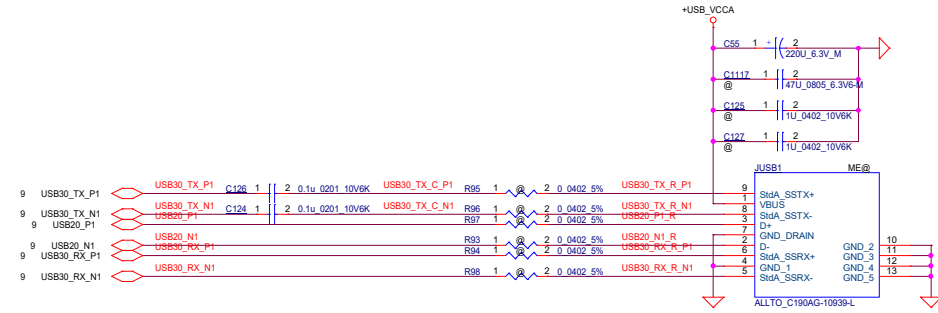
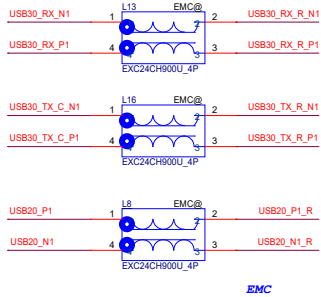
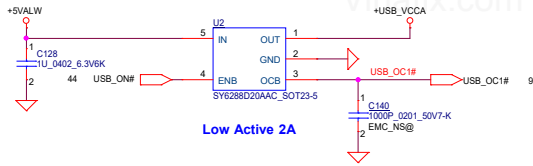
# Optane Memory



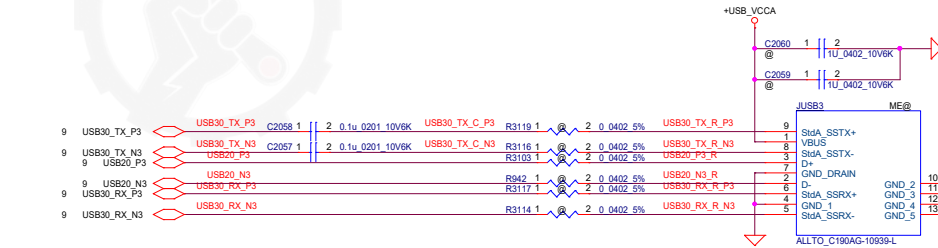
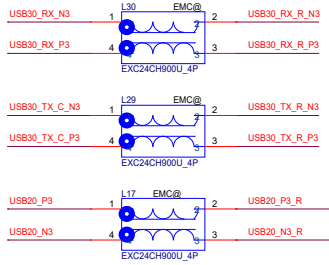
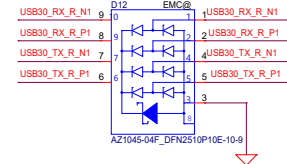
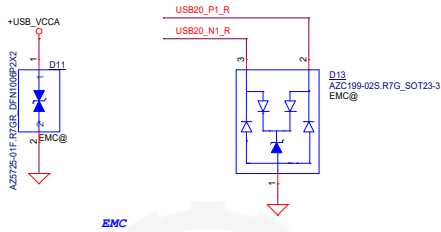
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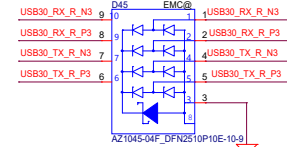
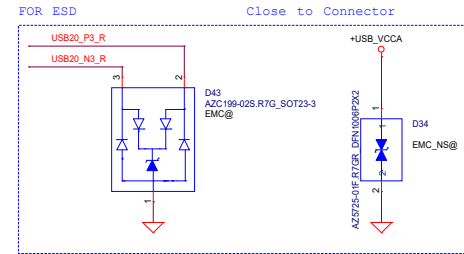
### LEFT SIDE USB3.0 PORT x2



09/05 Update USBConn. P/N DC021609011 wei



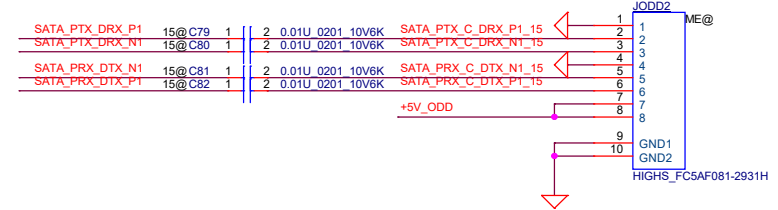
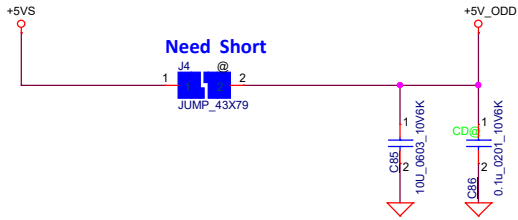
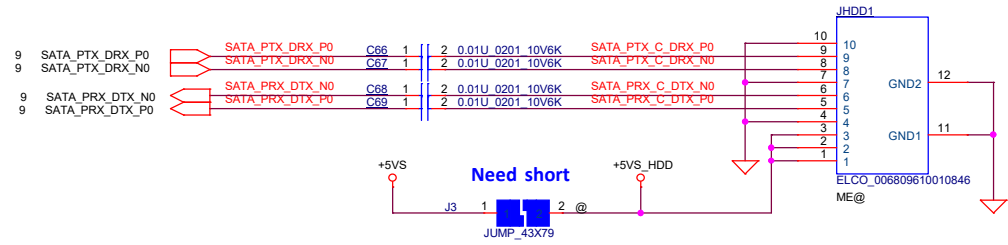
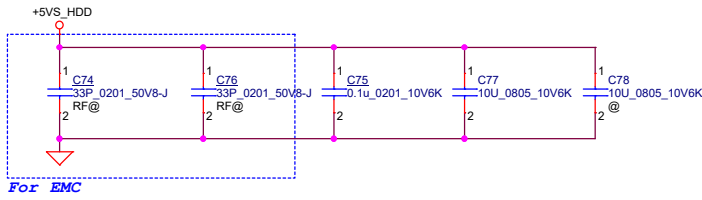
09/05 Update USBConn. P/N DC021609011 wei



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# SATA HDD Conn.

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FOR 15" 17"  
SATA ODD FFC Conn

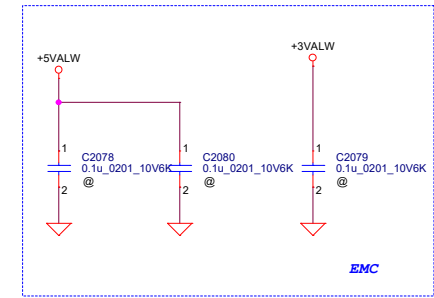
8/16 Update Conn. P/N SP01001YV00 wei

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Custom		EG521		Rev		0.2			

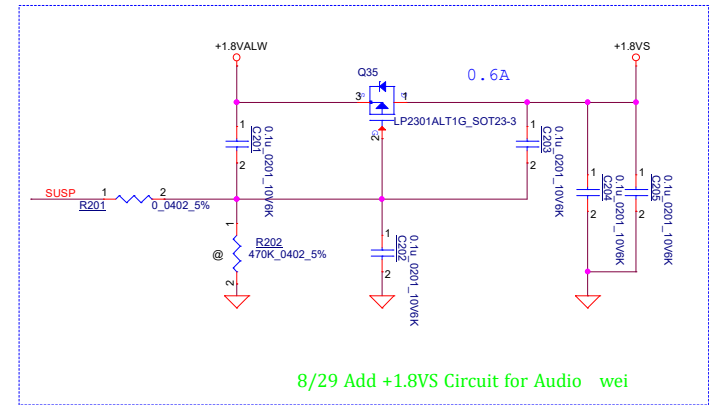
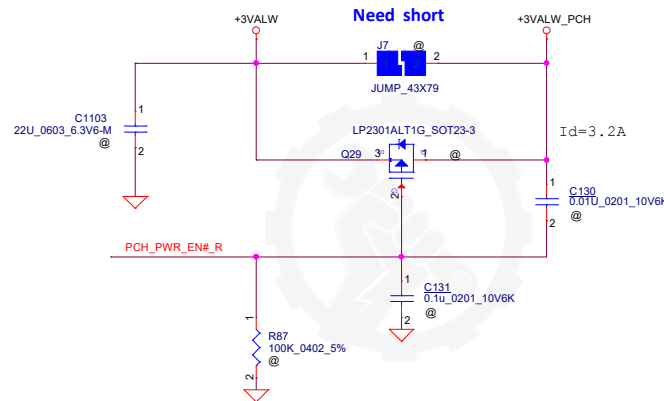
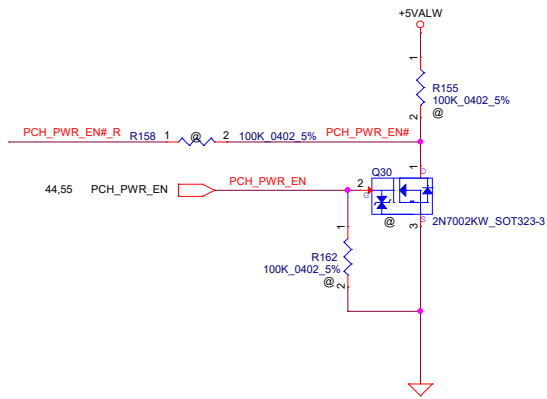




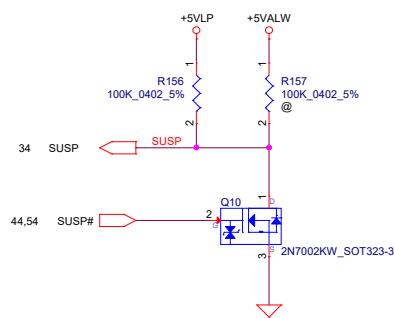




EMC



8/29 Add +1.8VS Circuit for Audio wei

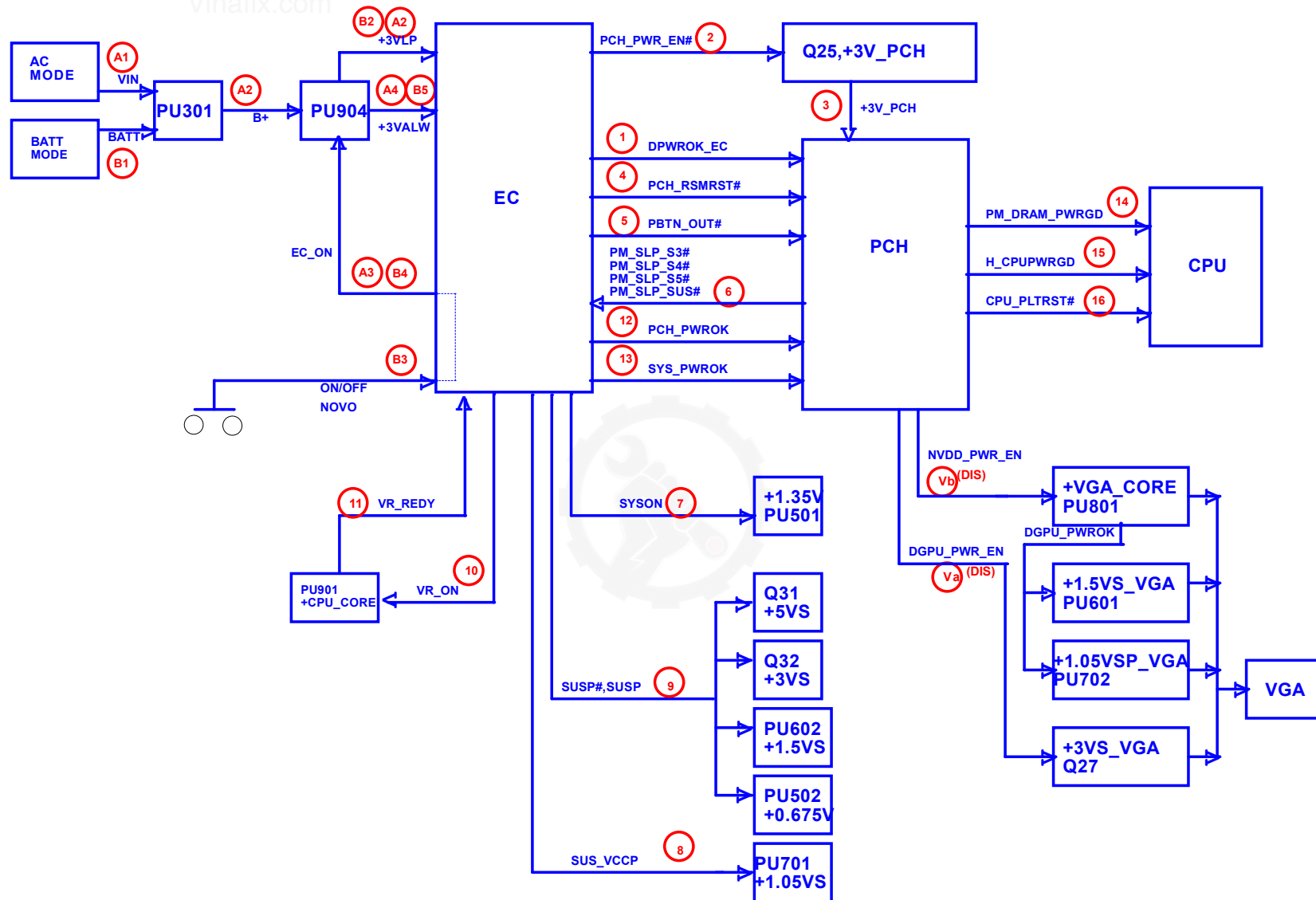


For DisCharge



08/29: Need double check enable signal and the resistance

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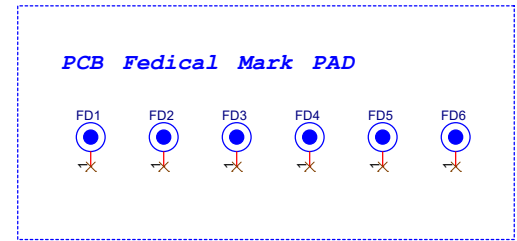
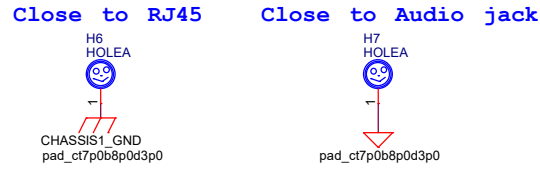
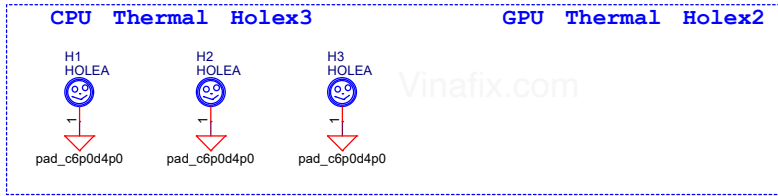


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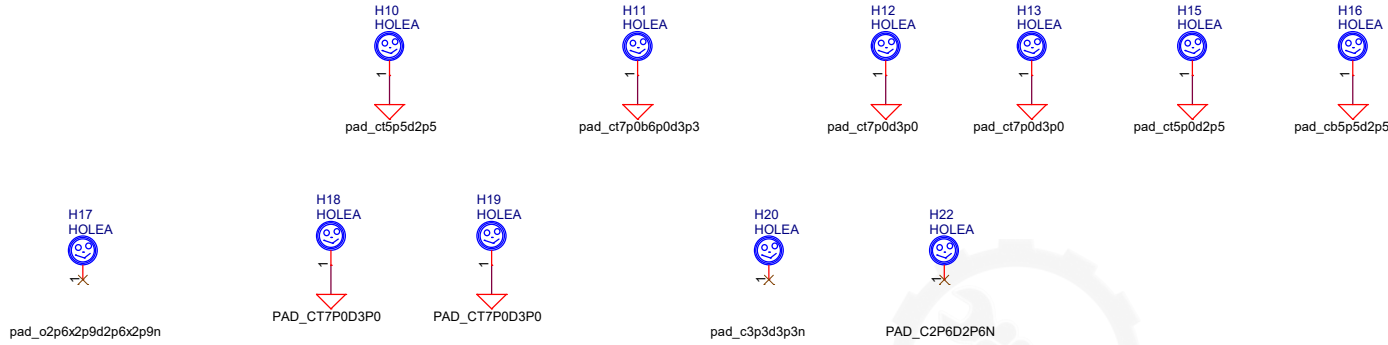


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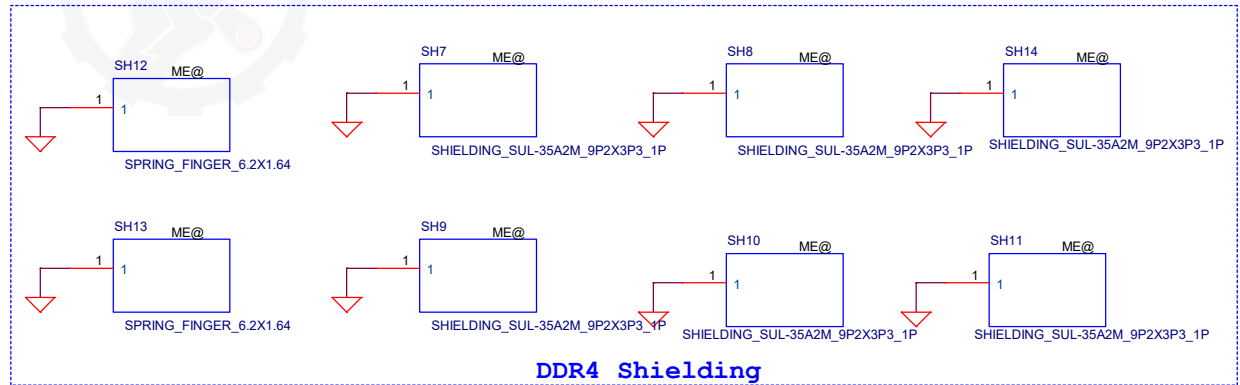
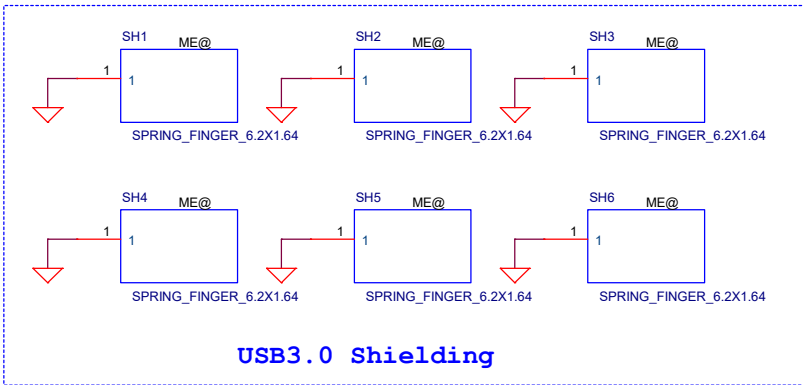
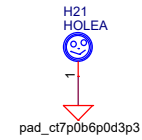





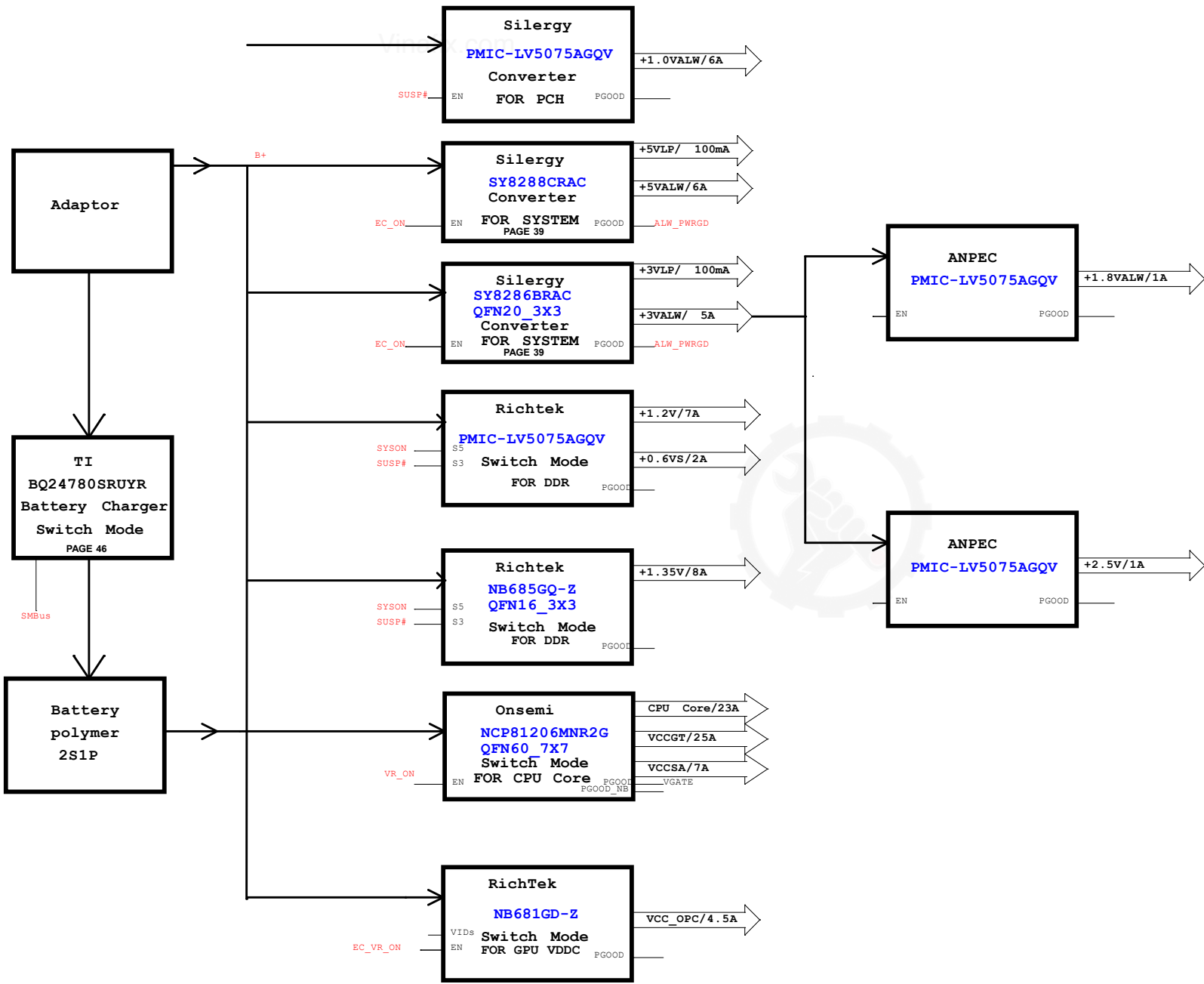
**WLAN Standoff**



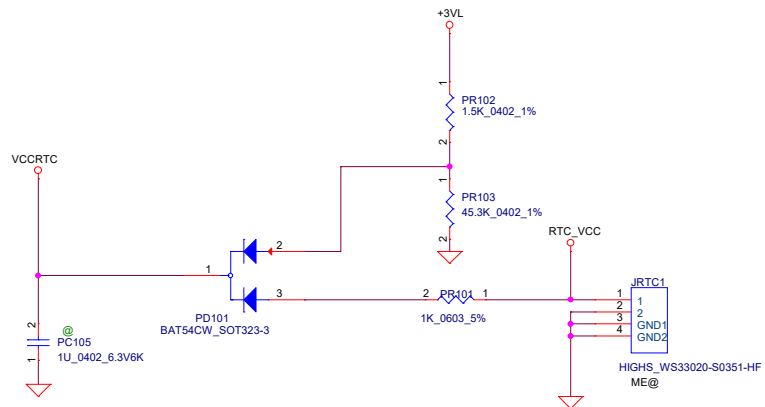
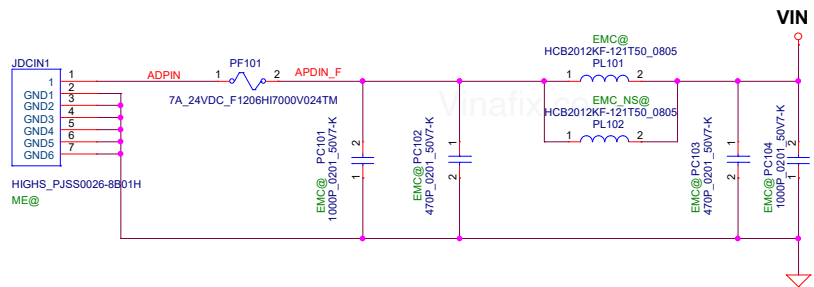
**Optane Standoff**



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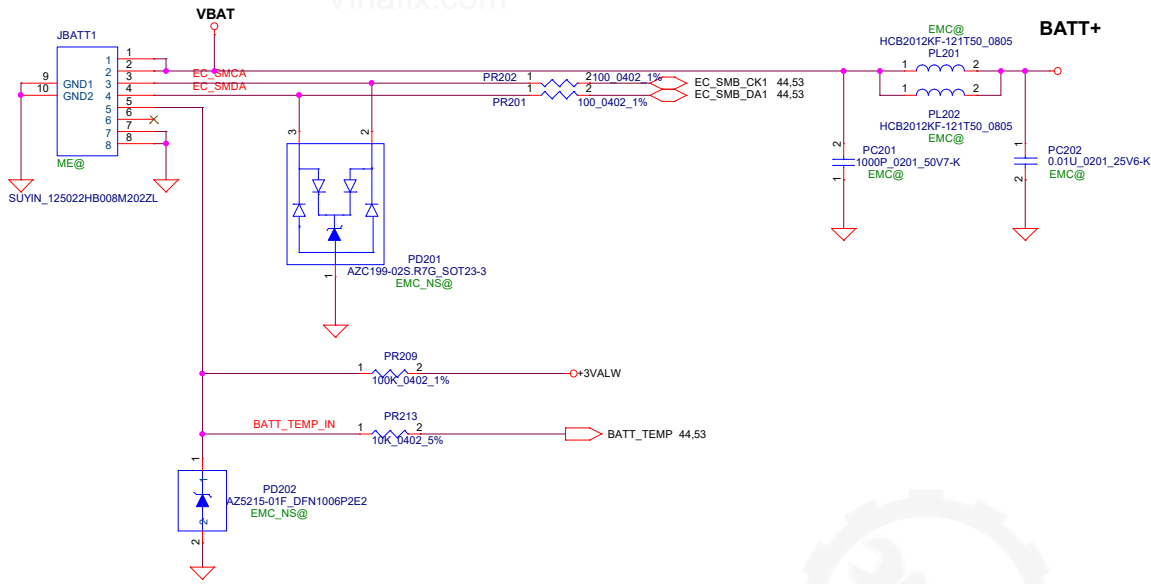


RTC\_VCC 20MIL  
+3V\_L 20MIL  
VCCRTC 20MIL

No charge RTC with 35mm cable  
RTC Battery for GCM BOM  
(2nd source and quoted price )



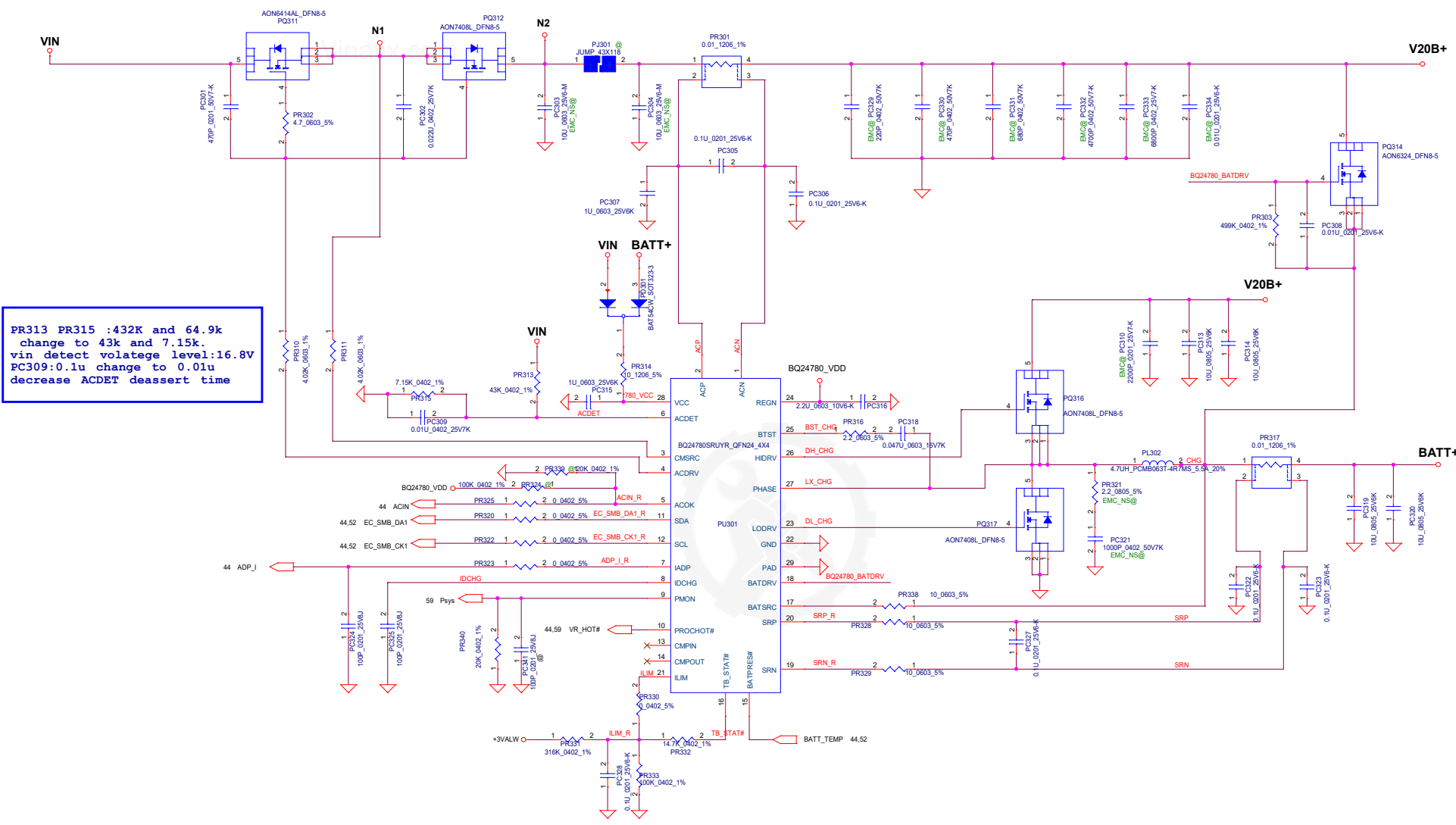
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2S1P polymer battery  
voltage level: +6V ~  
8.4 V

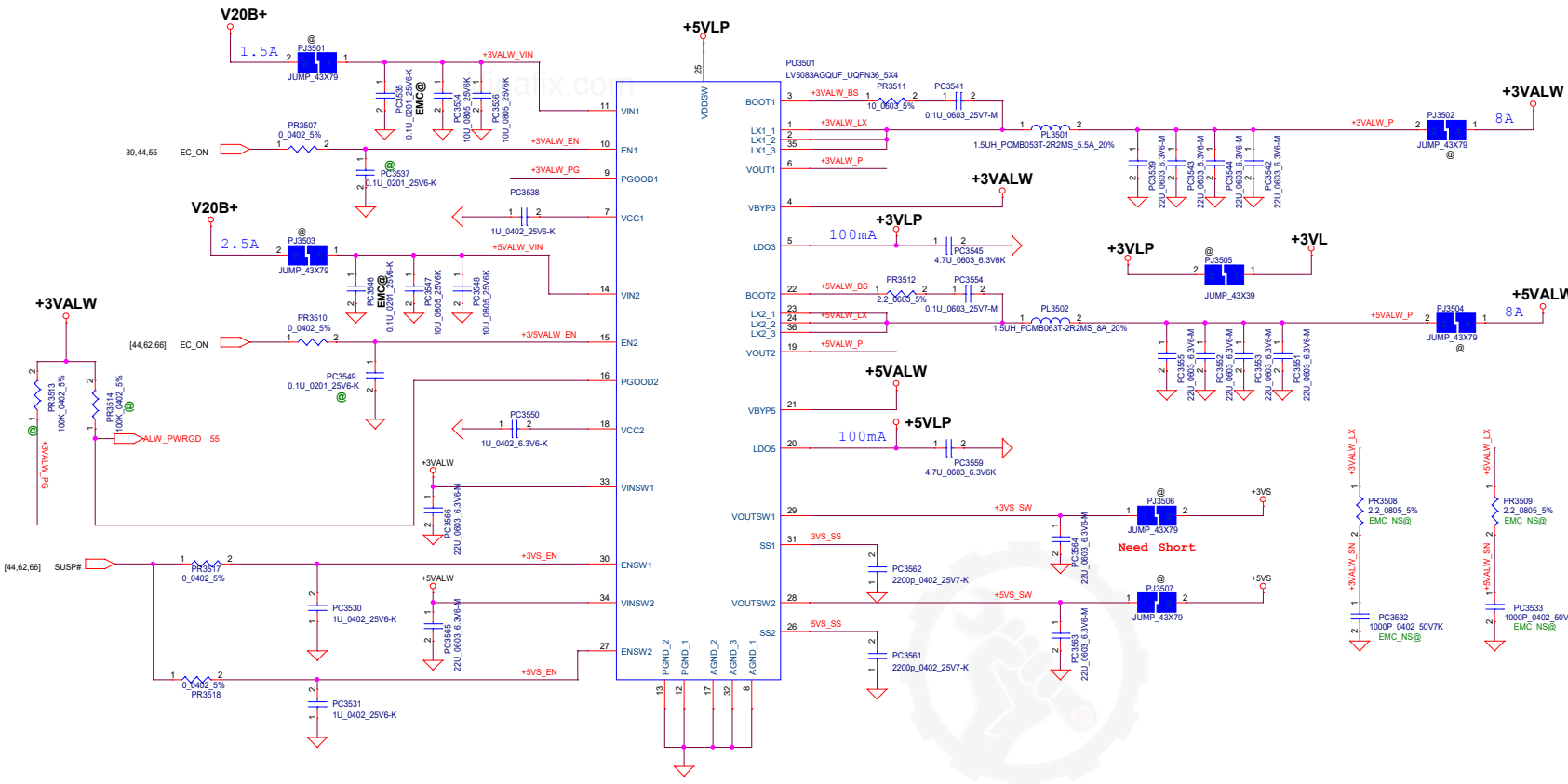


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PR313 PR315 :432k and 64.9k  
 change to 43k and 7.15k.  
 vin detect volatage level:16.8V  
 PC309:0.1u change to 0.01u  
 decrease ACDET deassert time

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$V_{out} = 3.3V \pm 5\%$   
 $V_{set} = 3.37V \pm 1.5\%$   
 $OC_P = 12A$   
 $OV_P = (1.15 - 1.25) * V_{out}$   
 $UV_P = (0.55 - 0.65) * V_{out}$   
 $F_{sw} = 500Khz$

$V_{out} = 5V \pm 3\%$   
 $V_{set} = 5.1V \pm 1.5\%$   
 $OC_P = 12A$   
 $OV_P = (1.15 - 1.25) * V_{out}$   
 $UV_P = (0.55 - 0.65) * V_{out}$   
 $F_{sw} = 500Khz$


Need Short

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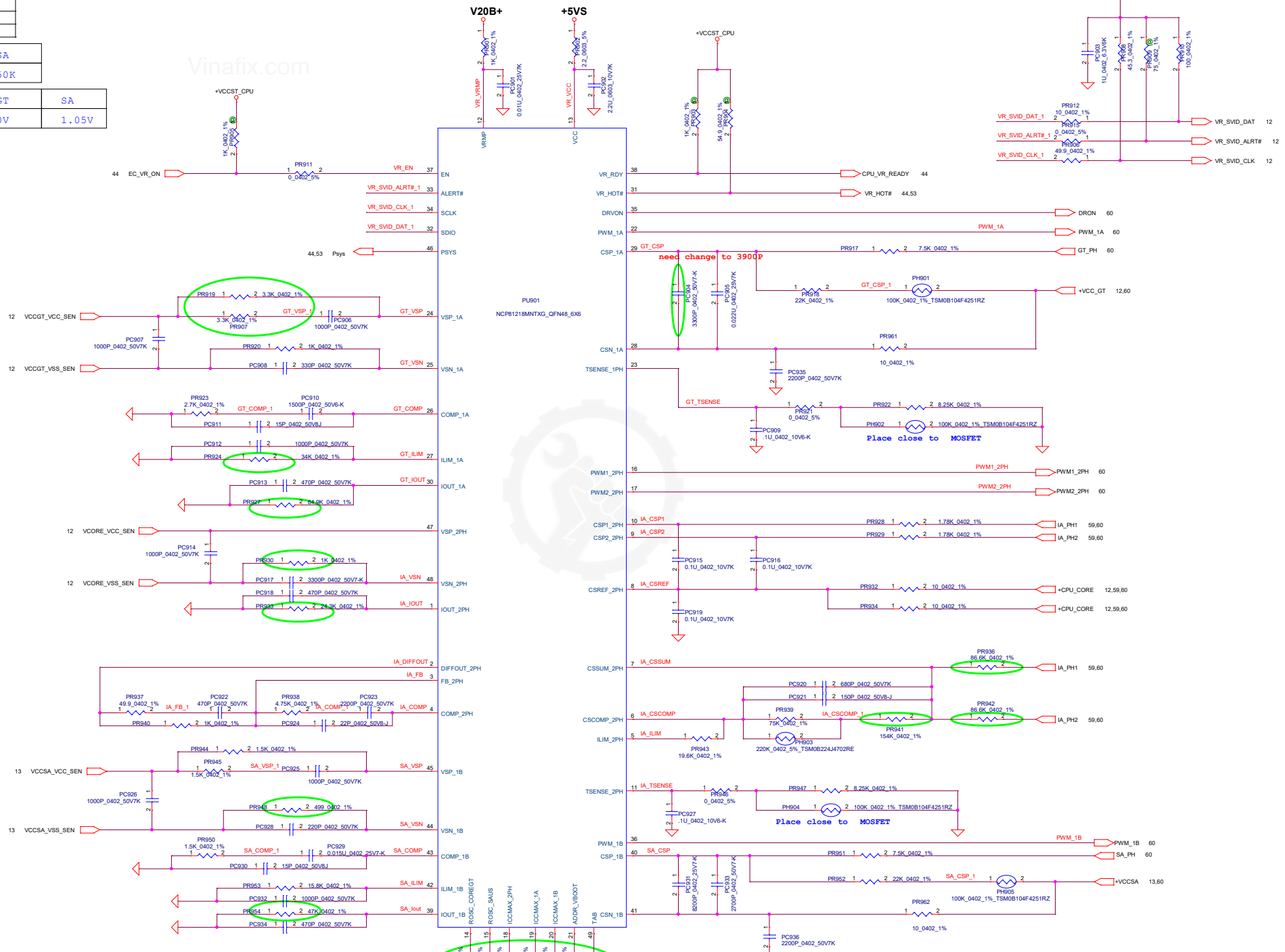
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SVID Specification	
	Config
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
28.7K	550K	550K

RVboot	Core	GT	SA
35.7K	0V	0V	1.05V

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