LCFC Confidential

FS441/FS540(NMC121) MB Schematics Document

WHL U42 with DDR4 + Nvidia N16V-GM

2018-01

REV:0.1

Title: *Cover Page*		
Size: Custom	Document Number: *FS441/FS540*	Rev: 0.1
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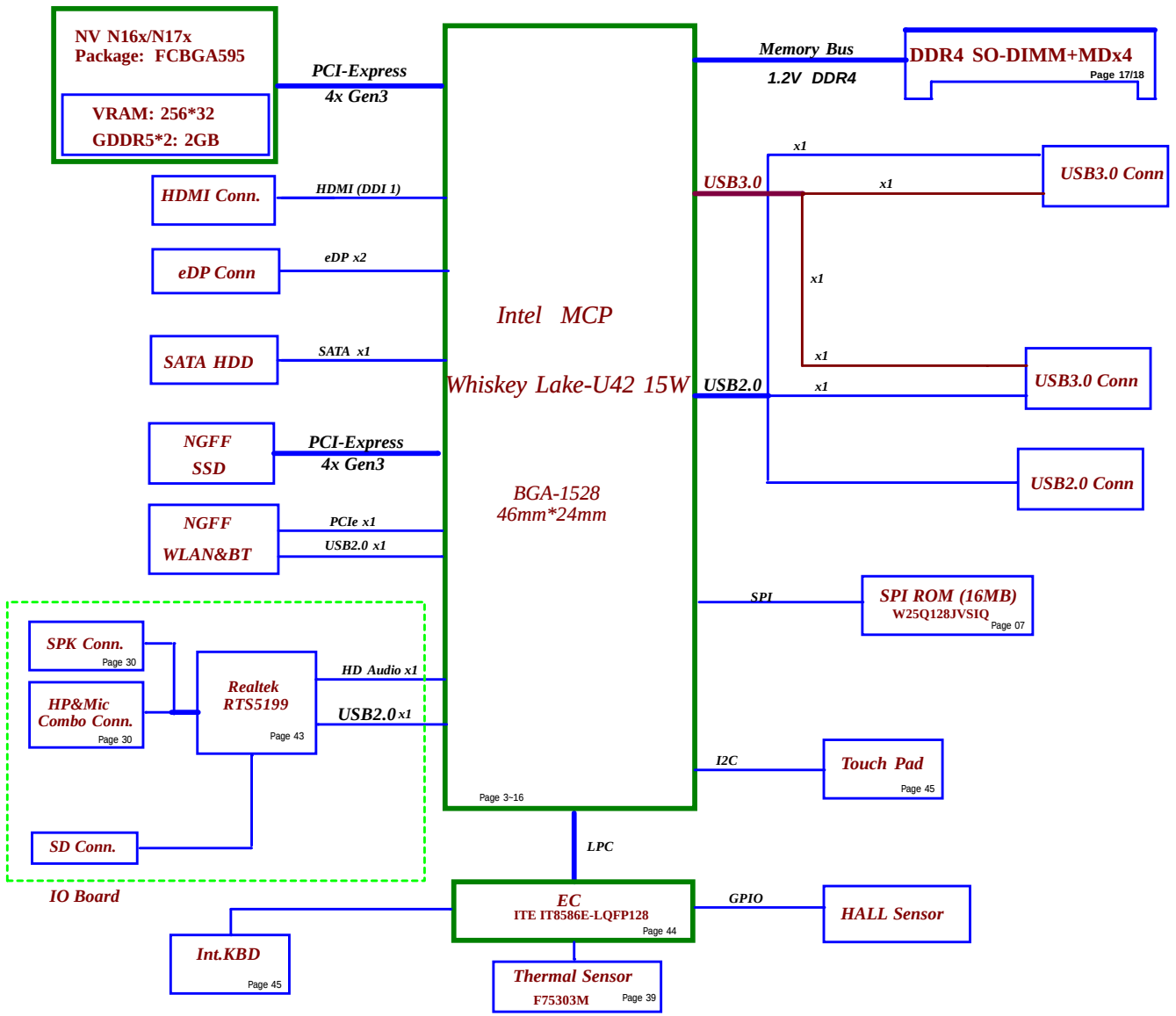

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn
	2	NC
	3	USB3.0 Conn
	4	USB2.0 conn
	5	Card reader
	6	Touch Screen
	7	Camera
	8	NC
	9	NC
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530S part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

DDP*_CTRLDATA strapping sampled on the rising edge of PCH_PWROK

Port	Strap	Enable	Disable
Port 1	GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Pull up to 3.3 V with 2.2Kohm *	NC
Port 2	GPP_E21 / DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Port 3	GPP_E23 / DDPD_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *
Reserve	GPP_H17/ DPPF_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC *

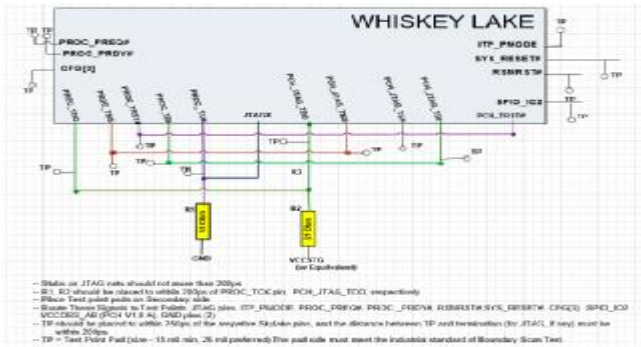
100Ohm for CNL

+VCCIO&EDP_COMP :
Trace Width: 20mil
Isolation Spacing: 25mil
Max length: 100mil

Change EC_SCI# to GPP_E16 based on CRB

Need to confirm stuff or not?

WHISKEY LAKE



- Stubs on JTAG nets should not exceed 9mil 200ps
- R1, R2 should be placed to within 250ps of PROC_TCK pin. PCH_JTAG_TDO respectively
- Place Test point pads on Secondary side
- Route These Signals to Test Points: JTAG pins: ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPI0_IO2
- VCCDSW_AB (PCH V1.8 A), GND pins (2)
- TP should be placed to within 250ps of the respective Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps
- TP = Test Point Pad (size - 15 mil min, 25 mil preferred) the pad side must meet the industrial standard of Boundary Scan Test

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Title: **MCP (DDI,EDP)**

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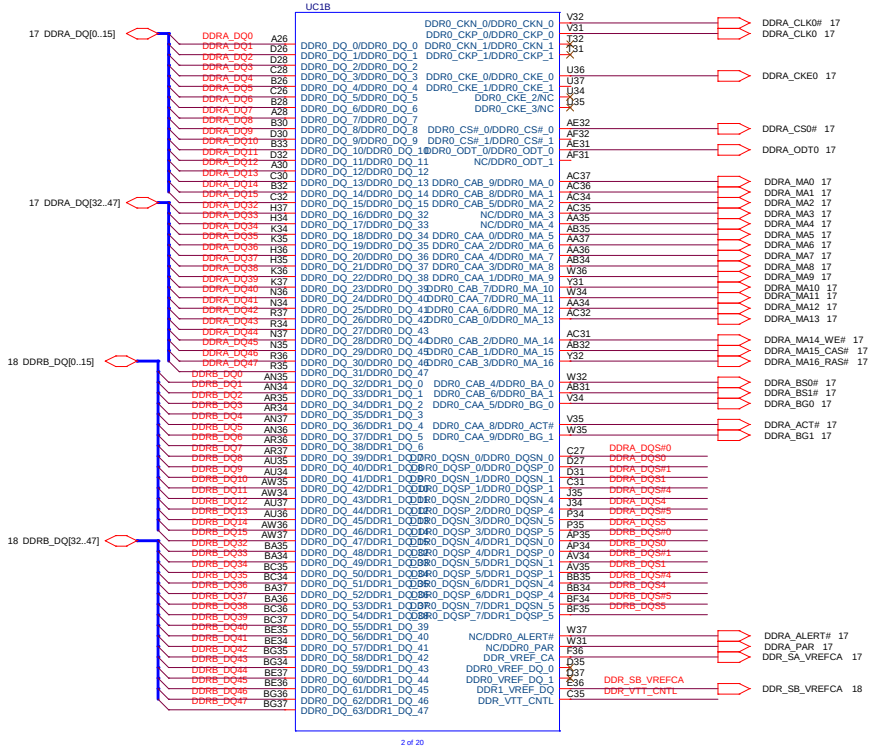
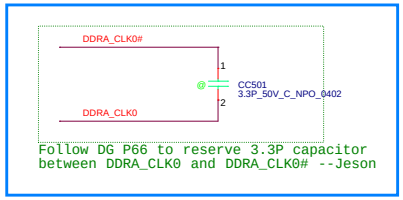
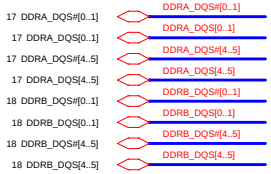
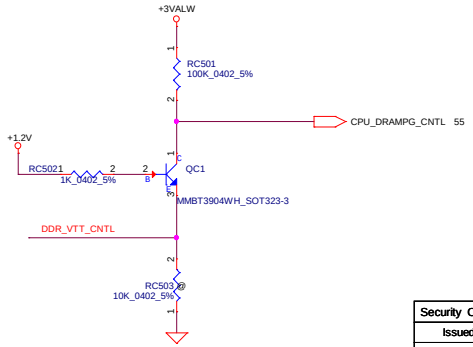






SMVREF
WIDTH:20MIL
SPACING: 20MIL



Security Classification	LC Future Center Secret Data		
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Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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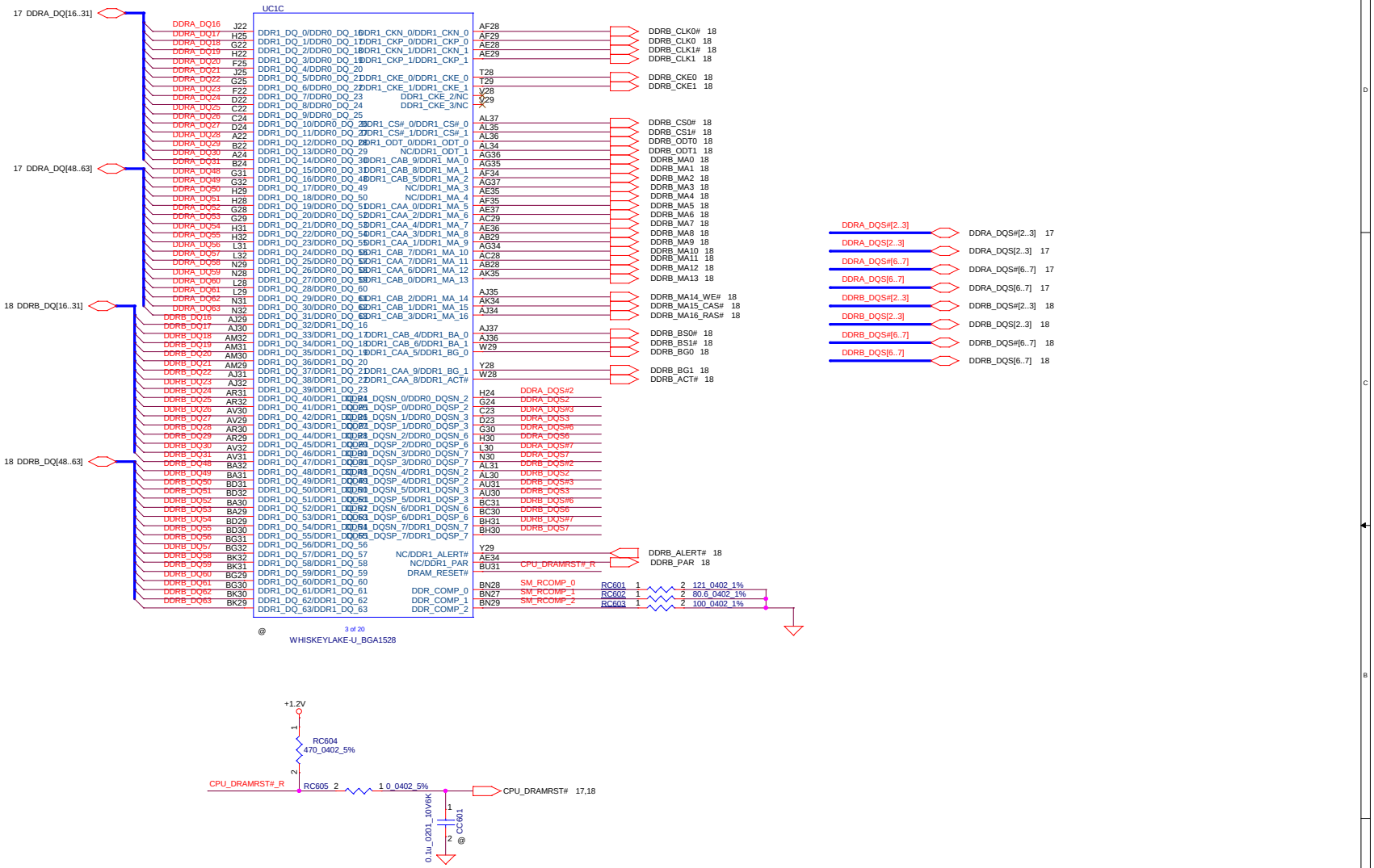

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Title: MCP (DDR4)

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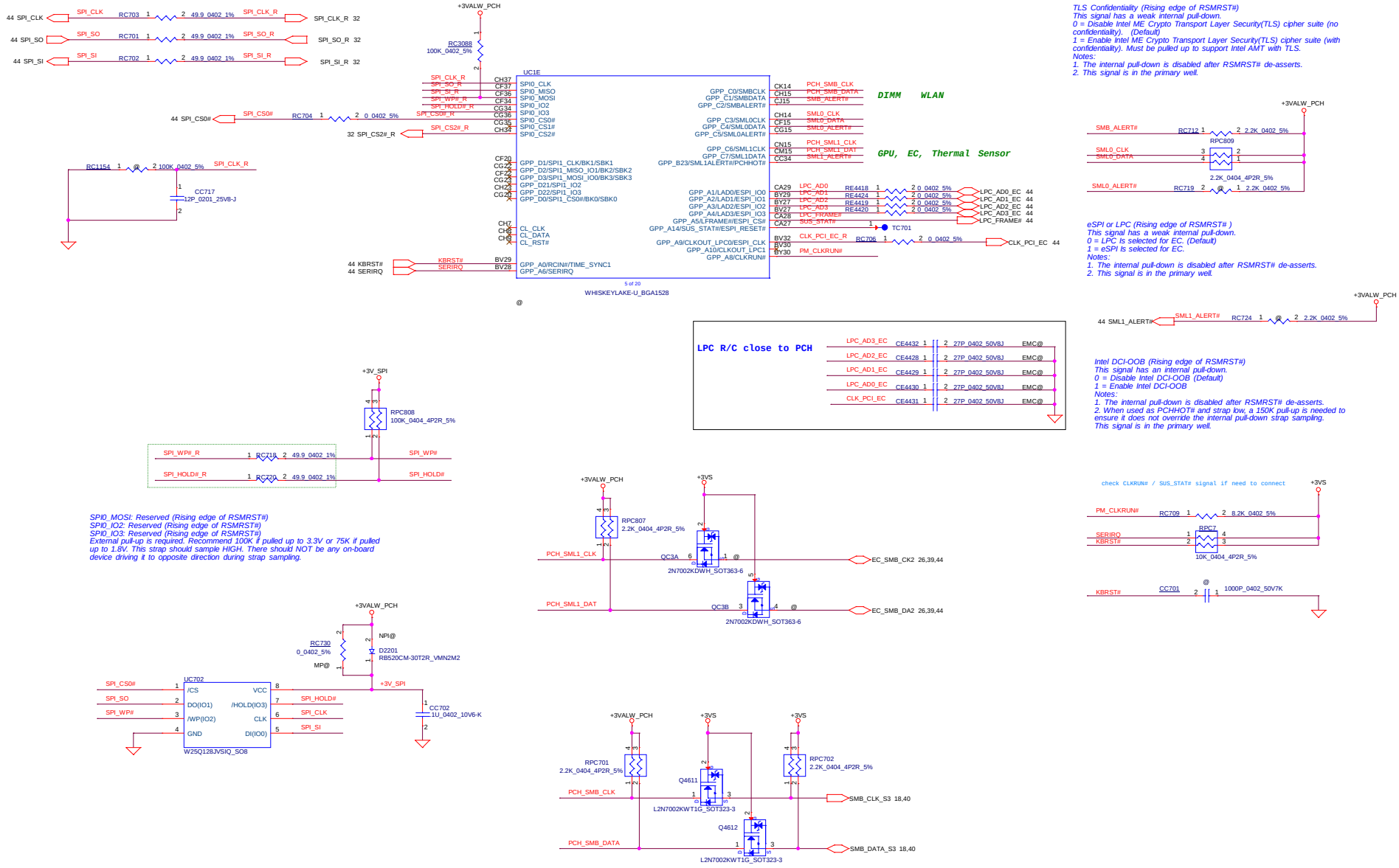

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Title: MCP (JTAG,SPI,LPC,SMB)

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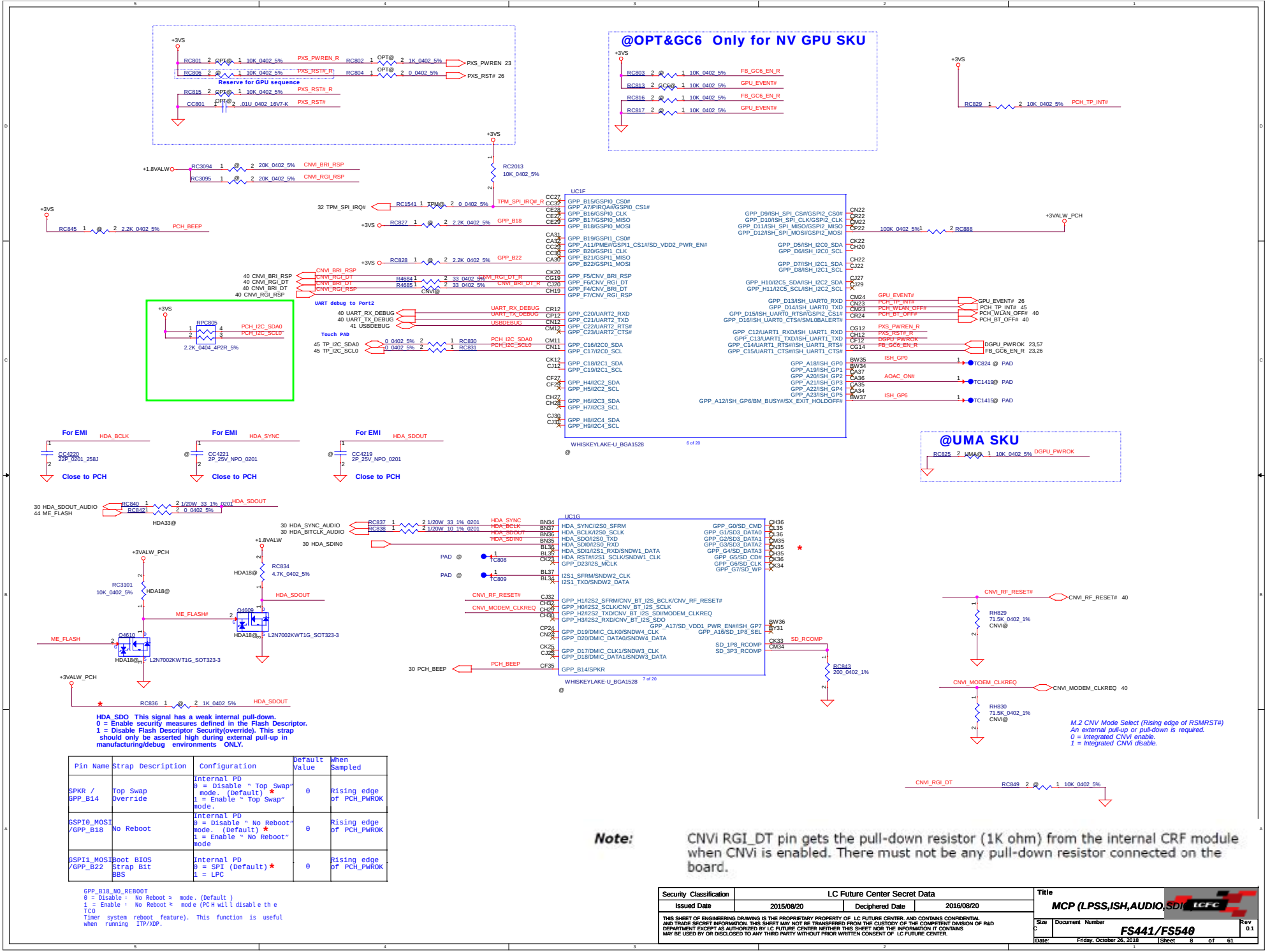

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) * 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) * 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) * 1 = LPC	0	Rising edge of PCH_PWROK

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Title: MCP (LPSS,ISH,AUDIO,SDI

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20 PCIE_CRX_GTX_N[5..8]
20 PCIE_CRX_GTX_P[5..8]
20 PCIE_CTX_C_GRX_N[5..8]
20 PCIE_CTX_C_GRX_P[5..8]

DGPU
WLAN
HDD
SSD

UC1H

PCIE_CRX_GTX_N5 BW9 PCIE5_RXN/USB31_5_RXN
PCIE_CRX_GTX_P5 BW8 PCIE5_RXP/USB31_5_RXP
PCIE_CTX_C_GRX_N5 OPT@ 0.22U 0201 6.3V6-K CC901 BW4 PCIE5_TXN/USB31_5_TXN
PCIE_CTX_C_GRX_P5 OPT@ 0.22U 0201 6.3V6-K CC902 BW3 PCIE5_TXP/USB31_5_TXP

PCIE_CRX_GTX_N6 BU6 PCIE6_RXN/USB31_6_RXN
PCIE_CRX_GTX_P6 BU5 PCIE6_RXP/USB31_6_RXP
PCIE_CTX_C_GRX_N6 OPT@ 0.22U 0201 6.3V6-K CC905 BU4 PCIE6_TXN/USB31_6_TXN
PCIE_CTX_C_GRX_P6 OPT@ 0.22U 0201 6.3V6-K CC906 BU3 PCIE6_TXP/USB31_6_TXP

PCIE_CRX_GTX_N7 BT7 PCIE7_RXN
PCIE_CRX_GTX_P7 BT6 PCIE7_RXP
PCIE_CTX_C_GRX_N7 OPT@ 0.22U 0201 6.3V6-K CC907 BU2 PCIE7_TXN
PCIE_CTX_C_GRX_P7 OPT@ 0.22U 0201 6.3V6-K CC903 BU1 PCIE7_TXP

PCIE_CRX_GTX_N8 BU9 PCIE8_RXN
PCIE_CRX_GTX_P8 BU8 PCIE8_RXP
PCIE_CTX_C_GRX_N8 OPT@ 0.22U 0201 6.3V6-K CC908 BT4 PCIE8_TXN
PCIE_CTX_C_GRX_P8 OPT@ 0.22U 0201 6.3V6-K CC904 BT3 PCIE8_TXP

40 PCIE_PRX_DTX_N9 PCIE_PRX_DTX_N9 BP5 PCIE9_RXN
40 PCIE_PRX_DTX_P9 PCIE_PRX_DTX_P9 BP6 PCIE9_RXP
40 PCIE_PTX_C_DRX_N9 CC918 1 2 .1U 0402 10V6-K PCIE_PTX_DRX_N9 BR2 PCIE9_TXN
40 PCIE_PTX_C_DRX_P9 CC919 1 2 .1U 0402 10V6-K PCIE_PTX_DRX_P9 BR1 PCIE9_TXP

BN6 PCIE10_RXN
BN5 PCIE10_RXP
BR3 PCIE10_TXN
BR4 PCIE10_TXP

38 SATA_PRX_DTX_N0 SATA_PRX_DTX_N0 BN10 PCIE11_RXN/SATA0_RXN
38 SATA_PRX_DTX_P0 SATA_PRX_DTX_P0 BN8 PCIE11_RXP/SATA0_RXP
38 SATA_PTX_DRX_N0 SATA_PTX_DRX_N0 BN4 PCIE11_TXN/SATA0_TXN
38 SATA_PTX_DRX_P0 SATA_PTX_DRX_P0 BN3 PCIE11_TXP/SATA0_TXP

BL6 PCIE12_RXN/SATA1A_RXN
BL5 PCIE12_RXP/SATA1A_RXP
BN2 PCIE12_TXN/SATA1A_TXN
BN1 PCIE12_TXP/SATA1A_TXP

37 PCIE_PRX_DTX_N13 PCIE_PRX_DTX_N13 BK6 PCIE13_RXN
37 PCIE_PRX_DTX_P13 PCIE_PRX_DTX_P13 BK5 PCIE13_RXP
37 PCIE_PTX_DRX_N13 PCIE_PTX_DRX_N13 BM4 PCIE13_TXN
37 PCIE_PTX_DRX_P13 PCIE_PTX_DRX_P13 BM3 PCIE13_TXP

37 PCIE_PRX_DTX_N14 PCIE_PRX_DTX_N14 BJ6 PCIE14_RXN
37 PCIE_PRX_DTX_P14 PCIE_PRX_DTX_P14 BJ5 PCIE14_RXP
37 PCIE_PTX_DRX_N14 PCIE_PTX_DRX_N14 BL2 PCIE14_TXN
37 PCIE_PTX_DRX_P14 PCIE_PTX_DRX_P14 BL1 PCIE14_TXP

37 PCIE_PRX_DTX_N15 PCIE_PRX_DTX_N15 BG5 PCIE15_RXN/SATA1B_RXN
37 PCIE_PRX_DTX_P15 PCIE_PRX_DTX_P15 BG6 PCIE15_RXP/SATA1B_RXP
37 PCIE_PTX_DRX_N15 PCIE_PTX_DRX_N15 BL4 PCIE15_TXN/SATA1B_TXN
37 PCIE_PTX_DRX_P15 PCIE_PTX_DRX_P15 BL3 PCIE15_TXP/SATA1B_TXP

37 PCIE_PRX_DTX_N16 PCIE_PRX_DTX_N16 BE5 PCIE16_RXN/SATA2_RXN
37 PCIE_PRX_DTX_P16 PCIE_PRX_DTX_P16 BE6 PCIE16_RXP/SATA2_RXP
37 PCIE_PTX_DRX_N16 PCIE_PTX_DRX_N16 BJ4 PCIE16_TXN/SATA2_TXN
37 PCIE_PTX_DRX_P16 PCIE_PTX_DRX_P16 BJ3 PCIE16_TXP/SATA2_TXP

RC905 1 2 100 0402 1% PCIE_RCOMPN CE6
PCIE_RCOMPP CE5
PCIE_RCOMP_N
PCIE_RCOMP_P

PCIE_RCOMPN and PCIE_RCOMPP
Trace Width: 12-15mil
Differential between RCOMPP/RCOMPN

CR28 GPP_H12/M2_SKT2/CFG_0
CP28 GPP_H13/M2_SKT2/CFG_1
CN28 GPP_H14/M2_SKT2/CFG_2
CM28 GPP_H15/M2_SKT2/CFG_3

WHISKEYLAKE-U_BGA1528 8 of 20
@

PCIE1_RXN/USB31_1_RXN CB5 USB30_RX_N1
PCIE1_RXP/USB31_1_RXP CB6 USB30_RX_P1
PCIE1_TXN/USB31_1_TXN CA4 USB30_TX_N1
PCIE1_TXP/USB31_1_TXP CA3 USB30_TX_P1

USB30_RX_N1 43
USB30_RX_P1 43
USB30_TX_N1 43
USB30_TX_P1 43
USB3.0

PCIE2_RXN/USB31_2_RXN/SSIC_1_RXN BY8 USB30_RX_N2
PCIE2_RXP/USB31_2_RXP/SSIC_1_RXP BY9 USB30_RX_P2
PCIE2_TXN/USB31_2_TXN/SSIC_1_TXN CA2 USB30_TX_N2
PCIE2_TXP/USB31_2_TXP/SSIC_1_TXP CA1 USB30_TX_P2

USB30_RX_N2 41
USB30_RX_P2 41
USB30_TX_N2 41
USB30_TX_P2 41
USB3.0

PCIE3_RXN/USB31_3_RXN BY7
PCIE3_RXP/USB31_3_RXP BY6
PCIE3_TXN/USB31_3_TXN BY4
PCIE3_TXP/USB31_3_TXP BY3

PCIE4_RXN/USB31_4_RXN BW6
PCIE4_RXP/USB31_4_RXP BW5
PCIE4_TXN/USB31_4_TXN BW2
PCIE4_TXP/USB31_4_TXP BW1

USB2_1N CE3 USB20_N1
USB2_1P CE4 USB20_P1

USB20_N1 41
USB20_P1 41
USB3.0

USB2_2N CE1
USB2_2P CE2

USB2_3N CG3 USB20_N3
USB2_3P CG4 USB20_P3

USB20_N3 43
USB20_P3 43
USB3.0

USB2_4N CD3 USB20_N4
USB2_4P CD4 USB20_P4

USB20_N4 43
USB20_P4 43
USB2.0

USB2_5N CG5 USB20_N5
USB2_5P CG6 USB20_P5

USB20_N5 30
USB20_P5 30
Card reader

USB2_6N CC1 USB20_N6
USB2_6P CC2 USB20_P6

USB20_N6 33
USB20_P6 33
Touch Screen

USB2_7N CG8 USB20_N7
USB2_7P CG9 USB20_P7

USB20_N7 33
USB20_P7 33
Camera

USB2_8N CB8
USB2_8P CB9

USB2_9N CH5
USB2_9P CH6

USB2_10N CC3 USB20_N10
USB2_10P CC4 USB20_P10

USB20_N10 40
USB20_P10 40
BT

USB2_COMP CC5 USB2_COMP RC901 2 1 113 0402 1%
USB2_ID CE8 USB2_ID RC902 @1 2 0 0402 5%
USB2_VBUSSENSE CC6 USB2_VBUSSENSE RC903 @1 2 1K 0402 5%

USBRBIAS
Width 20Mil
Space 15Mil
Length 500Mil

GPP_E9/USB2_OC0#/GP_BSSB_CLK CK6 USB_OC0#
GPP_E10/USB2_OC1#/GP_BSSB_DI CK5 USB_OC1#
GPP_E11/USB2_OC2# CK8 USB_OC2#
GPP_E12/USB2_OC3# CK9 USB_OC3#

USB_OC0# 43
USB_OC1# 41
USB_OC2# 43

GPP_E4 CP8 GPP_E4 RC904 1 2 0 0402 5%
GPP_E5/DEVSLP1 CR8 PCH_SATA_1_DEVSLP
GPP_E6/DEVSLP2 CM8 PCH_SATA_DEVSLP

TC1418
EC_SMI# 44
PCH_SATA_DEVSLP 37

GPP_E0/SATAXPCIE0/SATAGP0 CN8 SATA0GP
GPP_E1/SATAXPCIE1/SATAGP1 CM10 SSD_1_PCIE_DET#
GPP_E2/SATAXPCIE2/SATAGP2 CP10 SSD_PCIE_DET#

TC1417
SSD_PCIE_DET# 37

GPP_E8/SATALED#/SPI1_CS1# CN7
RSVD37 AR3

2016/05/03: Implement as Power Button function for Windows RedStone support

+3VS
GPP_E4 RC906 1 @ 2 10K 0402 5%

+3VS
RC3105 1 2 10K 0402 5% SSD_PCIE_DET#
RC3106 1 2 10K 0402 5% SATA0GP

+3VALW_PCH
RPC810
1 8 USB_OC0#
2 7 USB_OC1#
3 6 USB_OC3#
4 5 USB_OC2#
10K_0804_8P4R_5%

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Title: MCP (PCIE,SATA,USB3.0,USB2.0)

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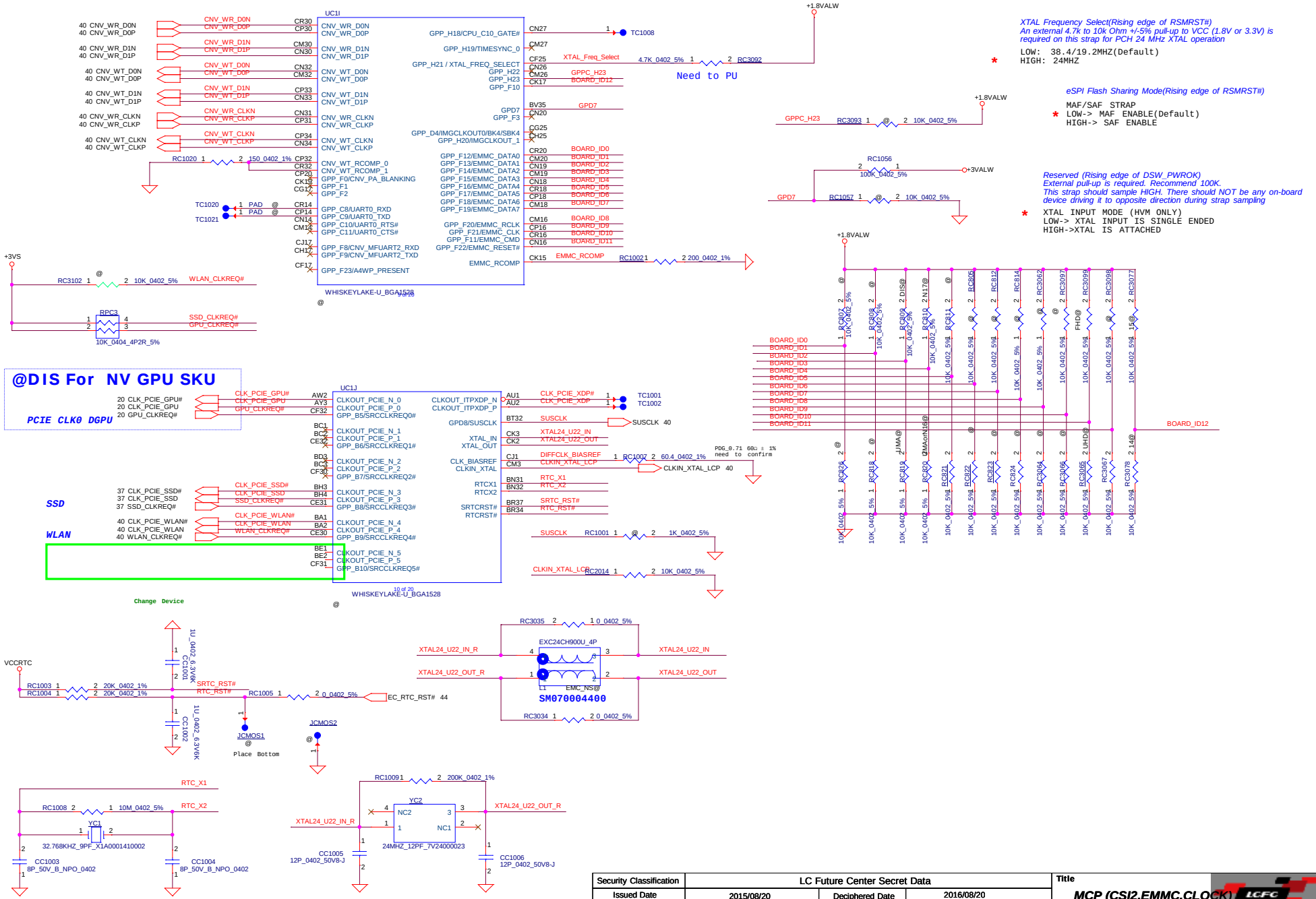
UC1I
WHISKEYLAKE-U_BGA1528
Need to PU
XTAL Frequency Select(Rising edge of RSMRST#)
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation
LOW: 38.4/19.2MHZ(Default)
HIGH: 24MHZ
eSPI Flash Sharing Mode(Rising edge of RSMRST#)
MAF/SAF STRAP
LOW-> MAF ENABLE(Default)
HIGH-> SAF ENABLE
Reserved (Rising edge of DSW_PWROK)
External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
XTAL INPUT MODE (HVM ONLY)
LOW-> XTAL INPUT IS SINGLE ENDED
HIGH->XTAL IS ATTACHED
@DIS For NV GPU SKU
PCIE CLK0 DGPU
SSD
WLAN
Change Device
UC1J
WHISKEYLAKE-U_BGA1528
SM070004400
Place Bottom
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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Title
MCP (CSI2,EMMC,CLOCK)
Size Custom
Document Number
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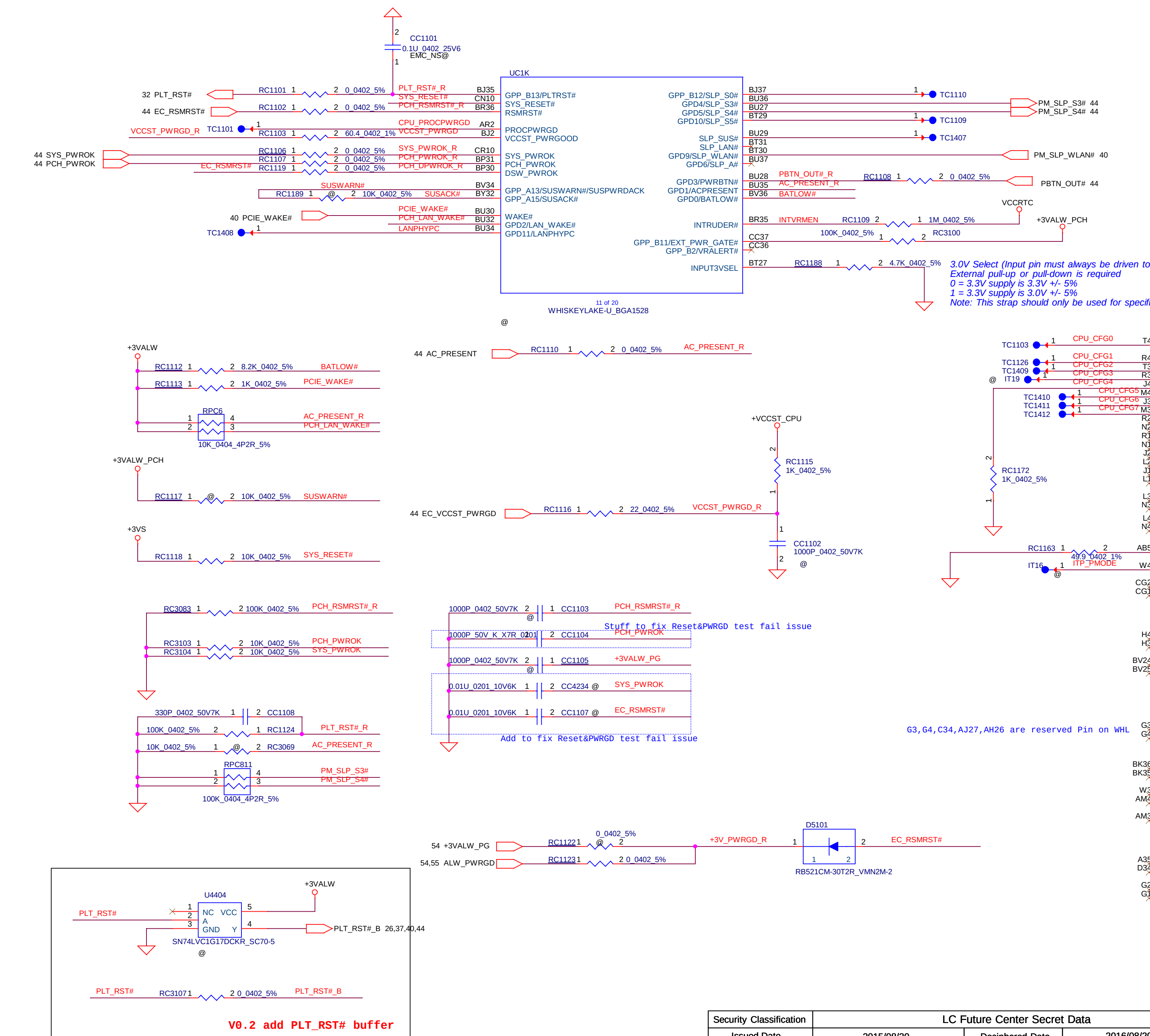
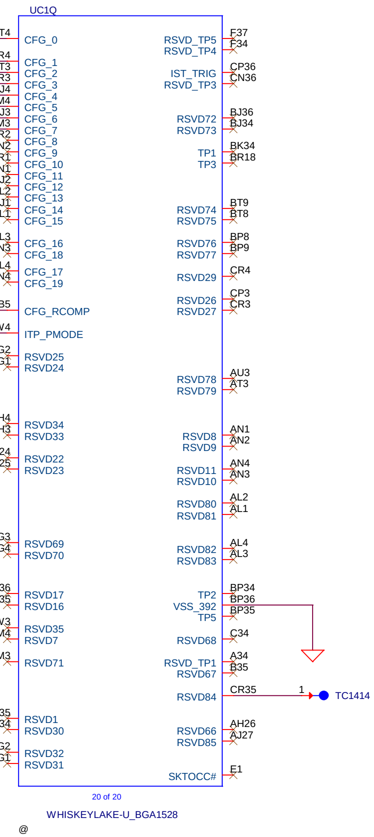
- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.





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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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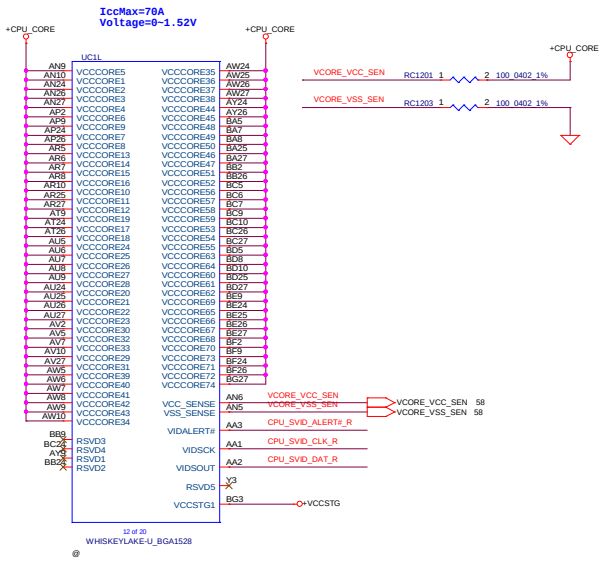
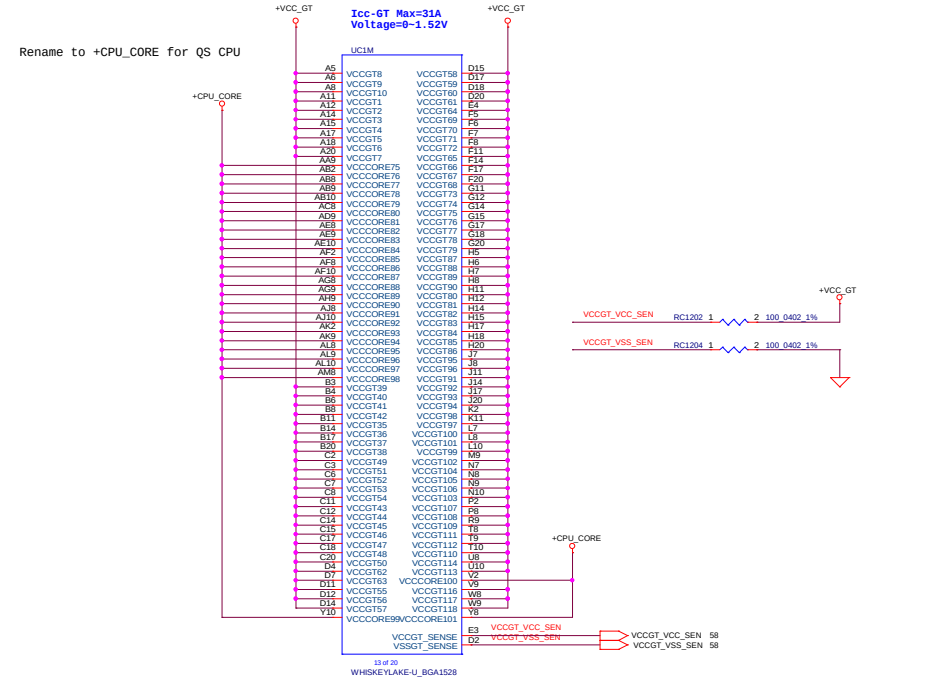
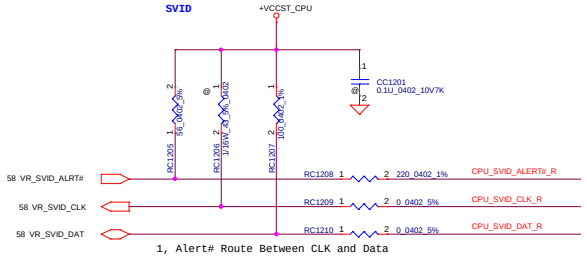
Title: **MCP (SYSTEM PWR MANAGEMENT)**

Size: Custom | Document Number: **FS441/FS540** | Rev 0.1

Date: Friday, October 26, 2018 | Sheet 11 of 61







1, Alert# Route Between CLK and Data

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

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Title: MCP (CPU PWR1)

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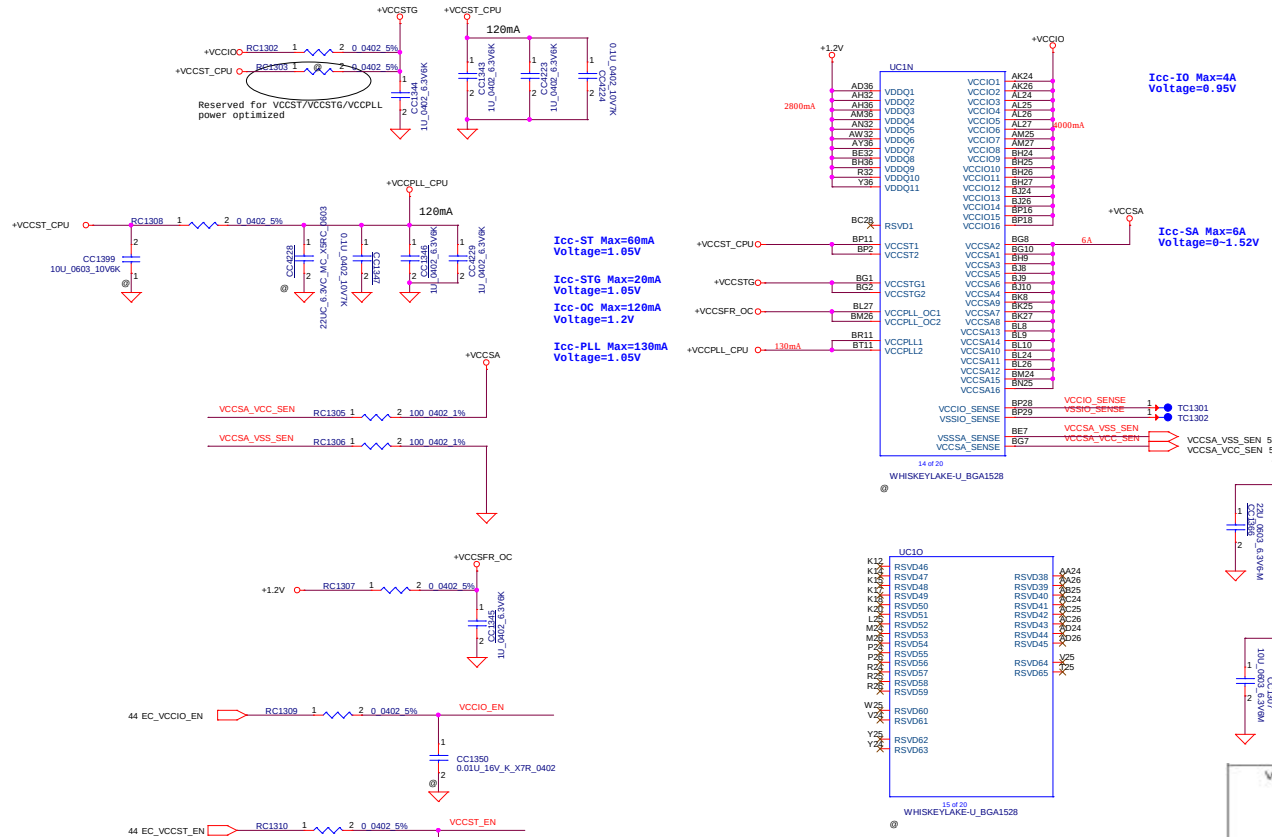
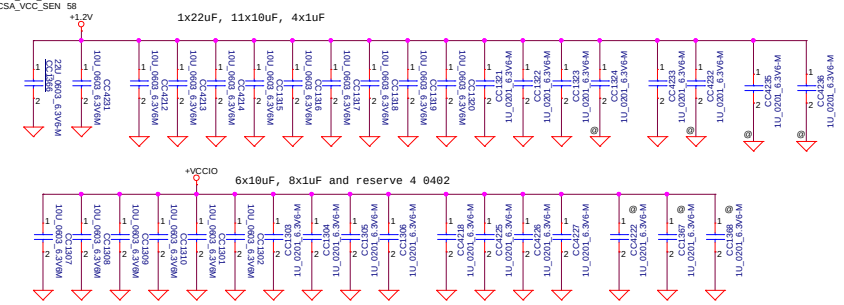
WHL ES1 will be a CFL-U43e fused down to CFL-U42

* Pins marked RSVD must be left as NC



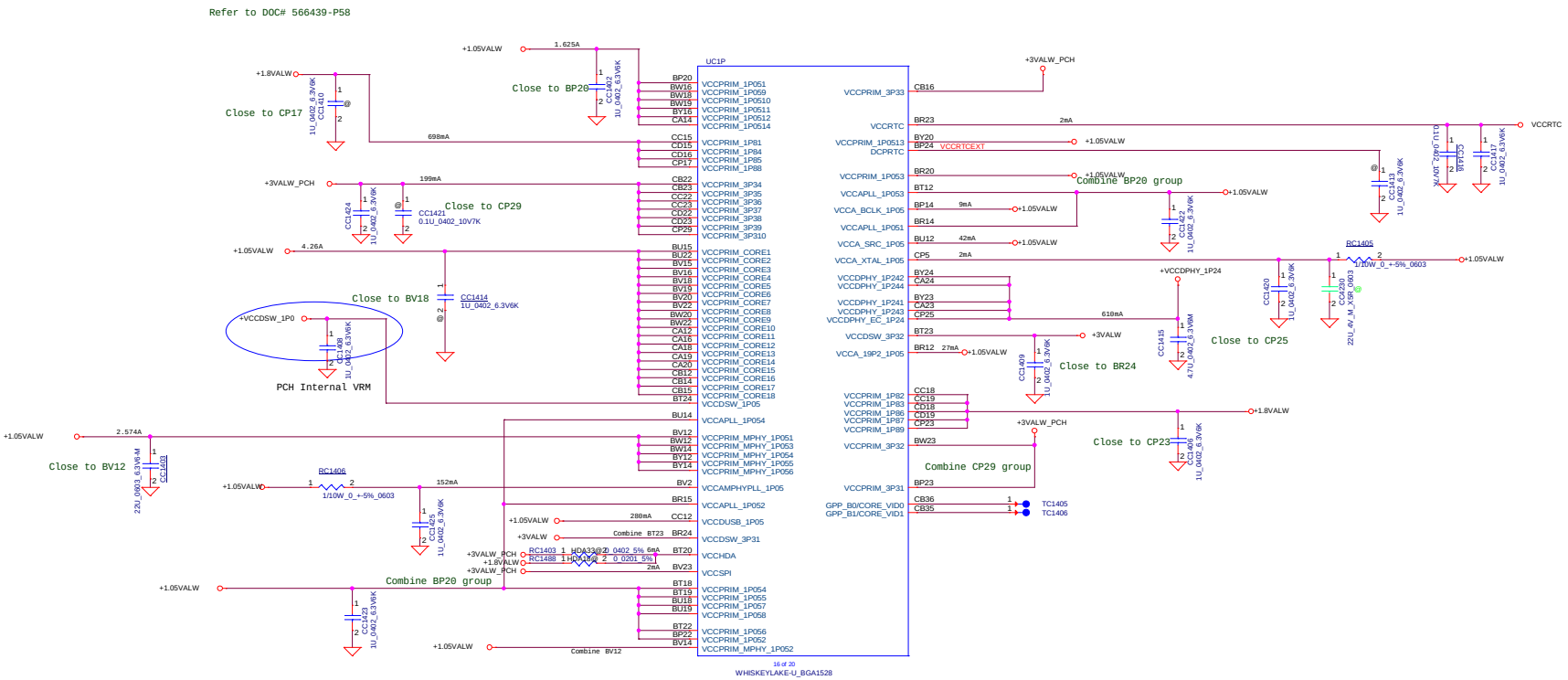


V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603 6x 10uF 0402		
V_{CCIO}	4x 1uF 0201		Place underneath the package
	4x 1uF 0402/0201		Place as close to the package as possible
	6x 10uF 0402		
	4x 0402		*Placeholder Only*
V_{CCPLL_OC}	1x 1uF 0402		Do not merge V_{CCPLL}, V_{CCPLL_OC} and V_{CCST} to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PIT failing to phase lock.
V_{CCPLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
V_{CCST}	1x 1uF 0402		
V_{CCSTG}	1x 1uF 0402		
$V_{CCEOPIO}$		6x 1uF 0201	Place under BGA.
		2x 22uF 0603	$V_{CCEOPIO}$ and V_{CCOPC} rails are merged on board. VT to be placed as close as possible to BGA and a wide plane routing to meet DC_R <= 7mOhm.
V_{CCOPC}		4x 10uF 0402	
		2x 22uF 0603	$V_{CCEOPIO}$ and V_{CCOPC} is required for CFL-U43e SKUs only.

Title: MCP (CPU PWR2)

Size: Custom | Document Number: FS441/FS540 | Rev: 0.1

Date: Friday, October 26, 2018 | Sheet 13 of 61

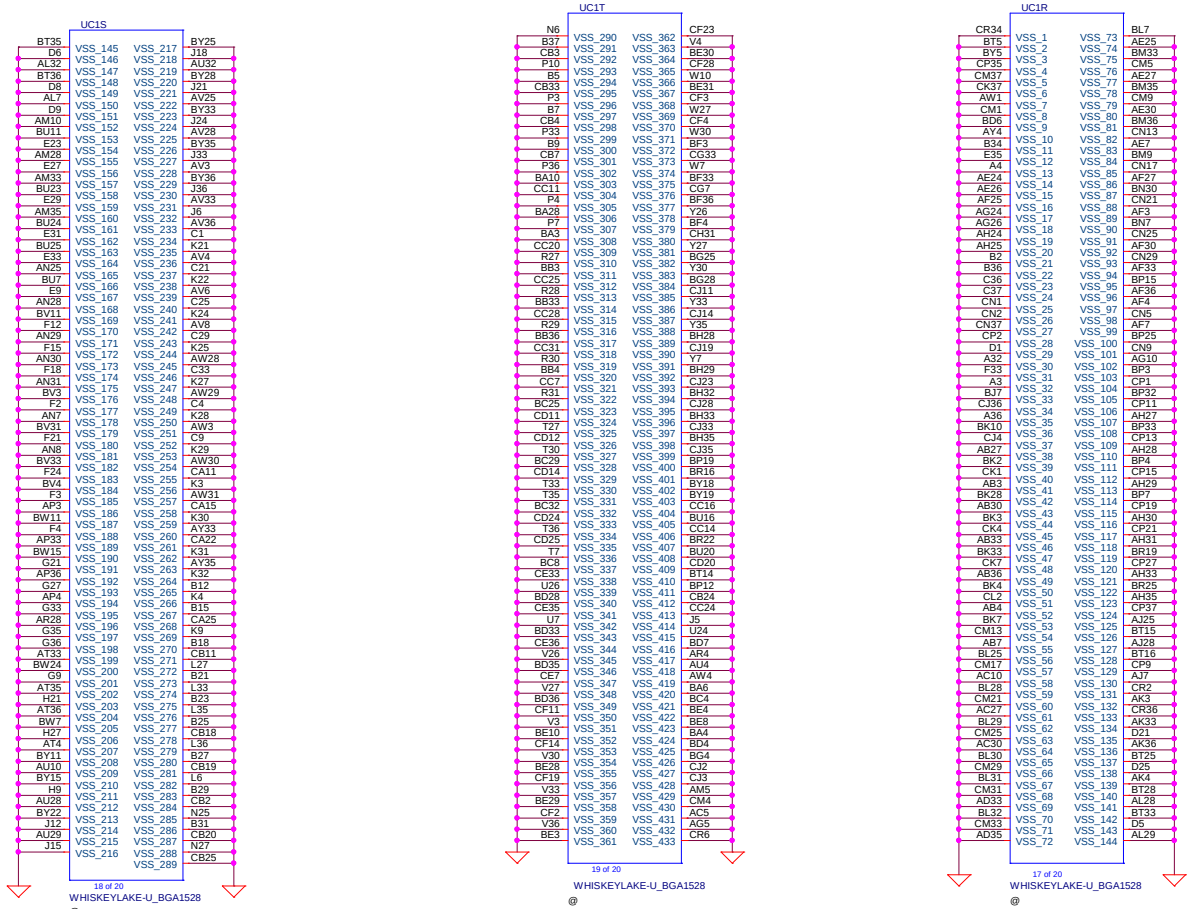


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (PCH PWR)**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

Date: Friday, October 26, 2018 | Sheet 14 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (VSS)

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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Place test points close to CPU

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

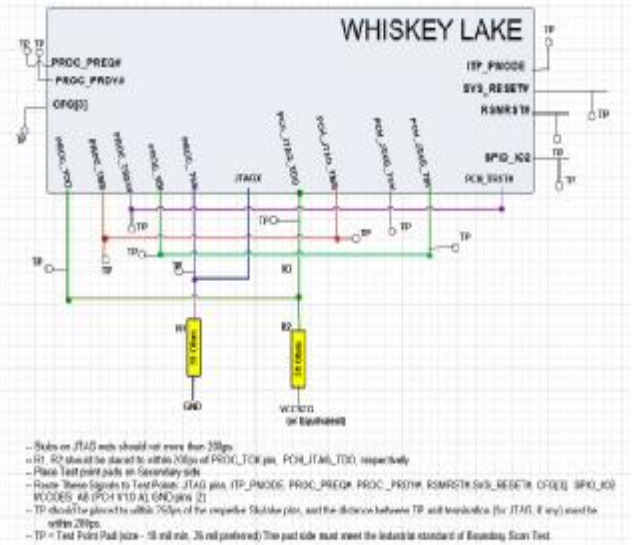
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



- Stubs on JTAG nets should not exceed than 200ps.
- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
- Place Test point pads on Secondary side
- Route these Signals to Test Points: JTAG pins ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[0], SPKR_IO2, VCCDIES, AB (PCH Y10,AL6),GND pins (2)
- TP should be placed to within 750ps of the respective Stub/via pins, and the distance between TP and test points (for JTAG, if any) must be within 200ps.
- TP = Test Point Pad (size - 18 mil min, 35 mil preferred) The pad side must meet the Industrial standard of Boundary Scan Test.

Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: XDP

Size	Document Number	Rev
Custom	FS441/FS540	0.1

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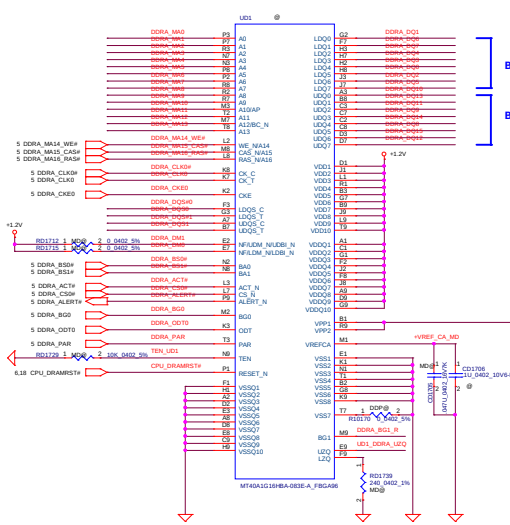
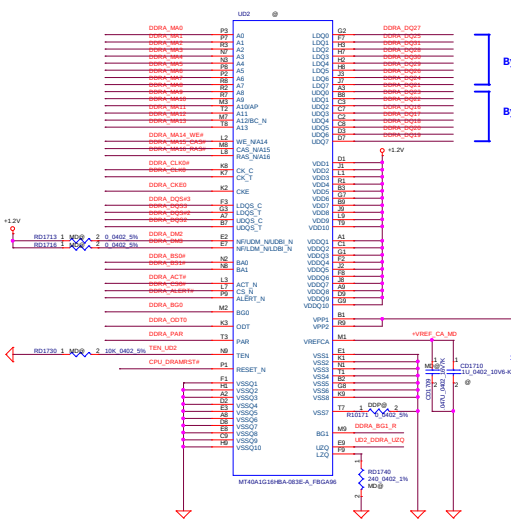
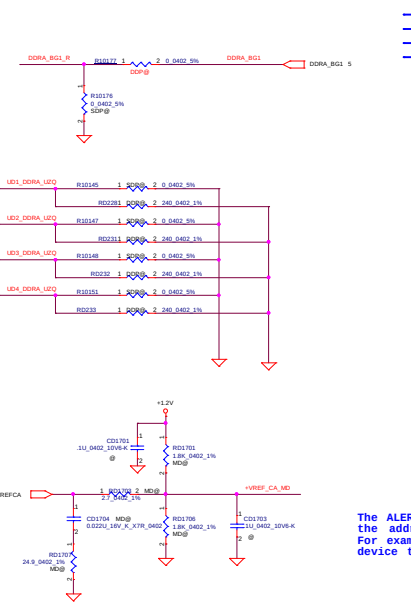
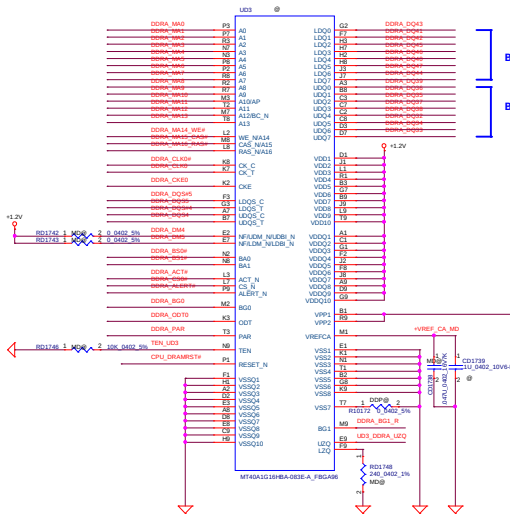
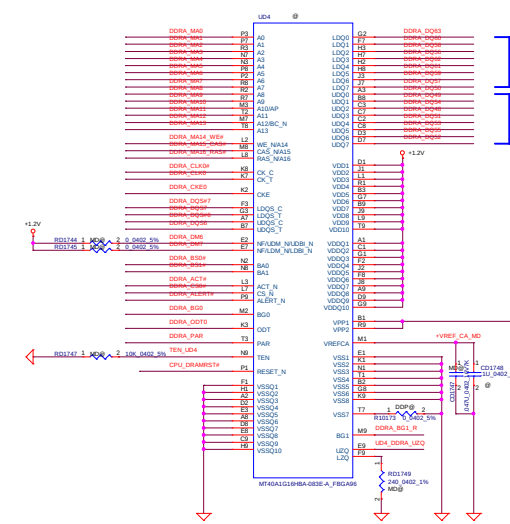
Apply X76 BOM to control DDP Memory Down stuff components!

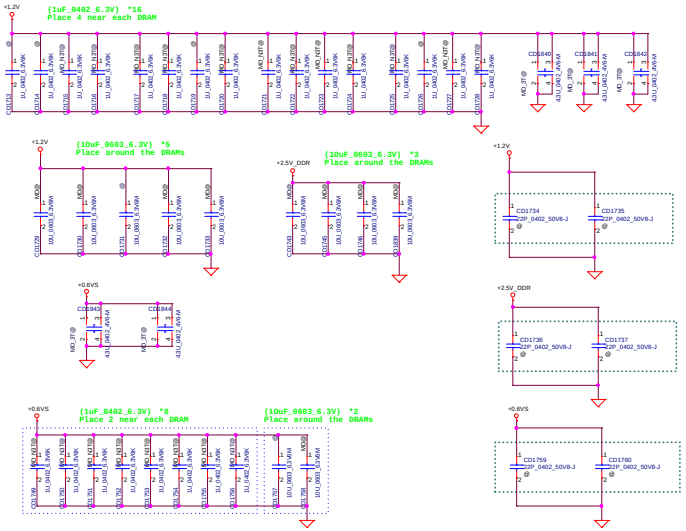












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Issued Date	2017/06/24	Deciphered Date	2018/06/23

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Title	DDR4 Memory Down		
Size	Document Number		Rev
Custom	FS441/FS540		0.1
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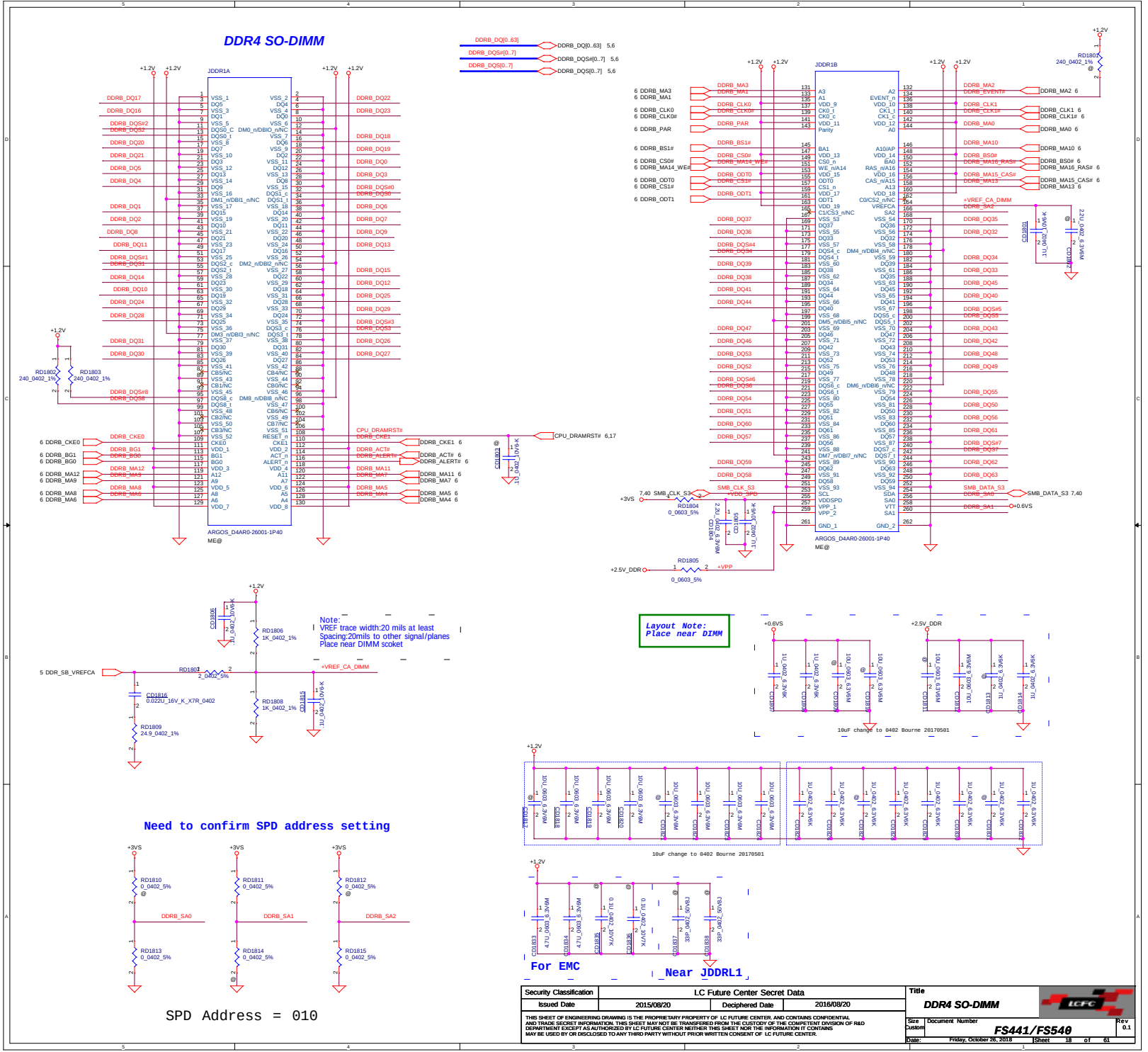

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	DDR4 SO-DIMM
Size	Custom
Document Number	FS441/FS540
Rev	0.1
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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Title: VGA Notes List

Size	Document Number	Rev
C	FS441/FS540	0.1

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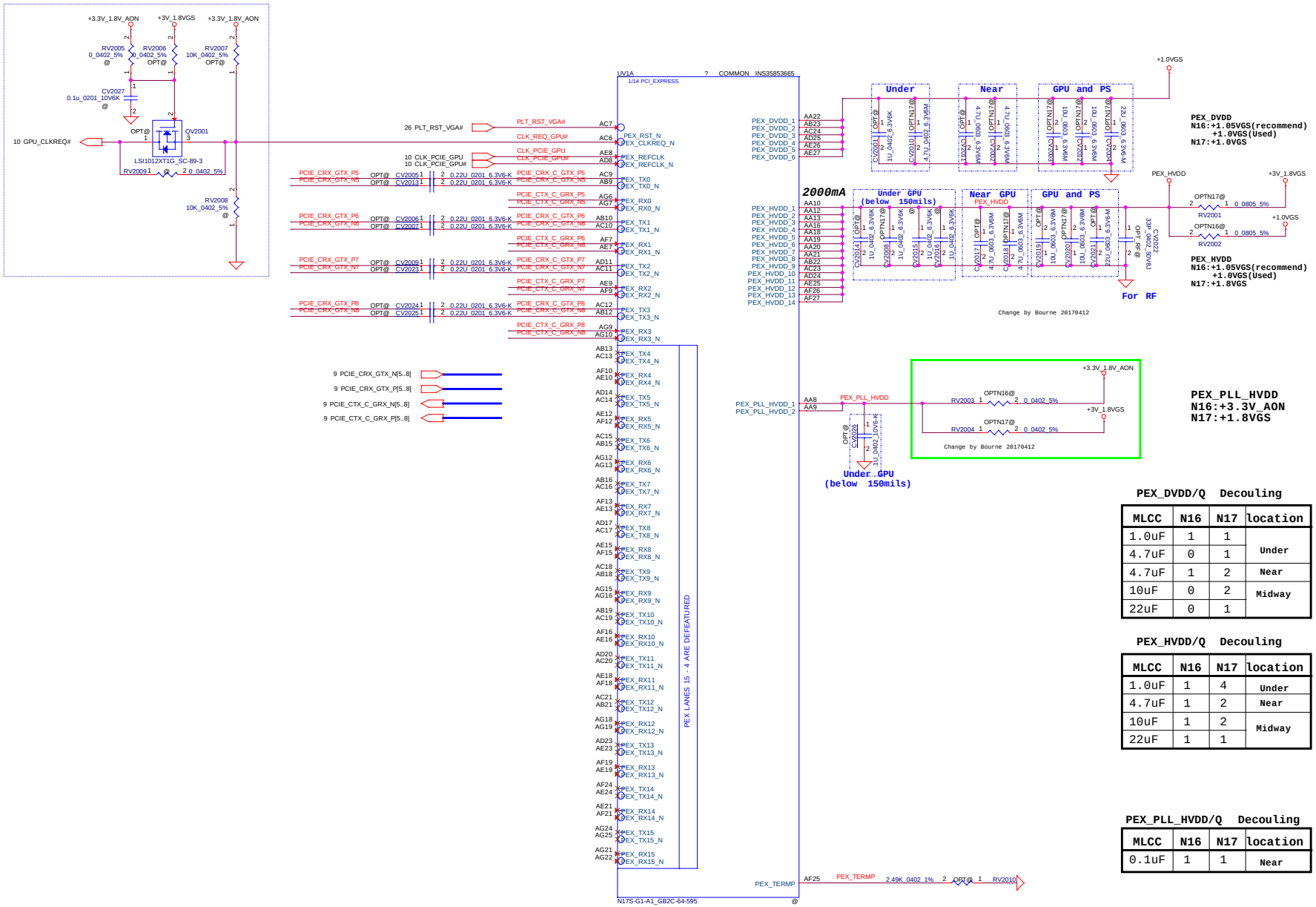

PEX_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

Title: **GPU_PCIE Interface**

Size	Document Number	Rev
C	FS441/FS540	0.1

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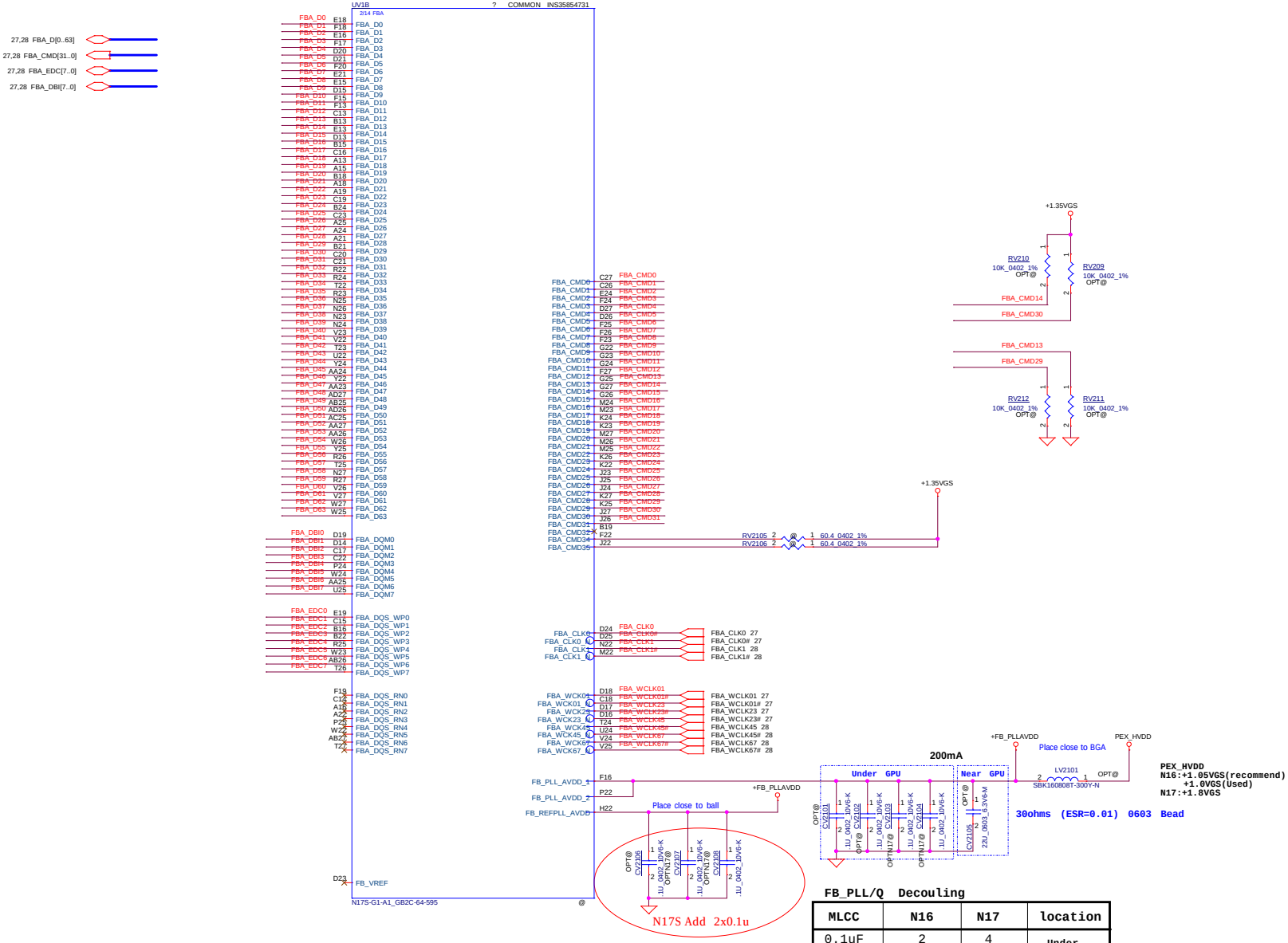

FB_PLL/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_MEM Interface**

Size	Document Number	Rev
C	FS441/FS540	0.1

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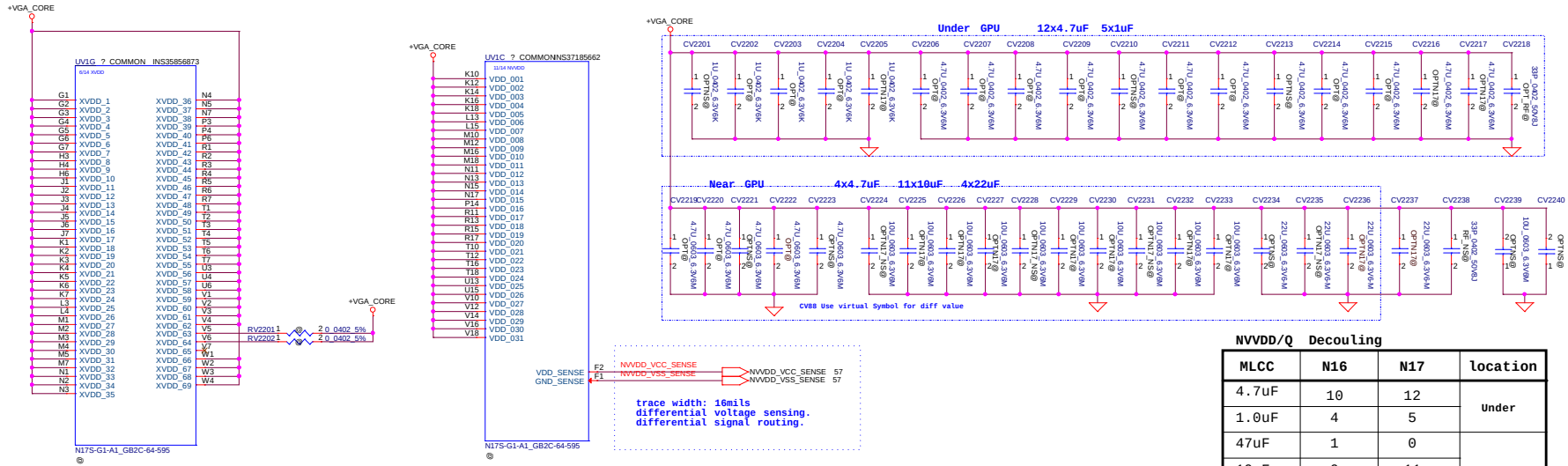
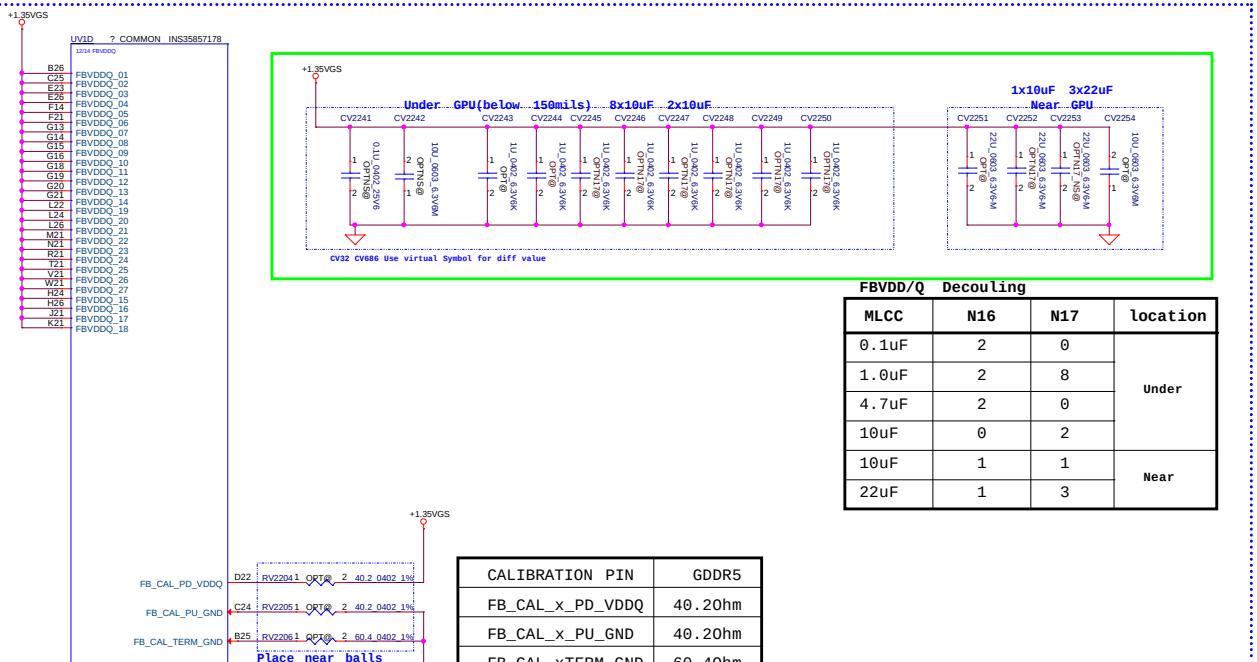


NVVDD/Q Decoupling

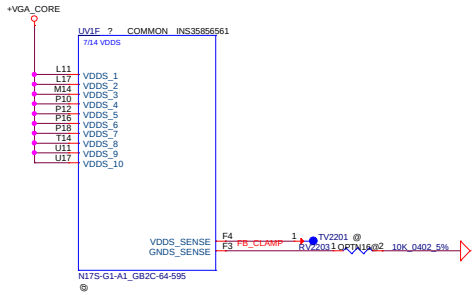
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_+VGA_CORE,FBVDDQ

Size: C | Document Number: FS441/FS540 | Rev: 0.1

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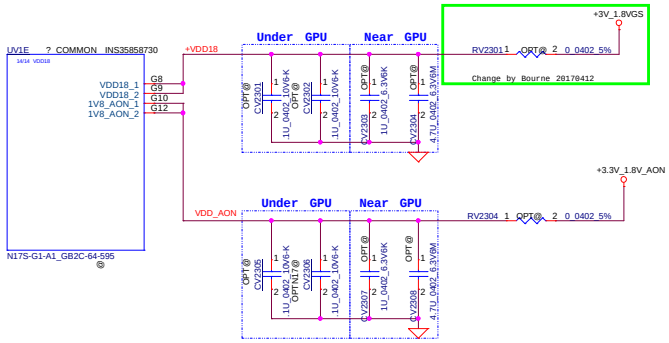
N16 3V3_MAIN(N17 VDD_18) Decouling

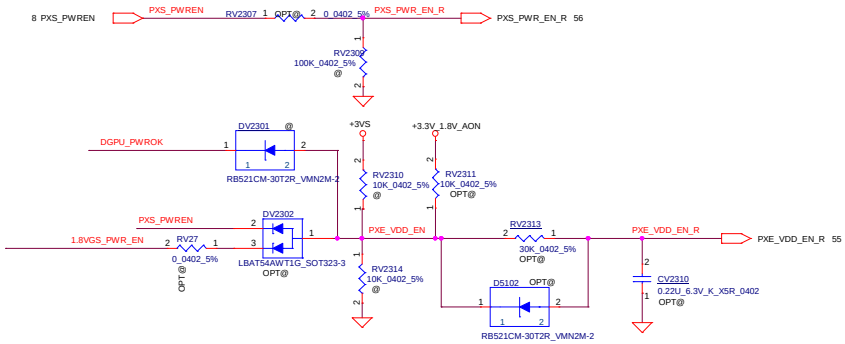
MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

N16 3V3_AON(N17 1V8_AON) Decouling

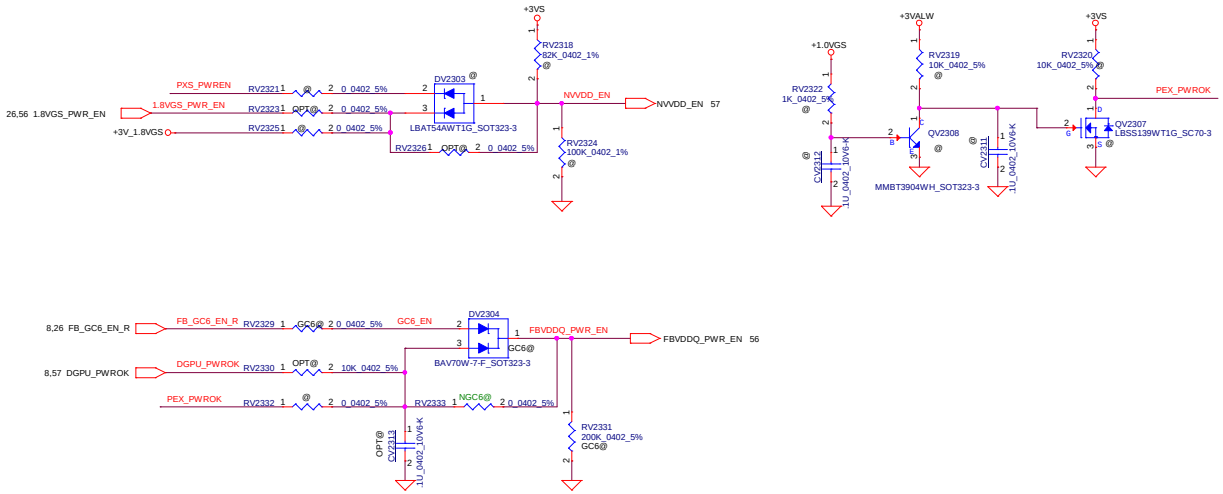
MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	



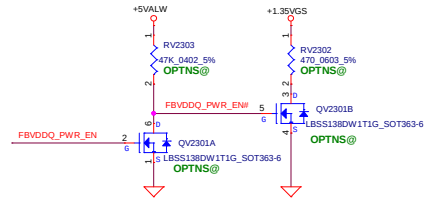
PXE_VDD & 1V8_AON

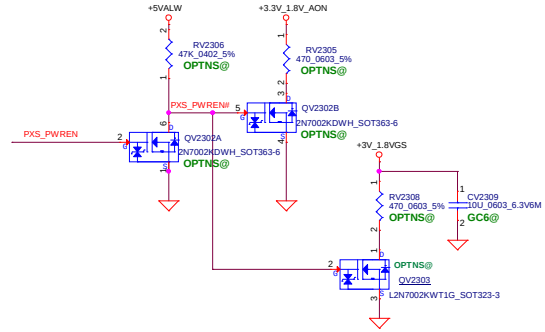


+1.8VG_AON TO +1.8VS

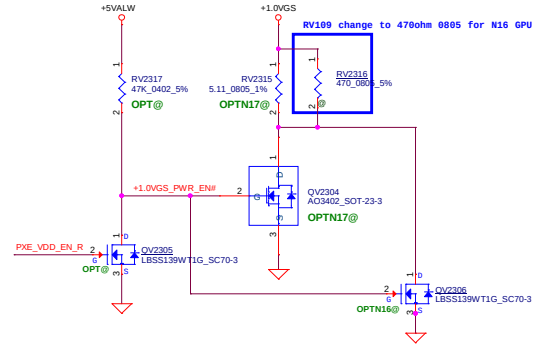


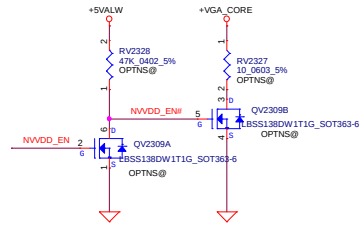
Discharge





RV2316 [illegible],N16 =470 ohm,N17= 5.11k





Title: GPU_AON/MAIN PWR/SEQ

Size: C | Document Number: FS441/FS540 | Rev: 0.1

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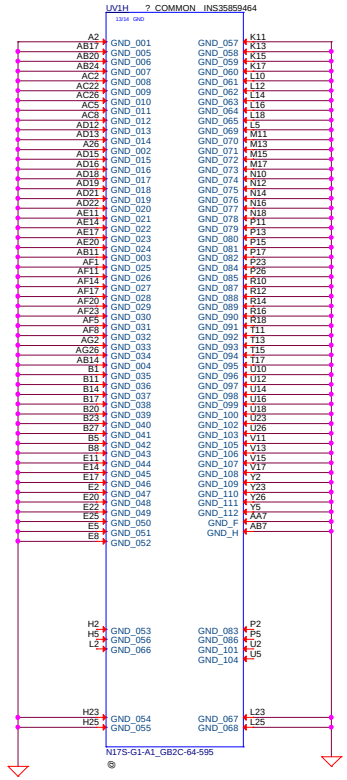

Title: **GPU_GND**

Size	Document Number	Rev
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PEX_PLLVDD/Q Decouling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

PEX_PLLVDD
N16:+1.0VGS(recommend)
N17:NC

PEX_SVDD_3V3
N16:+3.3V_AON(recommend)
N17:NC

PEX_SVDD/Q Decouling

MLCC	N16	N17	location
4.7uF	2	NA	Near

PEX_HVDD
N16:+1.05VGS(recommend)
+1.0VGS(Used)
N17:+1.8VGS

XS_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

GPCPLL_AVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

IFPAB (DEFEATURED ON GM108)

Security Classification	LC Future Center Secret Data
Issued Date	2015/08/20
Deciphered Date	2016/08/20

Title: GPU_STRAP/DP/HDMI

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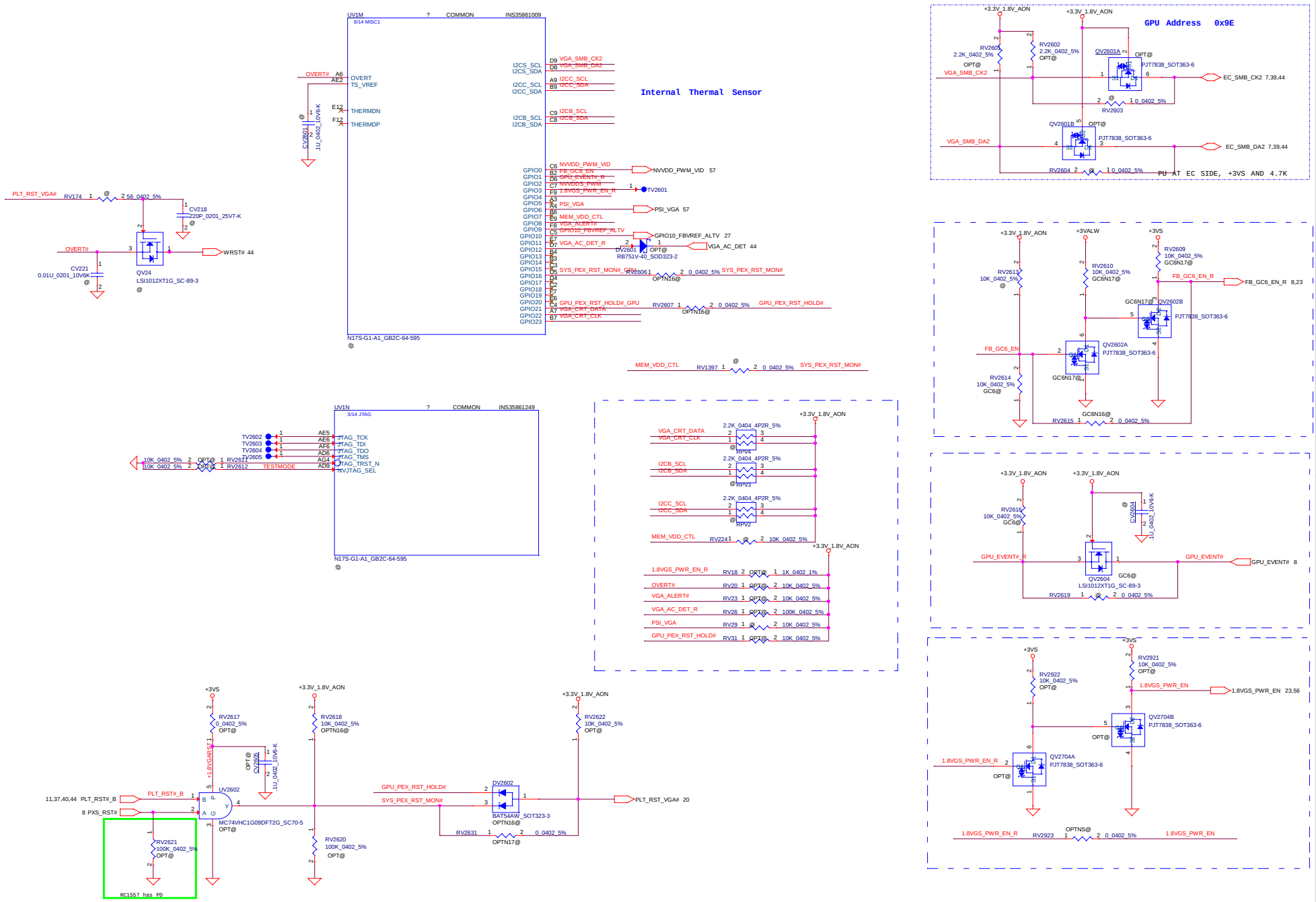
UV1M
8/14 MISC1
COMMON
INS35861009
Internal Thermal Sensor
OVERT#
OVERT
TS_VREF
THERMDN
THERMDP
CV2601
1U_0402_10V6-K
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
VGA_SMB_CK2
VGA_SMB_DA2
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
NVVDD_PWM_VID
FB_GC6_EN
GPU_EVENT#_R
NVVDDS_PWM
1.8VGS_PWR_EN_R
PSI_VGA
MEM_VDD_CTL
VGA_ALERT#
GPIO10_FBVREF_ALTV
VGA_AC_DET_R
SYS_PEX_RST_MON#_GPU
GPU_PEX_RST_HOLD#_GPU
VGA_CRT_DATA
VGA_CRT_CLK
NVVDD_PWM_VID 57
TV2601
PSI_VGA 57
GPIO10_FBVREF_ALTV 27
VGA_AC_DET 44
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
N17S-G1-A1_GB2C-64-595
PLT_RST_VGA#
RV174 56 0402 5%
CV218 220P_0201_25V7-K
OVERT#
CV221 0.01U_0201_10V6K
QV24 LSI1012XT1G_SC-89-3
WRST# 44
MEM_VDD_CTL
RV1397
SYS_PEX_RST_MON#
UV1N
3/14 JTAG
COMMON
INS35861249
TV2602
TV2603
TV2604
TV2605
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
NVJTAG_SEL
10K_0402_5% OPT@ RV2611
10K_0402_5% OPT@ RV2612
TESTMODE
N17S-G1-A1_GB2C-64-595
+3.3V_1.8V_AON
VGA_CRT_DATA
VGA_CRT_CLK
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
2.2K_0404_4P2R_5%
RPV4
RPV3
RPV2
MEM_VDD_CTL
RV2241 2K 0402 5%
1.8VGS_PWR_EN_R
RV18 OPT@ 1K_0402_1%
OVERT#
RV20 OPT@ 10K_0402_5%
VGA_ALERT#
RV23 OPT@ 10K_0402_5%
VGA_AC_DET_R
RV26 OPT@ 100K_0402_5%
PSI_VGA
RV29 10K_0402_5%
GPU_PEX_RST_HOLD#
RV31 OPT@ 10K_0402_5%
GPU Address 0x9E
+3.3V_1.8V_AON
RV2601 2.2K_0402_5% OPT@
RV2602 2.2K_0402_5% OPT@
QV2601A PJT7838_SOT363-6
QV2601B PJT7838_SOT363-6
VGA_SMB_CK2
VGA_SMB_DA2
EC_SMB_CK2 7,39,44
EC_SMB_DA2 7,39,44
RV2603 0 0402 5%
RV2604 0 0402 5%
PU AT EC SIDE, +3VS AND 4.7K
+3VALW
+3VS
RV2610 10K_0402_5% GC6N17@
RV2609 10K_0402_5% GC6N17@
RV2613 10K_0402_5%
FB_GC6_EN_R
FB_GC6_EN_R 8,23
QV2602B PJT7838_SOT363-6
QV2602A PJT7838_SOT363-6
RV2614 10K_0402_5% GC6@
RV2615 GC6N16@
RV2616 10K_0402_5% GC6@
CV2604 1U_0402_10V6-K
GPU_EVENT#_R
GPU_EVENT#
GPU_EVENT# 8
QV2604 LSI1012XT1G_SC-89-3
RV2619 GC6@
RV2617 0_0402_5% OPT@
RV2618 10K_0402_5% OPTN16@
RV2622 10K_0402_5% OPT@
CV2605 OPT@ 1U_0402_10V6-K
+1.8VGS
UV2602
MC74VHC1G09DFT2G_SC70-5
OPT@
11,37,40,44 PLT_RST#_B
8 PXS_RST#
PLT_RST#_B
GPU_PEX_RST_HOLD#
SYS_PEX_RST_MON#
DV2602
BAT54AW_SOT323-3
OPTN16@
PLT_RST_VGA# 20
RV2631 OPTN17@
RV2620 100K_0402_5% OPT@
RV2621 100K_0402_5% OPT@
RC1557 has PD
RV2921 10K_0402_5% OPT@
RV2922 10K_0402_5% OPT@
1.8VGS_PWR_EN
1.8VGS_PWR_EN 23,56
QV2704B PJT7838_SOT363-6
QV2704A PJT7838_SOT363-6
1.8VGS_PWR_EN_R
RV2923 OPTN@
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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Title
GPU_GPIO/JTAG
Size C
Document Number
FS441/FS540
Rev 0.1
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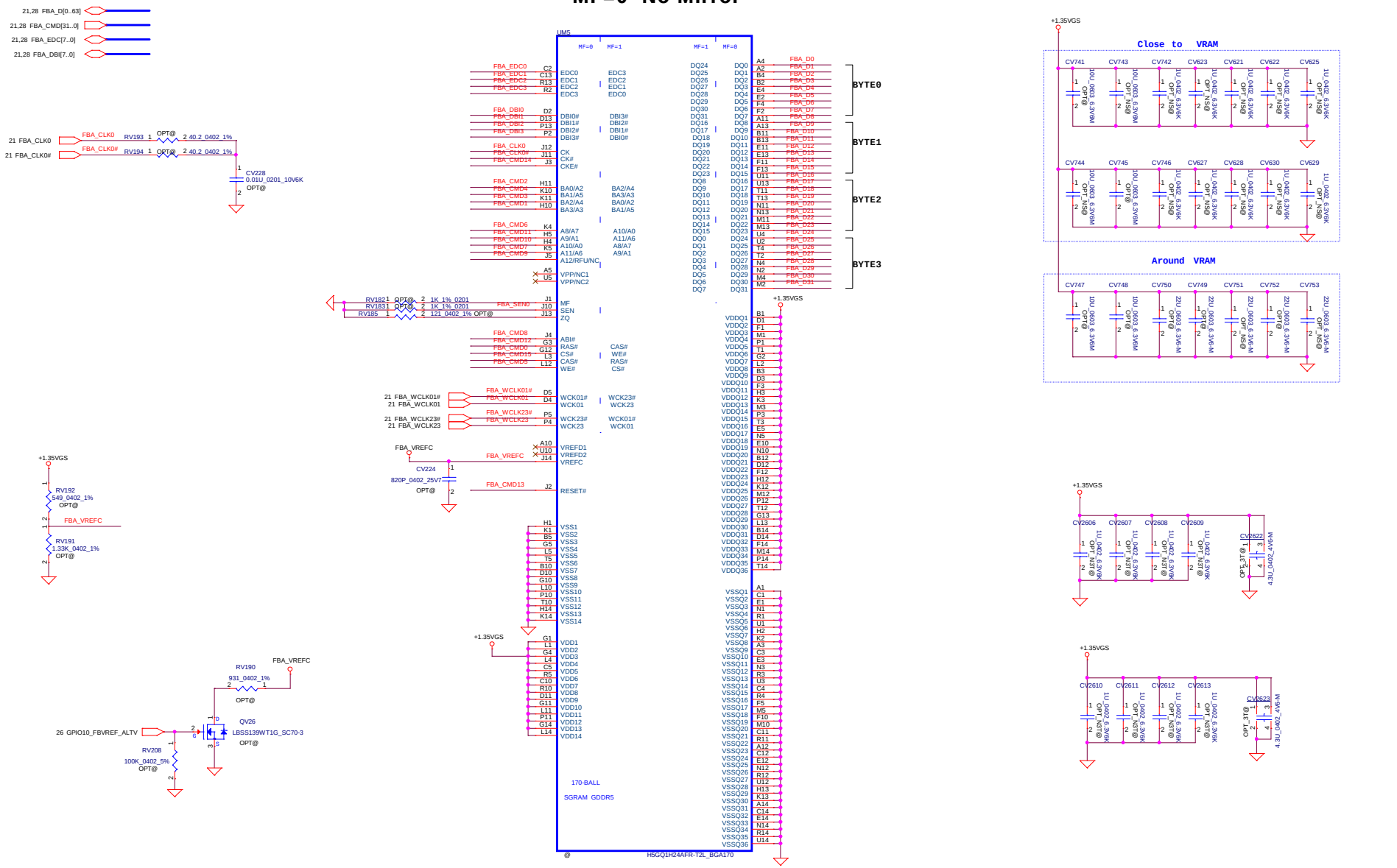
Lower 32 bits

MF=0 No Mirror



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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: GPU_GDDR5_Rank0_[31:0]

Size	Document Number	Rev
C	FS441/FS540	0.1

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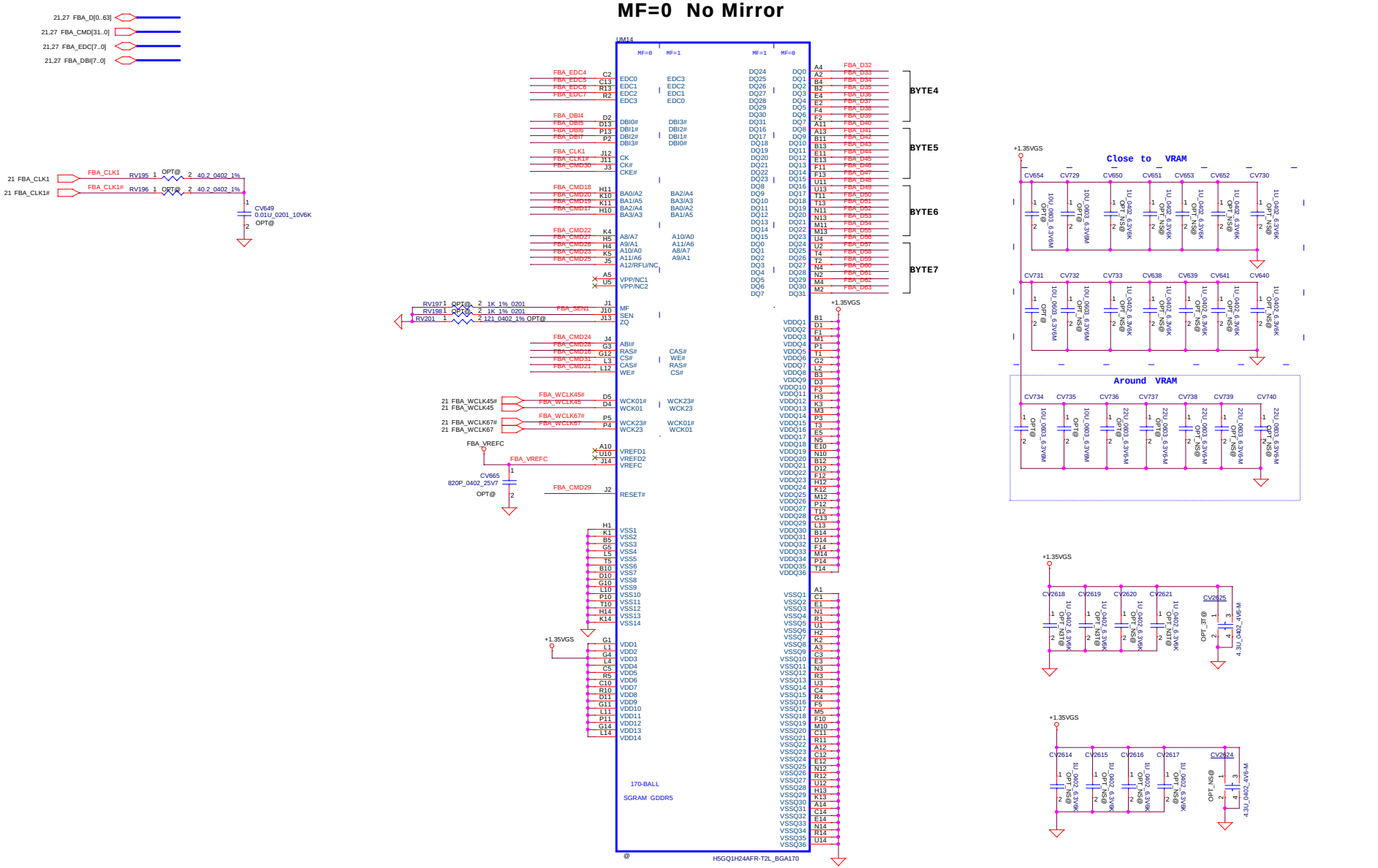
upper 32 bits

MF=0 No Mirror



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	GPU_GDDR5_Rank0_[64:32]		
Size C	Document Number FS441/FS540		Rev 0.1
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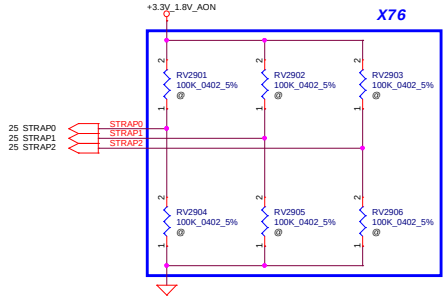
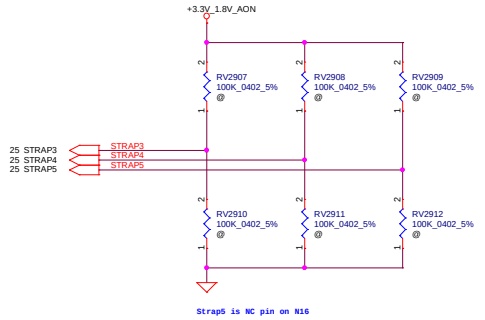


GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



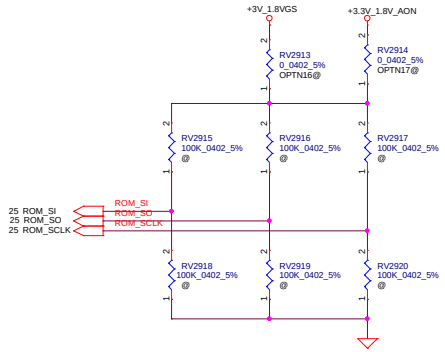
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

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Title: GPU_MISC

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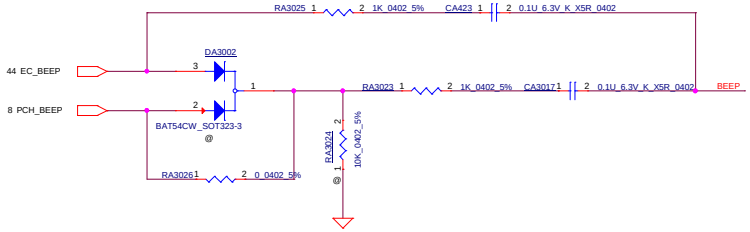

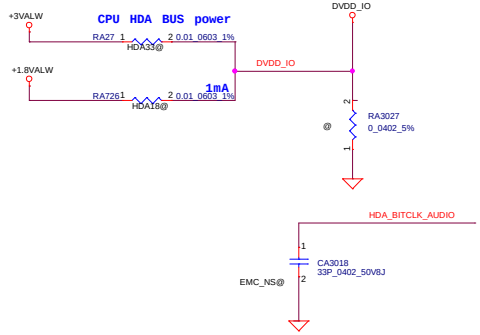

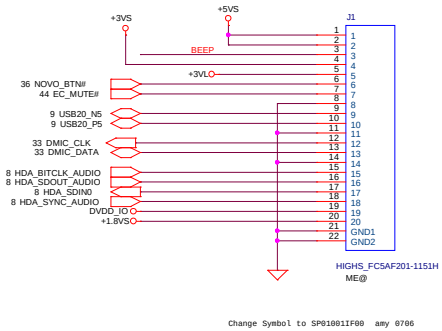

Change Symbol to SP01001IF00 amy 0706

20Pin CONN

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CODEC_RTS5199

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Title	<Title>
Size A	Document Number FS441/FS540
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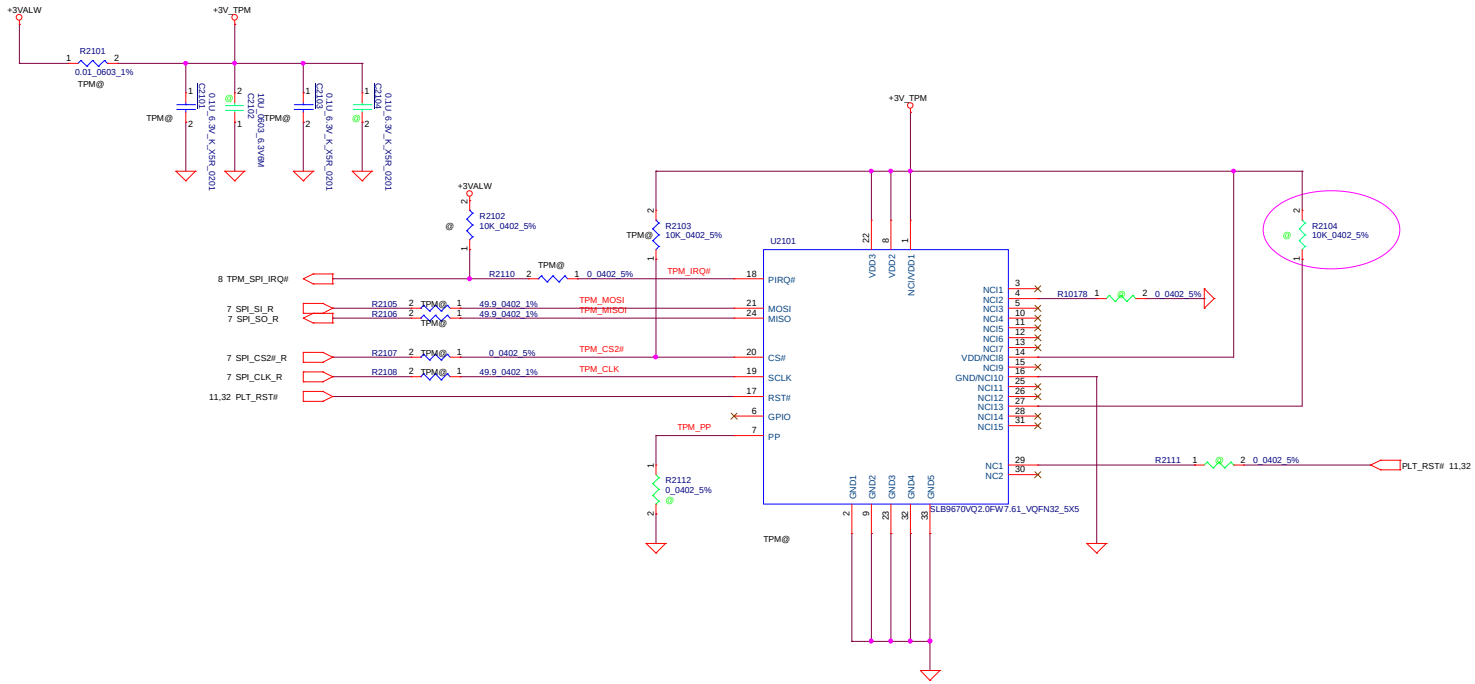

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H330TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

Title			
TPM			
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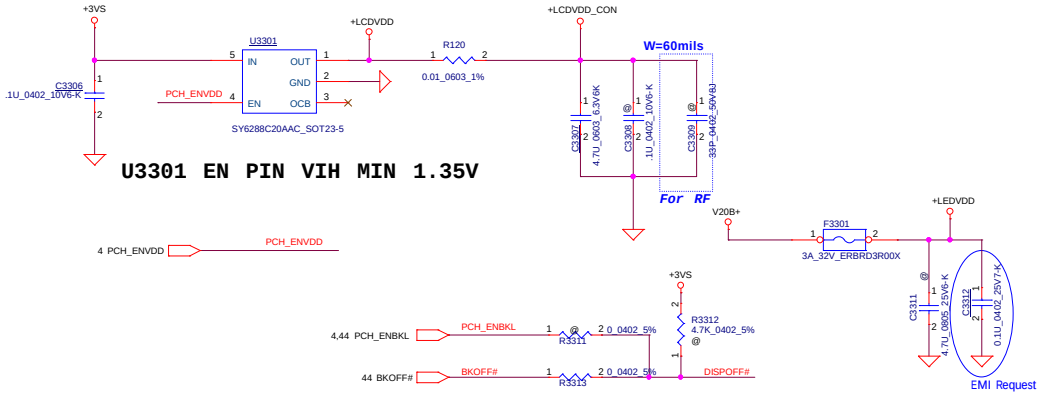
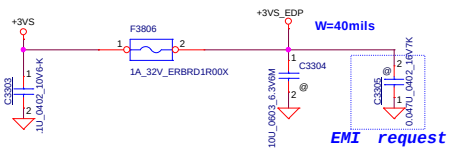
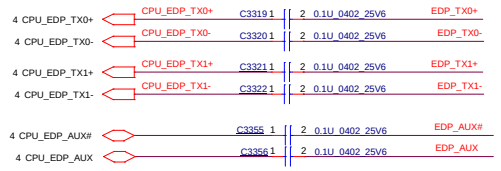
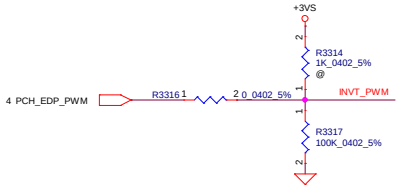
LCD POWER CIRCUIT

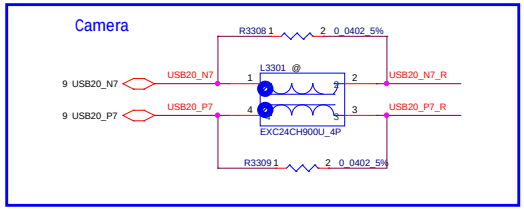


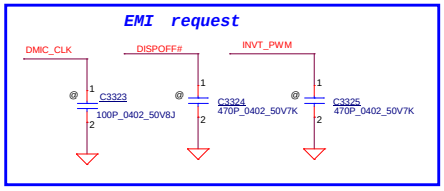
CMOS Camera

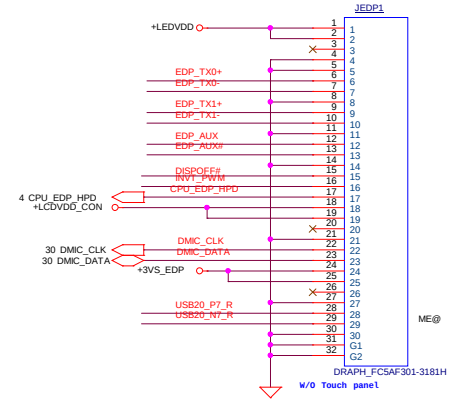




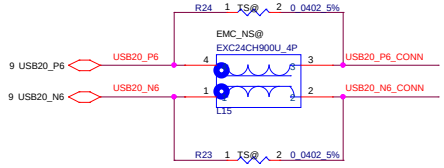


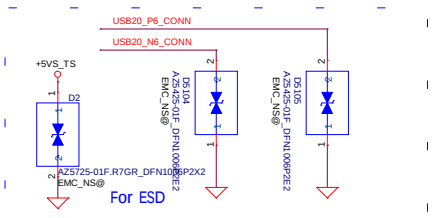


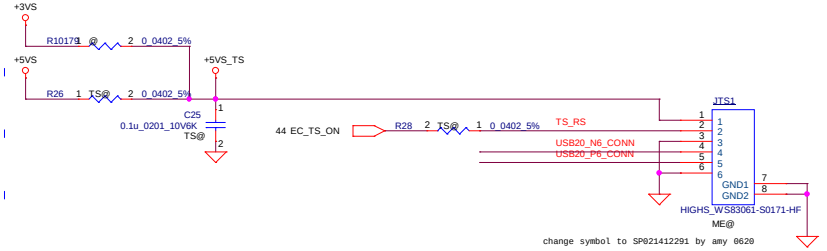




Touch Screen







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	eDP/CAMERA.		
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Custom	FS441/FS540		0.1
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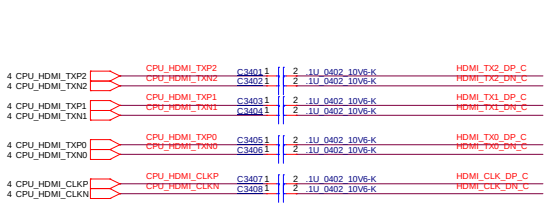
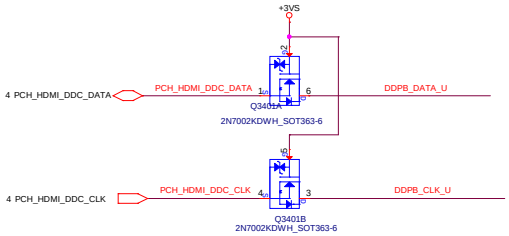
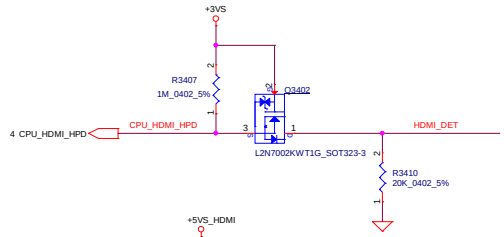
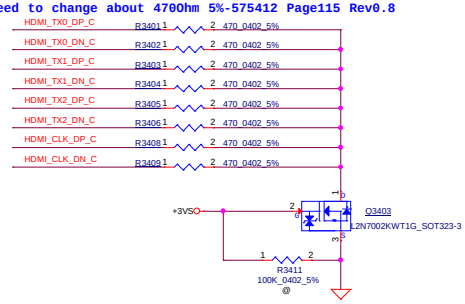
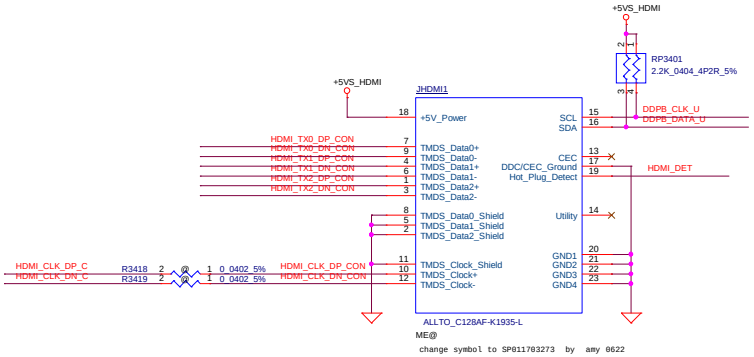




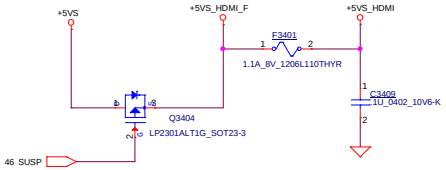


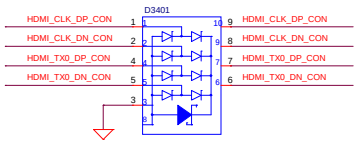
Need to change about 4700hm 5%-575412 Page115 Rev0.8



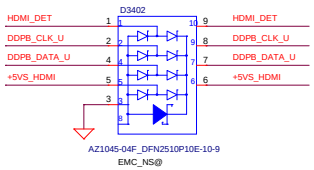


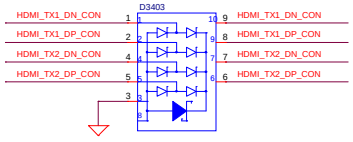
F1 use 1.1A

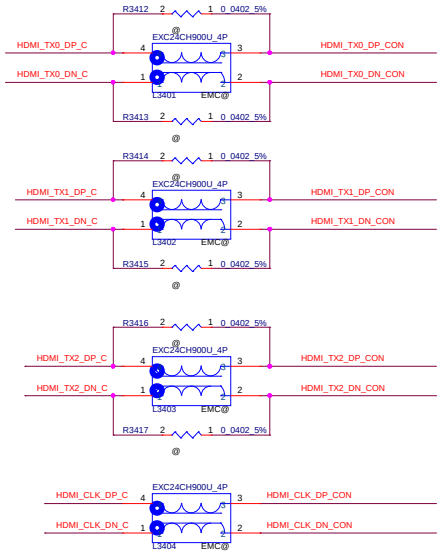




For EMC







For EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	HDMI_CONN		
Size Custom	Document Number	FS441/FS540	Rev 0.1
Date:	Friday, October 26, 2018	Sheet 34 of 61	

1.1.8VGS_PWR_EN_R pull high RV18----P26

2.ON/OFFBTN# add diode D25-----P36

3.del

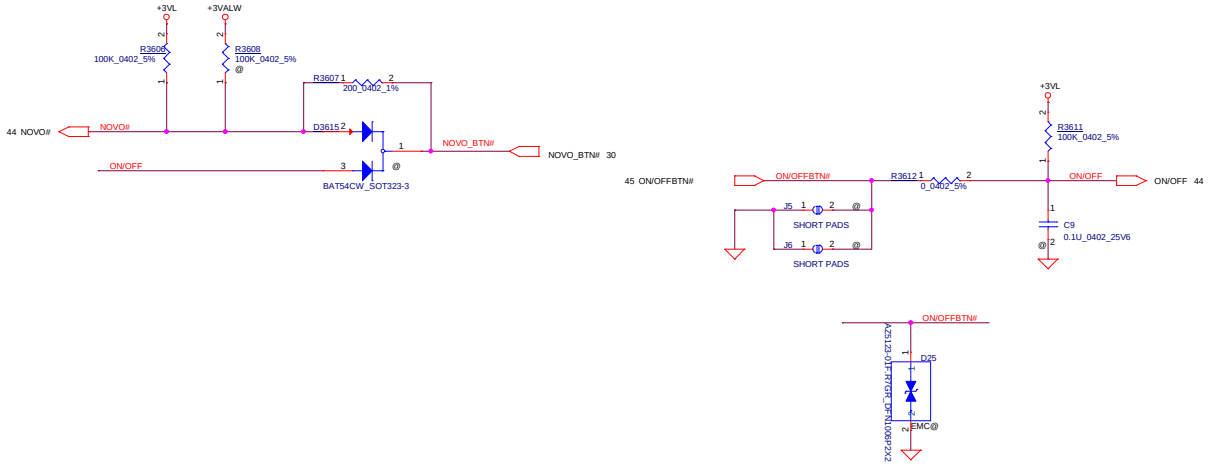
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

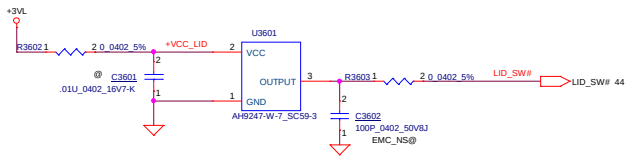
Blank

Size B	Document Number FS441/FS540	Rev 0.1
Date: Friday, October 26, 2018	Sheet 35 of 61	

ON/OFF switch



LID switch

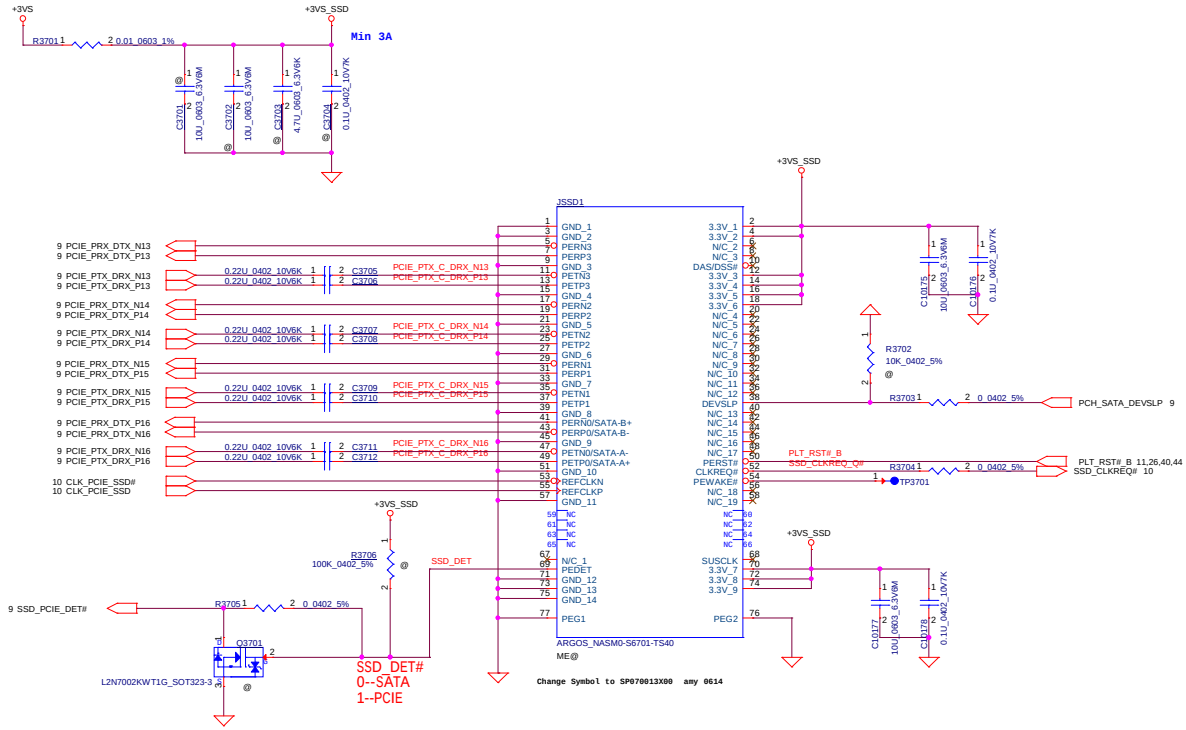


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **HALL Sensor**

Size	Document Number	Rev
Custom	FS441/FS540	0.1

Date: Friday, October 26, 2018 Sheet 36 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: NGFF_SSD_1

Size	Document Number	Rev
C	FS441/FS540	0.1

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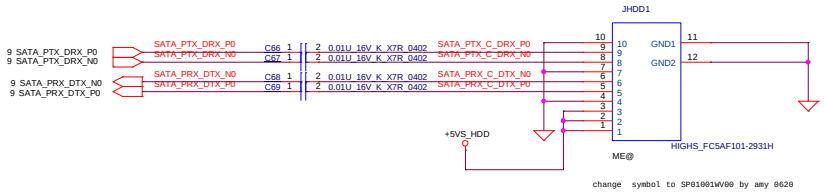

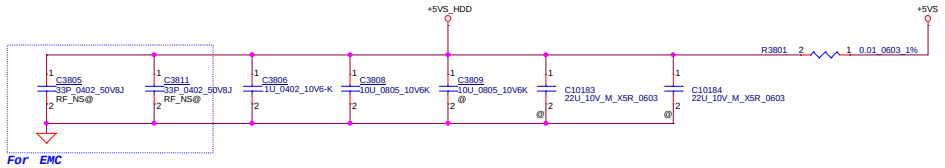

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **SATA HDD CONN**

Size	Document Number	Rev
C	FS441/FS540	0.1

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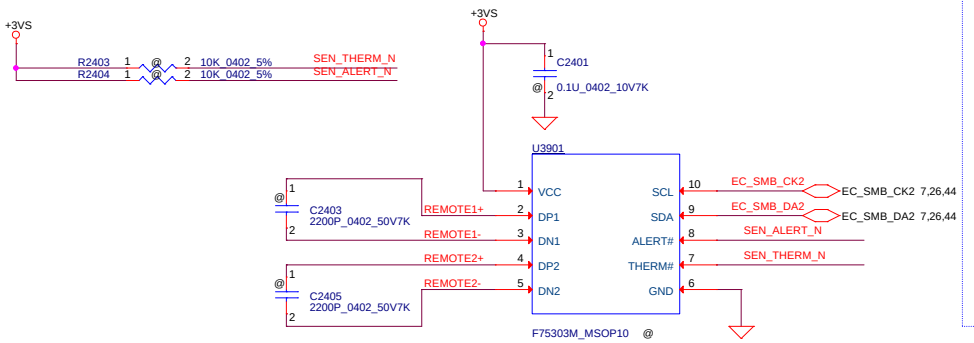
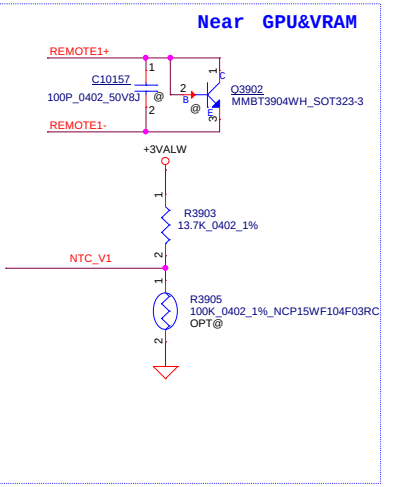
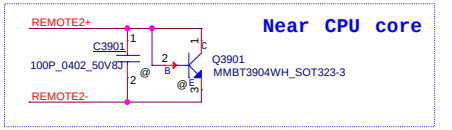
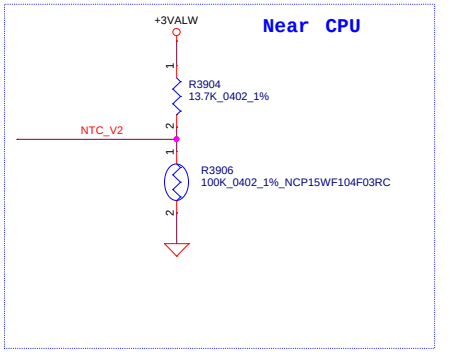
SMSC thermal sensor placed near DIMM

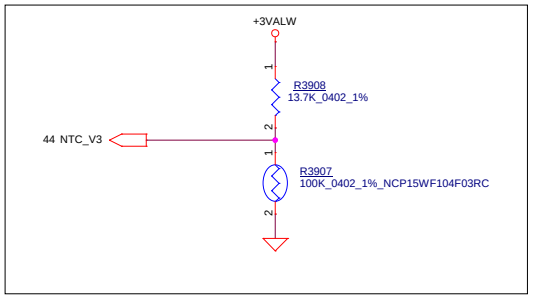
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



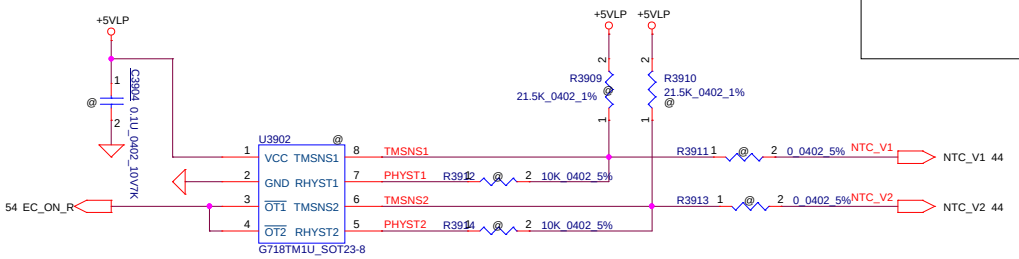




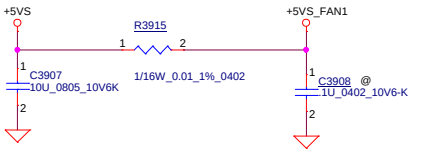




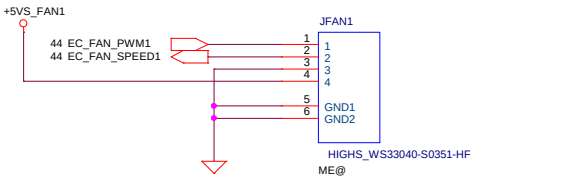
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



FAN Conn



Change Symbol to SP021410082 amy 0614

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: **Thermal sensor/FAN CONN**

Size	Document Number	Rev
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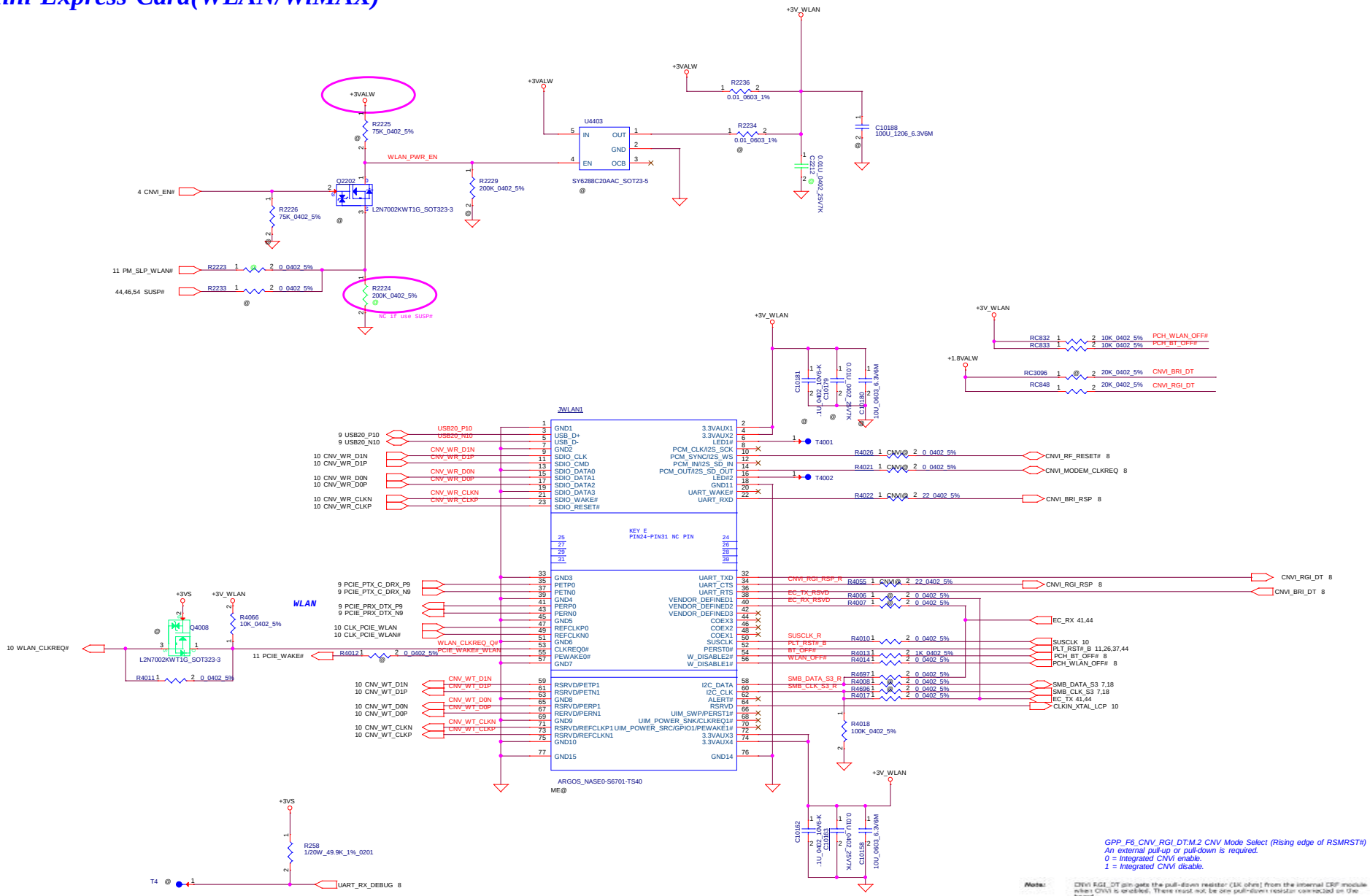
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

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Title: NGFF_WLAN

Size	Document Number	Rev
C	FS441/FS540	0.1

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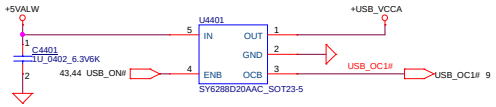
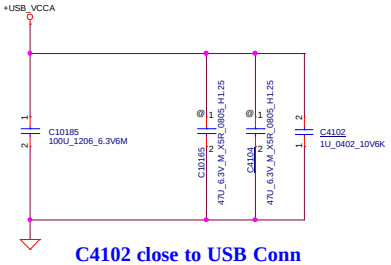
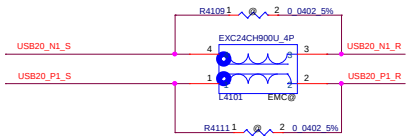
RIGHT SIDE USB3.0 PORT x1

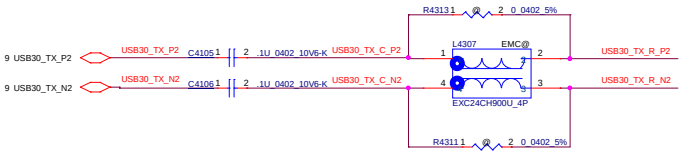


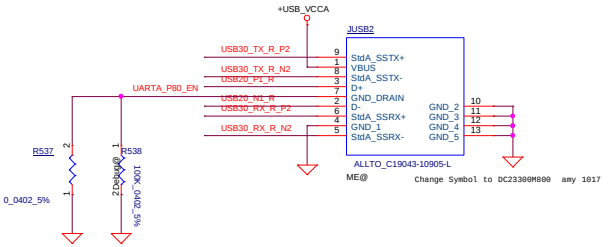
Low Active 2A

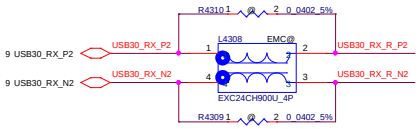


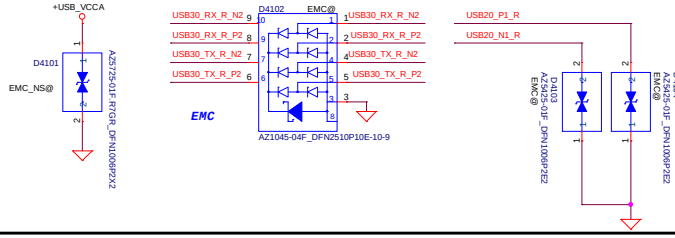
C4102 close to USB Conn



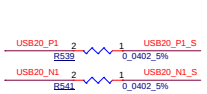


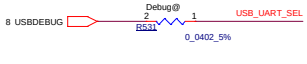


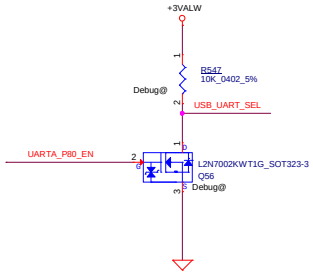




For USB Debug Function



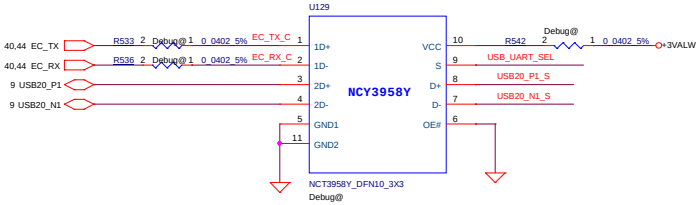




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



07/06 add USB debug function Amy

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: USB3 PORT_LEFT

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

Blank

Size	Document Number	Rev
Custom	***FS441/FS540***	0.1

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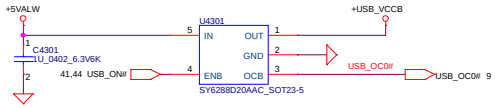
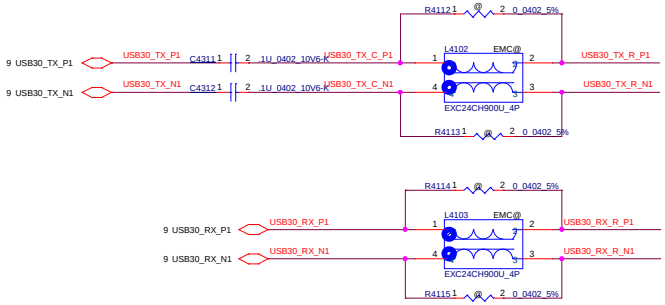
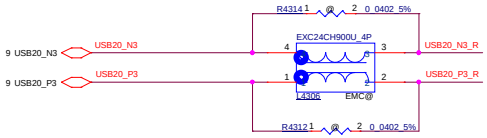
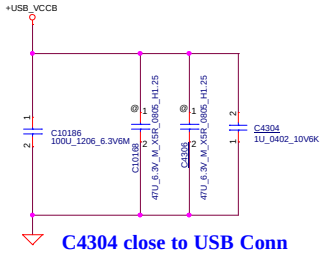
Right SIDE USB3.0 PORT



Low Active 2A

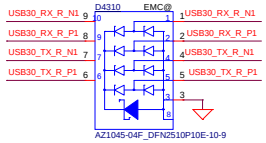




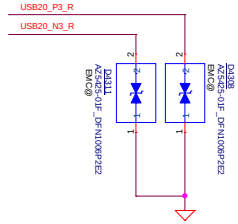


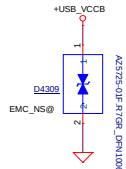
C4304 close to USB Conn

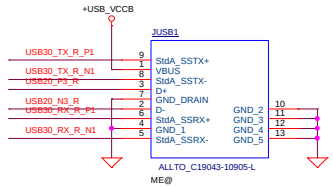
04/02 add USB debug function bron



EMC

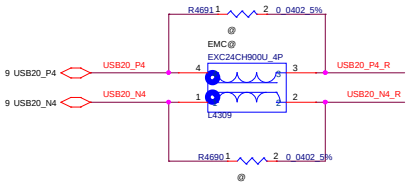


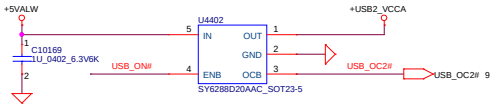




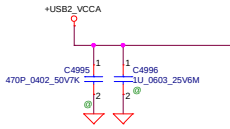
Change Symbol to SP011703284 amy 0614

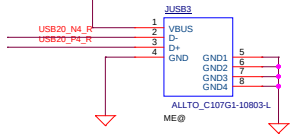
USB2.0 PORT x1



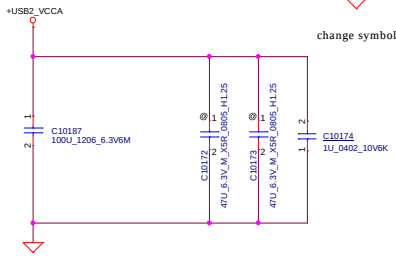


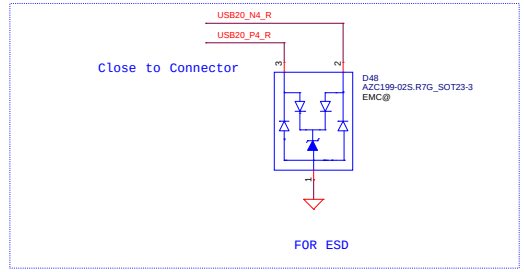
Low Active 2A

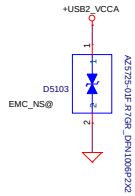




change symbol to SP011807041 amy 0710







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	USB3 Port_Right & USB2.0		
Size	Document Number		Rev
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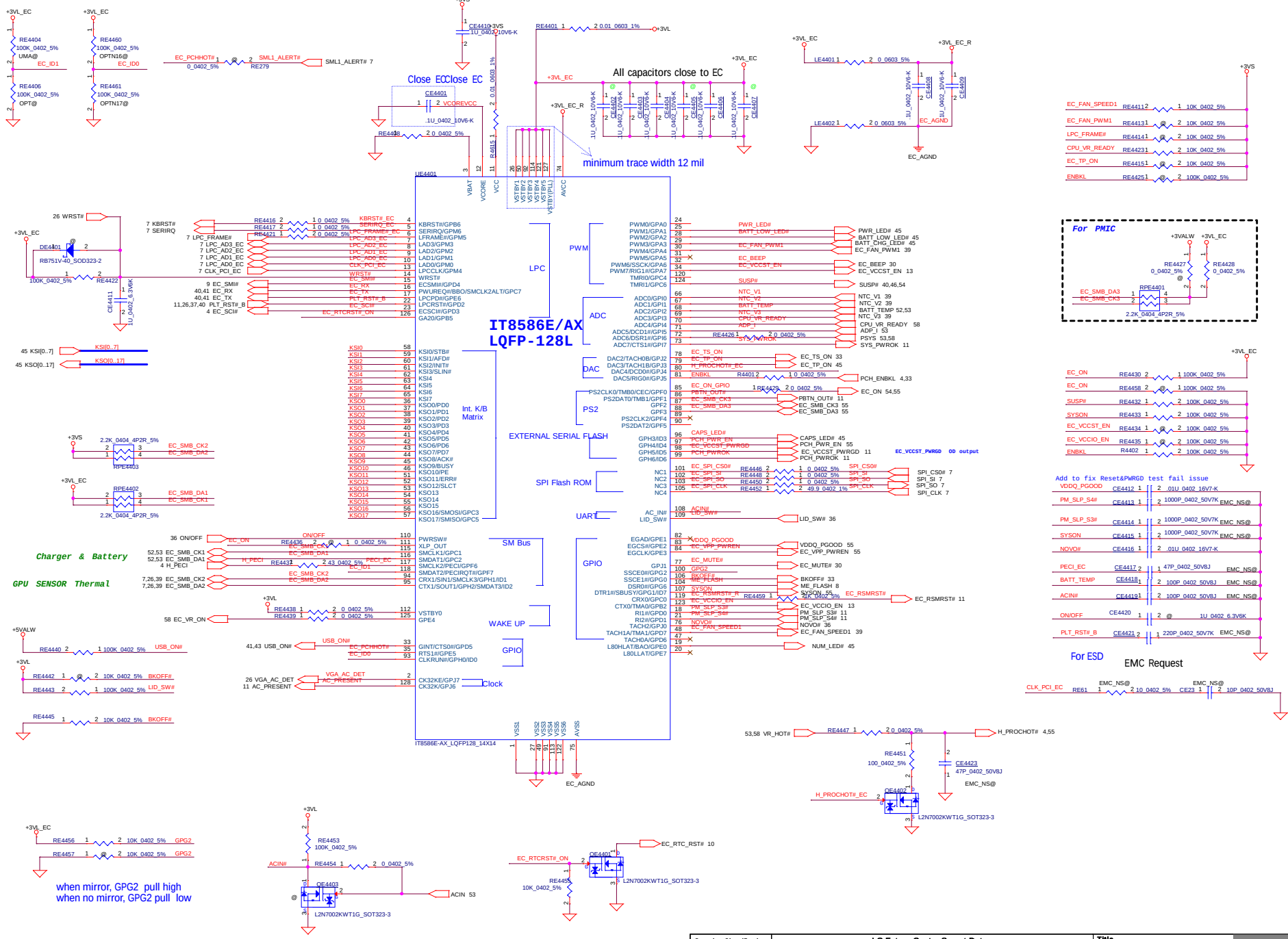
Date:	Friday, October 26, 2018	Sheet 43 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: EC_ITE8586

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C	FS441/FS540	0.1

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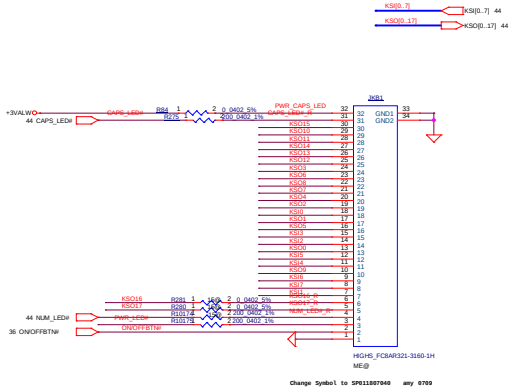
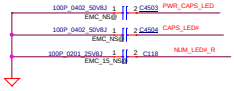
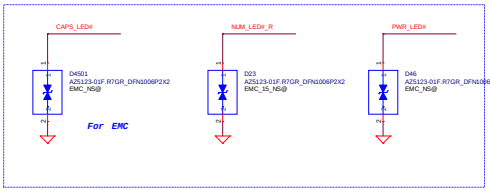
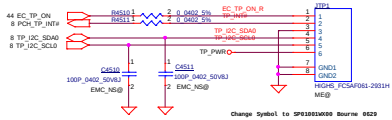
K/B Connector



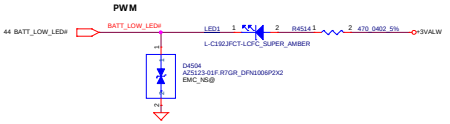




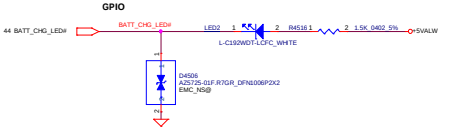
TP/B Connector

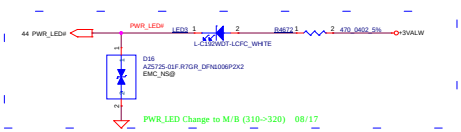


PWM



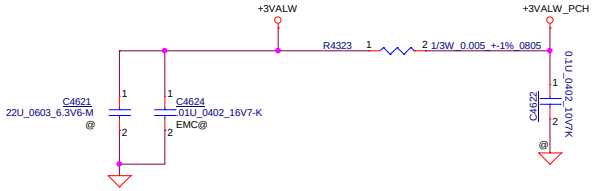
GPIO

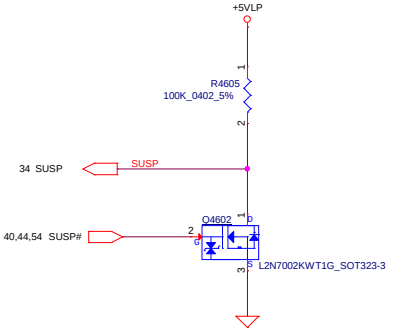


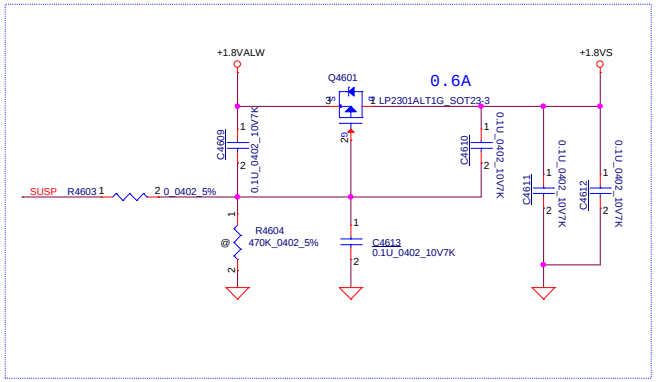


LED	Stute	LED Behavior
Power Button	System on	White_on(battery≥21%-100%)
		Amber_on(battery≥5%-20%)
	Standby LID closed	White_on(battery≥21%-100%)
		Amber_Blink_3S(battery≥5%-20%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on(battery≥1%-90%)
		White_on(battery≥91%-100%)

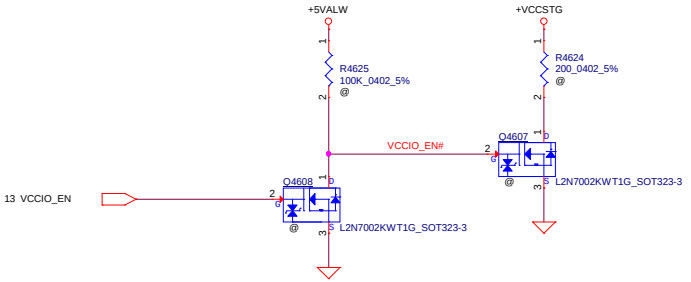
Title: KB/TP_CONN.
Size: Custom | Document Number: FS441/FS540 | Rev: 0.1
Date: Friday, October 26, 2018 | Sheet 45 of 51

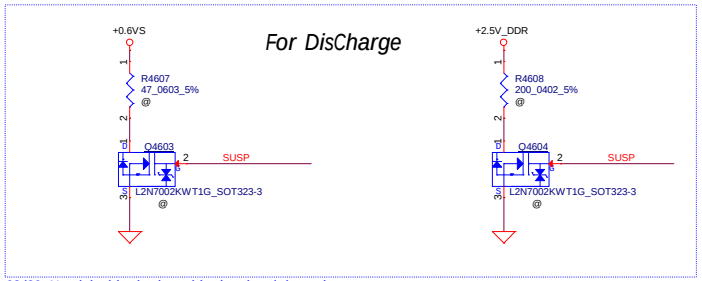






Reserve for VCCSGT discharge





08/29: Need double check enable signal and the resistance

12.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Whiskey Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal $R_{discharge}$ <= 300Ω to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal $R_{discharge}$ <= VccST/VccPLL $R_{discharge}$.
3. The total capacitance on VccSTG <= total capacitance on VccST/VccPLL.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	DC V TO VS INTERFACE		
Size: Custom	Document Number: FS441/FS540		Rev: 0.1
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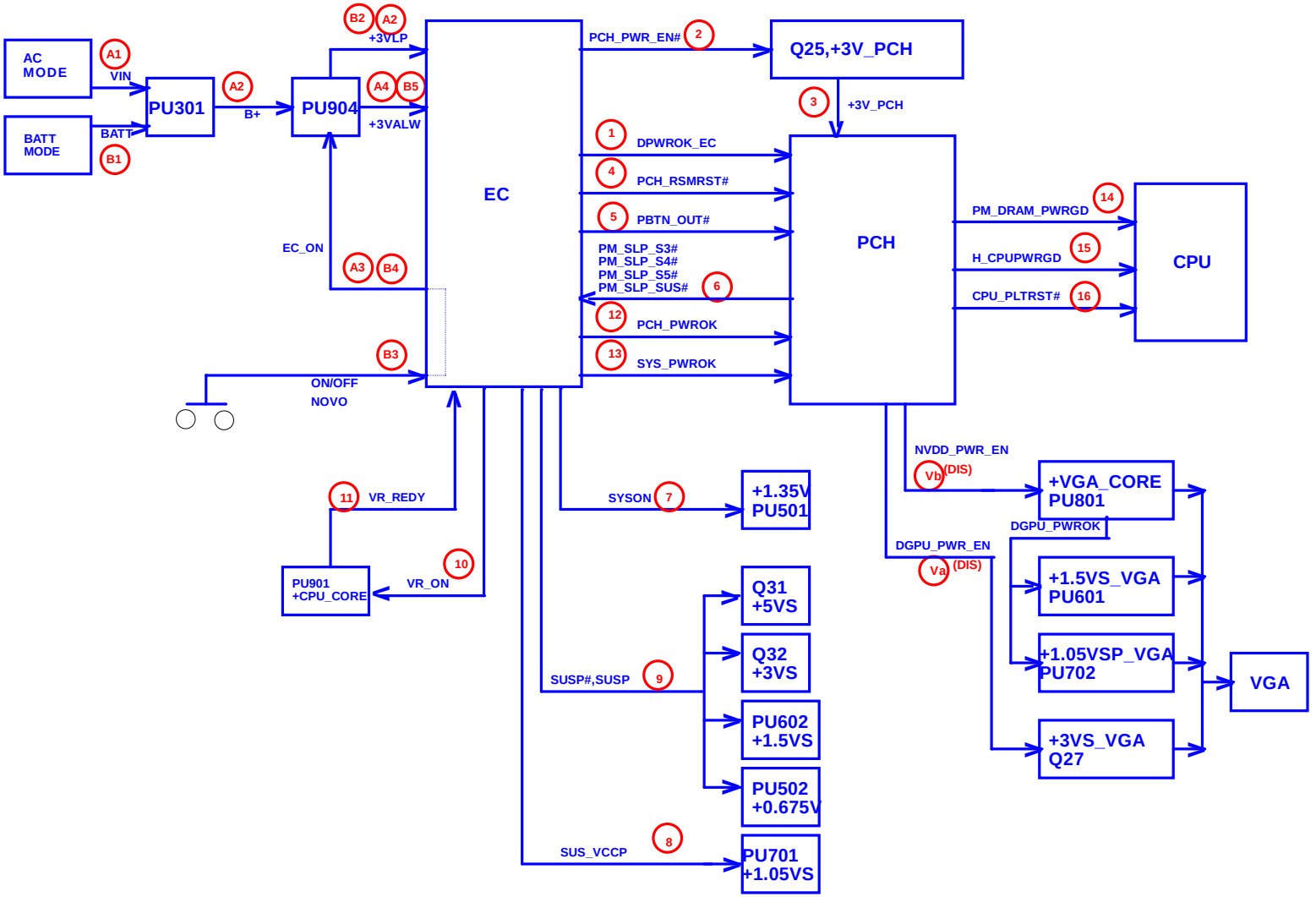

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Power sequence block***

Size	Document Number	Rev
Custom	***FS441/FS540***	0.1

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CPU

UC1 8565U@
Intel i7-8565U 1.8G/4C/8M
SA00009GY00

UC1 8265U@
Intel i5-8265U 1.6G/4C/6M
SA00009GZ00

UC1 8145U@
Intel i3-8145U 2.1G/2C/4M
SA00009H000

UC1 5405U@
Intel Pentium-5405U 2.3G/2C/2M
SA00009T100

UC1 4205U@
Intel Celeron-4205U 1.8G/2C/2M
SA00009T200

GPU

UV1 OPTN16@
N16V-GMR1 GPU
SA00007QX00

RV2316 OPTN17@
5.11_0805_1%
SD00001NQ00

RV2316 OPTN16@
470_0805_5%
SD00247008J

PCB_MB

ZZZ1 FS540@
NM-C121
DA600014P00

ZZZ6 SAM_VR_N16@
V2G SAM N16
X7646612001
VRAM_Samsung

ZZZ5 Hyn_VR_N16@
HYNIX V2G N16S
X7646612002
VRAM_Hynix

ZZZ4 Mic_VR_N16@
V2G MIC N16
X7646512001
VRAM_Micron

ZZZ9 SAM_DRAM@
D4G SAM
X7646512004
DRAM_Samsung

ZZZ8 Hyn_DRAM@
HYNIX D4G
X7646512003
DRAM_Hynix

ZZZ7 Mic_DRAM@
D4G MIC
X7646512002
DRAM_Micron

SO_DIMM only

RC805 NMD@
SO_DIMM
SD02810028J

RC812 NMD@
SO_DIMM
SD02810028J

RC814 NMD@
SO_DIMM
SD02810028J

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Virtual symbol

Size: C	Document Number: FS441/FS540	Rev: 0.1
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Hole

H2
HOLEA
PAD_C10P0D8P0

PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

MD Shielding

SH1 SPRING_FINGER_6.2X1.64
SH2 SPRING_FINGER_6.2X1.64
SH3 SPRING_FINGER_6.2X1.64
SH4 SPRING_FINGER_6.2X1.64
SH5 SPRING_FINGER_6.2X1.64
SH6 SPRING_FINGER_6.2X1.64

H3 HOLEA PAD_CT7P0B6P0D3P2
H4 HOLEA PAD_CT7P0B6P0D3P2
H5 HOLEA PAD_CT7P0B6P0D3P2
H6 HOLEA PAD_CT7P0B6P0D3P2
H7 HOLEA PAD_CT7P0B6P0D3P2
H8 HOLEA PAD_CT7P0B6P0D3P2

H9 HOLEA PAD_C7P0D4P0
H10 HOLEA PAD_C7P0D4P0

H17 HOLEA PAD_O2P5X3P0D2P5X3P0N
H18 HOLEA PAD_O2P5X3P0D2P5X3P0N

H11 HOLEA PAD_C7P0D2P8
H12 HOLEA PAD_C7P0D2P8
H13 HOLEA PAD_C7P0D2P8

H19 HOLEA PAD_C2P5D2P5N

H14 HOLEA PAD_C7P0D2P4

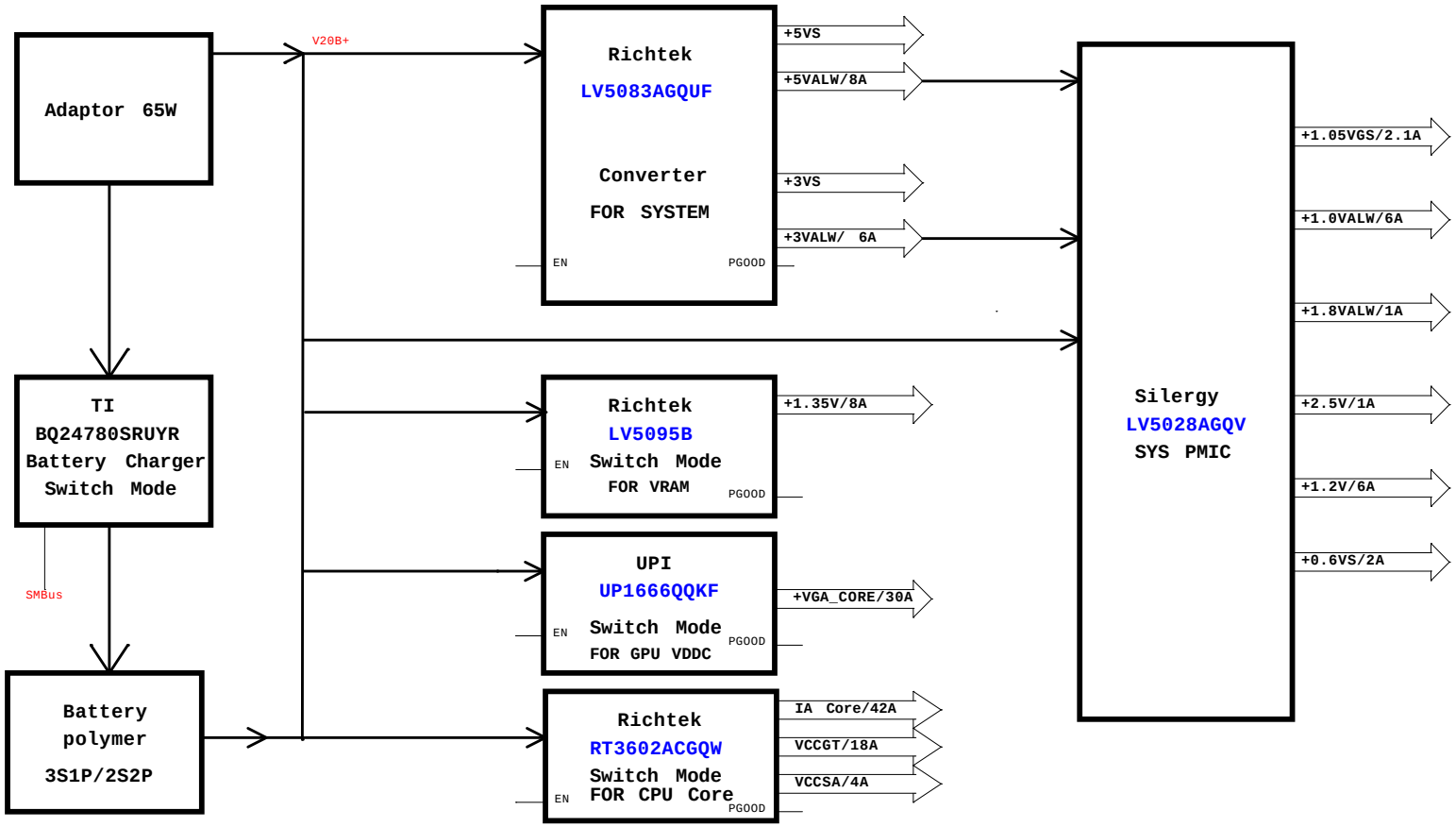
H15 HOLEA PAD_CT7P0B10P0D4P0
H16 HOLEA PAD_CT7P0B10P0D4P0

SODIMM Shielding

SH10 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Hole	
Size B	Document Number FS441/FS540	Rev 0.1
Date: Friday, October 26, 2018	Sheet 49 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-Power Diagram

Size	Document Number	Rev
C	140S-WHL	0.3

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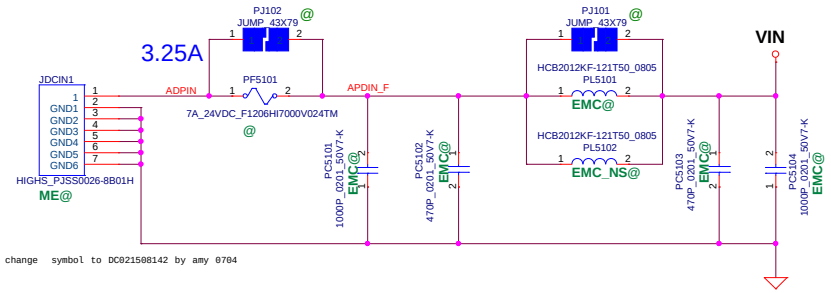
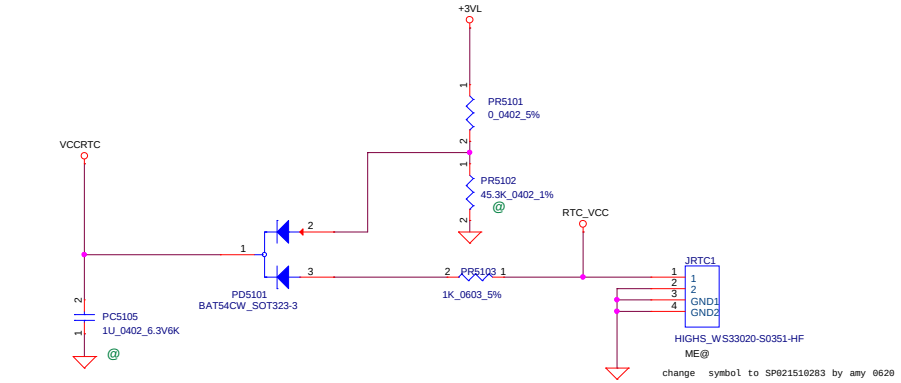




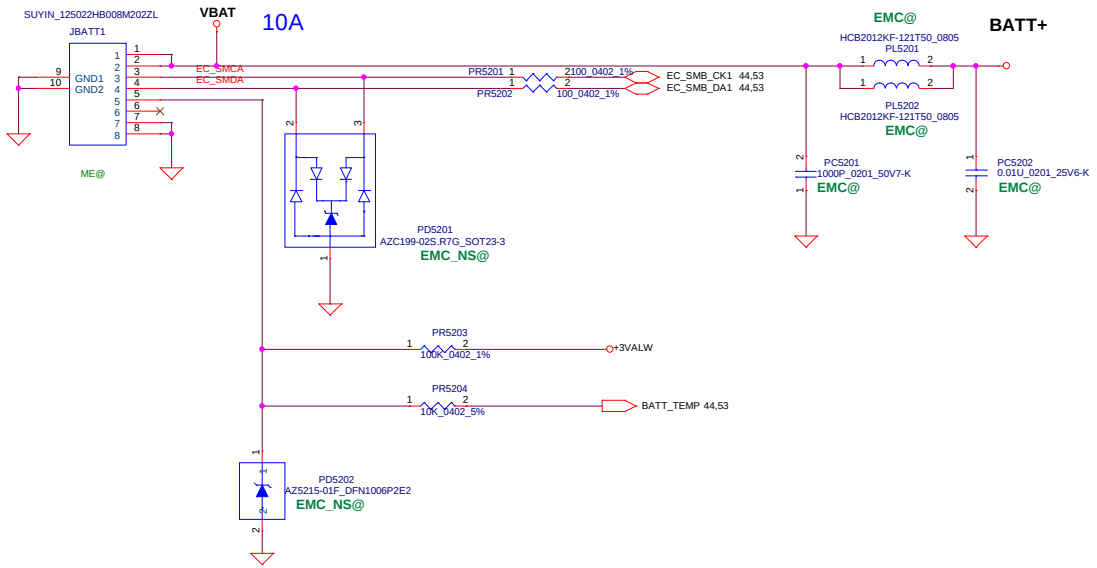
RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size	Document Number	Rev
Custom	140S-WHL	0.3

Date: Friday, October 26, 2018 Sheet 51 of 61



2S1P polymer battery voltage level: +5.5V ~ 8.8 V

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	140S-WHL	0.3

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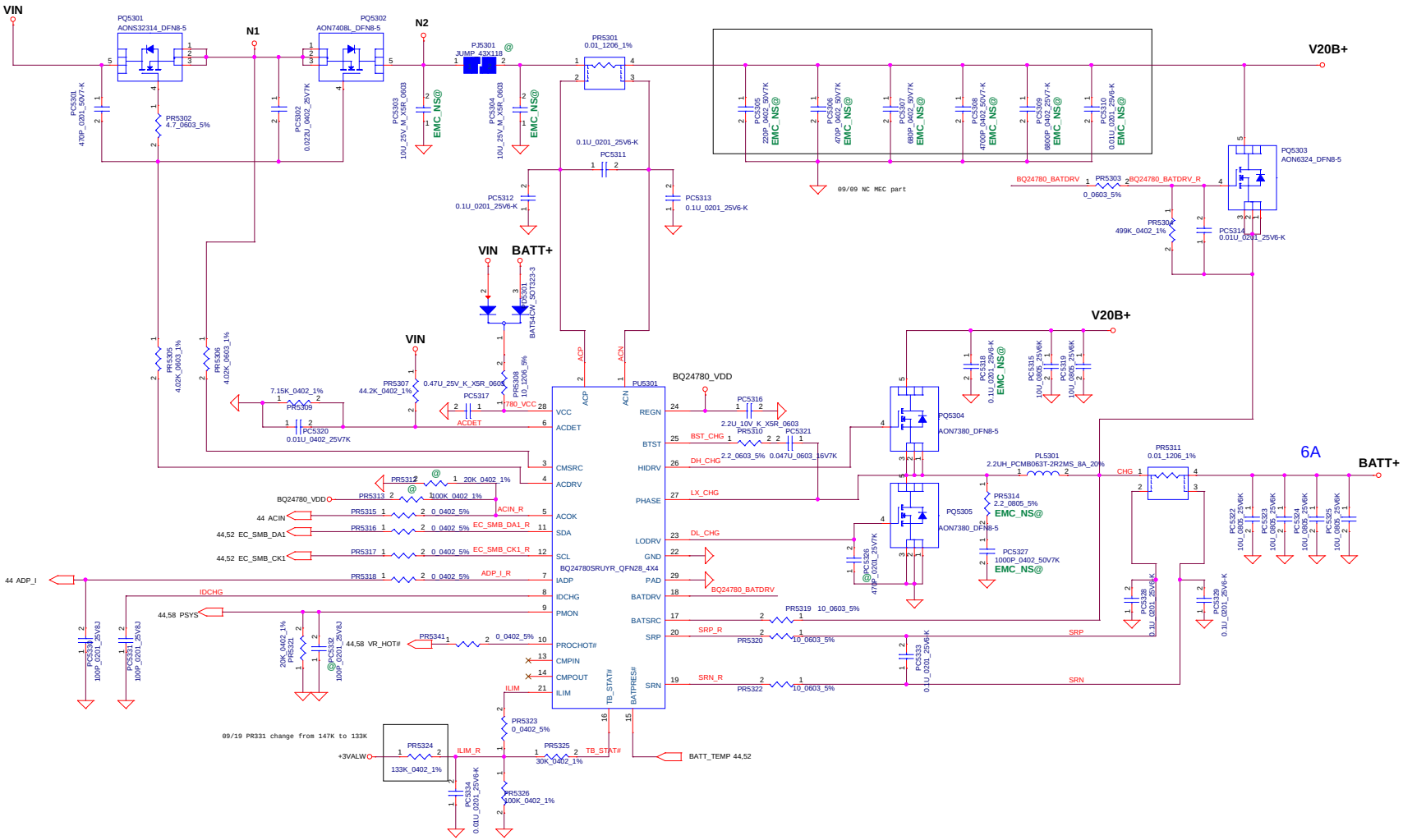

ACDECT setting 17.2V
Charge current limit HW=7A
DC discharge limit =26A
Discharge current limit HW=9A during Turbo boost

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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Title: PWR-CHARGER

Size	Document Number	Rev
C	140S-WHL	0.3
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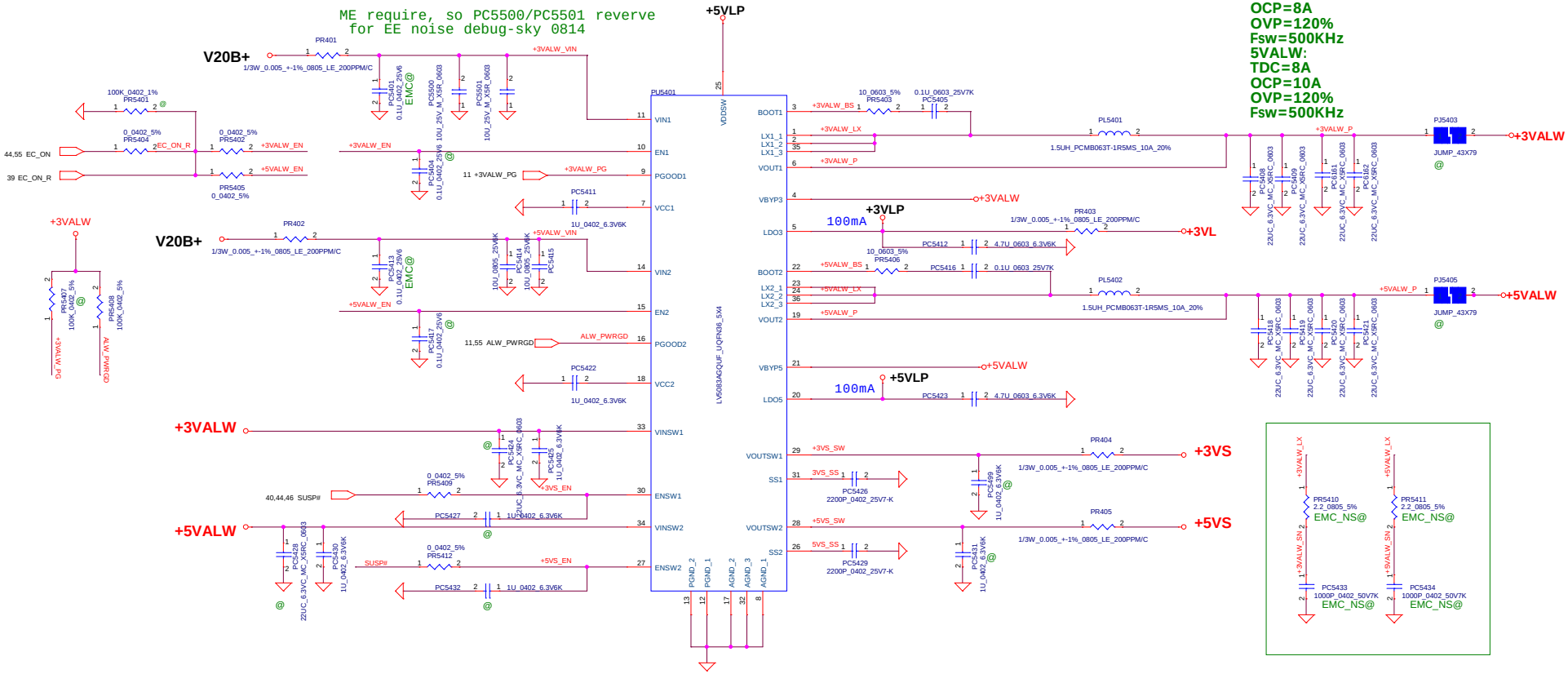
EC_ON pull high reserve at EC,
no need USM enable=1.57V USM

ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814

3VALW:
TDC=6A
OCP=8A
OVP=120%
Fsw=500KHz
5VALW:
TDC=8A
OCP=10A
OVP=120%
Fsw=500KHz



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR_3VALW/5VALW

Size	Document Number	Rev
C	140S-WHL	0.2
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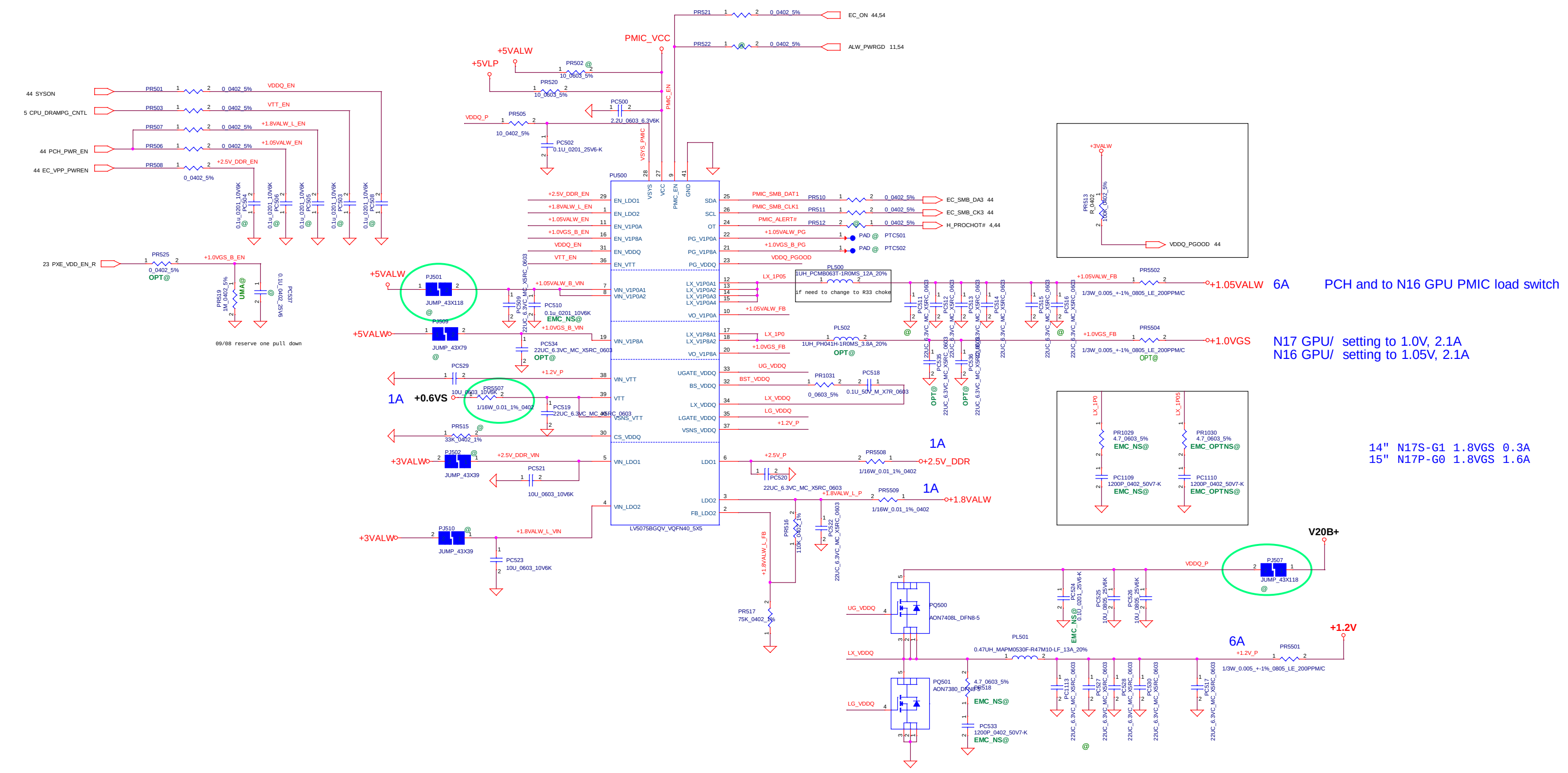

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Issued Date	2018/07/10	Deciphered Date	2018/07/10

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Title: PWR PMIC-DDR4/1.0ALW/1.8ALW

Size: Custom | Document Number: 140S-WHL | Rev: 0.3

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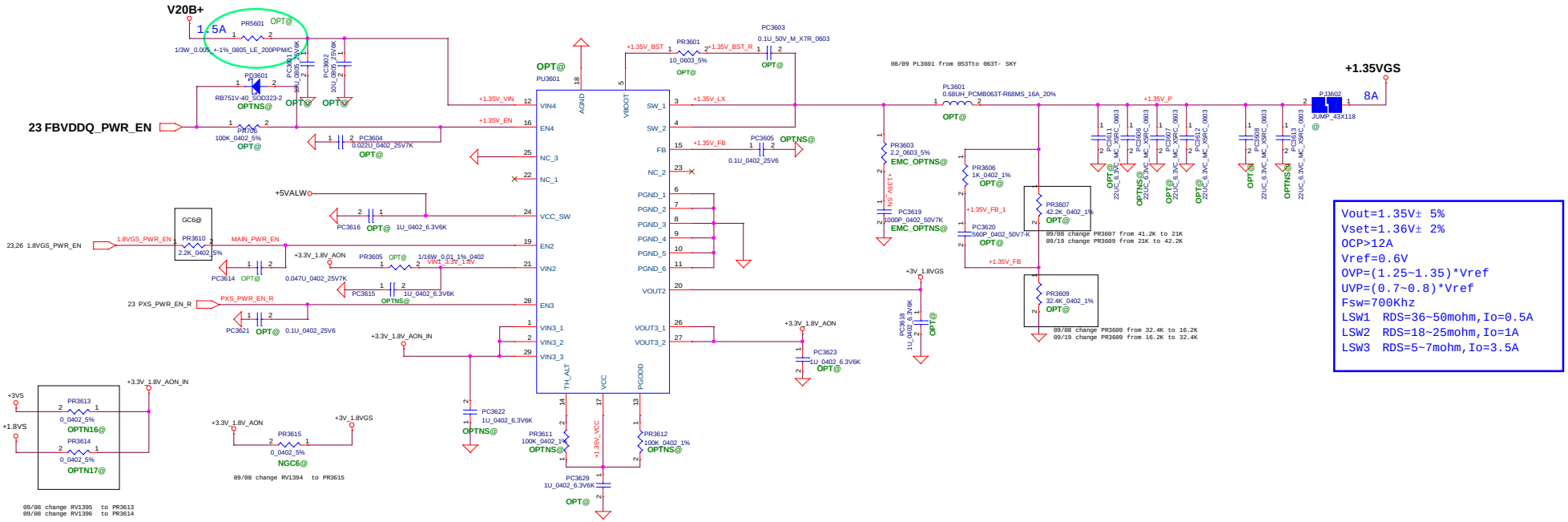

Vout=1.35V± 5%
Vset=1.36V± 2%
OCP>12A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz
LSW1 RDS=36~50mohm,Io=0.5A
LSW2 RDS=18~25mohm,Io=1A
LSW3 RDS=5~7mohm,Io=3.5A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-VGA-PMIC		
Size	Document Number		Rev
Custom	149S-WHL		0.3
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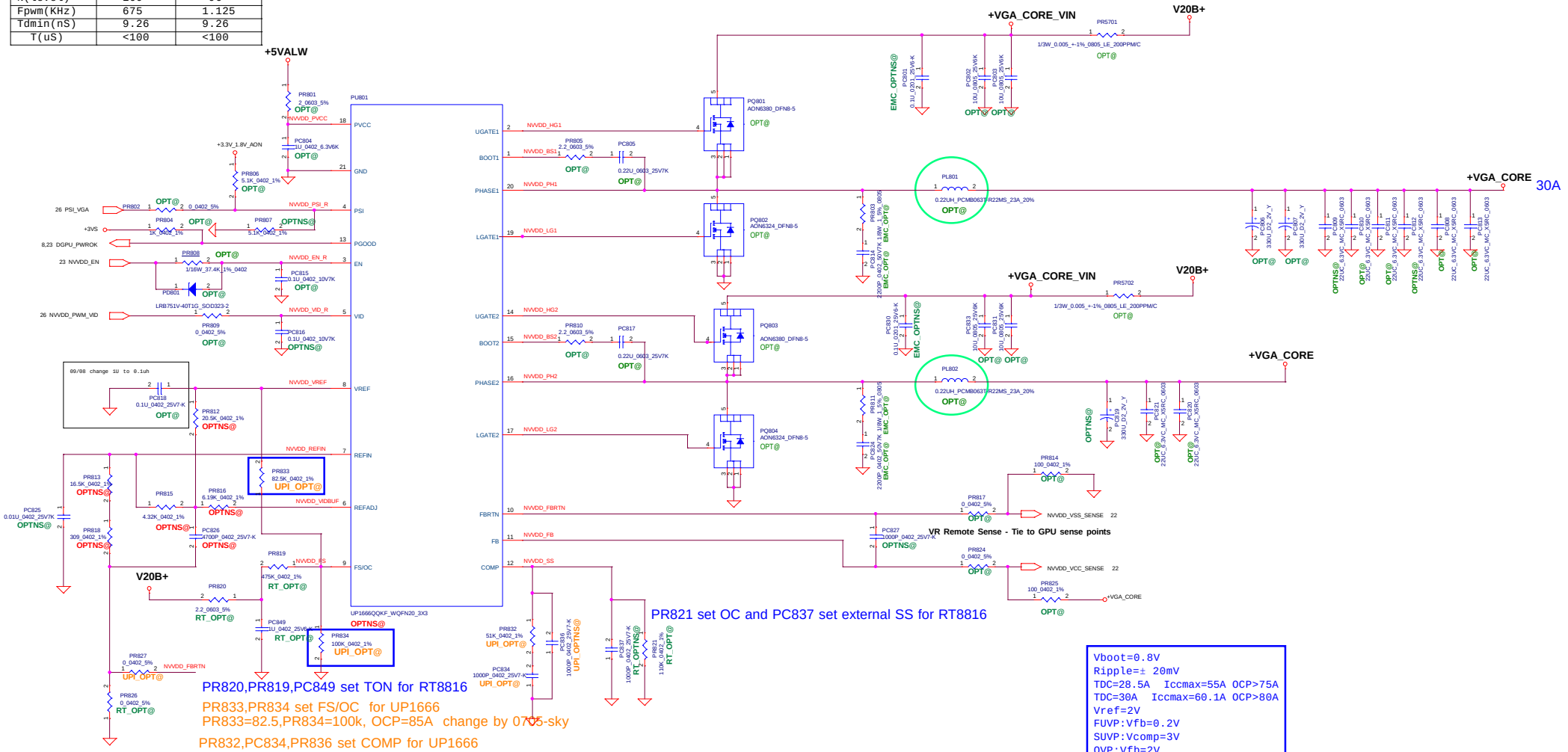
PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-VGA_CORE

Size: Custom | Document Number: 140S-WHL | Rev: 0.3

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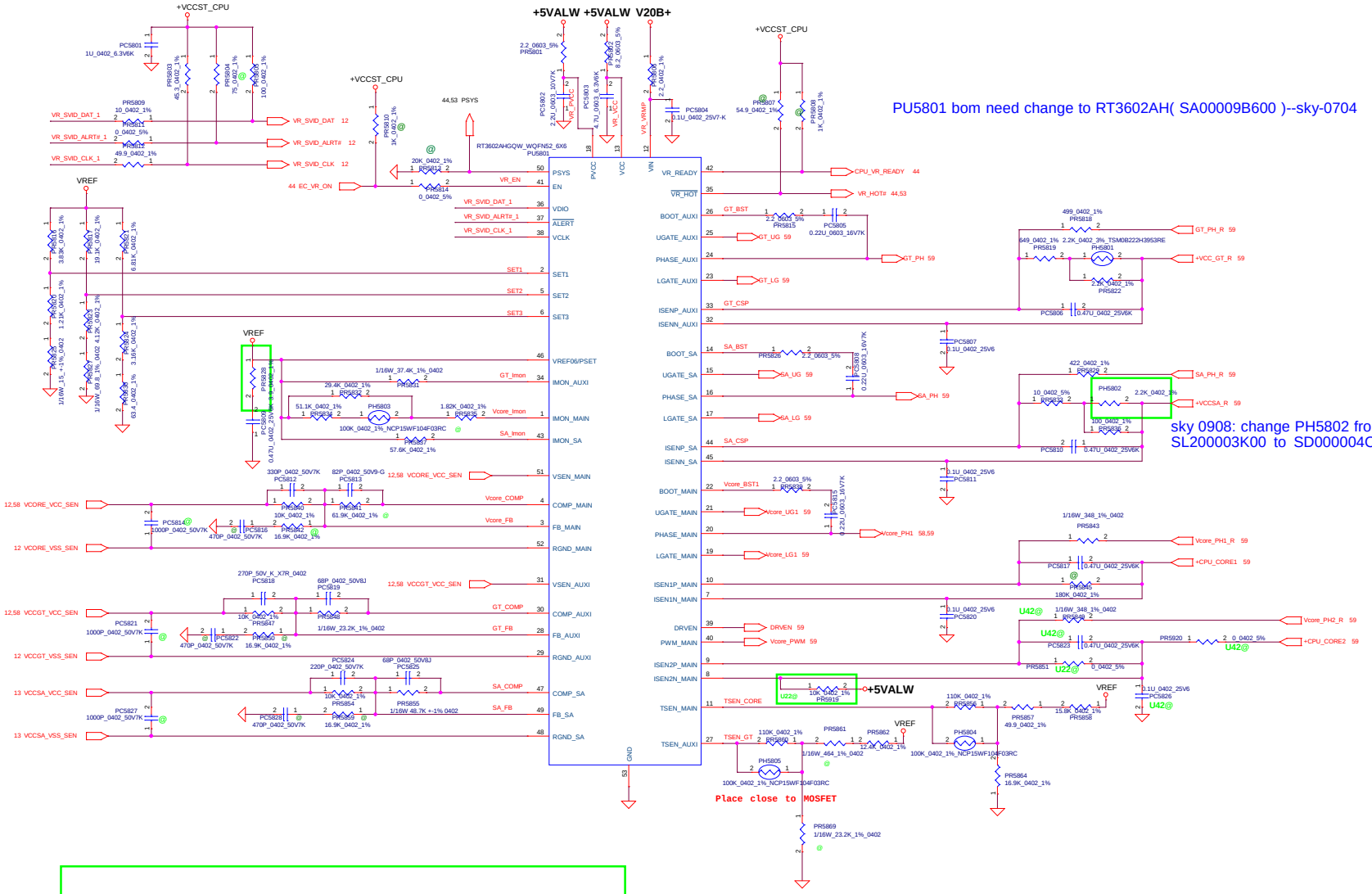

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Decipered Date	2018/07/10

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Title: PWR-CPU-CORE-1

Size: b2 | Document Number: 140S-WHL | Rev: 0.3

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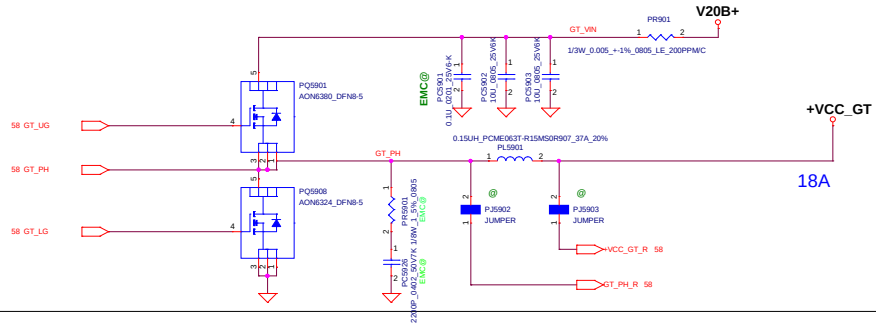
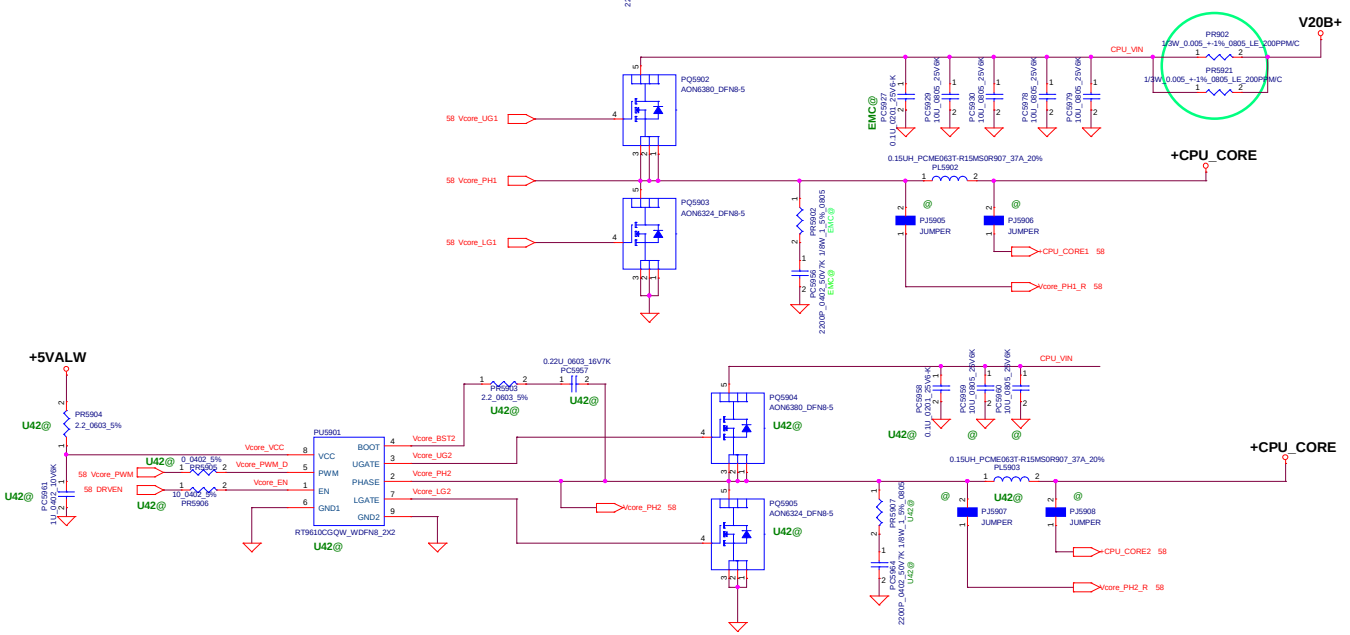


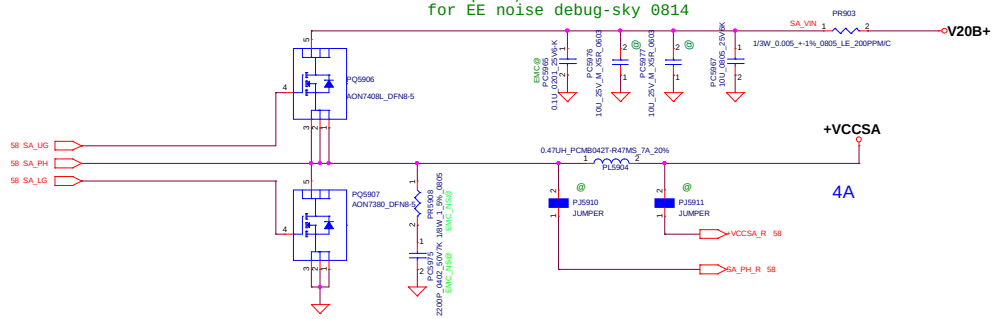

```
Vboot=0V        Loadline=3.1mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=18A  Iccmax=31A  OCP=37A
OVP=VID+370mV~VID+430mV
Max  Overshoot:70mv/10us
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```




```
U22 :21A
U42: 48A

Vboot=0V        Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=21A/48A  Iccmax=32A/70A
OCP=37A / 74A
Max  Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```

ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814




```
Vboot=0V        Loadline=10.3Ω
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=± 10mV(0.5A~TDC)
Ripple=± 15mV(TDC~Iccmax)
TDC=4A  Iccmax=4.5A  OCP=7A
Max  Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz
```

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU-CORE-2

Size	Document Number	Rev
A2	140S-WHL	0.3

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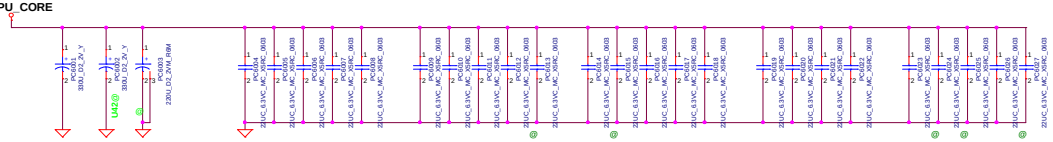
+CPU_CORE



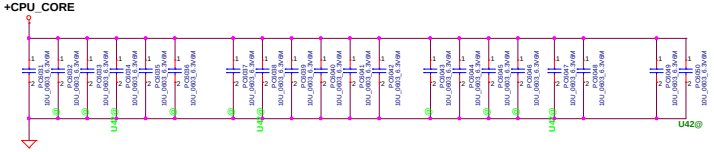
CPU_CORE: 2PCS_330U_D2_2V+1PCS_220U_D2_2V
+13PCS_22U_0603_6V+18PCS_10U_0402_6V
+16PCS_1U_0201_6V=

Vender modify_20180705
PC6003 @ and stuff 6 pcs 22U/0603

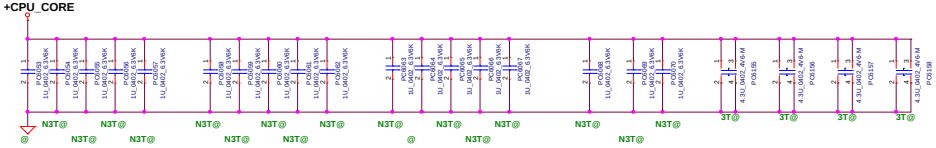
sky modify_20180709
change 10U/0402 to 10U/0603, 1U/0201 to 1U/0402

sky modify_20180925
layout change PC6024/PC6025 to PC6036/PC6046

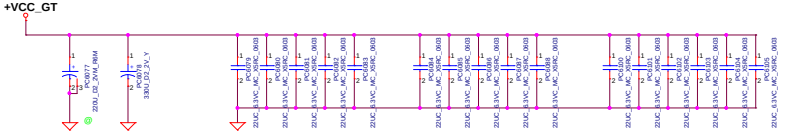
+CPU_CORE



+CPU_CORE

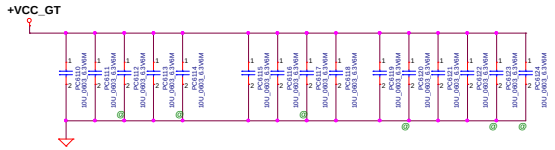


+VCC_GT

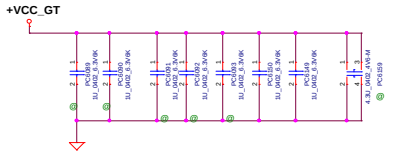


VCCGT: 1PCS_330U_D2_2V+1PCS_220U_D2_2V
+10PCS_22U_0603_6V+9PCS_9U_0603_6V
+2PCS_1U_0402_6V= sky_07_09

+VCC_GT

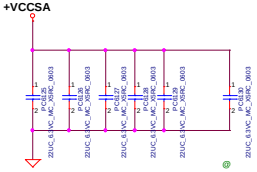


+VCC_GT

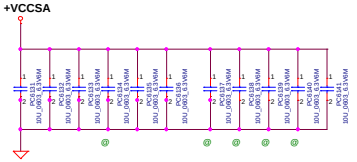


VCCSA:5PCS_22U_0603_6V+6PCS_10U_0603_6V
+2PCS_1U_0402_6V=07-09 sky

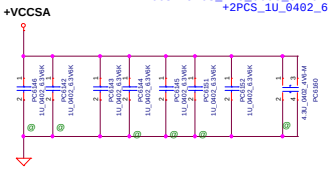
+VCCSA



+VCCSA



+VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU Decoupling Cap

Size: Custom | Document Number: 14GS-WHL | Rev: 0.3

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PU801 RT_OPT@

RT8816AGQW_WQFN20_3X3
SA000081U00

PU801 UPI_OPT@

UP1666QQKF WQFN 20P CONTROLLER
SA00008G000

GPU solution

OPTN17@ PR816	OPTN17@ PR812	OPTN17@ PR815	OPTN17@ PR813	OPTN17@ PR818	OPTN17@ PC826
6.19K_0402_1% SD000015G00	20.5K_0402_1% SD03420528J	4.32K_0402_1% SD00000J28J	16.5K_0402_1% SD03416528J	309_0402_1% SD00001XX00	4700P_0402_25V SE075472K8J

N17 solution

OPTN16@ PR816	OPTN16@ PR812	OPTN16@ PR815	OPTN16@ PR813	OPTN16@ PR818	OPTN16@ PC826
20K_0402_1% SD03420028J	20K_0402_1% SD03420028J	2K_0402_5% SD03420018J	18K_0402_1% SD00000058J	0_0402_5% SD02800008j	2700P_0402_50V SE00000ZJ00

N16 solution

U42@ PR5835	U42@ PR5841	U42@ PR5861	U42@ PR5869
1.8K +-1% 0402 SD00000R58J	61.9K +-1% 0402 SD03461928J	464 +-1% 0402 SD00001CP00	23.2K +-1% 0402 SD00001NZ00

U42 solution

U22@ PR5835	U22@ PR5841	U22@ PR5861	U22@ PR5869
2.32K +-1% 0402 SD000016300	47.5K +-1% 0402 SD03447528J	1.8K +-1% 0402 SD00000R58J	19.6K +-1% 0402 SD00000358J

U22 solution

Component	Value	N17	N16S-GTR
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

Title: ***NGFF_SSD_1***

Size	Document Number	Rev
C	***EYG10***	0.2

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