

# LCFC Confidential


## S145-IGM M/B FS440/FS541 Schematics Document

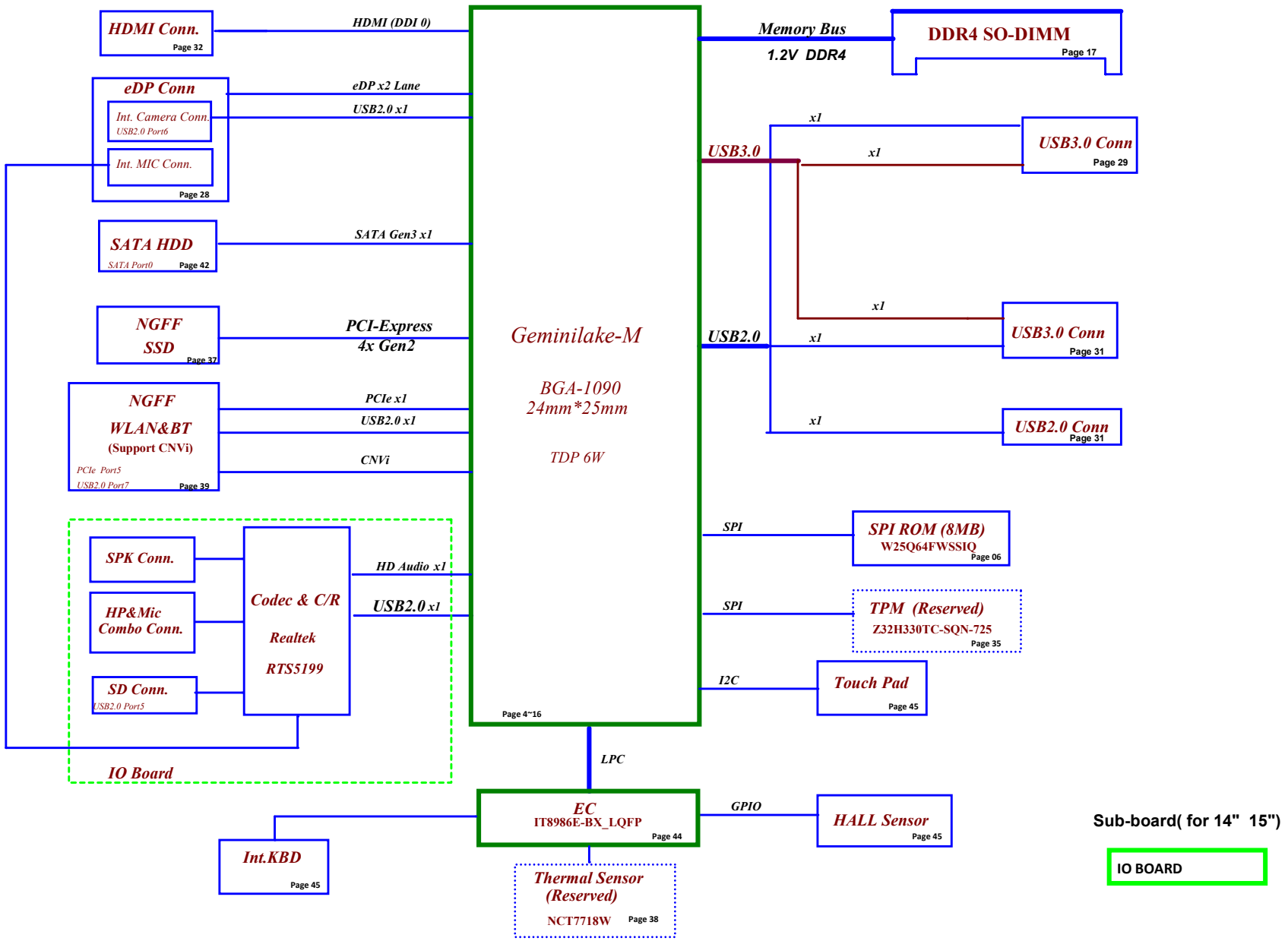
Intel Geminilake M-Processor with DDR4 + UMA

2018-07-09

REV: 0.2

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2018/07/09	Deciphered Date	2019/07/08	Cover Page		
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Date: Monday, November 05, 2018				Sheet	1	of 60





Sub-board( for 14" 15")

IO BOARD

Security Classification		LC Future Center Secret Data		Title	
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Size	C	Document Number	FS440/FS541		Rev
Date:	Monday, November 05, 2018	Sheet	2	of	60

Voltage Rails (0 --> Means ON, X --> Means OFF)

Power Plane	V20B+	+3VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.2V	+5VS +3VS +1.8VS +1.05VS +0.6VS +CPU_CORE +VNN
State	+3VL +5VL	+5VALW			
S0	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0IX(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB3.0
	1	USB3.0
USB 2.0	0	
	1	USB3.0 (2.0)
	2	BT
	3	USB3.0 (2.0)
	4	USB2.0
	5	CARD READER
	6	CAMERA
	7	Touch Screen(RSVD)

DDI PORT LIST

Port	Device
DDI0	HDMI
DDI1	NC
eDP	eDP

PCIE PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0			
1	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
2			
3			
4	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
14@	For 14" part
15@	For 15" part
RF@	For RF part
CD@	Cost Down part
DIS@	DIS SKU ID part
UMA@	UMA SKU ID part
IGM@	IGM CPU SKU part
IGMR@	IGMR CPU SKU part
LBG@	LBG project SKU part
NEC@	NEC project SKU part
CNVI@	CNVI SKU part
TMSEN@	Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
Debug@	USB debug feature part
USB@	Non USB debug feature part
TS@	Touch Screen part
TS_LBG@	LBG project Touch Screen part
TS_NEC@	NEC project Touch Screen part
UART@	UART debug part
RTCRST@	Clear RTCRST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N4100@	GLK N4100 CPU part
N4000@	GLK N4000 CPU part
N5000@	GLK N5000 CPU part
N4100_QS@	GLK N4100 QS CPU part
HDA18@	HDA Bus 1.8V power part
HDA33@	HDA Bus 3.3V power part
NM_C111@	MB PCB part
NS_C121@	ODD PCB part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	X	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

EC SM Bus0 address		EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery	0x16	Thermal Sensor	0x38(reserve)	DDR SO-DIMM	0xA0
		Charger	0x12			Wlan	Rsvd




I2C4/I2C7 Bus address (Touch Pad)

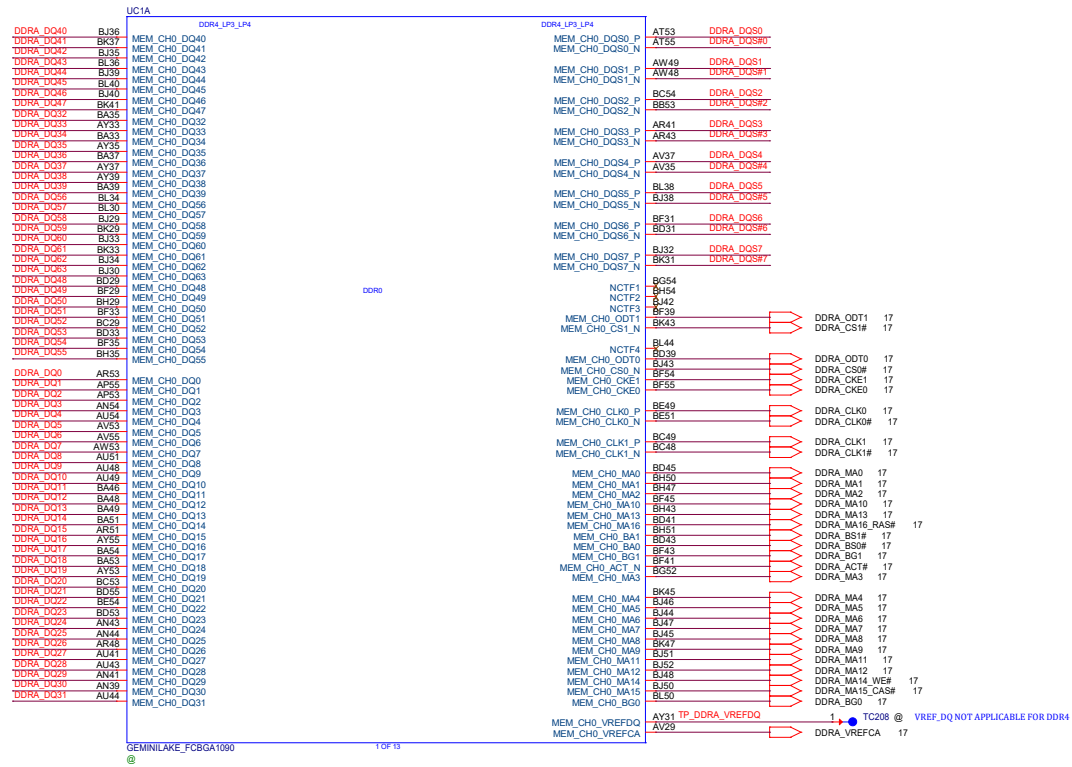
Device	Address
Slave	0x15
Descriptor	0x0001

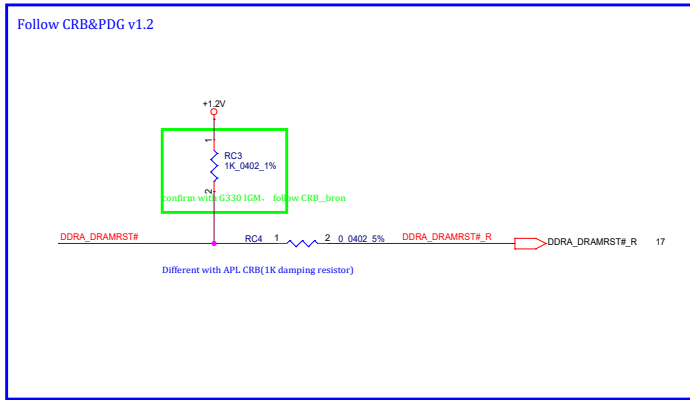
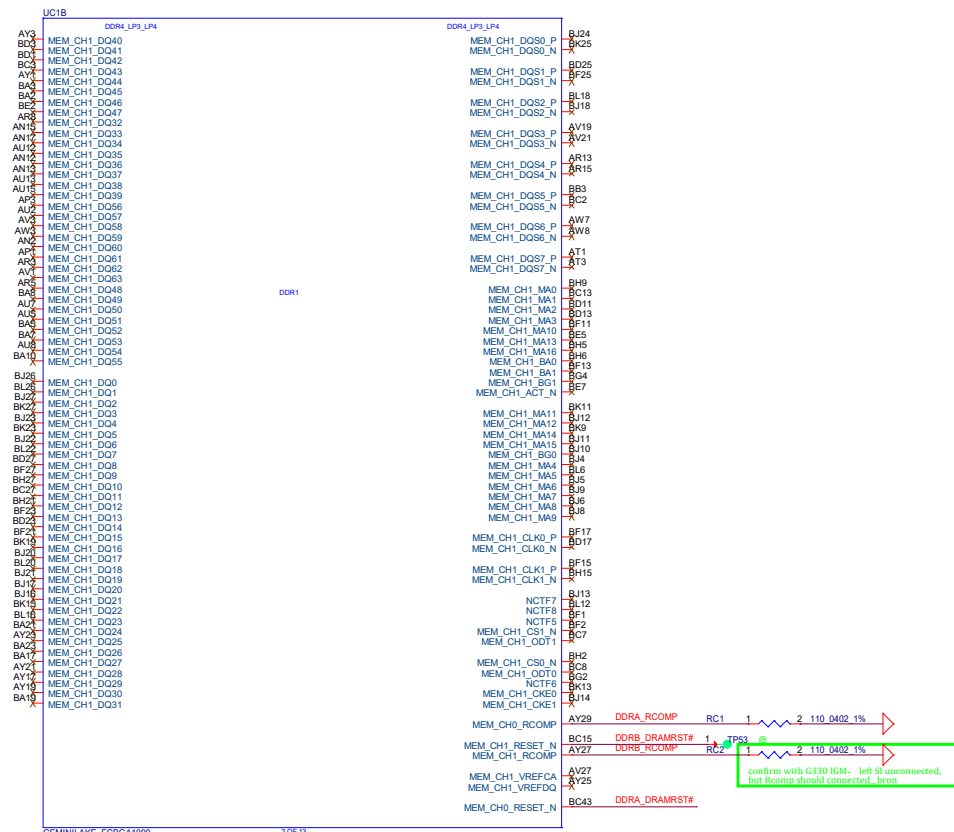
RCOMP RESISTOR REQUIREMENT

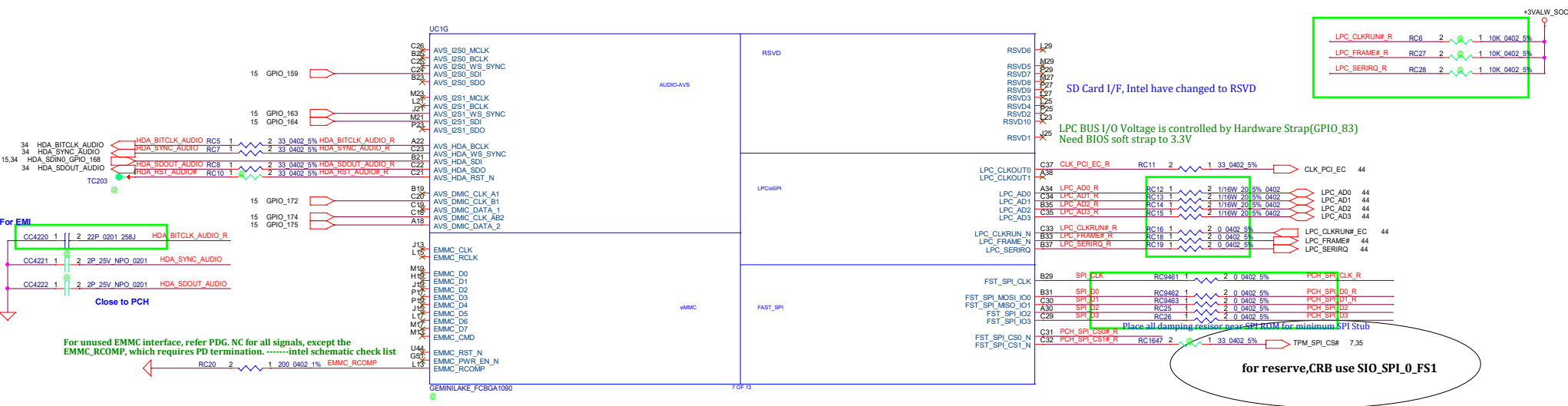
INTERFACE	PIN NAME	LOCATION	VALUE(ohm)	
Memory	MEM_CH0_RCOMP	RC1	110 +/-1%	
	MEM_CH1_RCOMP	RC2	110 +/-1%	
USB2	USB2_RCOMP	RC64	113 +/-1%	
USB3/PCIe/SATA	PCIE2_USB3_SATA3_RCOMP_P/N	RC63	100 +/-1%	
PCIe Refclk	PCIE_REF_CLK_RCOMP	RC62	56 +/-1%	
DP/eDP*/HDMI*	EDP_RCOMP_P/N	RC79	100 +/-1%	
MDSI	MDSI_RCOMP	RC78	150 +/-1%	
CNVI	CNV_WT_RCOMP	RC48	150 +/-1%	
SMBUS/GPIO/EMMC for all 1.8V only and 1.8V mode operation of 1.8/3.3V CFIO interfaces		EMMC_RCOMP	RC20	200 +/-1%

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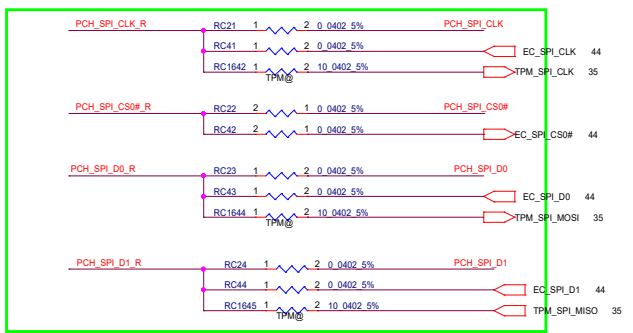
 DDRA\_DQ[63:0] 17  
 DDRA\_DQS[7:0] 17  
 DDRA\_DQS#[7:0] 17



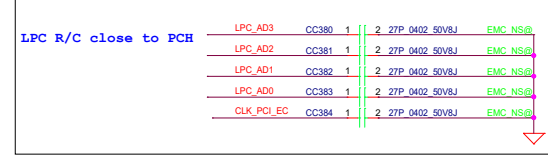
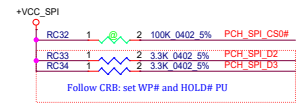




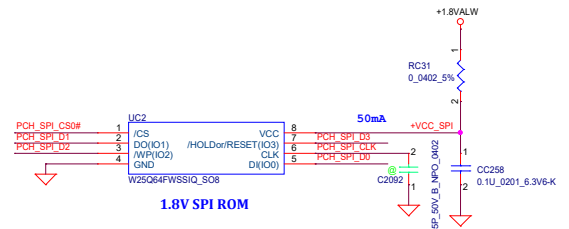
**SPI ROM**

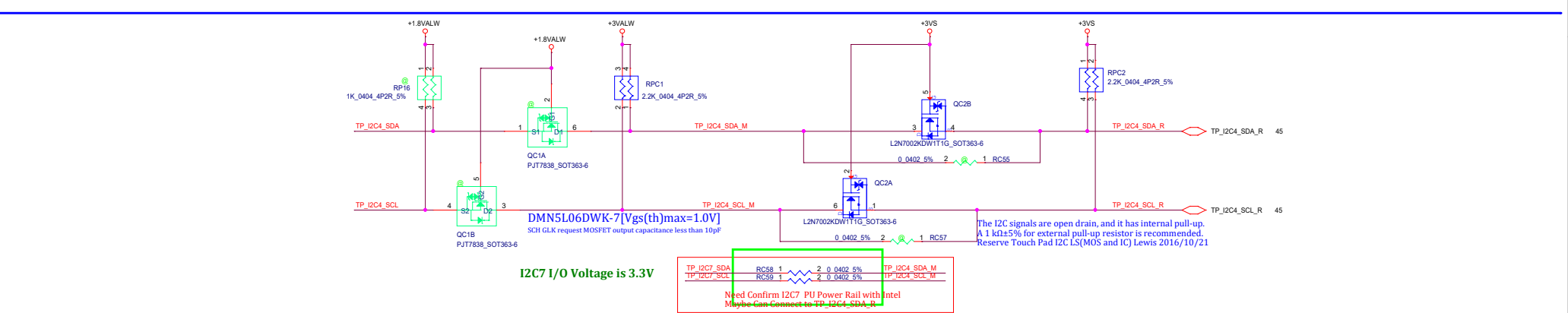
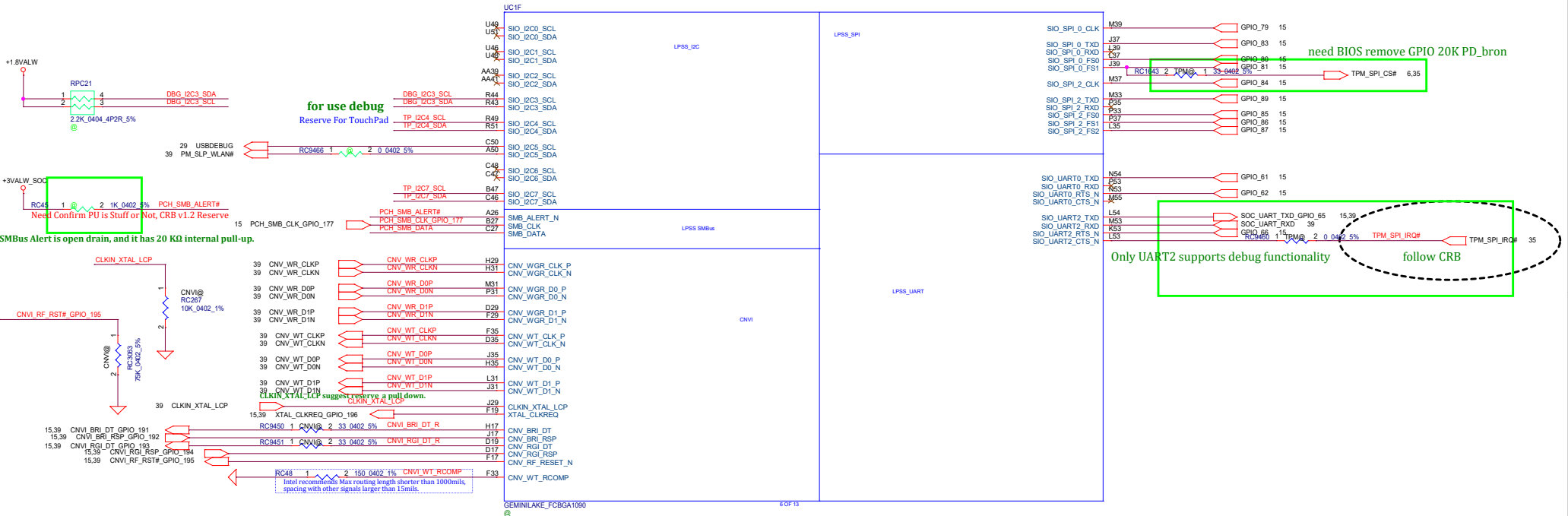


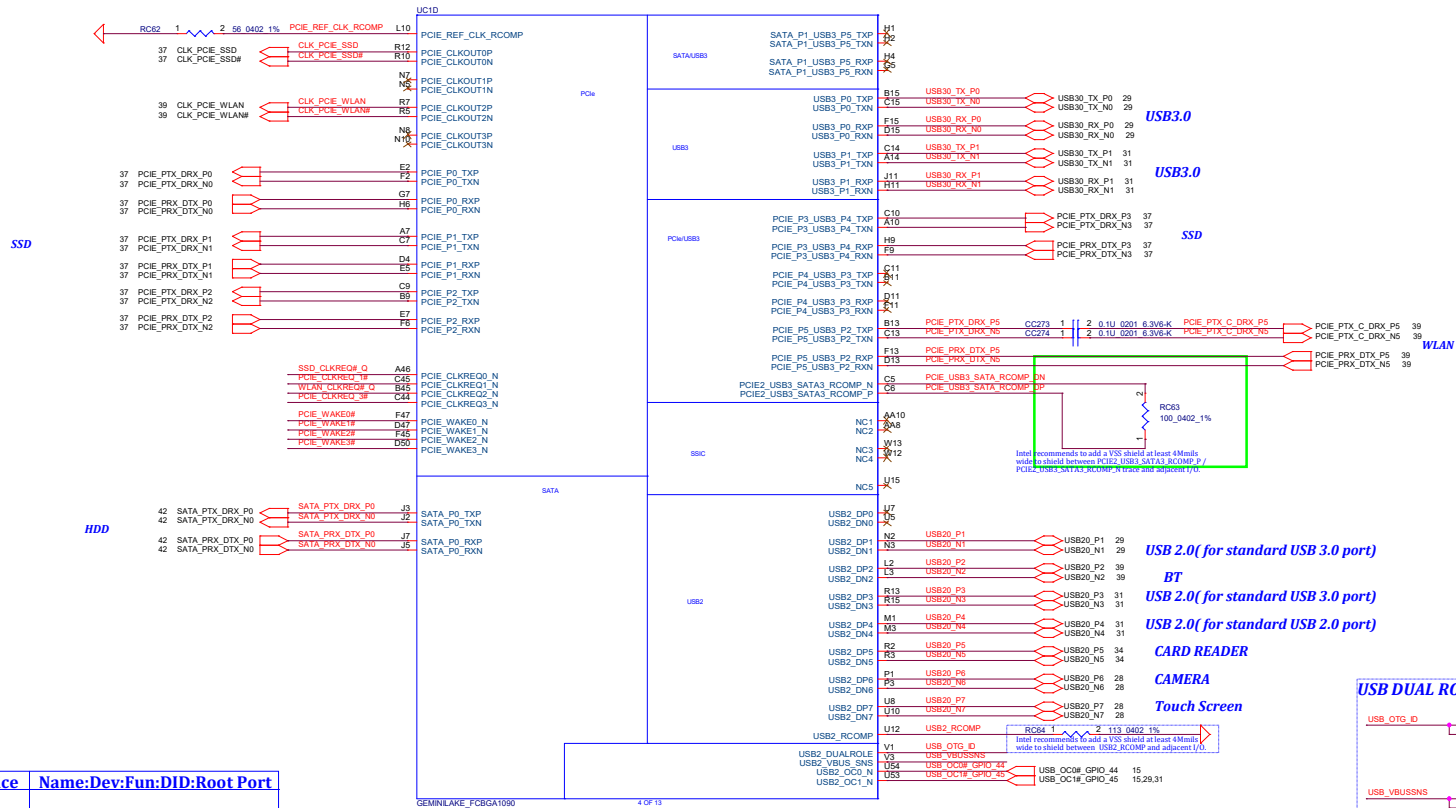
Near place RC21&RC41; RC22&42; RC23&RC43; RC24&RC44



Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
FST_SPI_CS0_N	PCH_SPI_CS0#	1.8V	Native	HSMV
FST_SPI_MOSI_I00	PCH_SPI_D0	1.8V	Native	HSMV
FST_SPI_MISO_I01	PCH_SPI_D1	1.8V	Native	HSMV
FST_SPI_IO2	PCH_SPI_D2	1.8V	Native	HSMV
FST_SPI_IO3	PCH_SPI_D3	1.8V	Native	HSMV
FST_SPI_CLK	PCH_SPI_CLK	1.8V	Native	HSMV



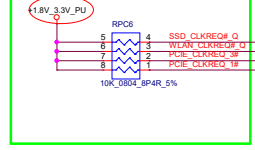




**PCIE Configuration**

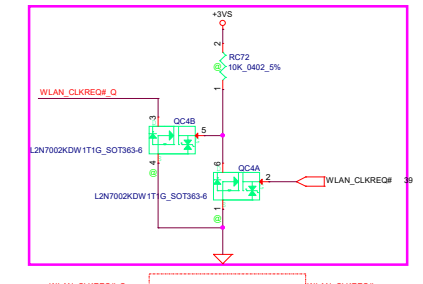
Port	Config	Device	Name:Dev:Fun:ID:Root Port
P0			
P1	X4	SSD	PCIe1(Func0):19:0:0x31D8:2
P2			
P3			
P4	X1		PCIe0(Func0):20:0:0x31D6:0
P5	X1	WLAN	PCIe0(Func1):20:1:0x31D7:1

**CLOCK REQUEST**

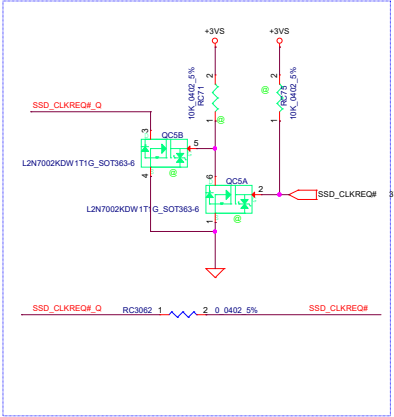


Need Check CLKREQ# can be set 1.8V/3.3V by soft strap  
 CLKREQ0/2/4 default 3.3V  
 CLKREQ1 default 1.8V

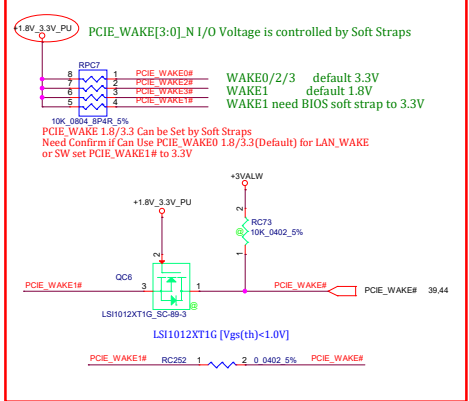
PCIE\_CLKREQ[3:0]\_N I/O Voltage is controlled by Soft Straps



CLKREQ# can be set 1.8V/3.3V by soft strap



**LAN WAKE**

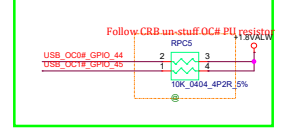


PCIE\_WAKE[3:0]\_N I/O Voltage is controlled by Soft Straps

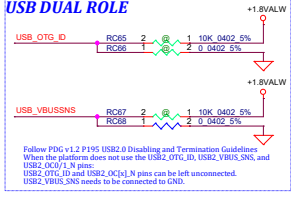
WAKE0/2/3 default 3.3V  
 WAKE1 default 1.8V  
 WAKE1 need BIOS soft strap to 3.3V

10K\_0402\_5%  
 PCIE\_WAKE 1.8V/3.3 Can be Set by Soft Straps  
 Need Confirm if Can Use PCIE\_WAKE0 1.8/3.3(Default) for LAN\_WAKE or SW set PCIE\_WAKE1# to 3.3V

**USB OC**

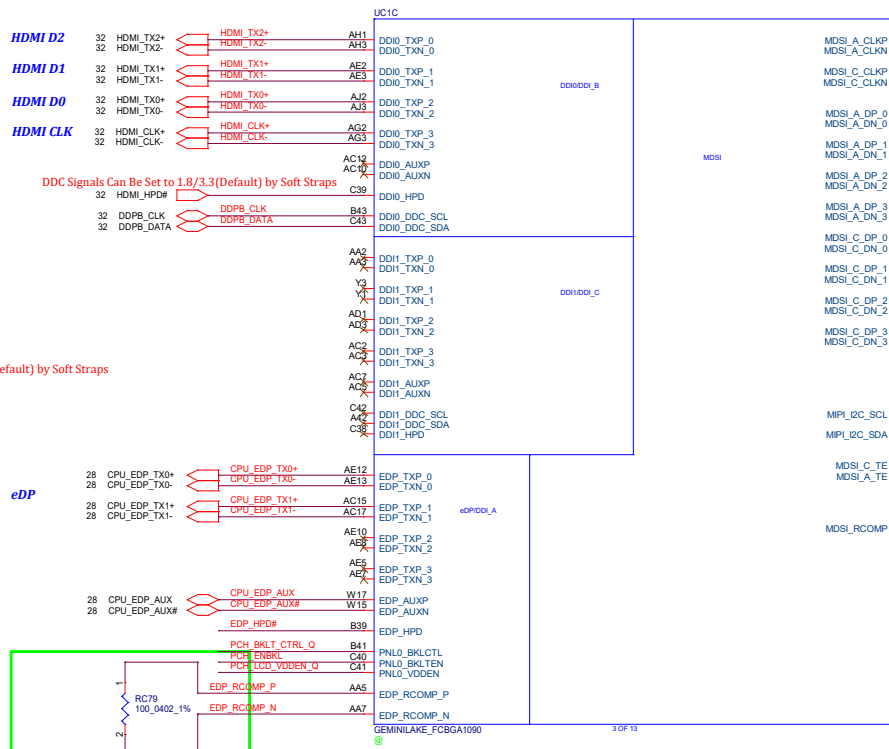


Follow CRB un-stuff OC# PU resistors



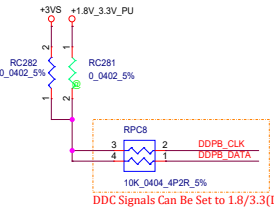
Follow PDG v1.2 P195 USB2.0 Disabling and Termination Guidelines  
 When the platform does not use the USB2\_OTG\_ID, USB2\_VBUS\_SNS, and USB2\_OC#/N pins:  
 USB2\_OTG\_ID and USB2\_OC#(N) pins can be left unconnected.  
 USB2\_VBUS\_SNS needs to be connected to GND.



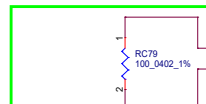


**DDI PORT LIST**

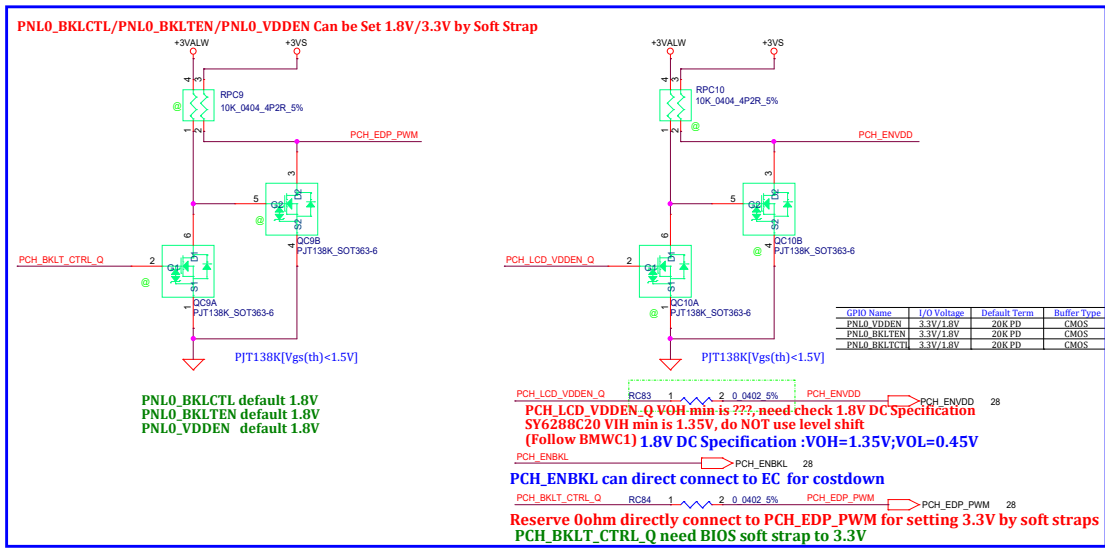
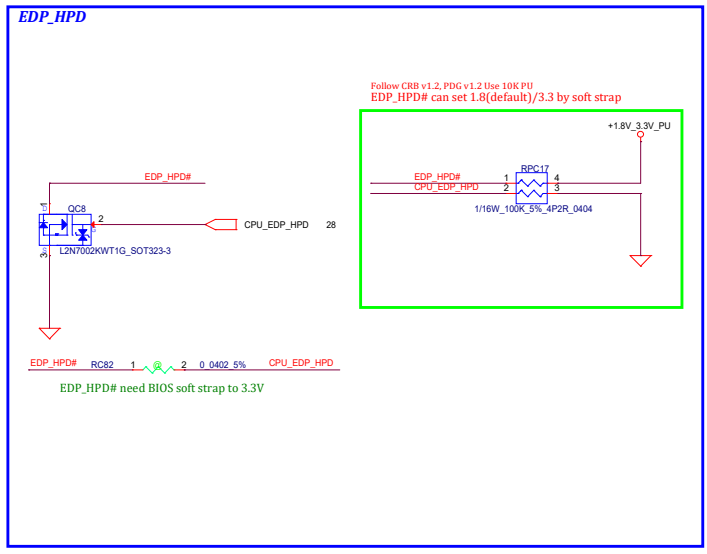
Port	Device	HPD Net	HPD Pin
DD10	HDMI	HDMI_HPD#	C39
DD11	N/A	N/A	C38
EDP	eDP	EDP_HPD#	B39

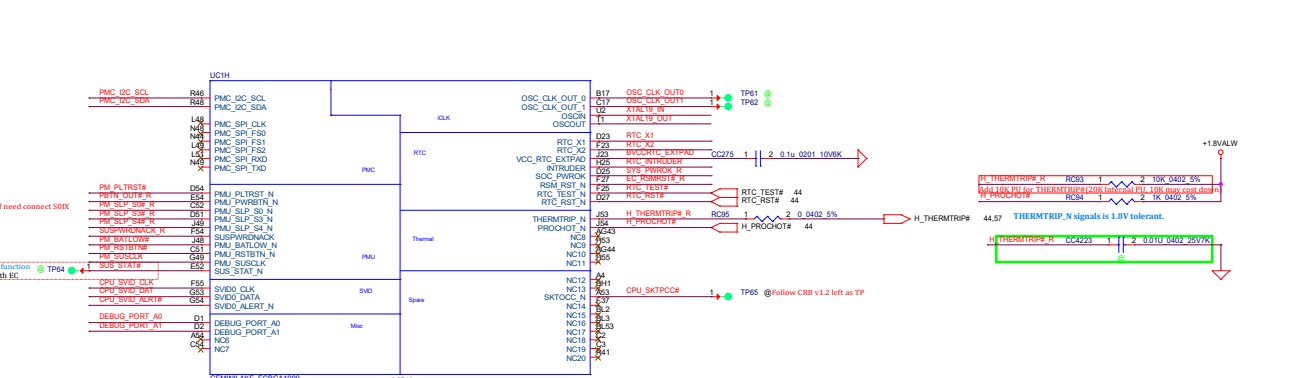
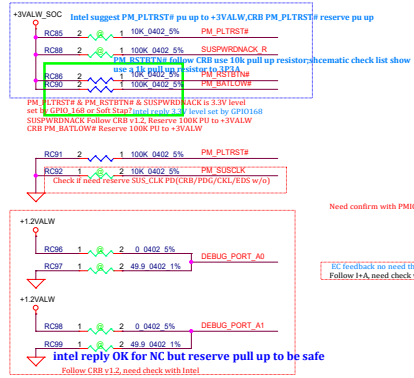


DDC Signals Can Be Set to 1.8/3.3(Default) by Soft Straps

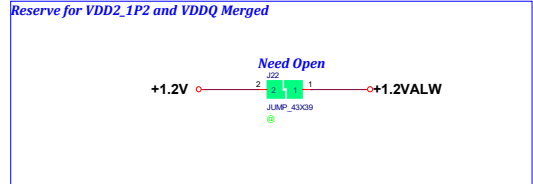
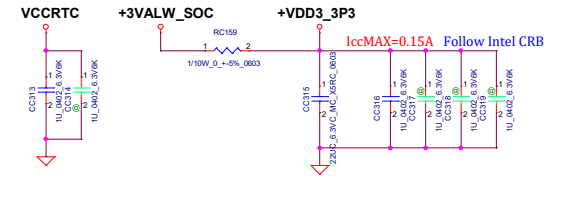
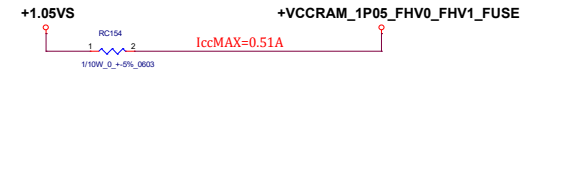
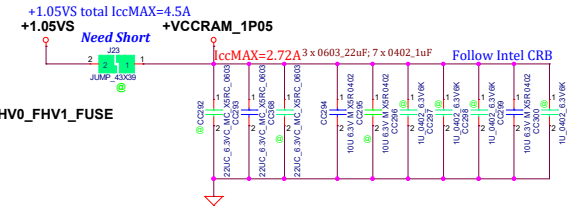
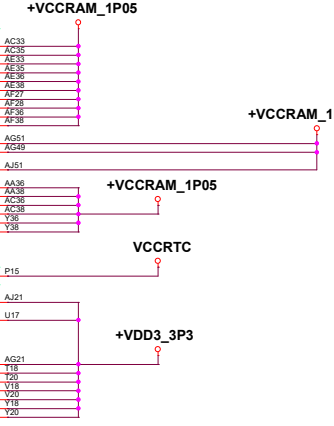
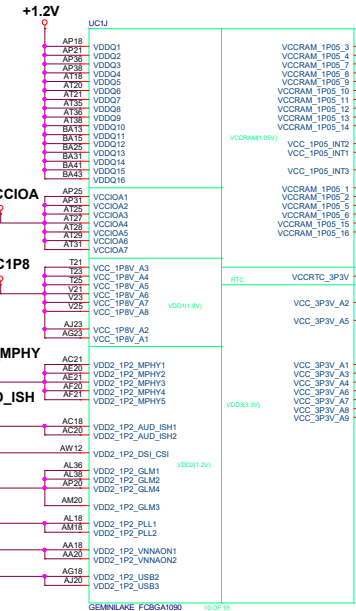
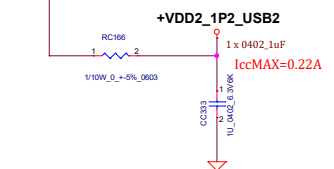
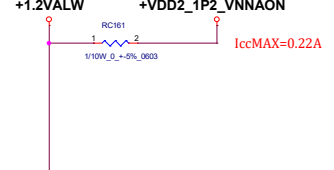
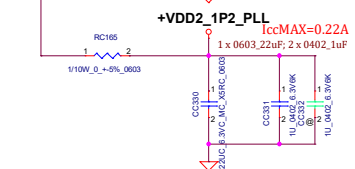
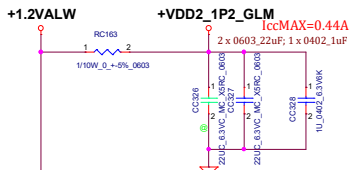
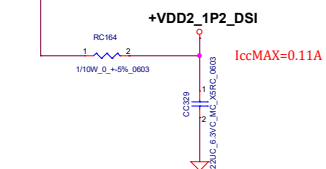
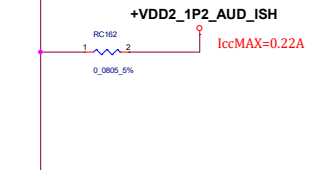
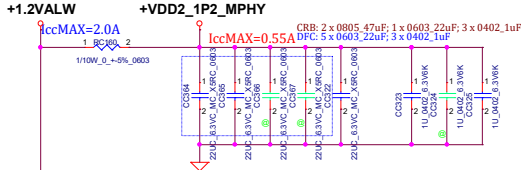
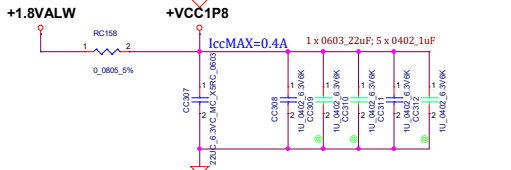
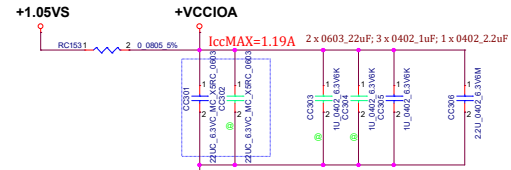
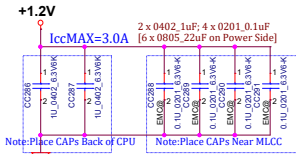


EDP RCOMP is used for DD10/DD11 ports of HDMI/DP as well as the eDP interface. DD10\_RCOMP removed for GLK

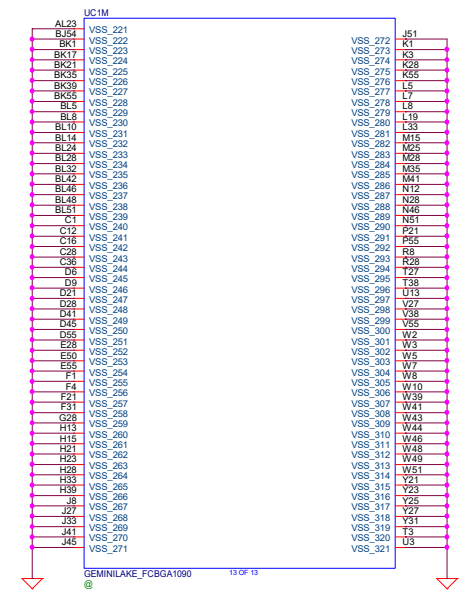
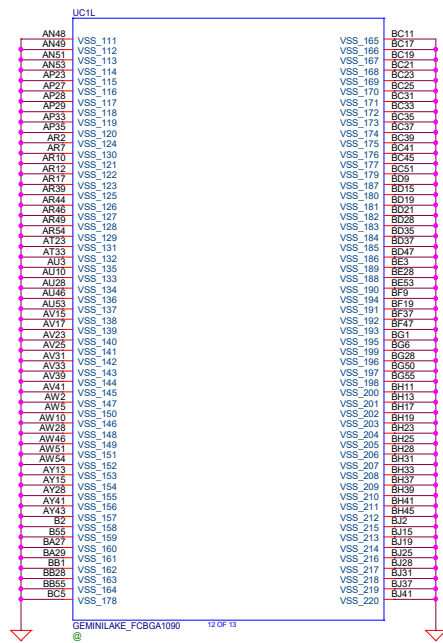
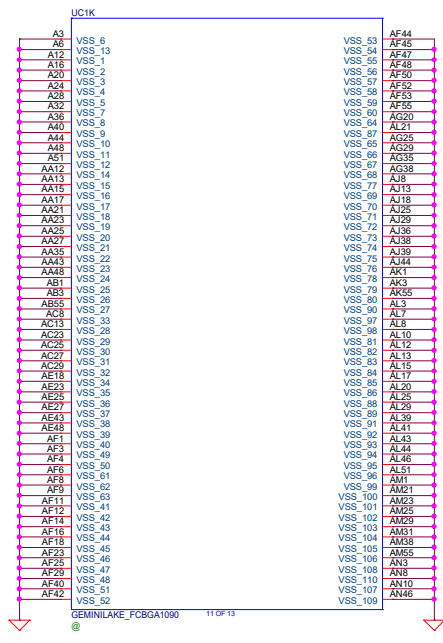




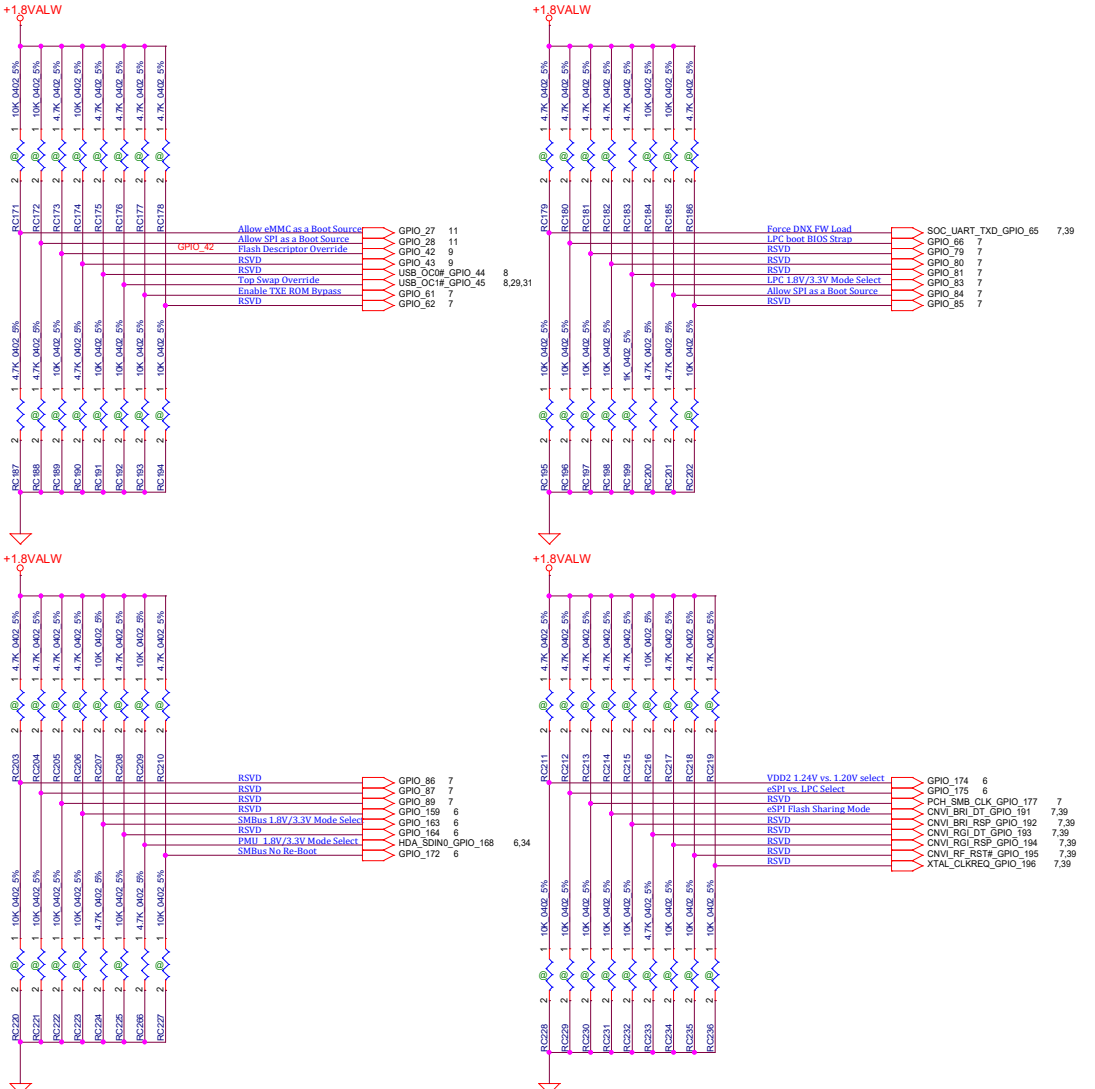




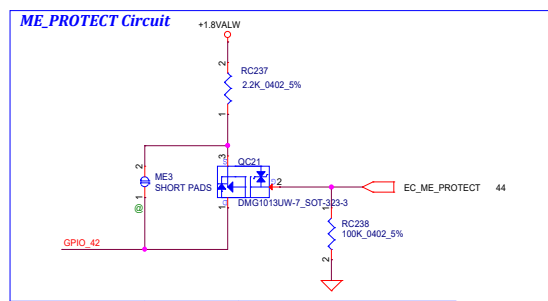




# Hardware STRAPS(Follow up CRB)



GPIO#	Purpose	Internal Termination	Schematics Setting	Pin Usage	Remark
GPIO_27	Allow eMMC as a Boot Source	20K PU	4.7K PD	1 = Enable(Default); 0 = Disable[V] If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_28	Allow SPI as a Boot Source	20K PU	Floating	1 = Enable(Default)[V]; 0 = Disable If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_42	Flash Descriptor Override	20K PD	Floating	1 = Override; 0 = No Override(Normal Operation)[V] This strap enables the platform to override security features in the SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_43	RSVD	20K PU	Floating	Ensure this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_44	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_45	Top swap override	20K PD	Floating	1 = Enable; 0 = Disable(Default)[V] This strap enables platform to change where the core will look for BIOS code for a SPI boot only	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_61	Enable TXE ROM Bypass	20K PD	Floating	1 = Enable Bypass; 0 = Disable Bypass(Default)[V] This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_62	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_65	Force DNFX FW Load	20K PD	Floating	1 = Force; 0 = Do Not Force(Default)[V] This strap is a recovery strap for corrupted FW image, will force TXE3.0 to execute a DoX flow	Follow CRB(v1.2 P58); EDS(v1.2 P40); PDG(v1.2 P471)
GPIO_66	LPC boot BIOS strap	20K PD	Floating	1 = Boot From LPC; 0 = Do Not(Default)[V] The board should strap this low and do not use others	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_79	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_80	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_81	RSVD	20K PU	4.7K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_83	LPC 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_84	Allow SPI as a boot source	20K PU	4.7K PD	1=disable 0=enable (default)[V]	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_85	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_86	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_87	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_89	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_159	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_163	SMBus 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_164	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_168	PMU 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_172	SMBus No Re-Boot	20K PD	Floating	1 = Enable; 0 = Disable (default)[V] Note: Platforms should strap this LOW. Functionality is handled by the PMU.	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_174	VDD2 1.24V vs. 1.20V select	20K PD	Floating	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default) Need Check	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_175	eSPI vs. LPC	20K PD	Floating	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_177	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_191	eSPI Flash Sharing Mode	20K PD	Floating	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_192	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_193	RSVD	20K PU	Floating	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_194	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_195	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_196	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)



EC_ME_PROTECT	GPIO_42	TXE Flash Descriptor Override
Low	High	Override
High	Low	No Override (Normal Operation)

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Size	Document Number		Rev	
C	FS440/FS541		0.2	
Date:	Monday, November 05, 2018	Sheet	15	of 60

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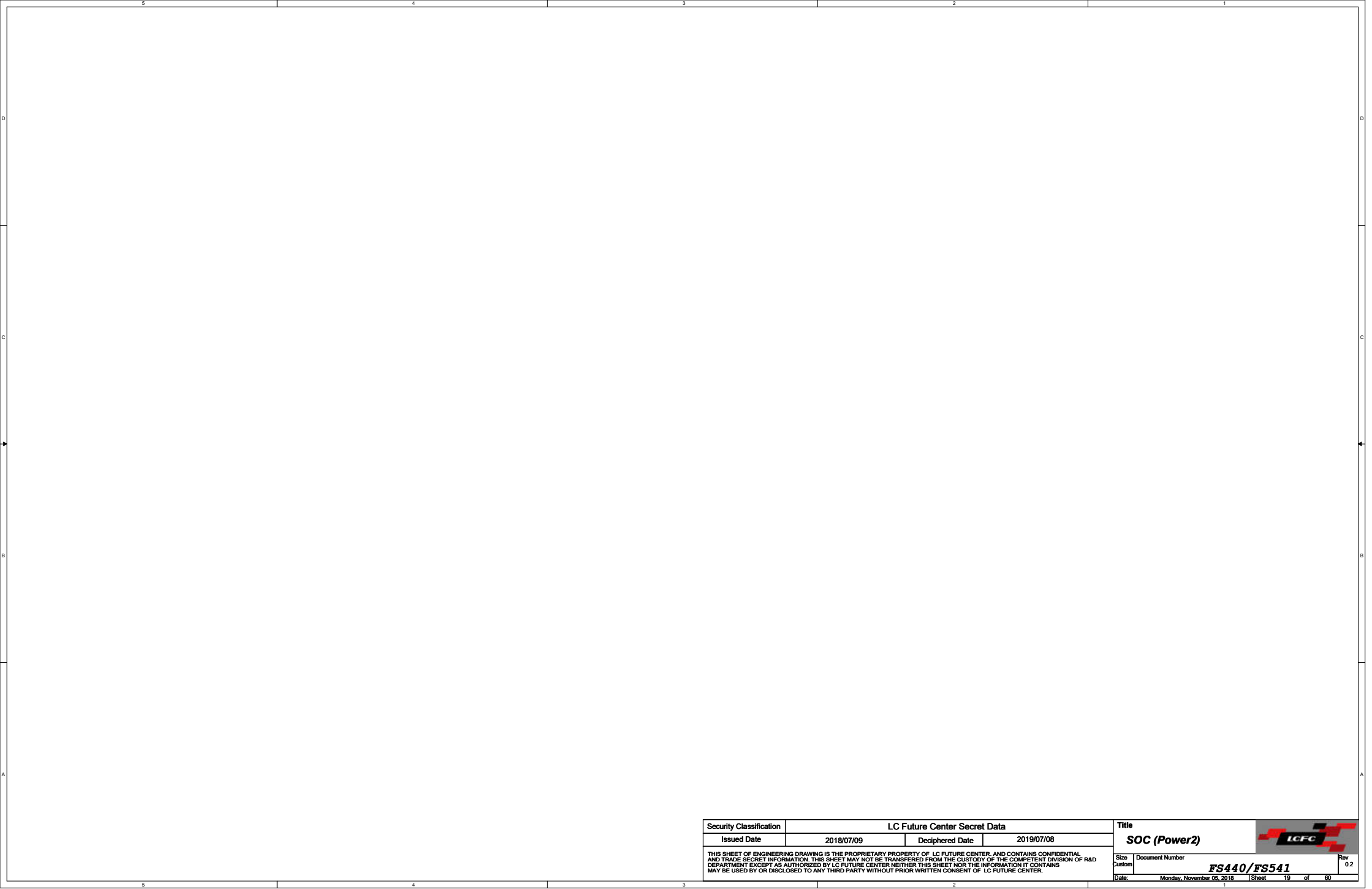
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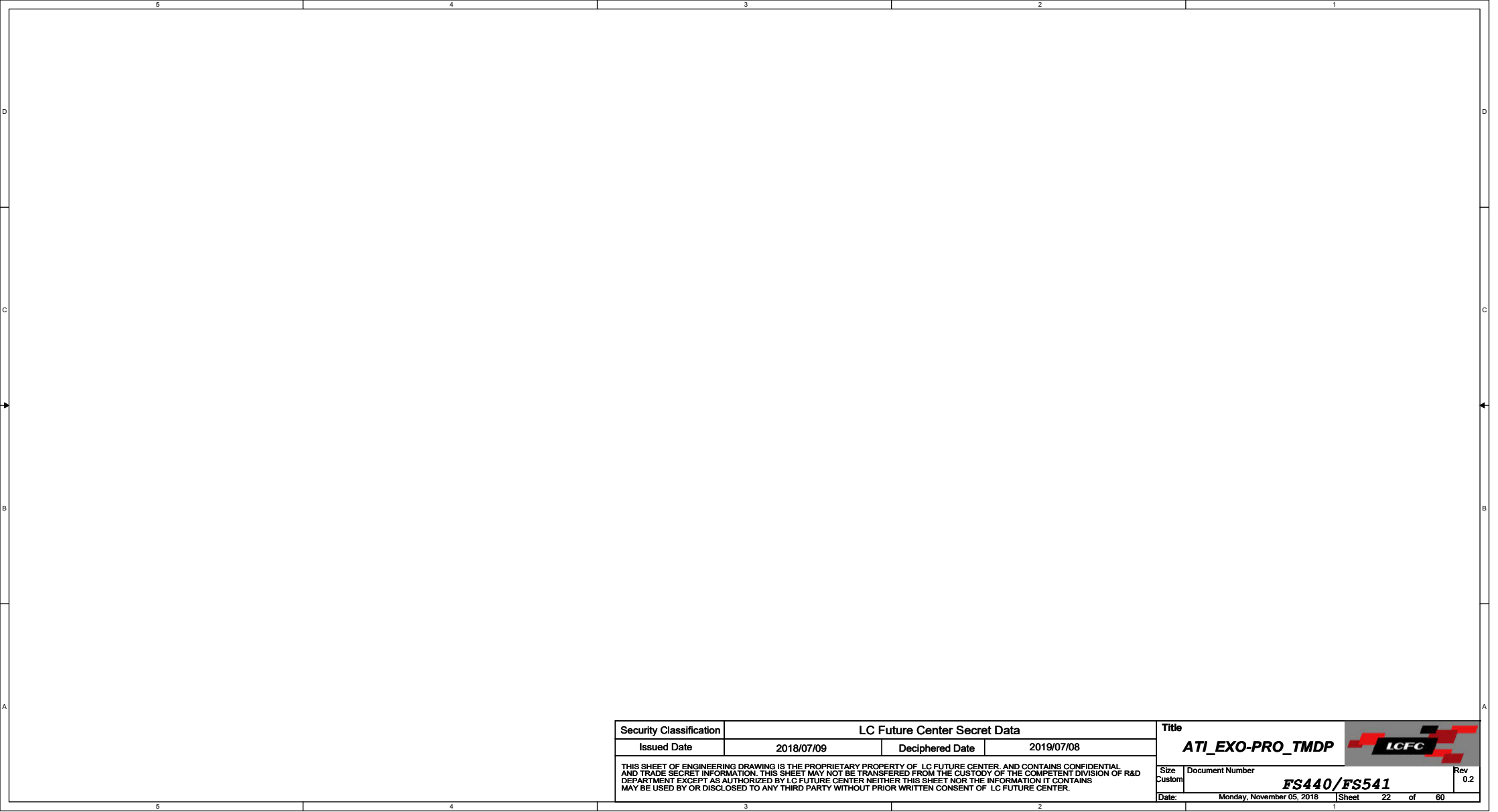
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					Date:	Monday, November 05, 2018	Sheet 19 of 60




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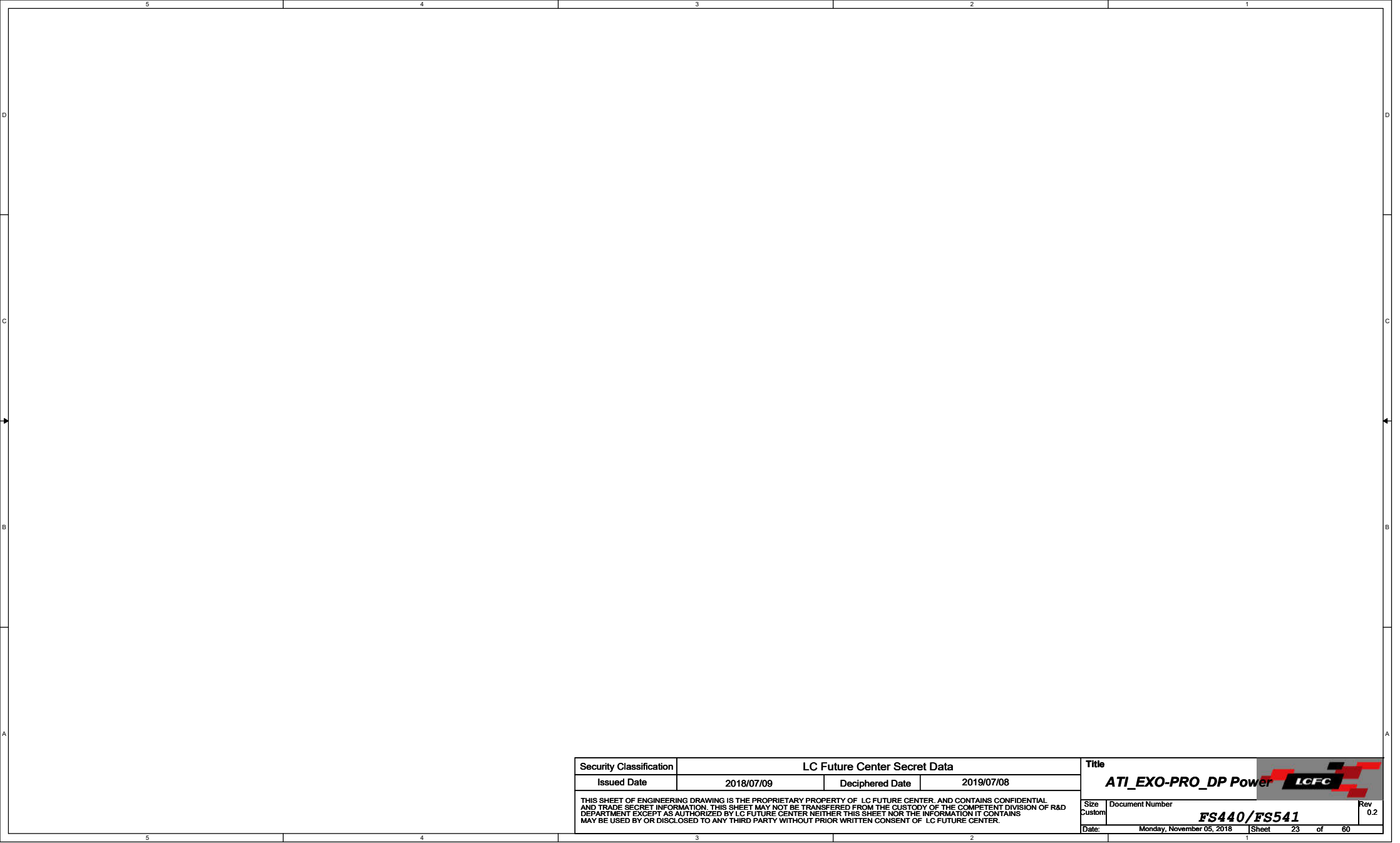
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Custom	<b>FS440/FS541</b>	0.2
<b>Date:</b>	Monday, November 05, 2018	<b>Sheet</b> 20 <b>of</b> 60

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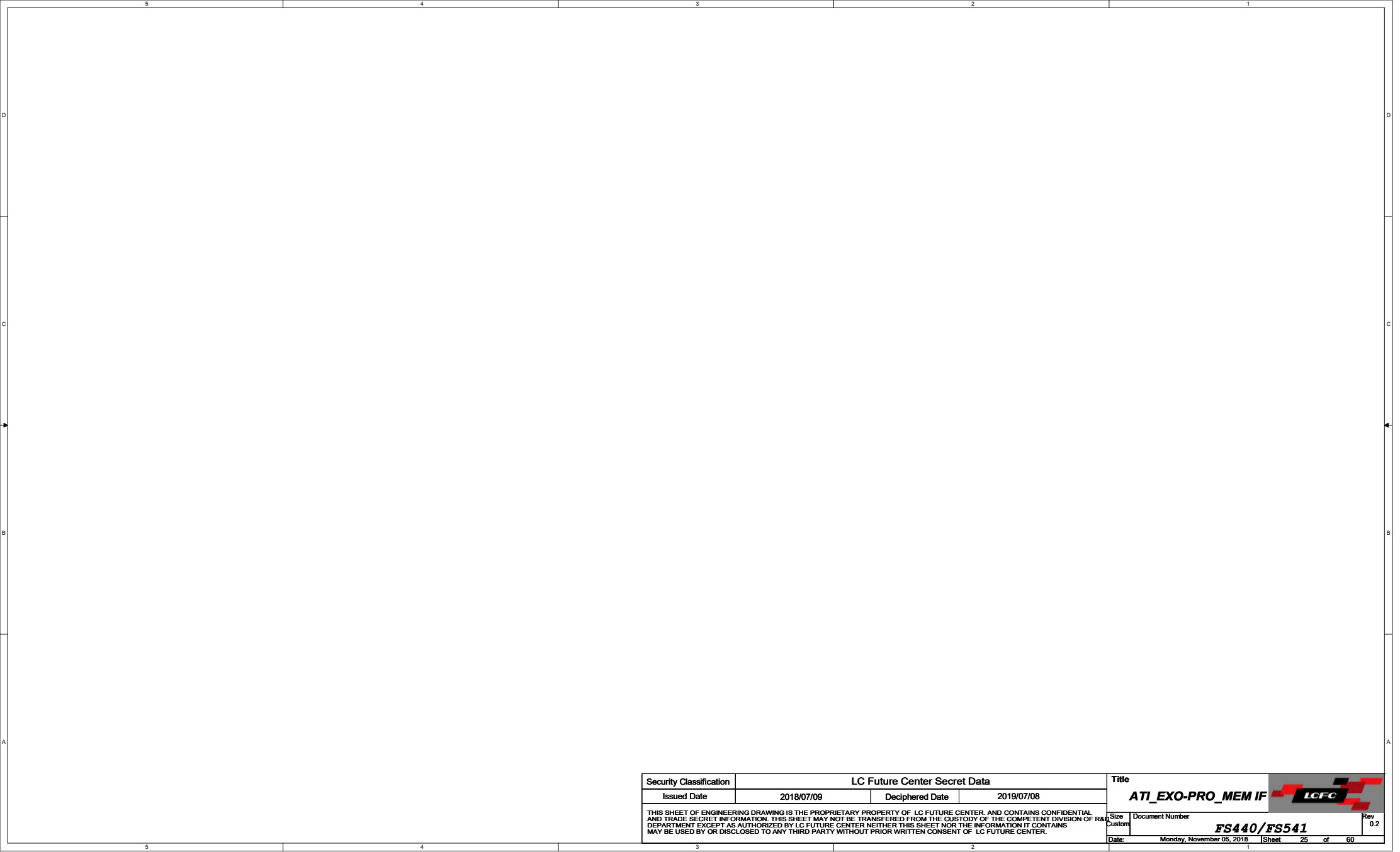



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<b>Issued Date</b>	2018/07/09	<b>Deciphered Date</b>	2019/07/08	<b>ATI_EXO-PRO_DP Power</b>	
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				Page	24 of 82





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Custom	<b>FS440/FS541</b>		0.2
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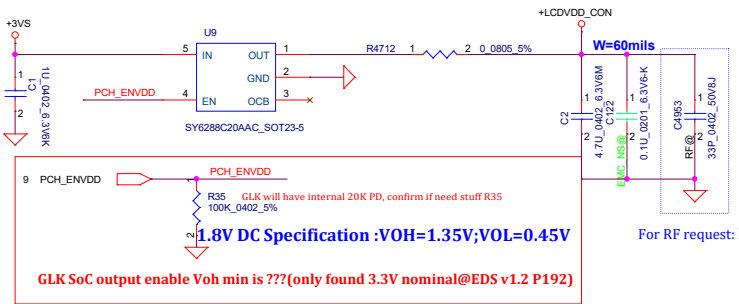
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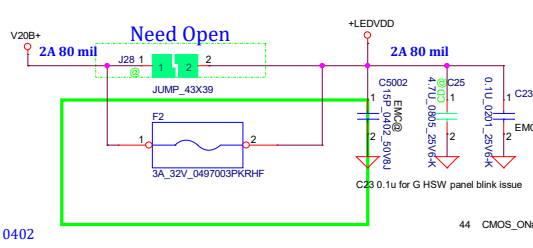
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Date:	Monday, November 05, 2018	Sheet 27 of 60

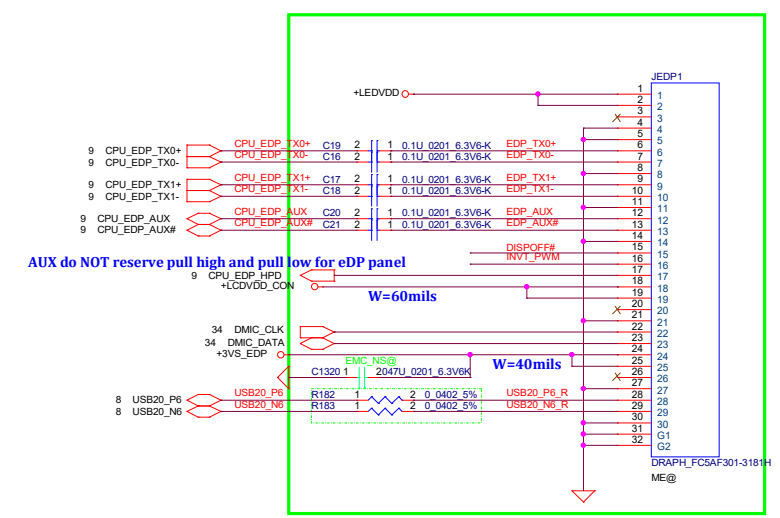
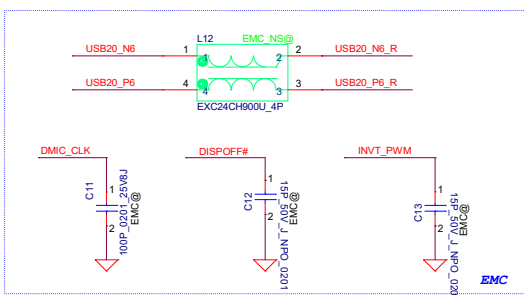
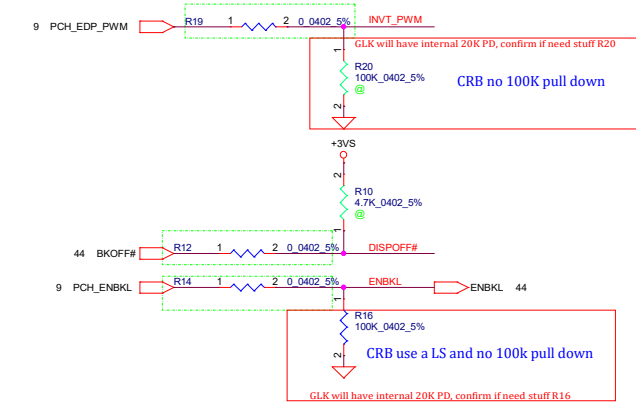
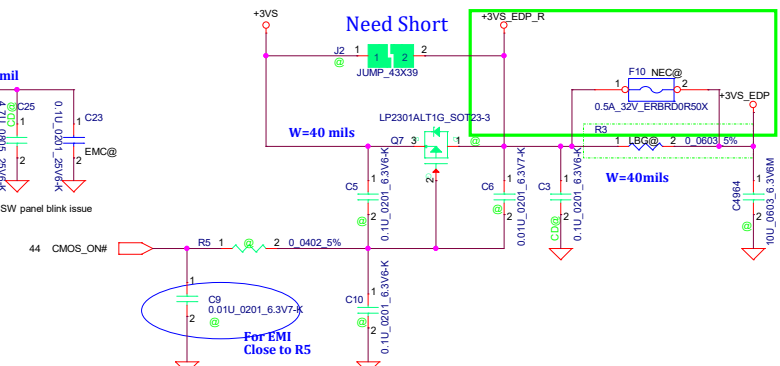
### LCD POWER CIRCUIT



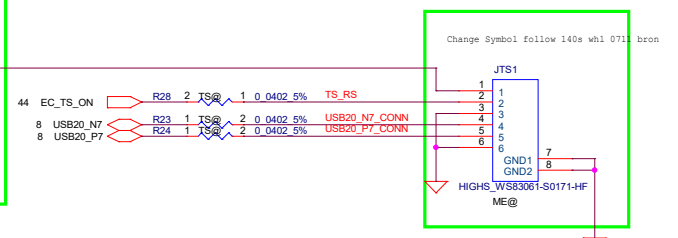
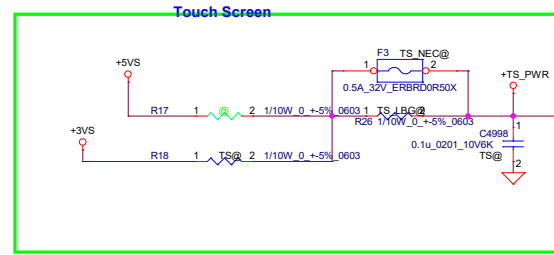
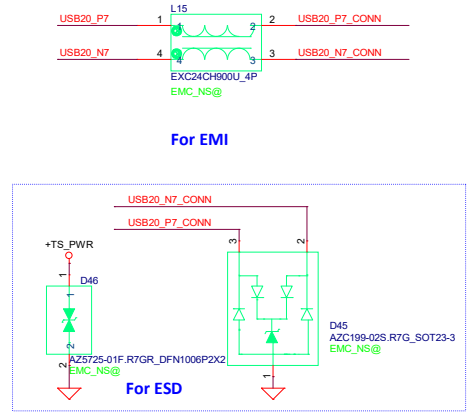
### B+ to +LEDVDD POWER



### CMOS CAMERA

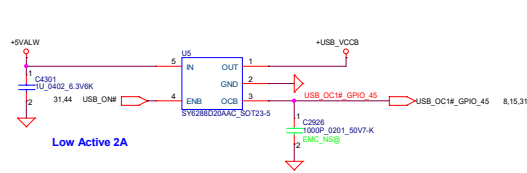


### Touch Screen

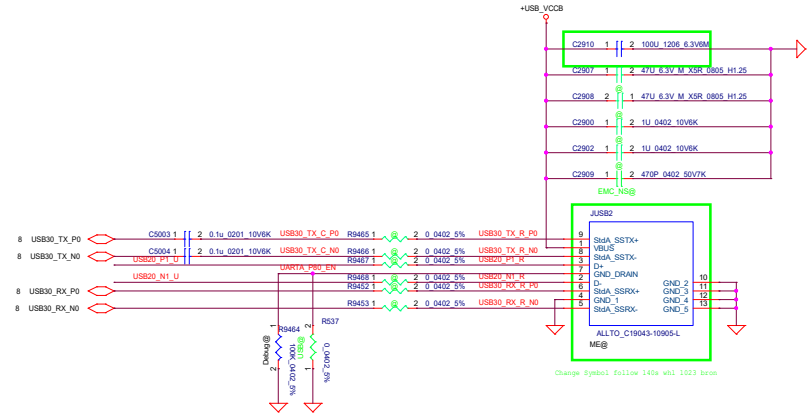
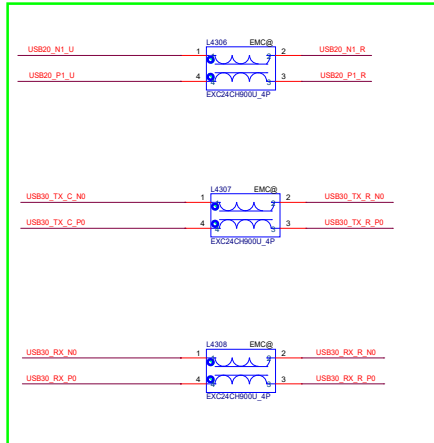


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Date:	Monday, November 05, 2018	Sheet	28	of 60	

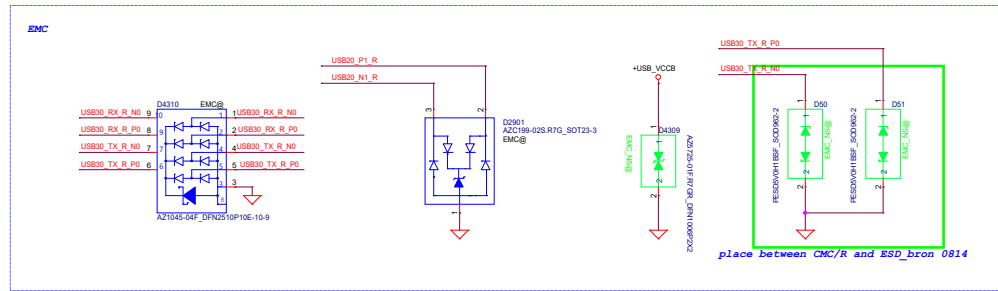
# RIGHT SIDE USB3.0 PORT



Low Active 2A

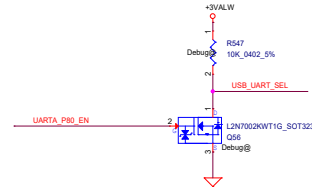
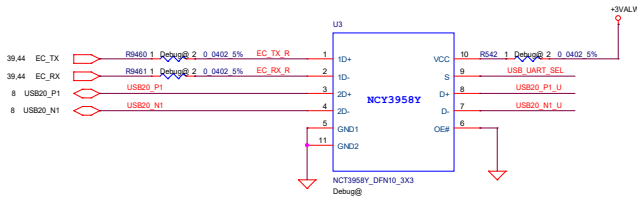


Change symbol follow 1409 whi 1023 doc



place between CMC/R and ESD\_bron 0814

## For USB Debug Function



ISBDEBUG	Kernel debug
Set Input	Set Input
Set output Low	ENABLE

JARTA_P0F_EN	POST 80
Set Input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
0	X	DISABLE
1	1	0(+/-) to 10(+/-)
1	0	0(+/-) to 20(+/-)

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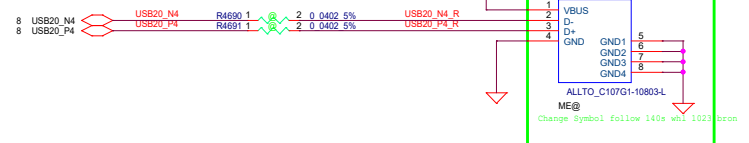
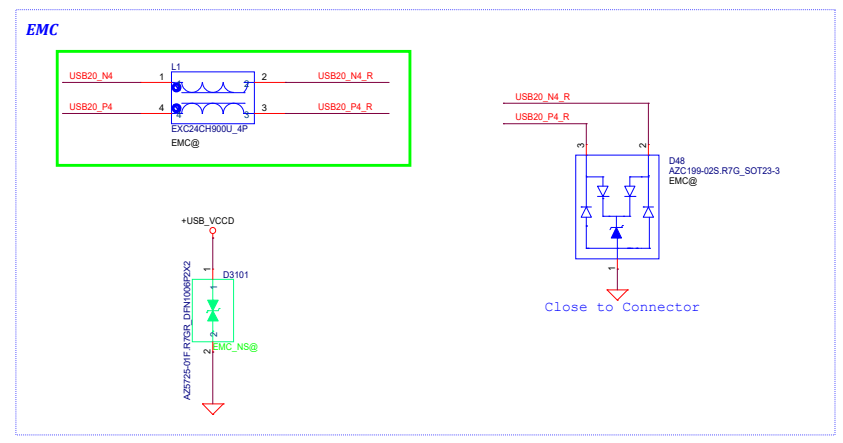
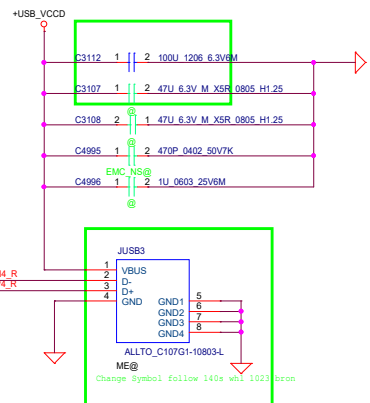
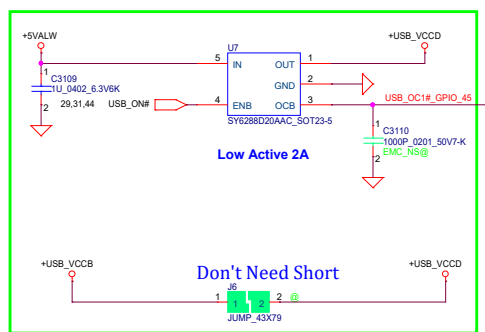
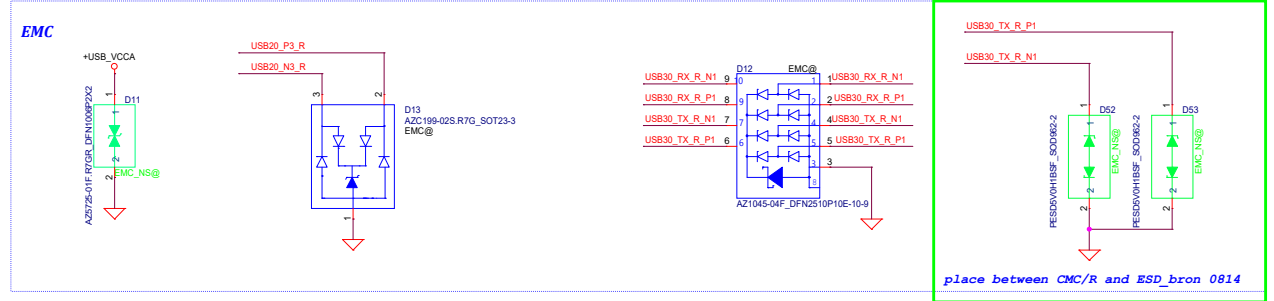
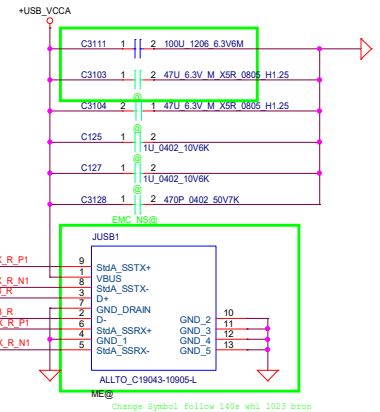
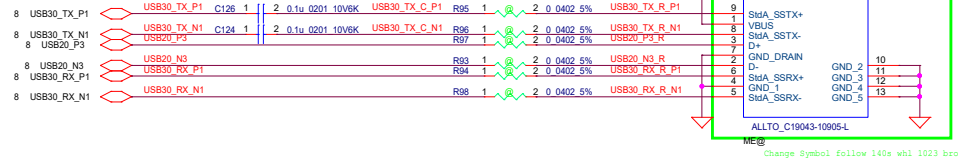
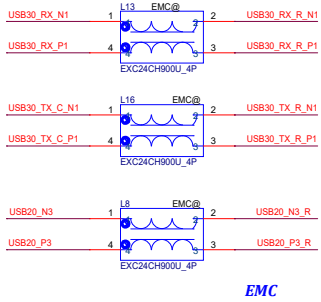
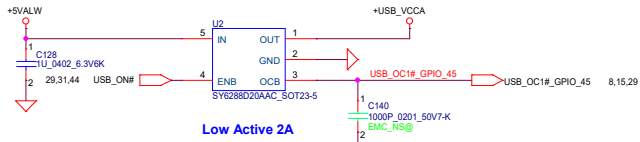
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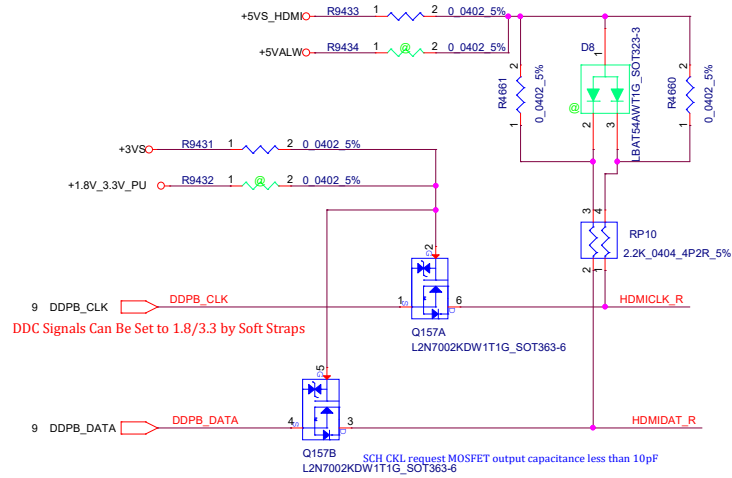
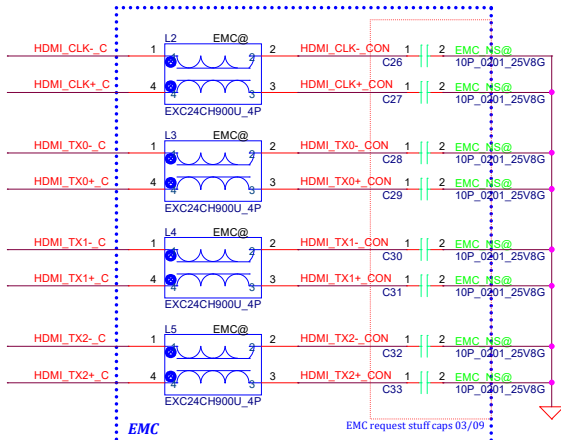
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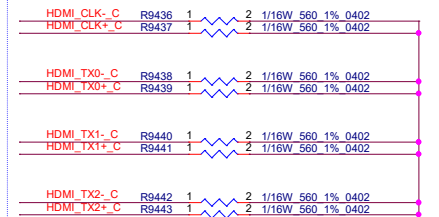
# LEFT SIDE USB3.0 PORT x1



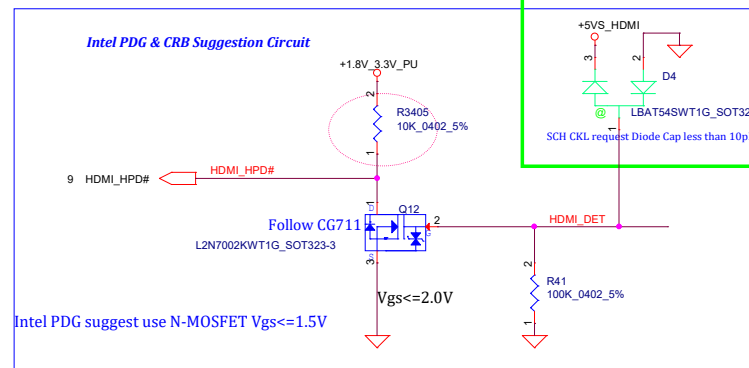
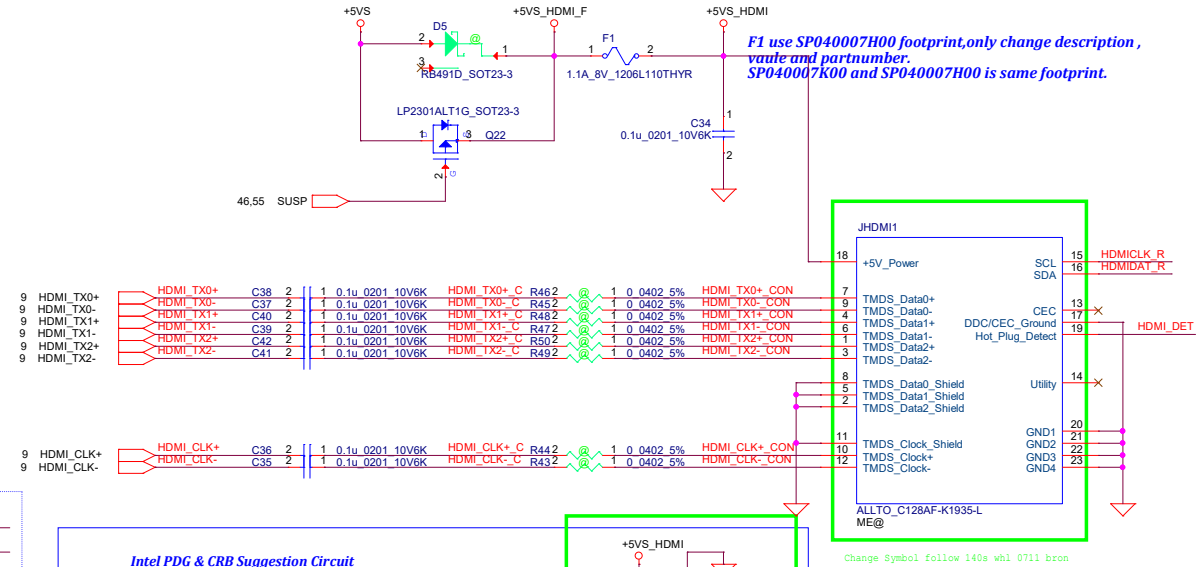
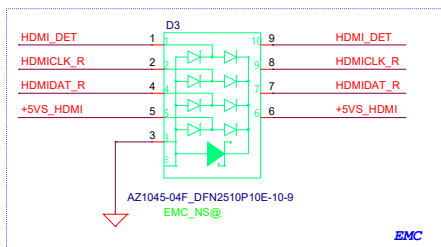
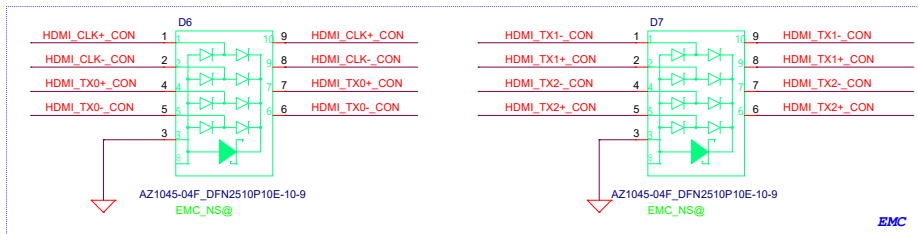
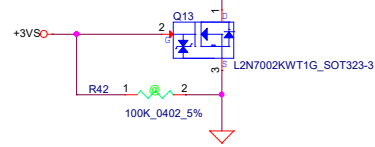
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/07/09	Deciphered Date	2019/07/08	USB3.0&USB2.0 CONN	
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Size	Document Number			Rev	
	FS440/FS541			0.2	
Date:	Monday, November 05, 2018		Sheet	31 of 60	



Follow PDG & CRB use 470ohm,SVT change 470 to 560 for HDMI issue



Change to 0404 RP 04/29



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Size Document Number								Rev	
Date								Monday, November 05, 2018	
Sheet								32 of 60	
FS440/FS541								0.2	



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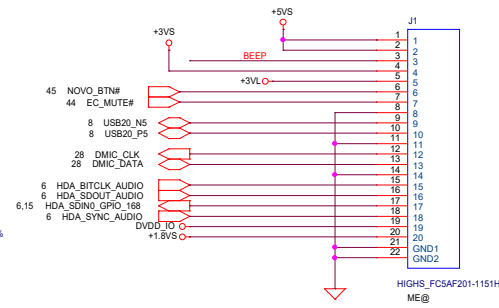
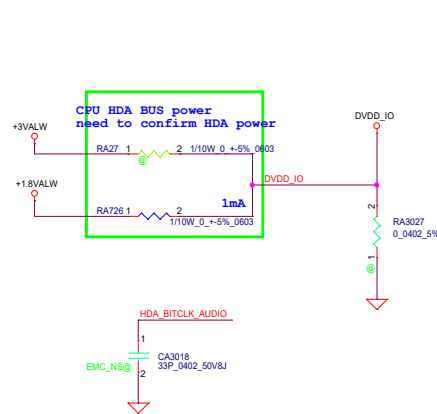
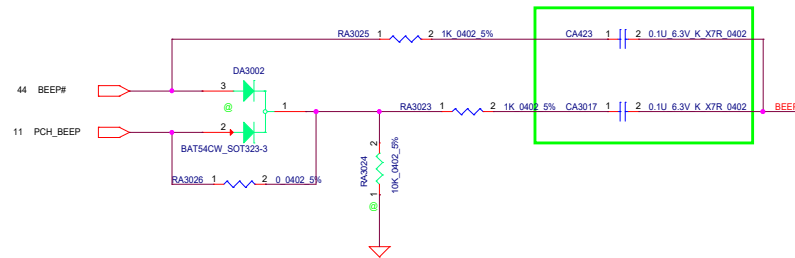
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				<small>Date</small> Monday, November 05, 2018	<small>Rev</small> 0.2
				<small>Sheet</small> 33	<small>of</small> 60






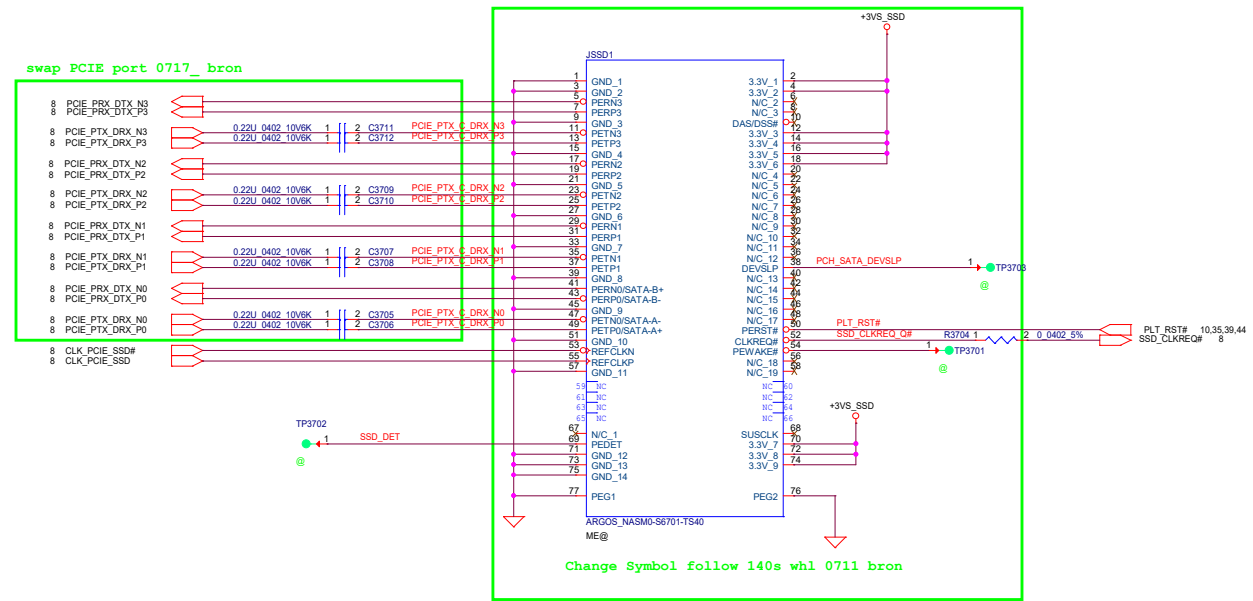
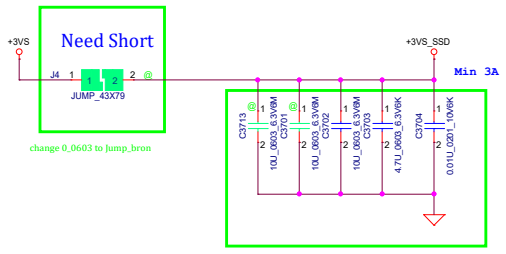
Change Symbol follow 140s whl 0711 bron

20Pin CONN

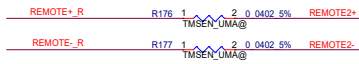
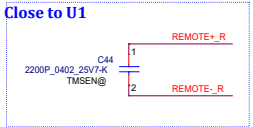




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				Date:	Monday, November 05, 2018	Sheet 36 of 60

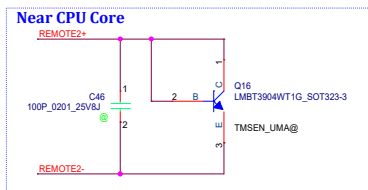


**THERMAL SENSOR**

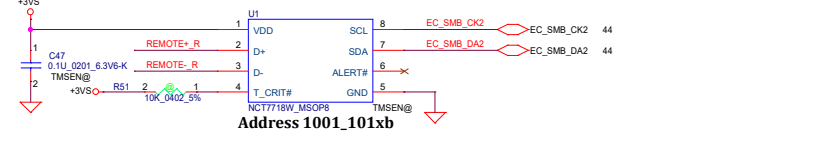


REMOTE+/-R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

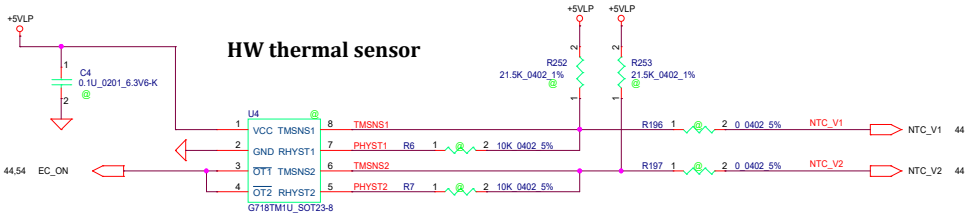
Set Thermal Sensor as a BOM Structure



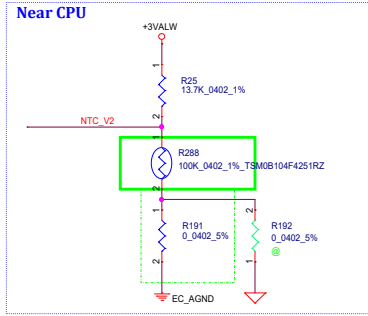
**SMSC thermal sensor placed near DIMM**



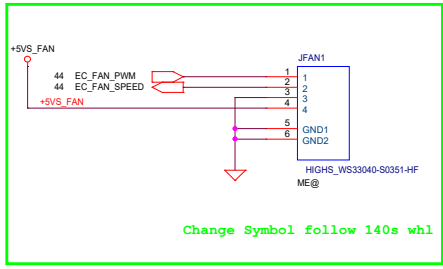
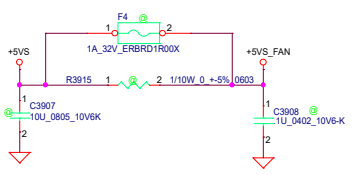
**HW thermal sensor**



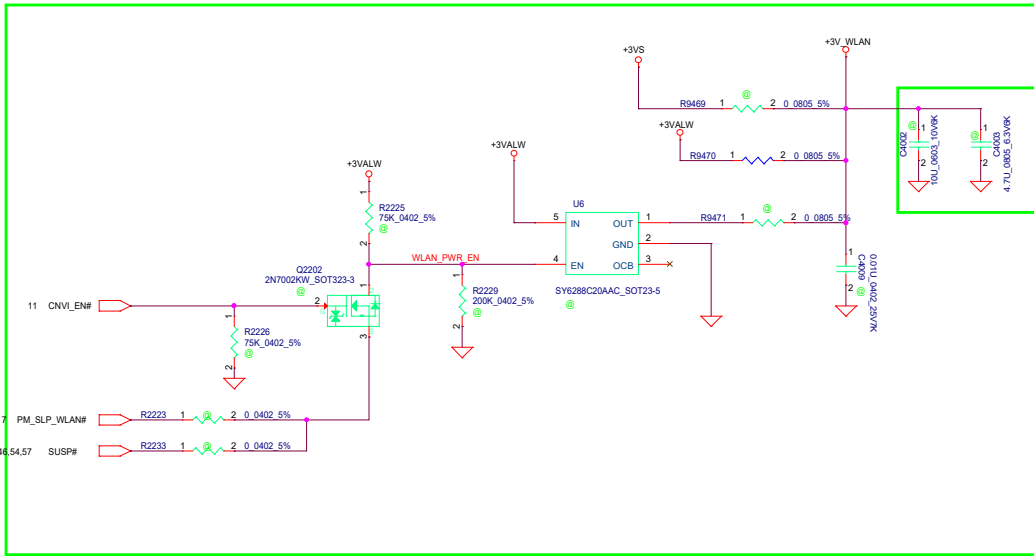
Over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C



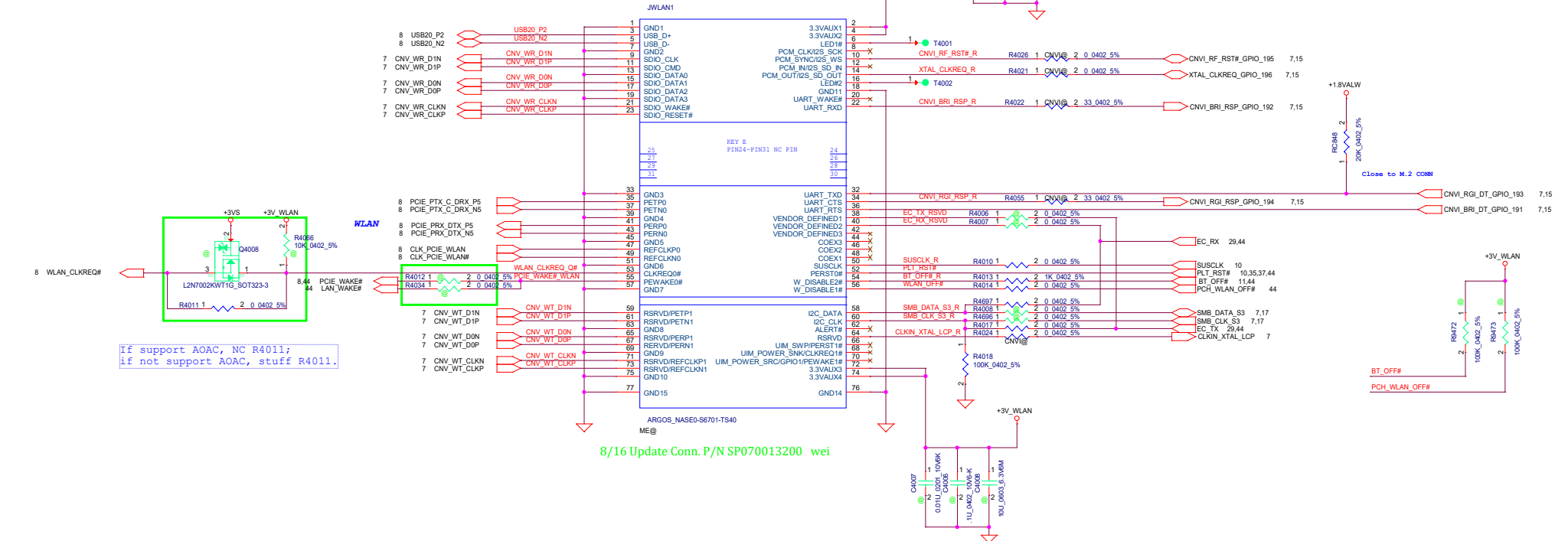
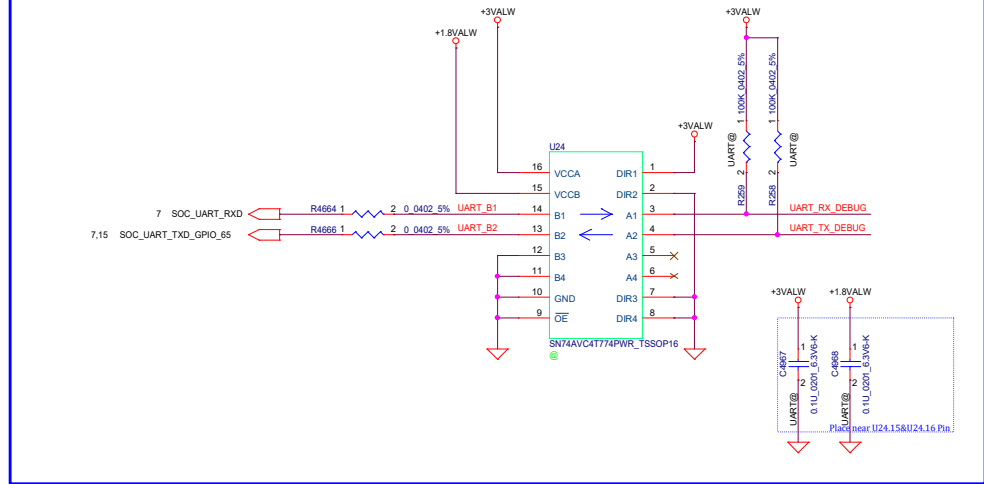
**FAN Conn**



# Mini-Express Card(WLAN/WiMAX)



# UART Transceiver



If support AOAC, NC R4011;  
if not support AOAC, stuff R4011.

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Size	C	Document Number	FS440/FS541		Rev
Date	Monday, November 05, 2018	Sheet	38	of	60

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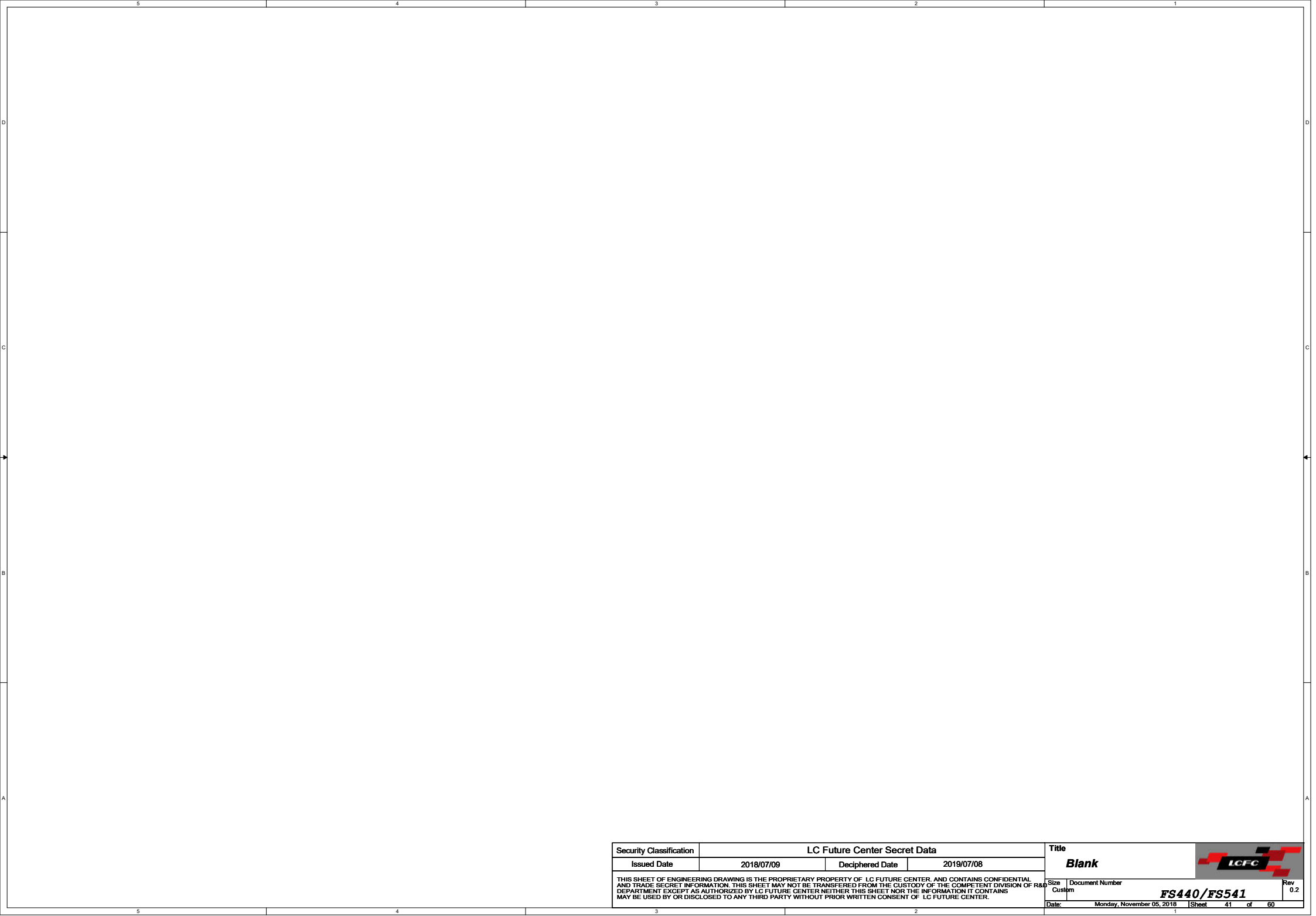
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Custom	<b>FS440/FS541</b>	0.2
Date:	Monday, November 05, 2018	Sheet 40 of 60

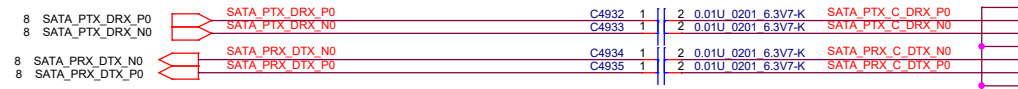




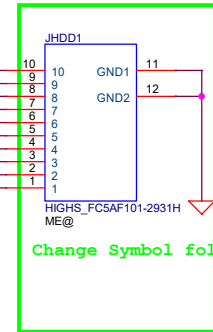
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Issued Date	2018/07/09	Deciphered Date	2019/07/08	Blank		
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				Custom	FS440/FS541	0.2
				Date:	Monday, November 05, 2018	Sheet 41 of 60

### SATA HDD Conn.

SATA HDD P/N Pin Define Same as CG411

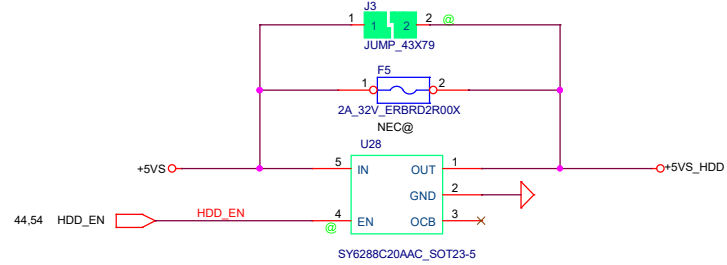


+5VS\_HDD

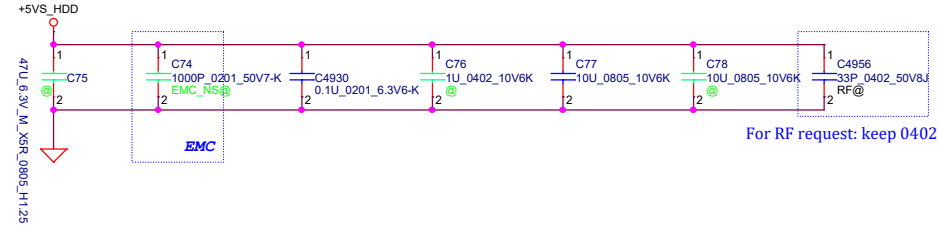



Change Symbol follow 140s whl 0711 bron

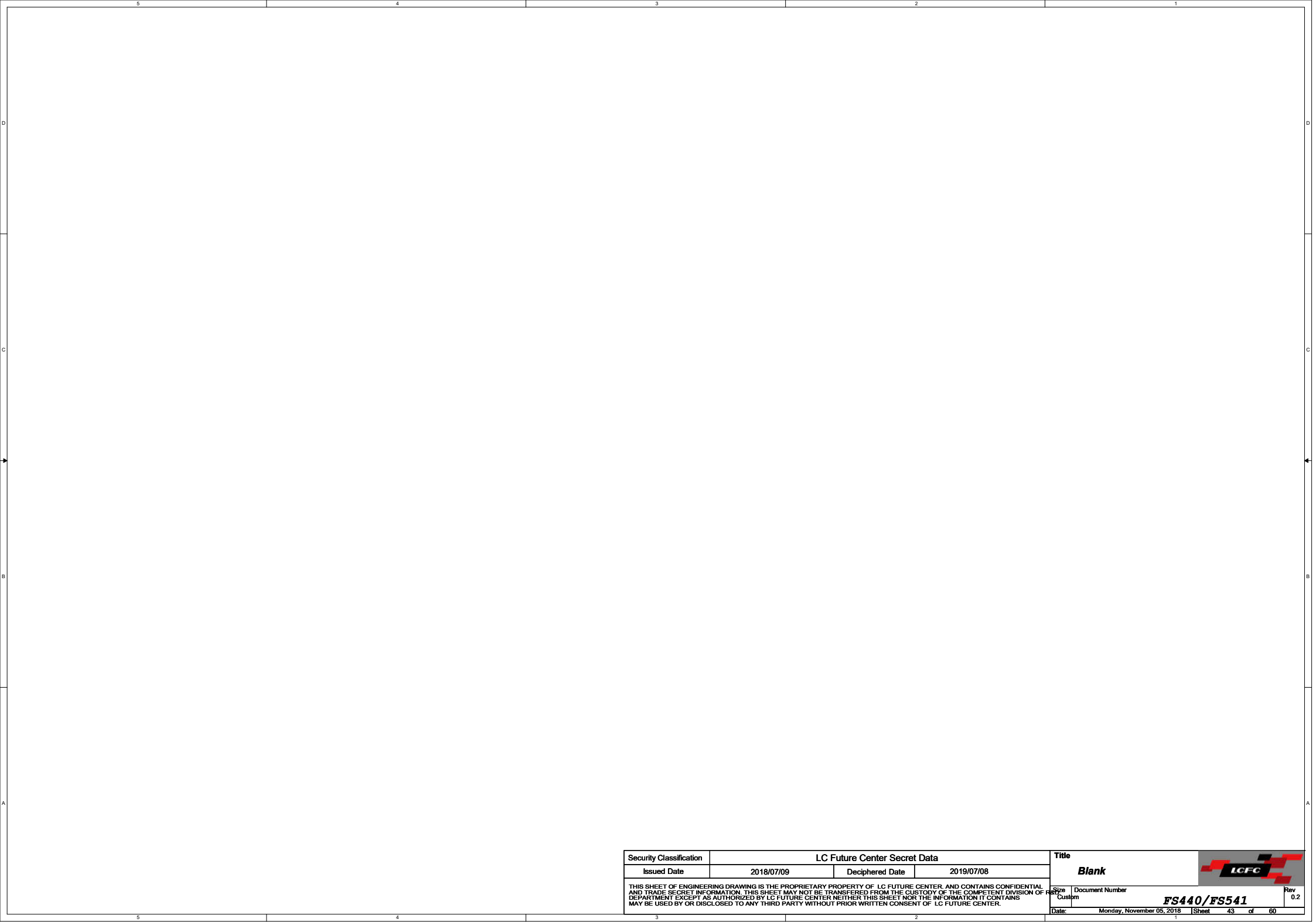
Need Short




High Active 2A

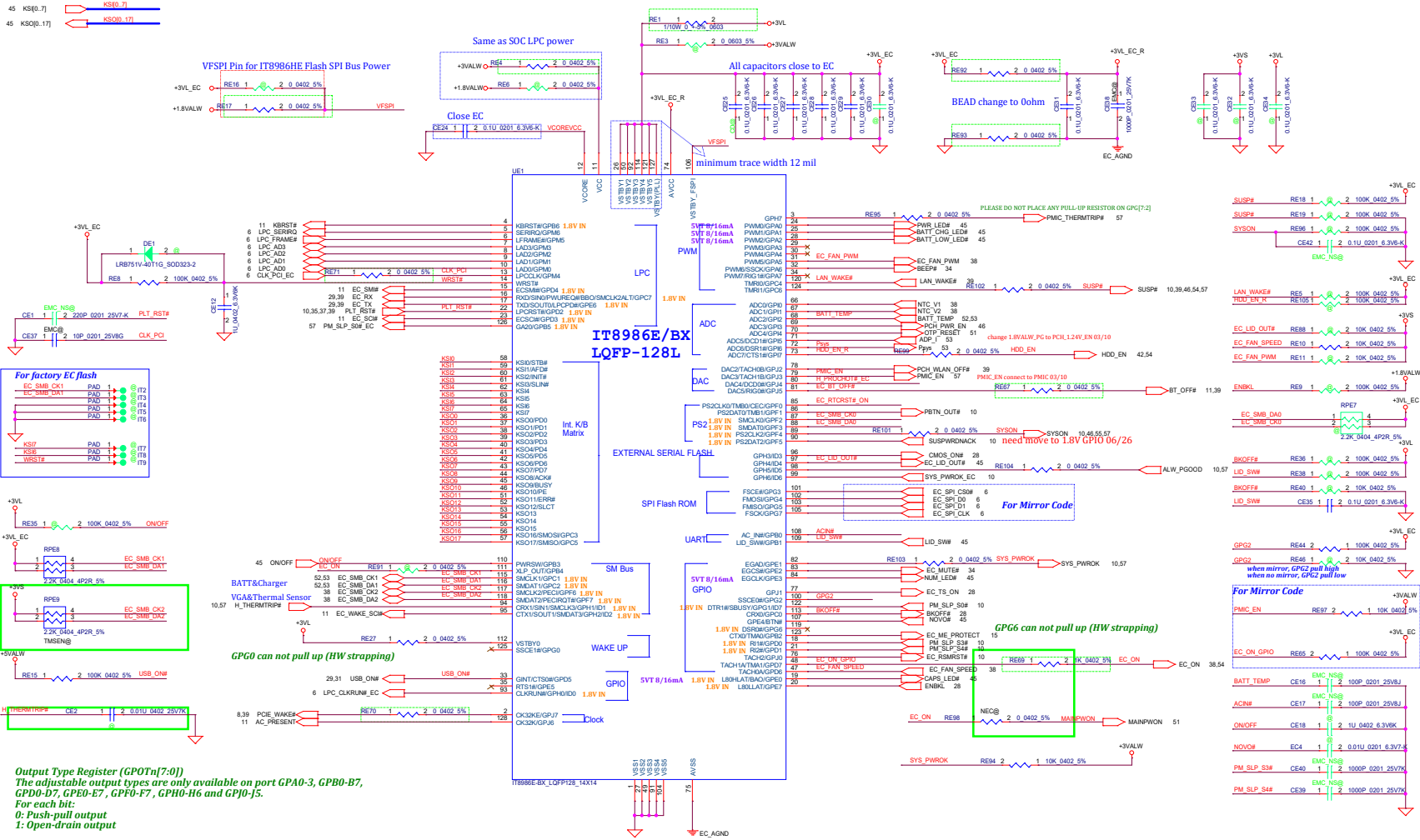


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				Rev 0.2



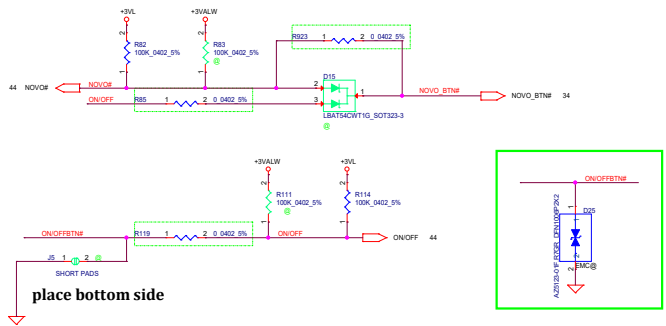
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Size	Document Number	Rev
Custom	FS440/FS541	0.2
Date:	Monday, November 05, 2018	Sheet 43 of 60

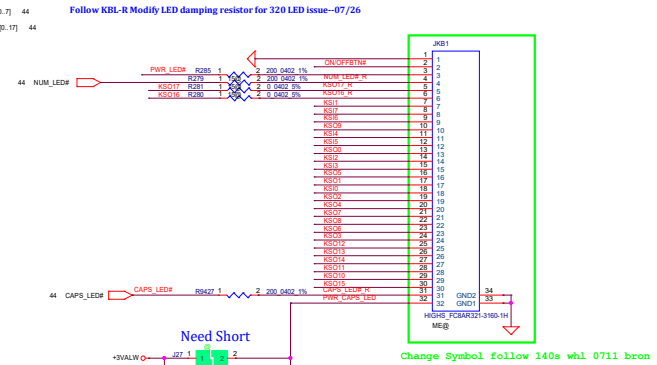
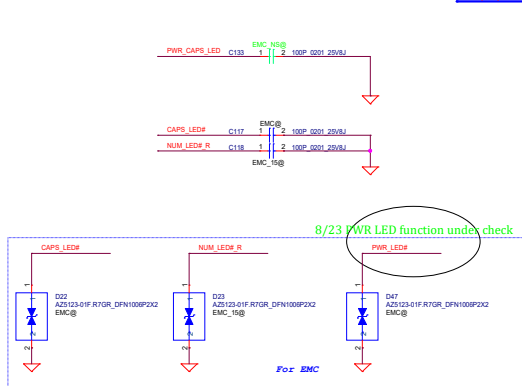


**Output Type Register (GPOTn[7:0])**  
 The adjustable output types are only available on port GPA0-3, GPB0-B7, GPD0-D7, GPE0-E7, GPF0-F7, GPH0-H6 and GPJ0-J5.  
 For each bit:  
 0: Push-pull output  
 1: Open-drain output

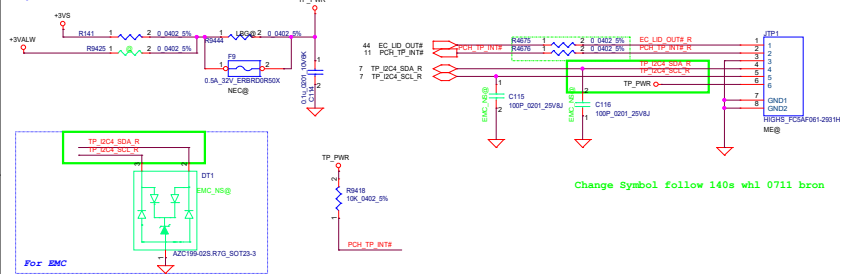
### ON/OFF switch



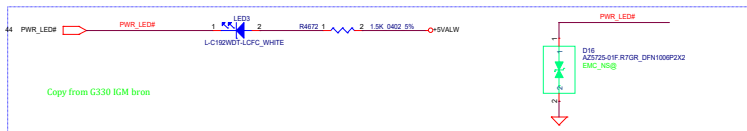
### K/B Connector



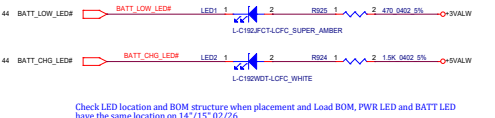
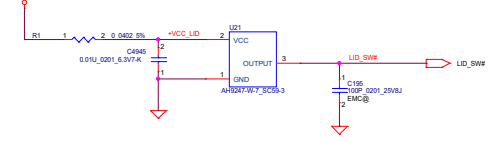
### TP/B Connector



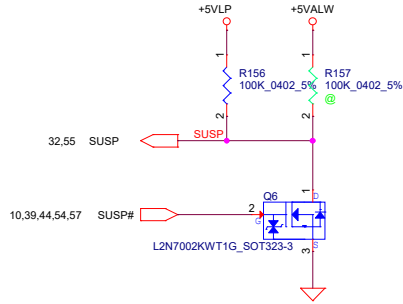
### LED



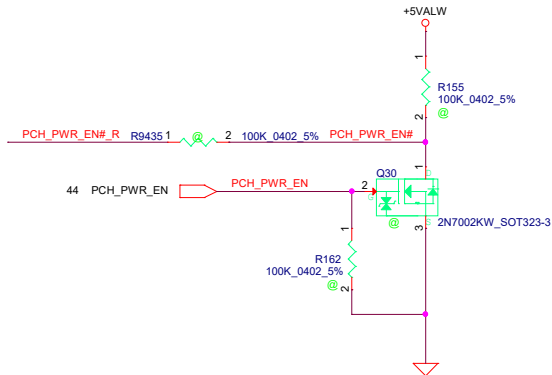
### LID Switch



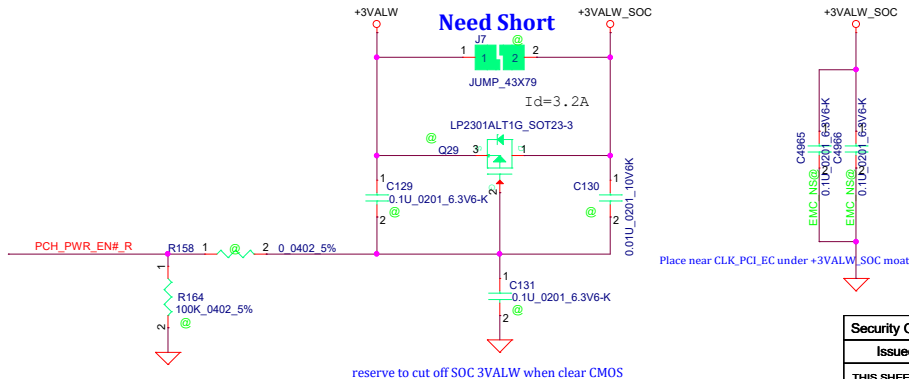
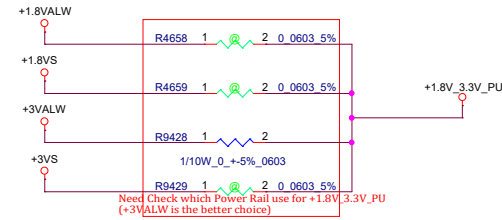
Check LED location and BOM structure when placement and Load BOM, PWR LED and BATT LED have the same location on 14/15/02/26



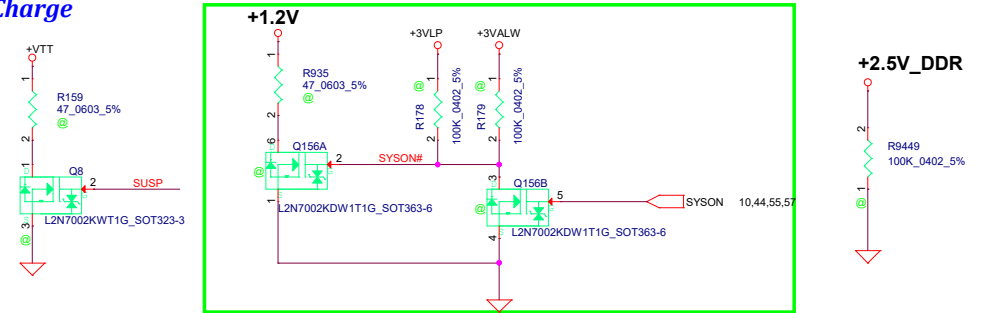
### +3VALW to +3VALW\_SOC



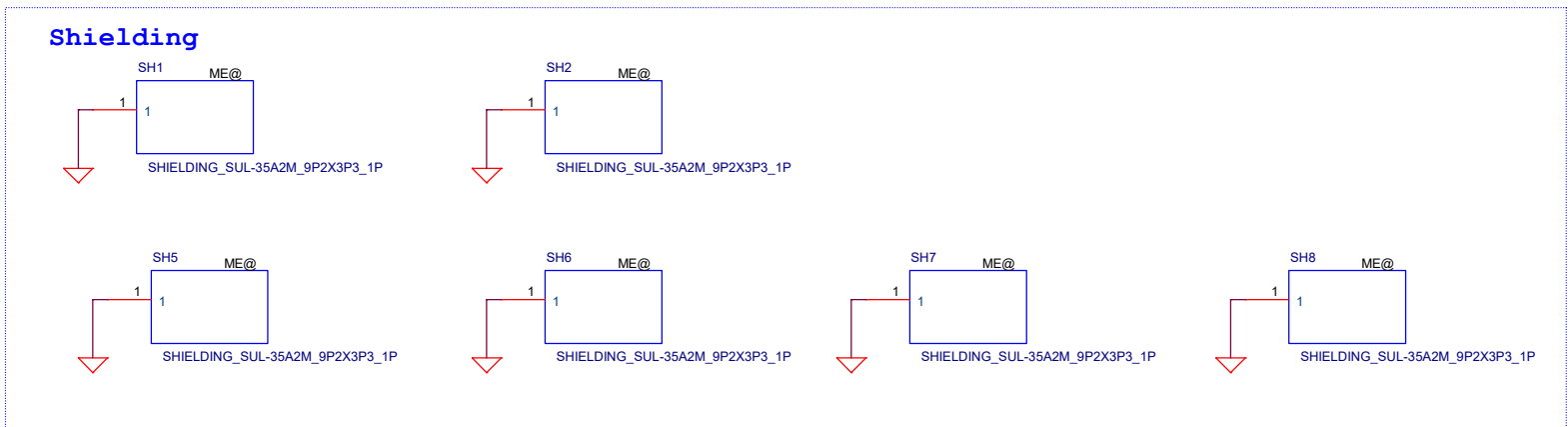
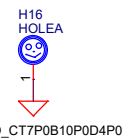
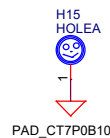
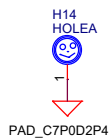
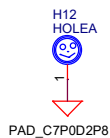
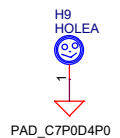
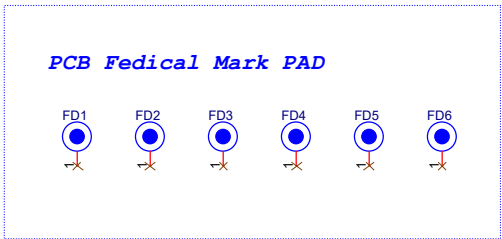
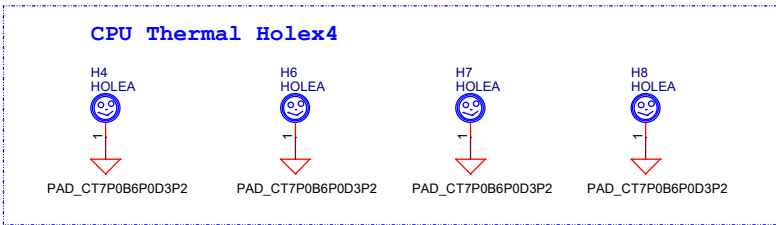
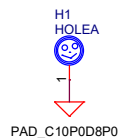
### +1.8V\_3.3V\_PU Power Rail for 1.8/3.3 Select by Soft Strap



### For DisCharge



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Size	Custom	Document Number	FS440/FS541		Rev
Date:	Monday, November 05, 2018	Sheet	46	of	60



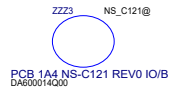
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Size	Document Number	Rev
B	FS440/FS541	0.2
Date:	Monday, November 05, 2018	Sheet 47 of 60

**14&15 PCB MB**

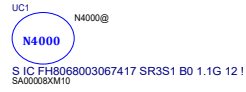
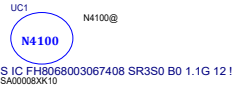


**PCB ODD/B**



**GLK CPU**

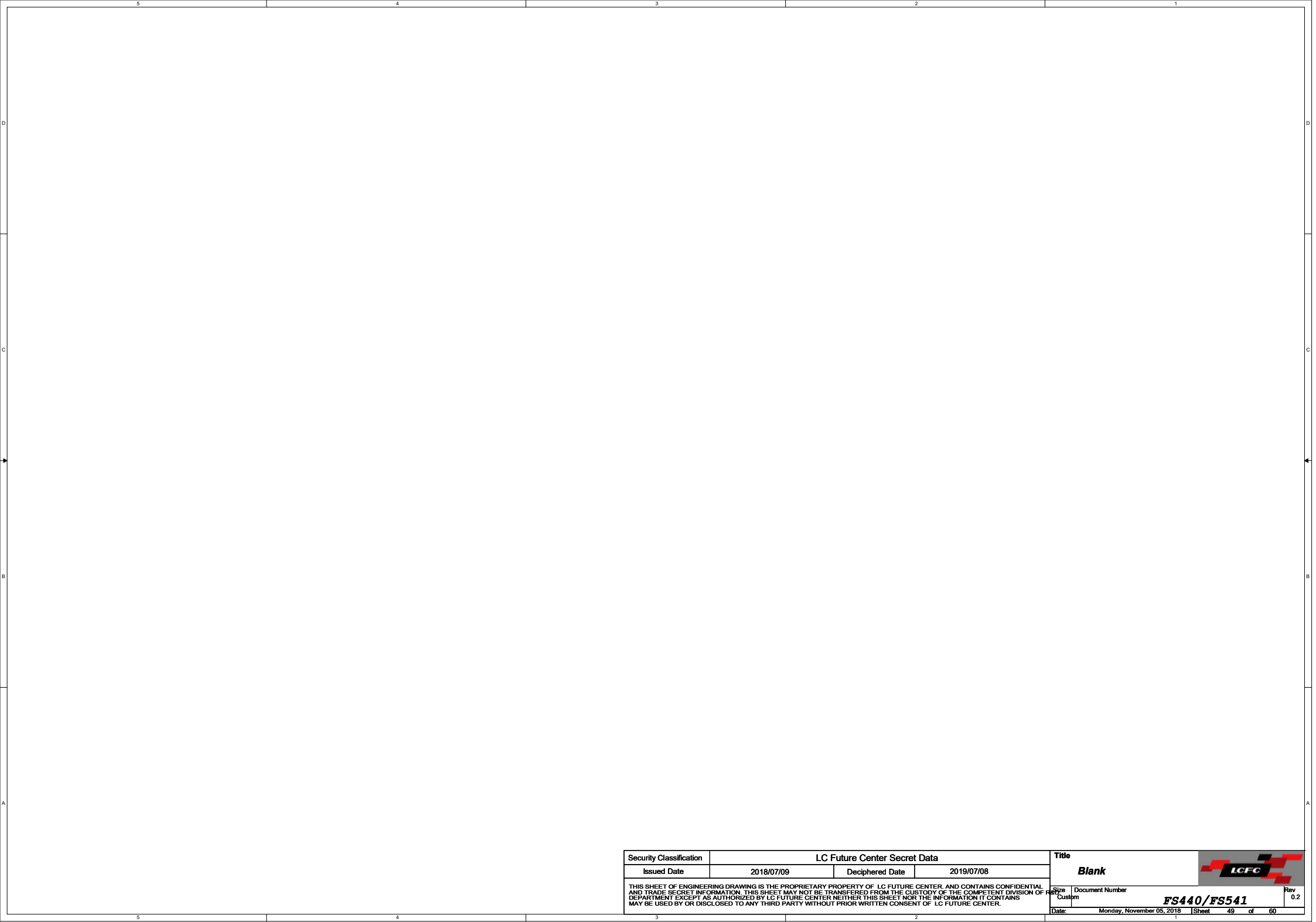
**MP Sample**




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				C	FS440/FS541
				Date	Monday, November 05, 2018
				Sheet	48 of 60
				Rev	0.2

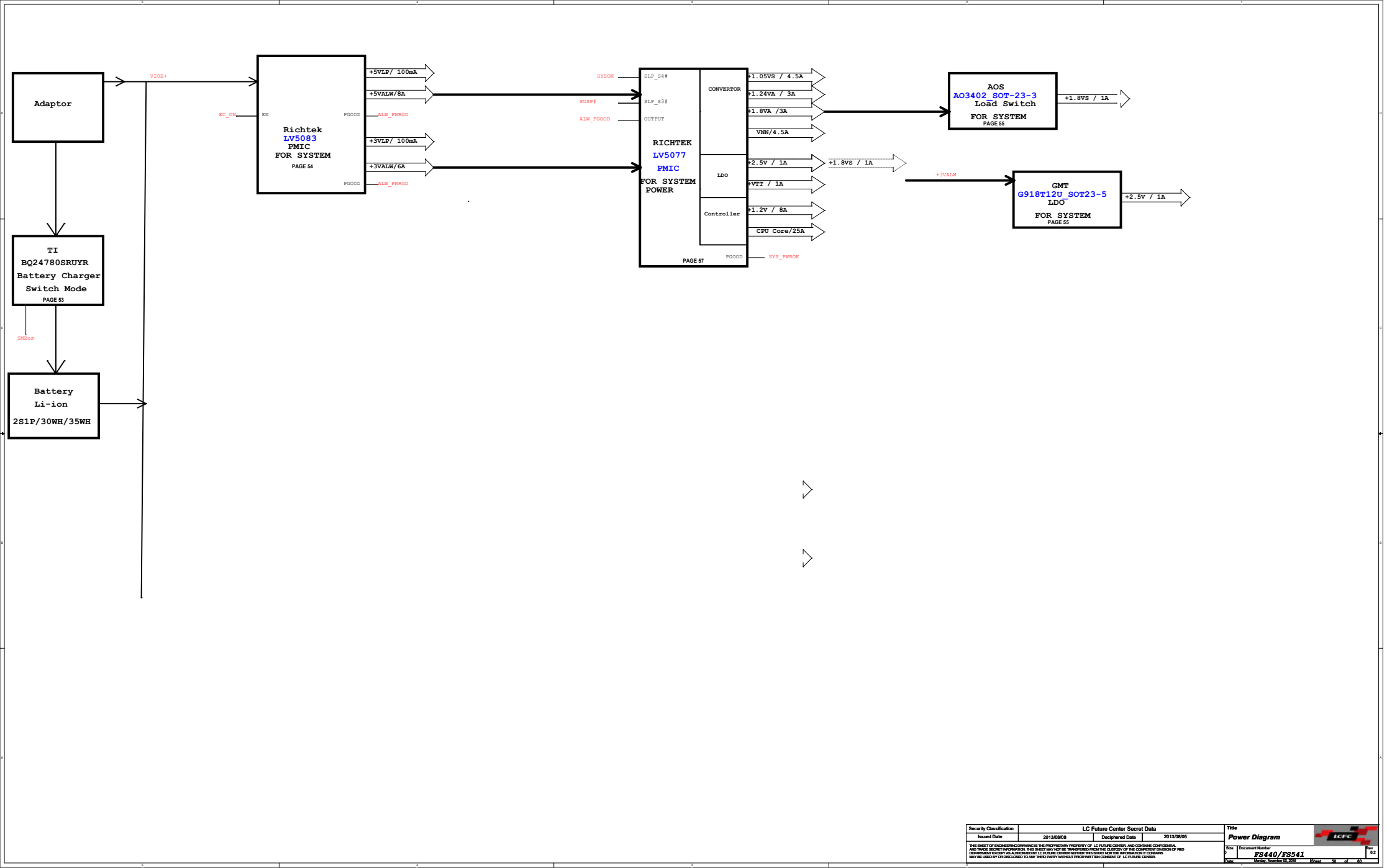


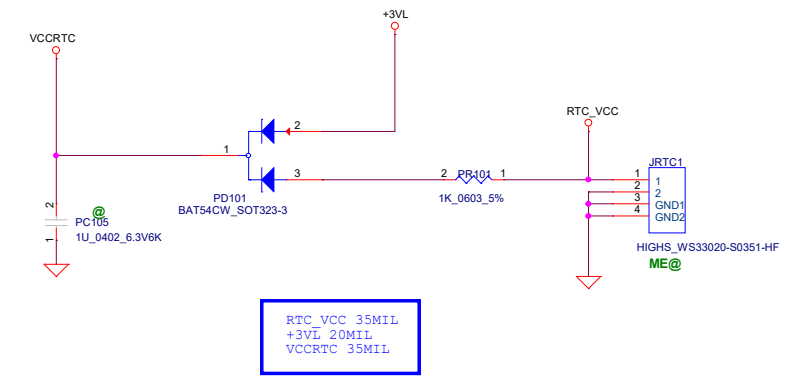
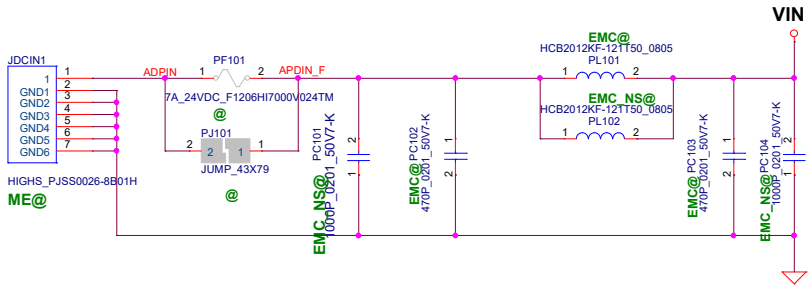




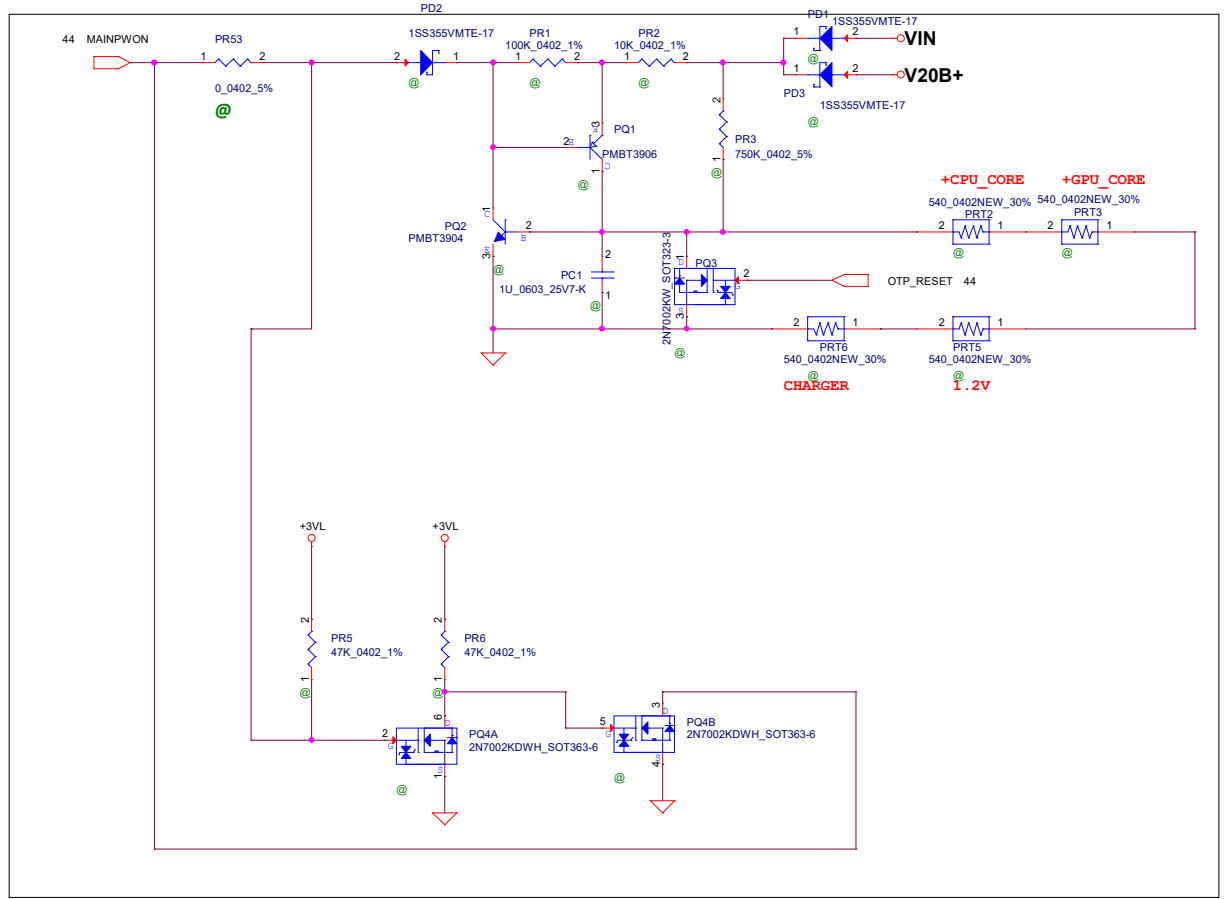
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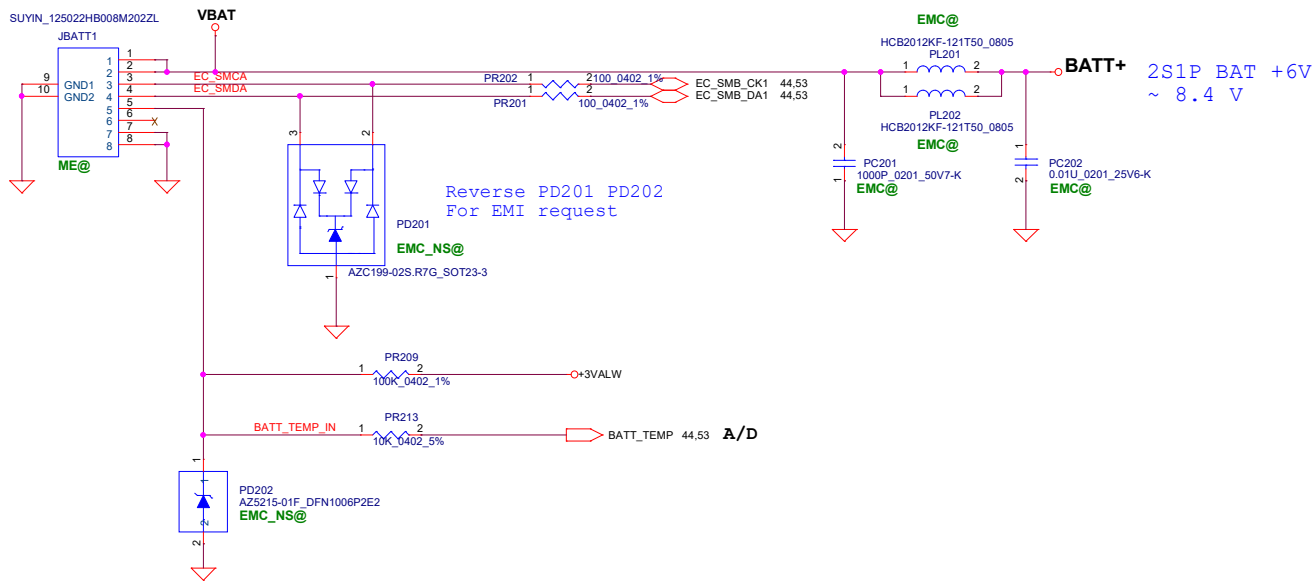
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Custom	<b>FS440/FS541</b>	0.2
Date:	Monday, November 05, 2018	Sheet 49 of 60



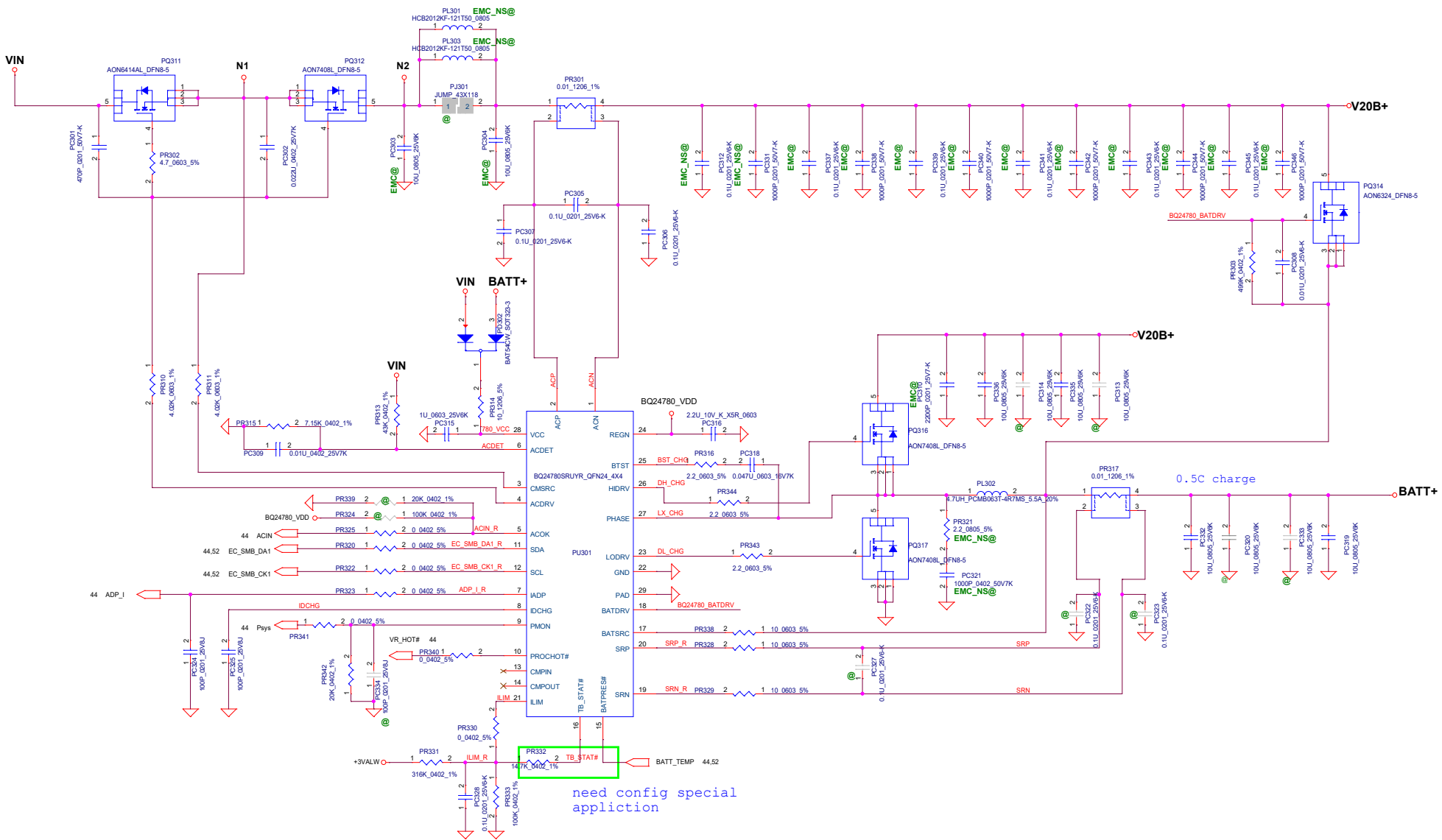


OTP

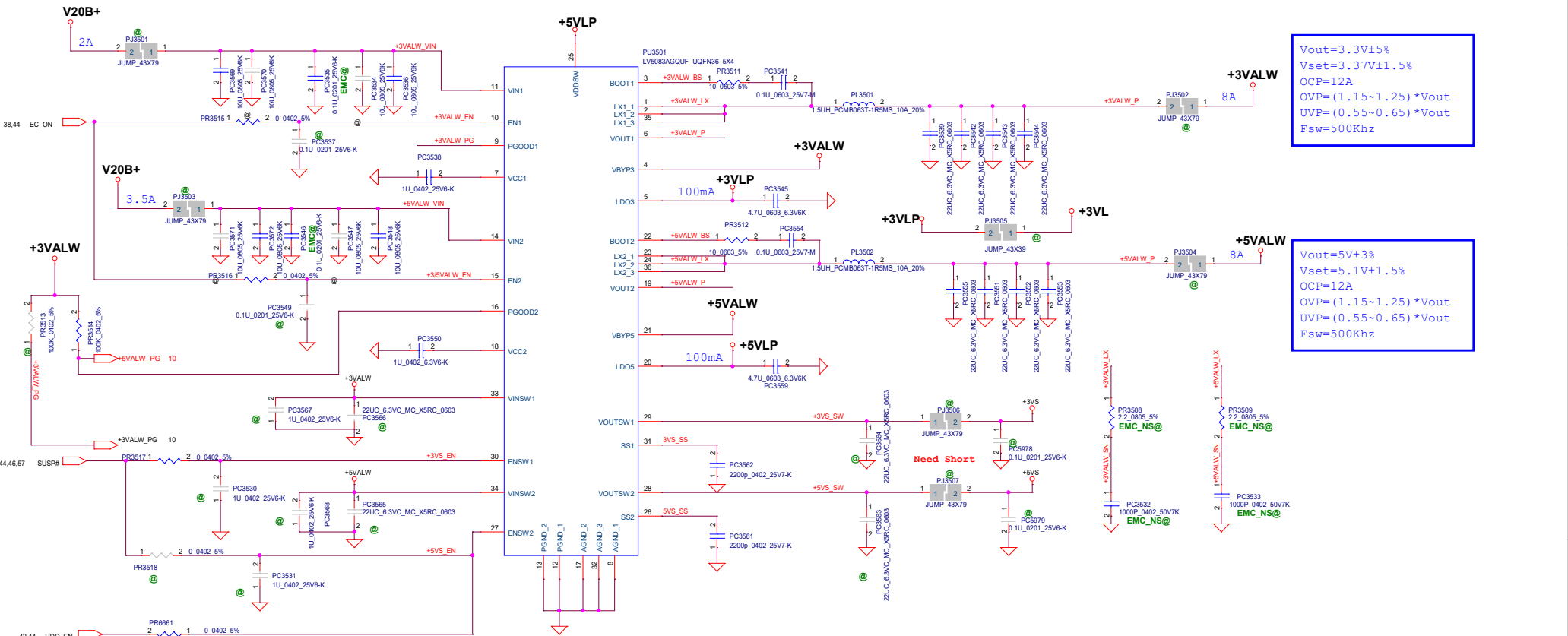




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Date:	Monday, November 05, 2018	Sheet	52	of	60

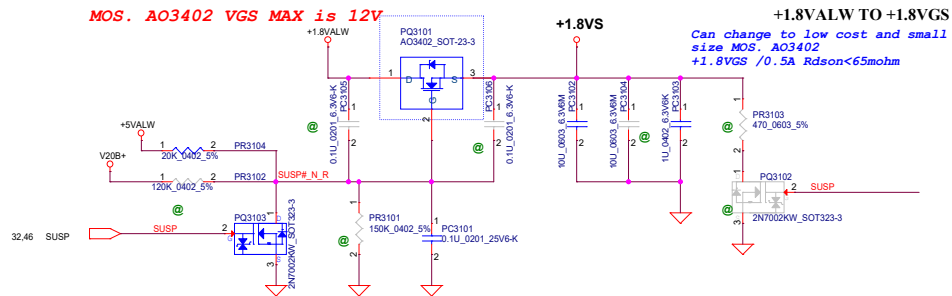


need config special application

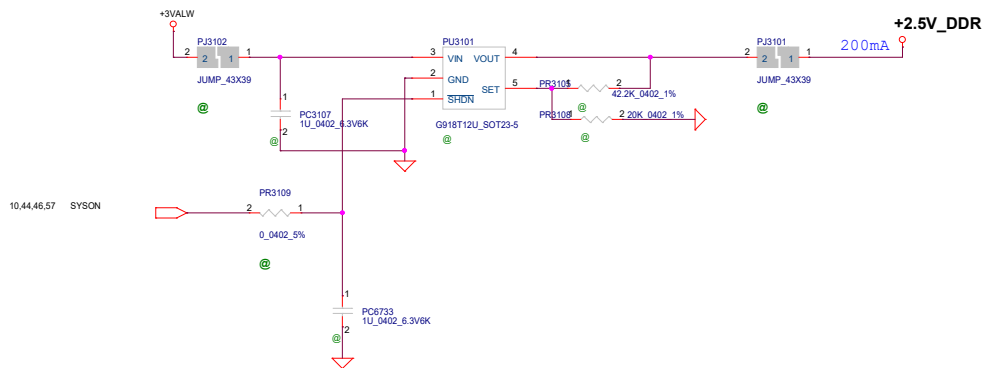


$V_{out} = 3.3V \pm 5\%$   
 $V_{set} = 3.37V \pm 1.5\%$   
 $OC = 12A$   
 $OVP = (1.15 \sim 1.25) * V_{out}$   
 $UVP = (0.55 \sim 0.65) * V_{out}$   
 $F_{sw} = 500Khz$


$V_{out} = 5V \pm 3\%$   
 $V_{set} = 5.1V \pm 1.5\%$   
 $OC = 12A$   
 $OVP = (1.15 \sim 1.25) * V_{out}$   
 $UVP = (0.55 \sim 0.65) * V_{out}$   
 $F_{sw} = 500Khz$



**RT5077A Test high temperature must add this solution**  
**SDV Must Add in bom**



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				Page 55 of 60	

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			<small>Document Number</small>	<b>FS440/FS541</b>
			<small>Date</small>	Monday, November 05, 2018
			<small>Sheet</small>	56 of 60





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Rev 0.2

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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR-+1.05VGS/+1.35V_VRA/CFC	
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				C	FS440/FS541
				Date:	Monday, November 15, 2016
				Sheet	59 of 60
				Rev	0.2

5

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20161216:SDV to SIT

- 1.p56-p57 add R=100ohm,C=680pF in FB pin;
- 2.pr3324 change to 55.4kohm,pr3323 change to 24.3k;
- 3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
- 4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
5. GPU change 14 items to support AMD request.

20161219:SDV to SIT


- 1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT

1. PMIC change 1.24V Vin from 3VALW to 1.8VALW;
- 2.change PR2431 from PX@ to @, PR2433 from @ to PX@,
- 3.change PR734 to @.

20170104:SDV to SIT

1. PMIC change LV5075B TO LV5075A

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Date: Monday, November 05, 2018				Sheet	60	of 60