LCFC Confidential

GS44B/GS54B/GS44C/GS54C MB Schematics Document

KBL-U22/U42 with DDR4 + Nvidia N16S-GTR/N17S-G1

2019-02

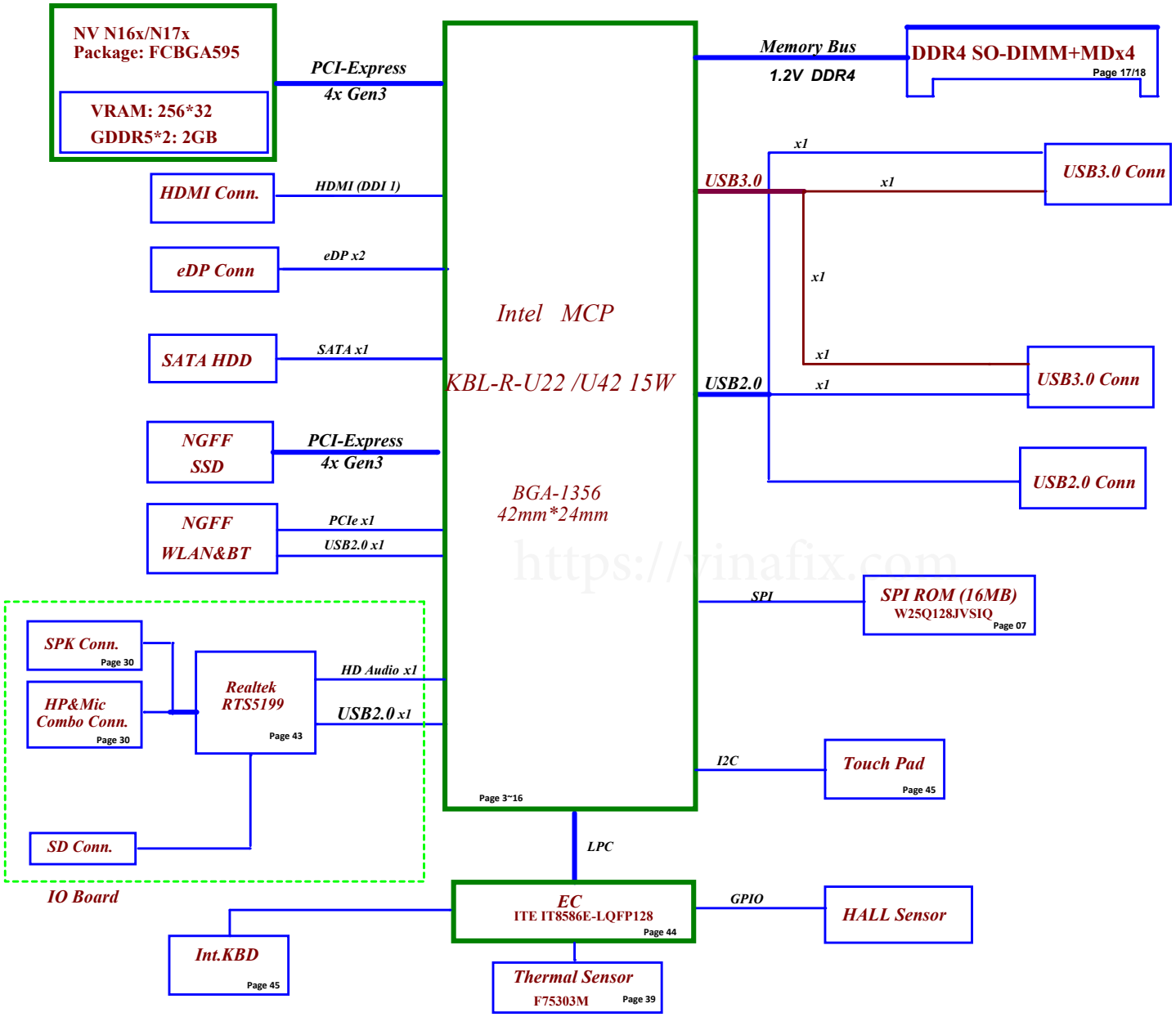
REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 1 of 60



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Title: **Block Diagram**

Size: Custom	Document Number: GS44B/GS54B	Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 2 of 61	

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn
	2	NC
	3	USB3.0 Conn
	4	USB2.0 conn
	5	Card reader
	6	Touch Screen
	7	Camera
	8	NC
	9	NC
	10	Bluetooth
PCIE	5~8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13~16 X4	PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530S part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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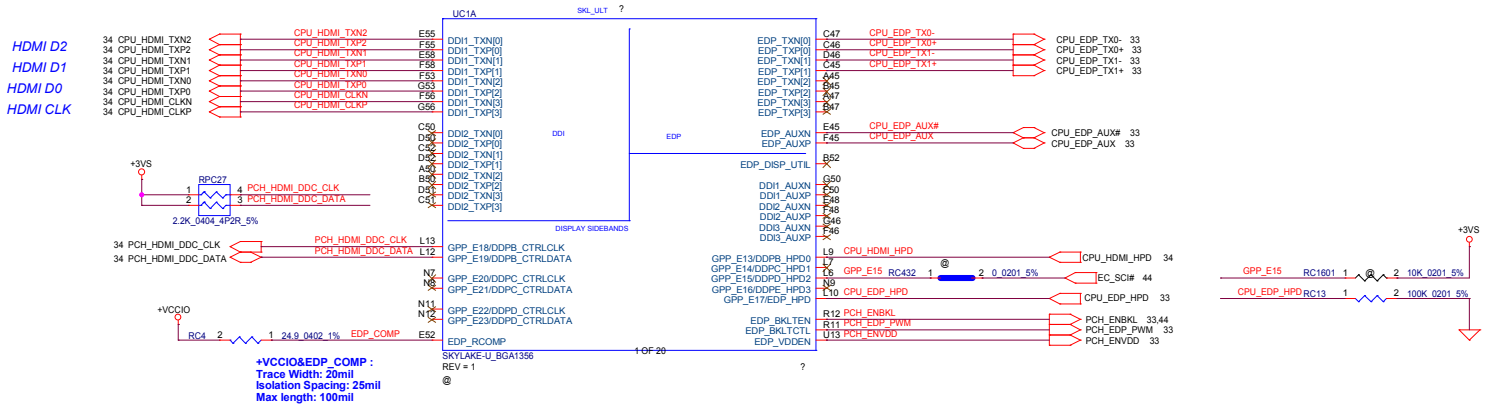
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Notes List**

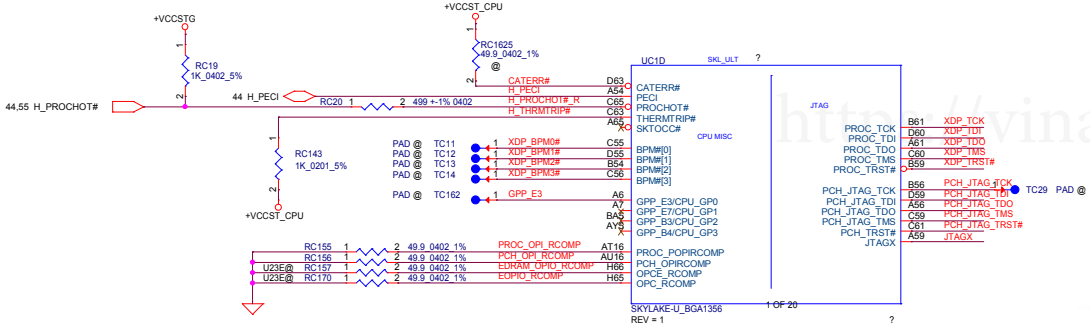
Size	Document Number	Rev
Custom	GS44B/GS54B	0.1

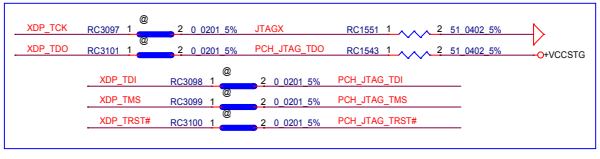
Date: Wednesday, May 29, 2019 Sheet 3 of 61

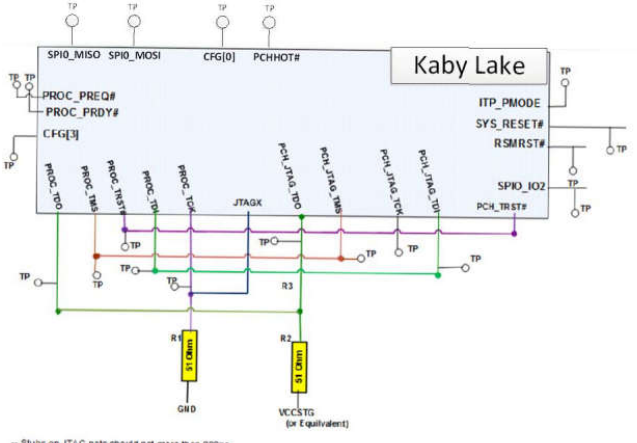


DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC







-- Stubs on JTAG nets should not more than 200ps
-- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
-- Place Test point pads on Secondary side
-- Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2
VCCDBS_AB (PCH V1.0 A), GND pins (2)
-- TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
-- TP = Test Point Pad (size - 16 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

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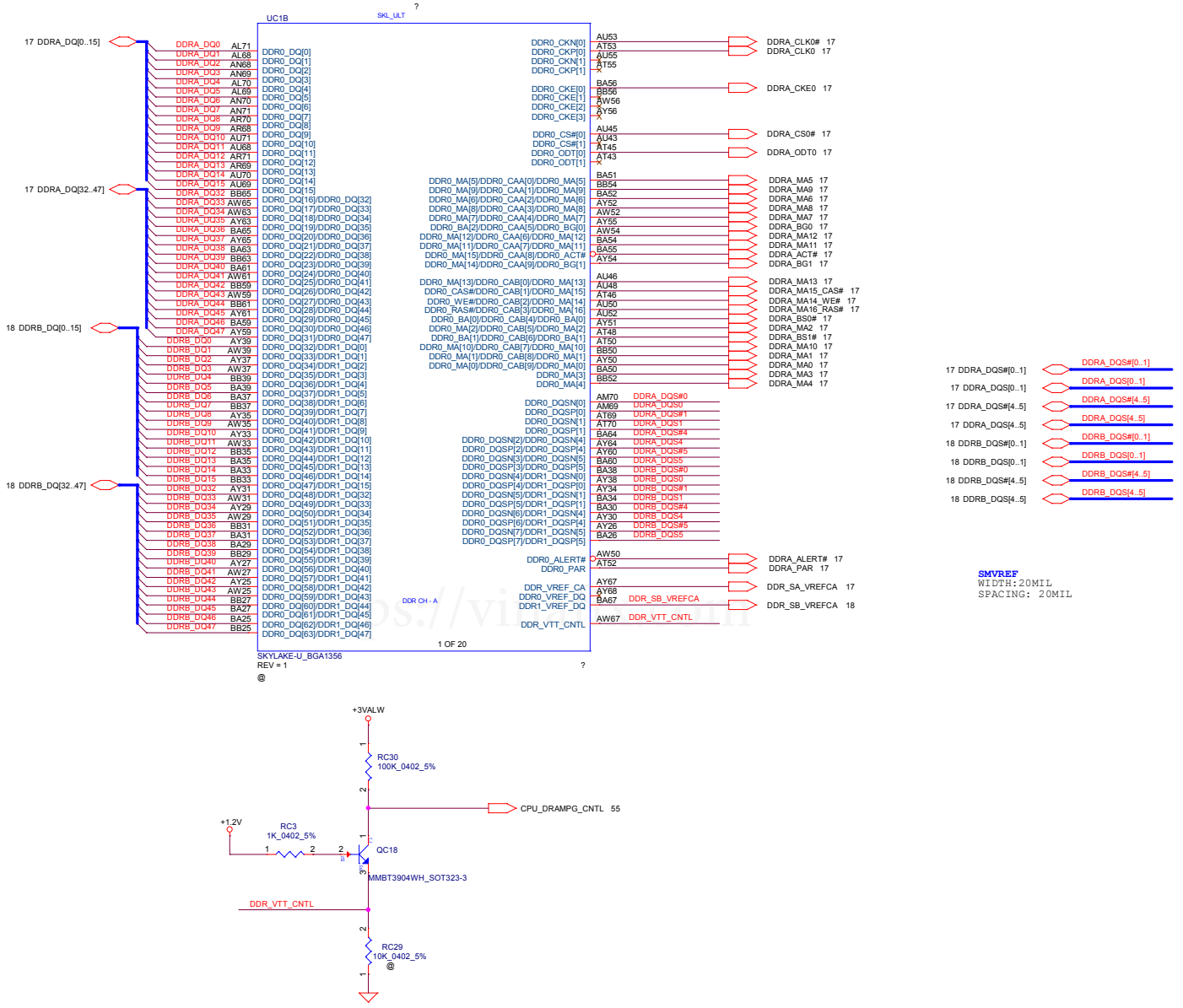
Title: **MCP (DDI,EDP)**

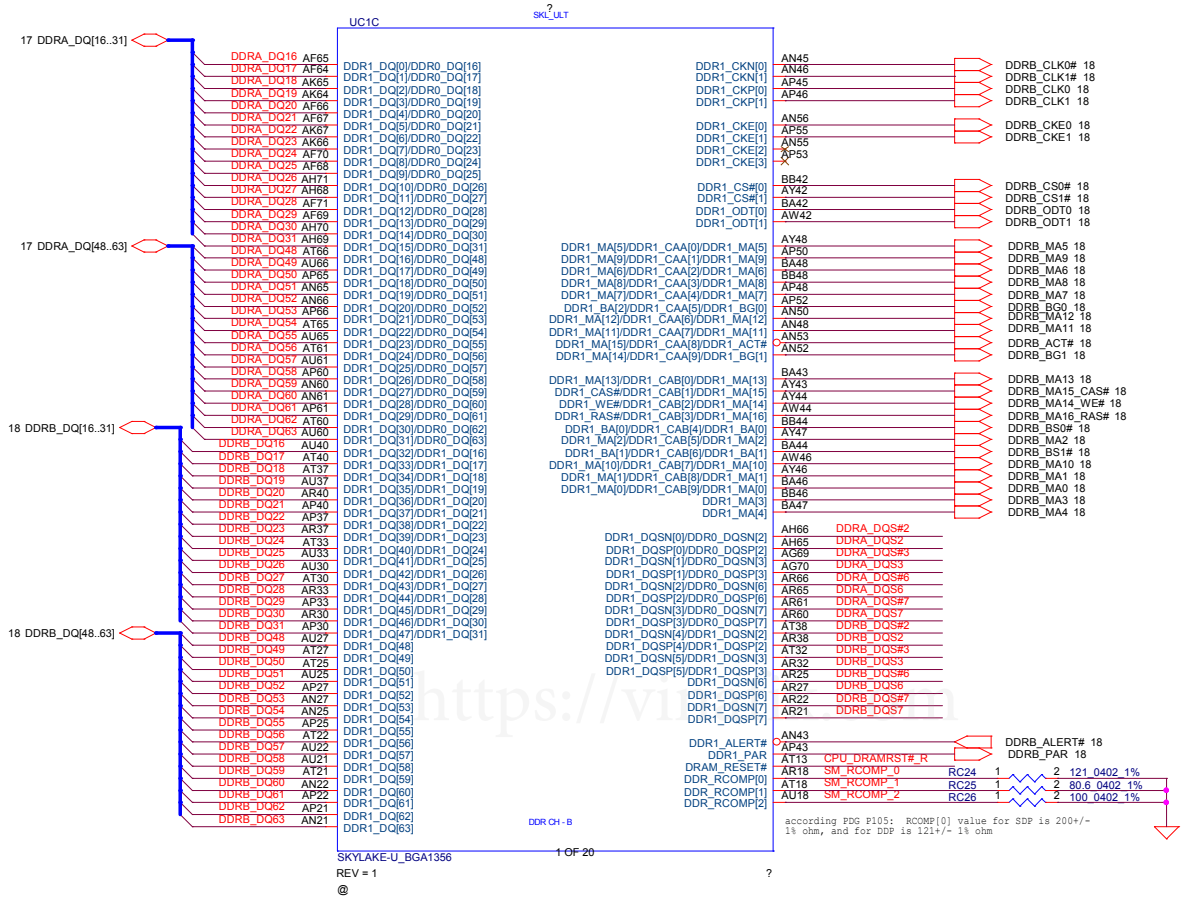
Size	Document Number	Rev
Custom	GS44B/GS54B	1.0
Date: Wednesday, May 29, 2019	Sheet 4 of 60	

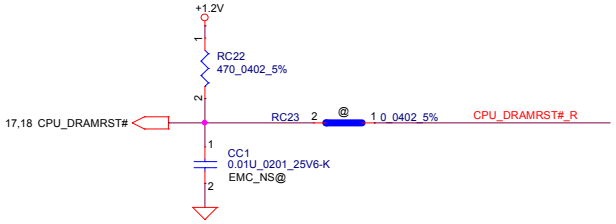


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0
Date: Wednesday, May 29, 2019	Sheet 5 of 60	



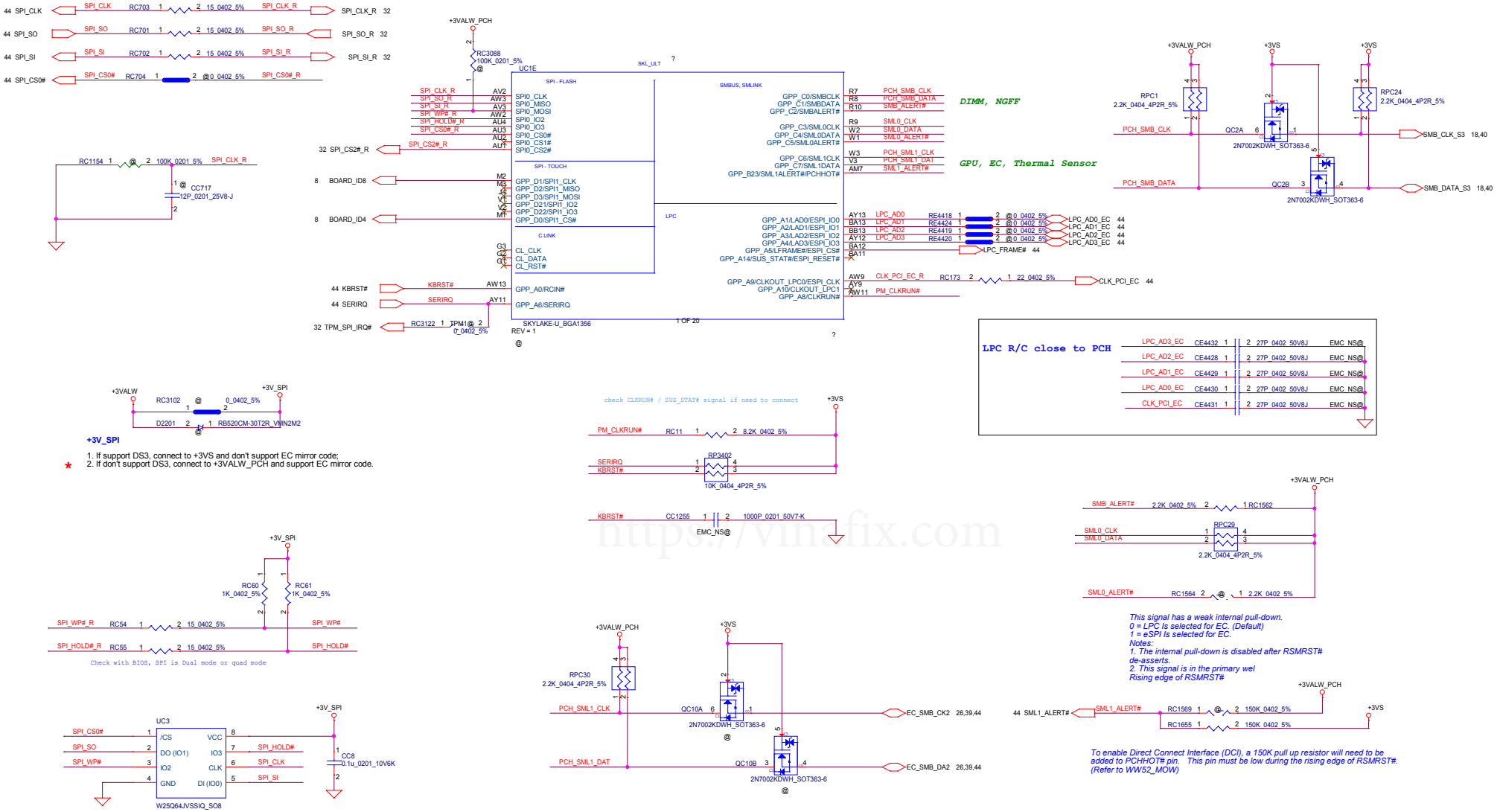


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (DDR4)

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 6 of 60



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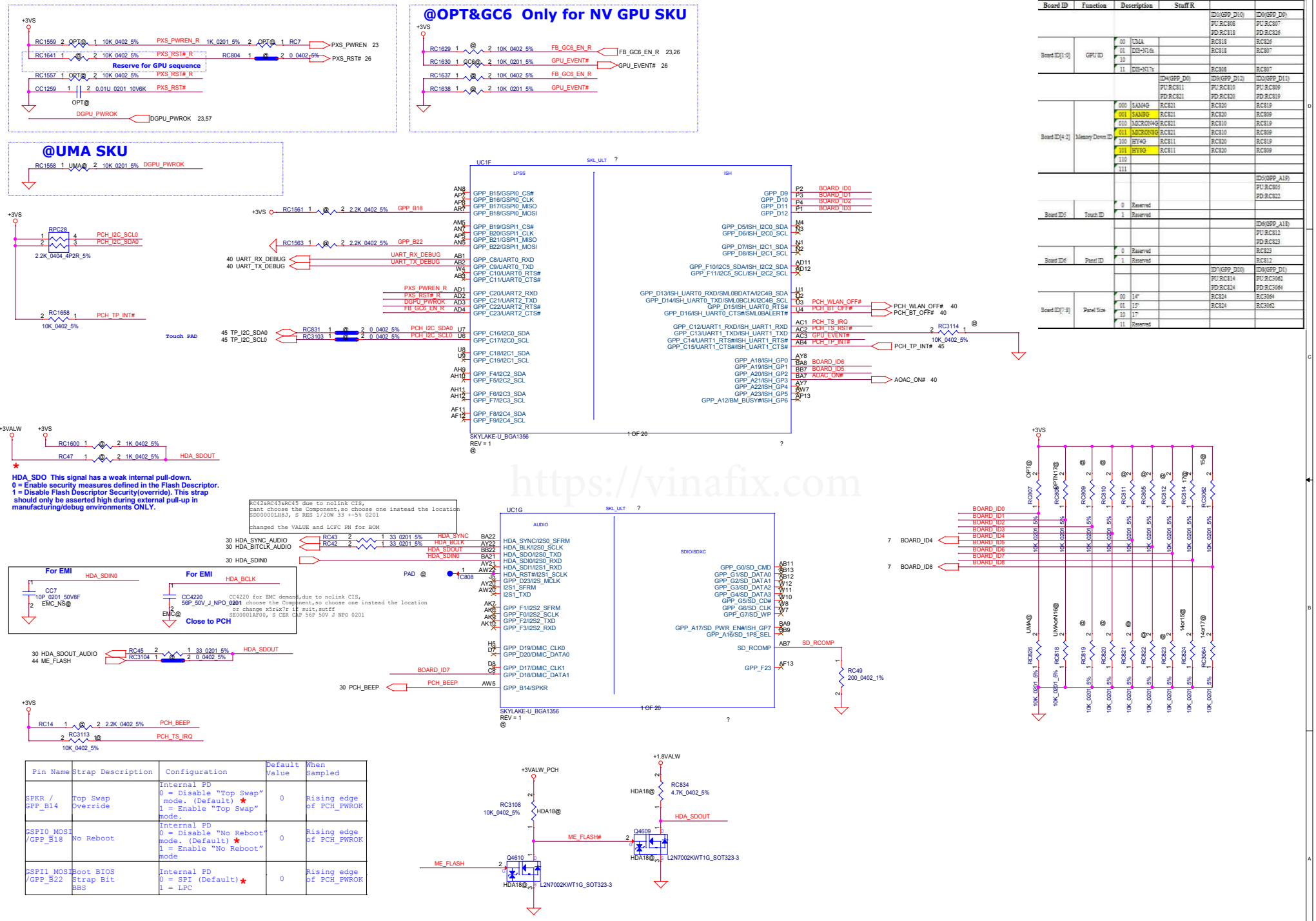
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	MCP (MISC,JTAG,SPI,LPC,SM		
Size	Document Number		Rev
C	GS44B/GS54B		1.0
Date:	Wednesday, May 29, 2019	Sheet	7 of 60



Board ID	Function	Description	Stuff R		
				ID1(GPP_D10)	ID0(GPP_D9)
				PU:RC808	PU:RC807
				PD:RC818	PD:RC826
Board ID[1:0]	GPU ID	00 UMA		RC818	RC826
		01 DIS-N16s		RC818	RC807
		10			
		11 DIS-N17s		RC808	RC807
			ID4(GPP_D8)	ID3(GPP_D12)	ID2(GPP_D11)
			PU:RC811	PU:RC810	PU:RC809
			PD:RC821	PD:RC820	PD:RC819
Board ID[4:2]	Memory Down ID	000 SAMG	RC821	RC820	RC819
		001 SAMG	RC821	RC820	RC809
		010 MICRON4G	RC821	RC810	RC819
		011 MICRON8G	RC821	RC810	RC809
		100 HY4G	RC811	RC820	RC819
		101 HY8G	RC811	RC820	RC809
		110			
		111			
					ID5(GPP_A19)
					PU:RC802
					PD:RC822
Board ID5	Touch ID	0 Reserved			
		1 Reserved			
					ID6(GPP_A18)
					PU:RC813
					PD:RC823
Board ID6	Panel ID	0 Reserved			RC832
		1 Reserved			RC812
				ID7(GPP_D20)	ID8(GPP_D1)
				PU:RC814	PU:RC5062
				PD:RC824	PD:RC5064
Board ID[7:8]	Panel Size	00 14"		RC824	RC5064
		01 15"		RC824	RC5062
		10 17"			
		11 Reserved			

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

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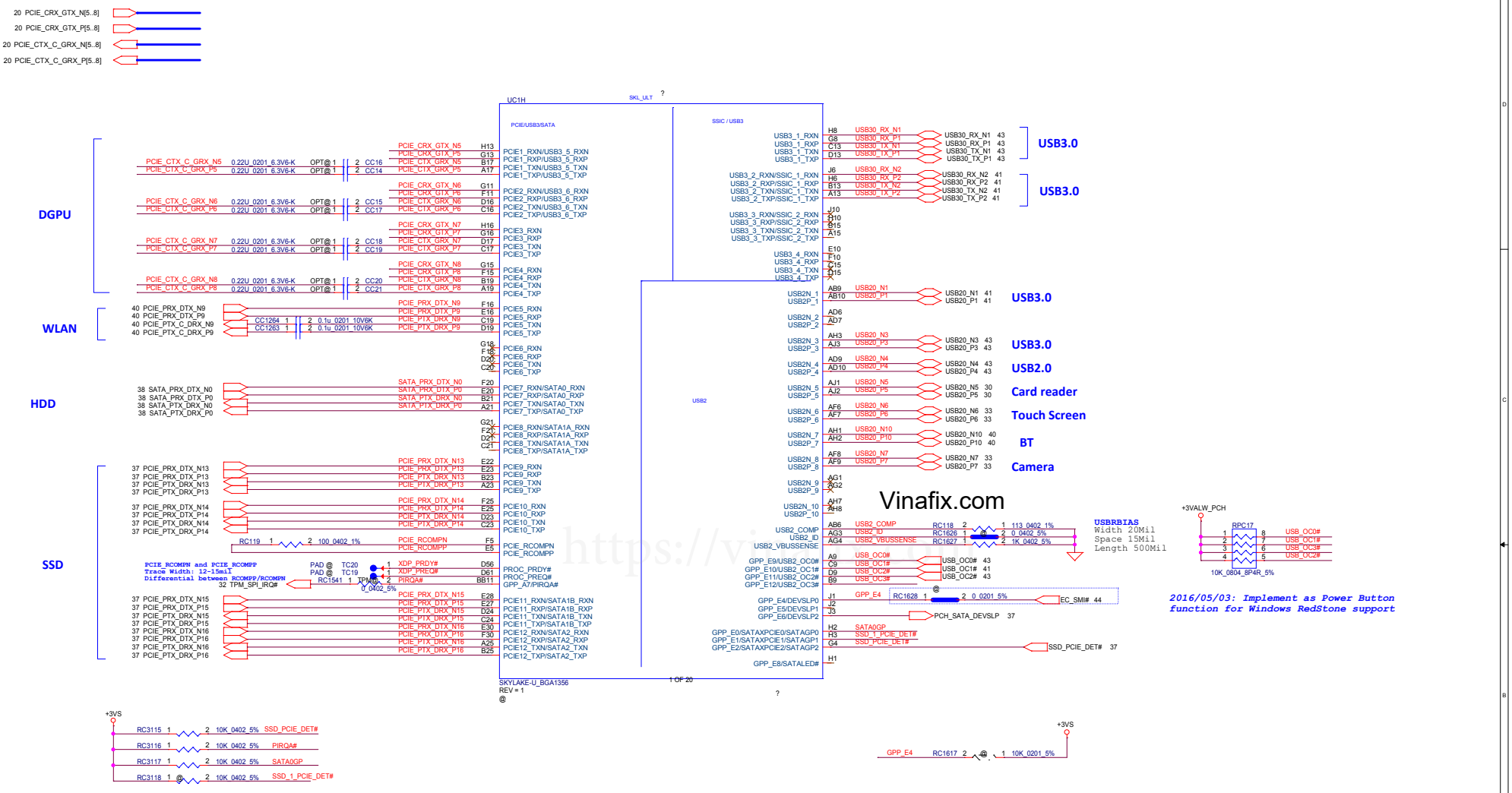
Title: MCP (LPSS,ISH,AUDIO,SDI

Size	Document Number	Rev
C	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 8 of 60



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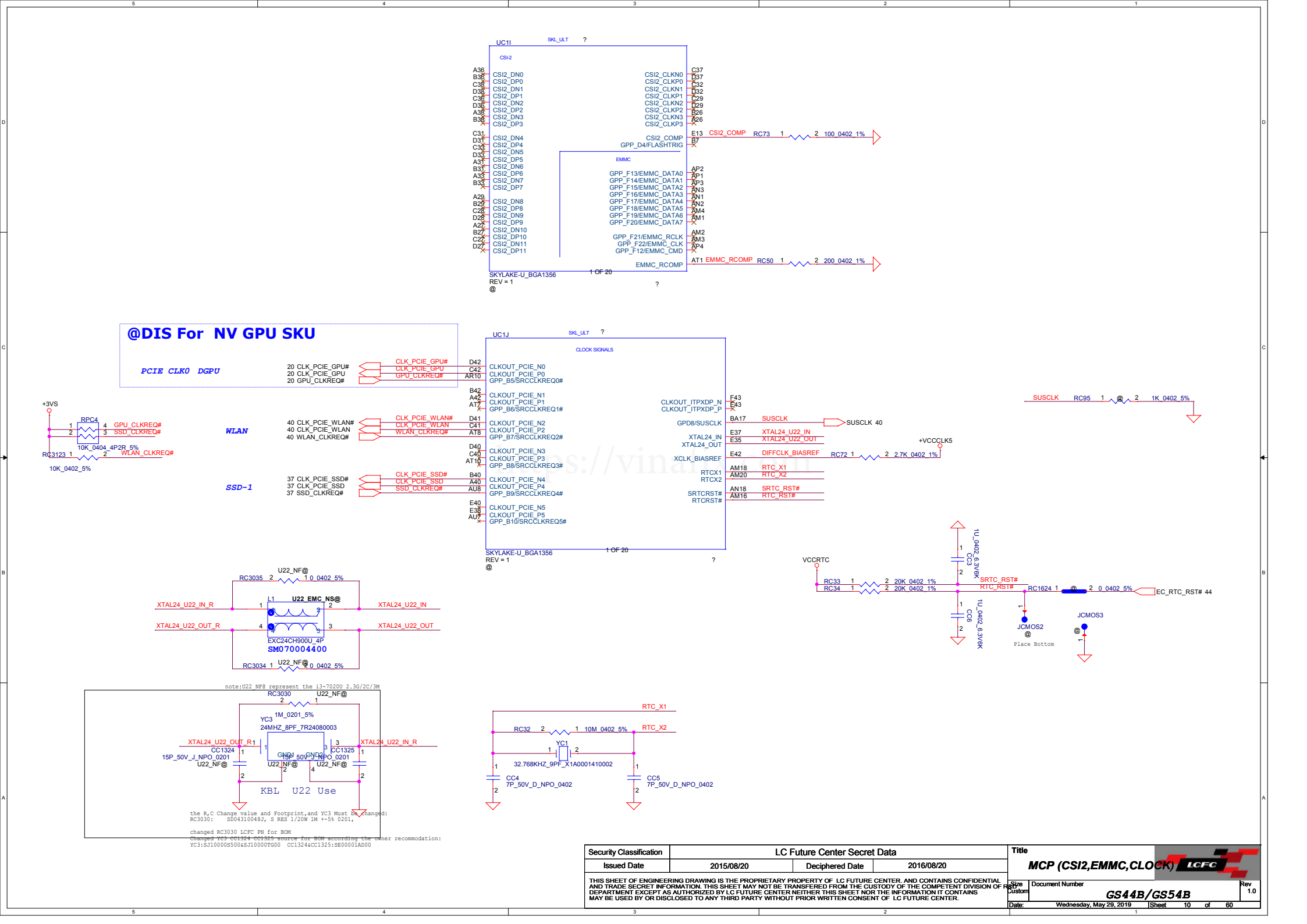
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (PCIE,SATA,USB3,USB2)

Size	Document Number	Rev
C	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 9 of 60



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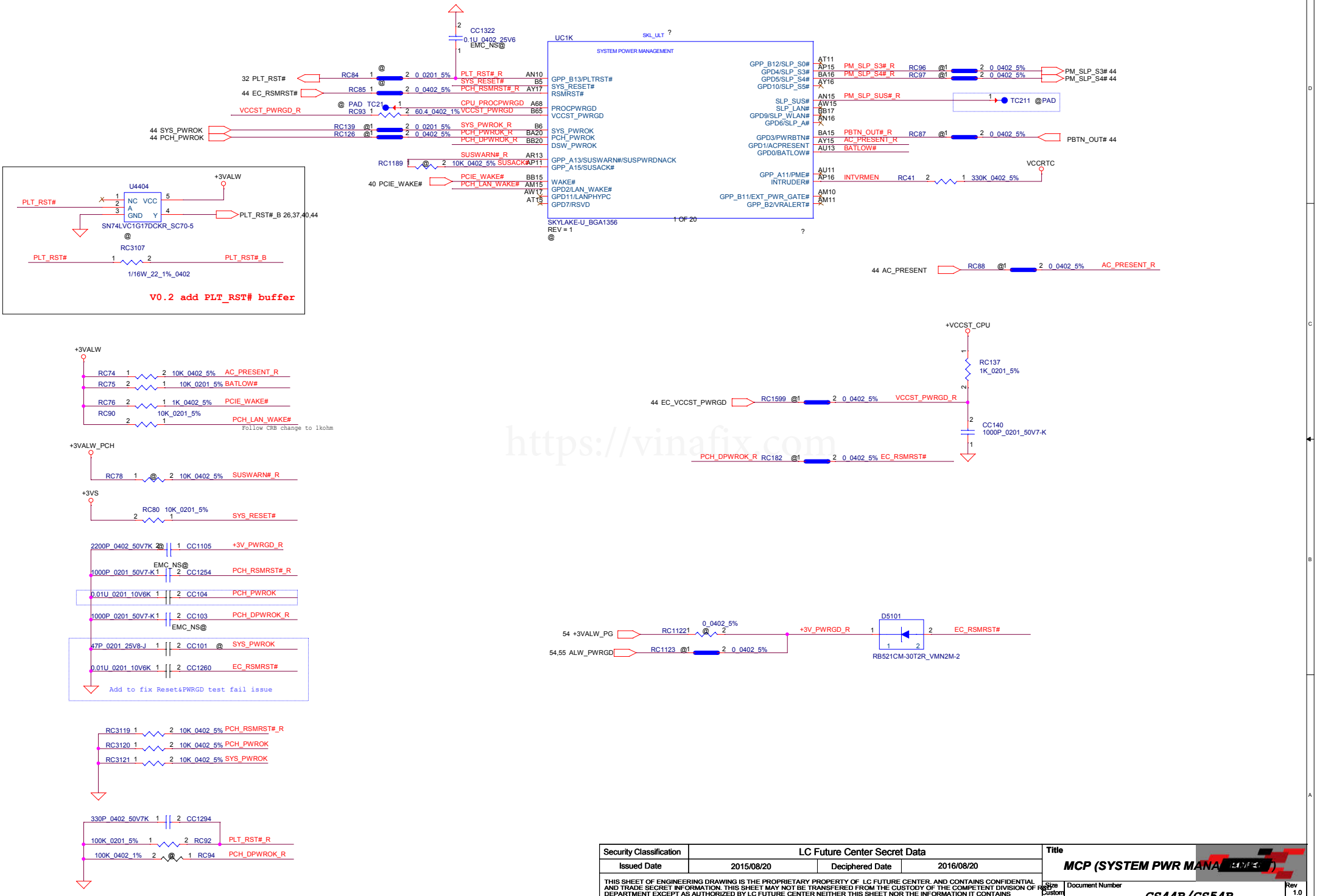
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (CSI2,EMMC,CLOCK)

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 10 of 60



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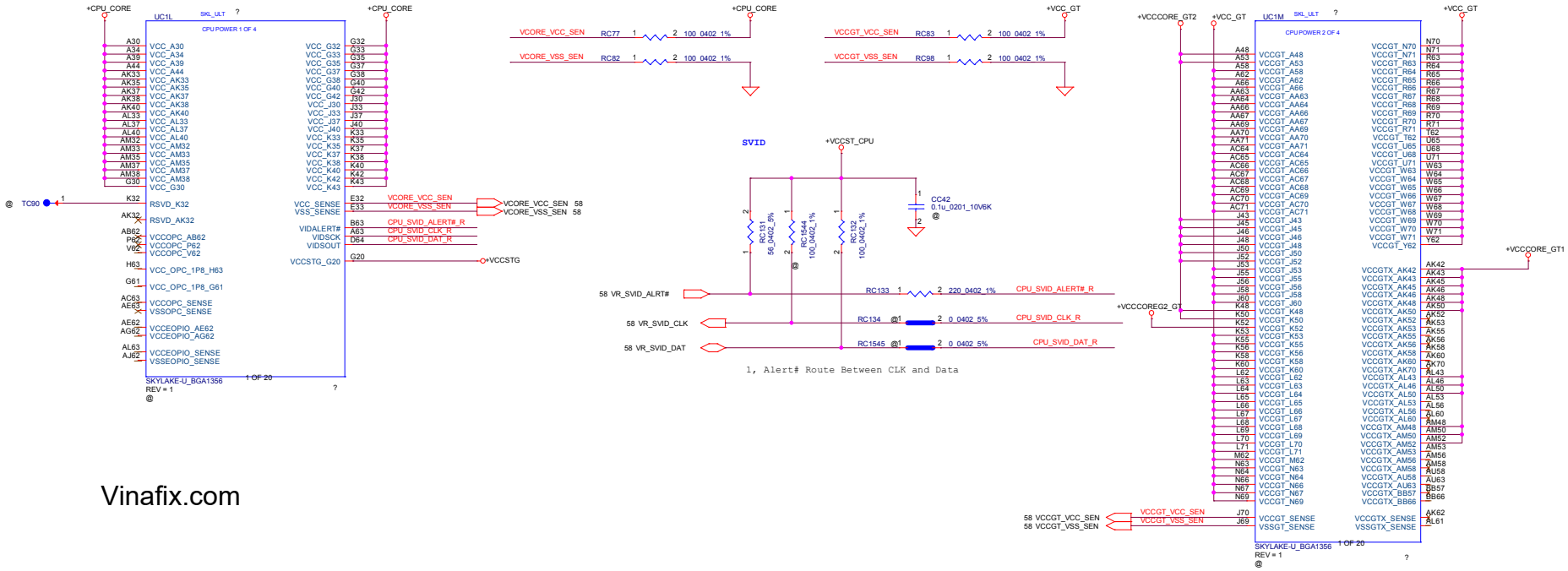
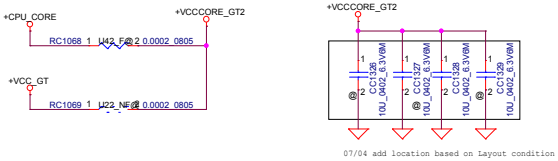
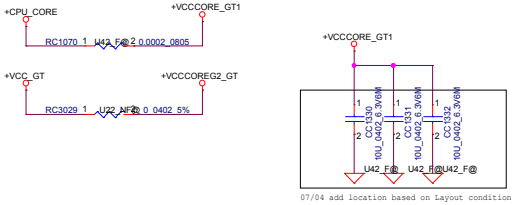
Title: MCP (SYSTEM PWR MANAGEMENT)

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 11 of 60

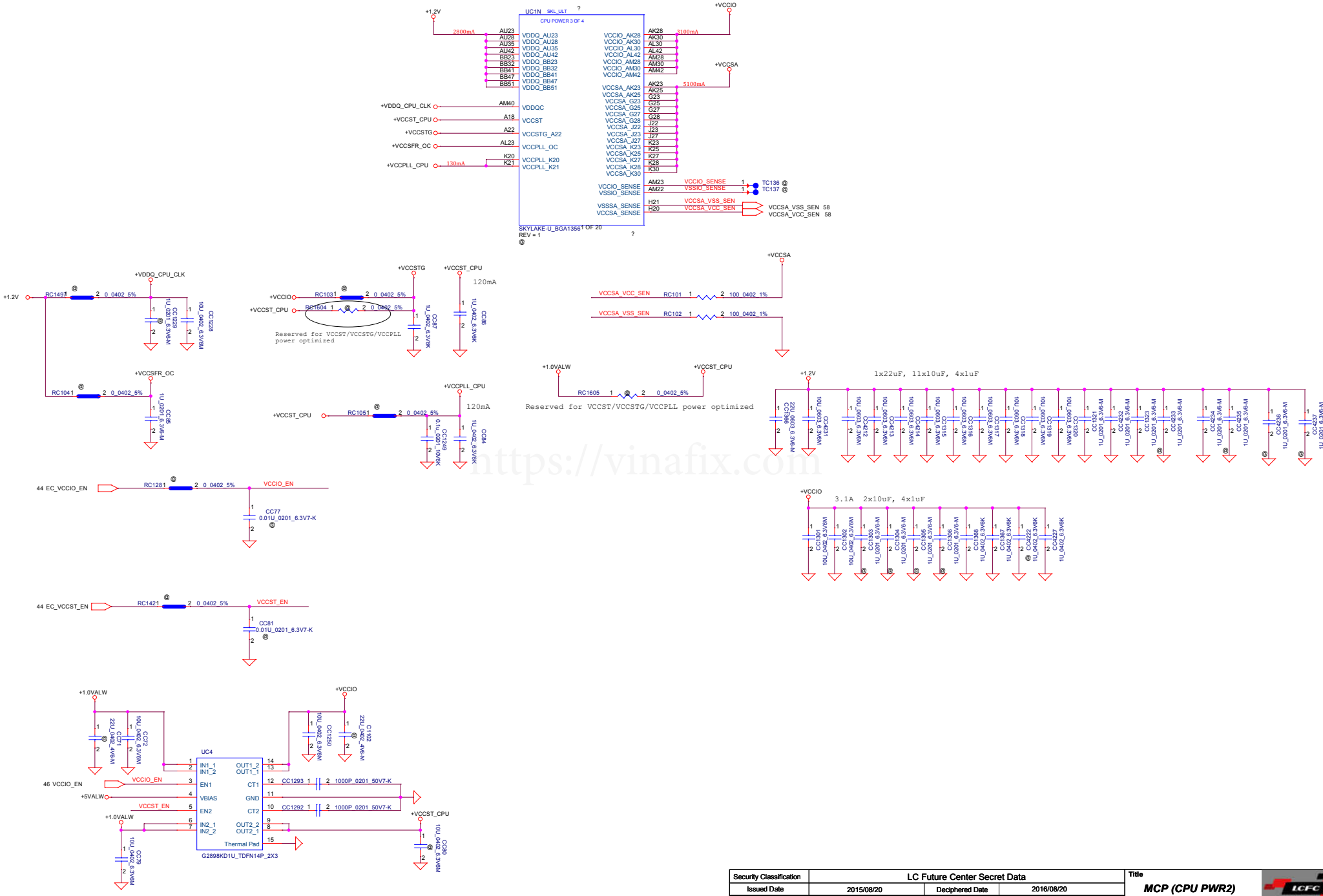






Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title	MCP (CPU PWR1)		
Size: Custom	Document Number: GS44B/GS54B		Rev: 1.0
Date: Wednesday, May 29, 2019	Sheet 12 of 60		

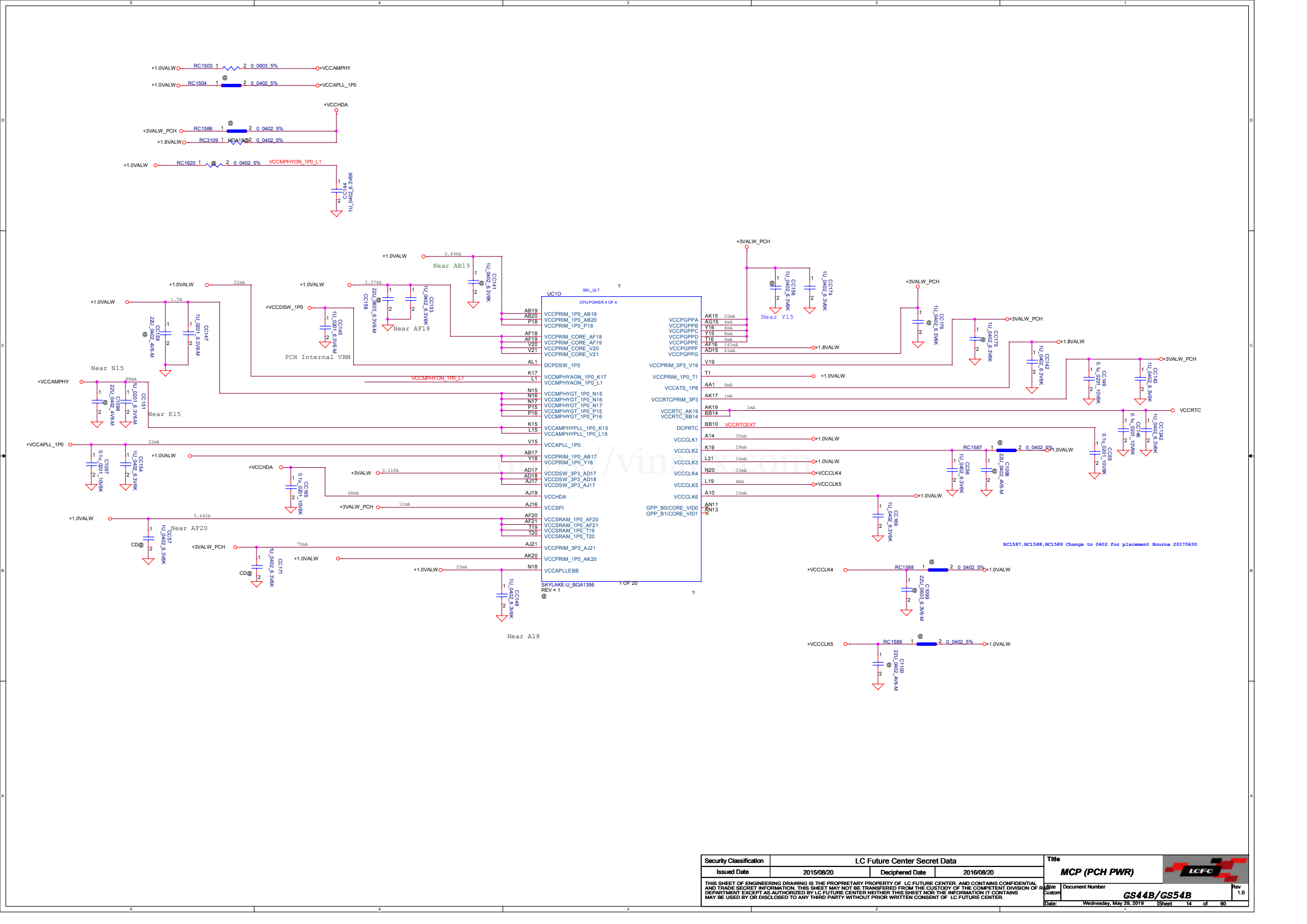


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (CPU PWR2)**

Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

Date: Wednesday, May 29, 2019 Sheet 13 of 60



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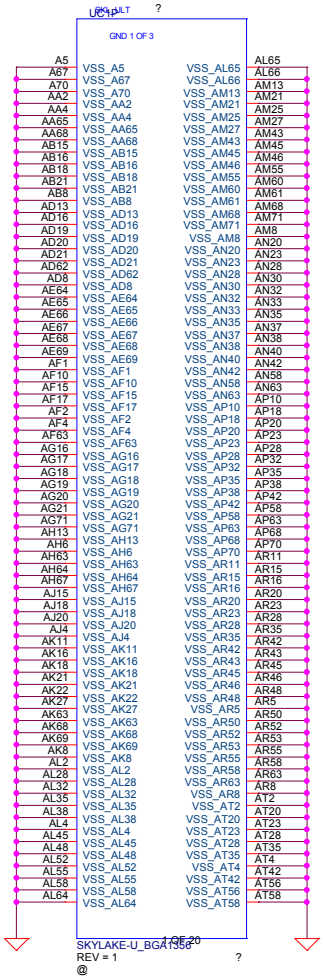
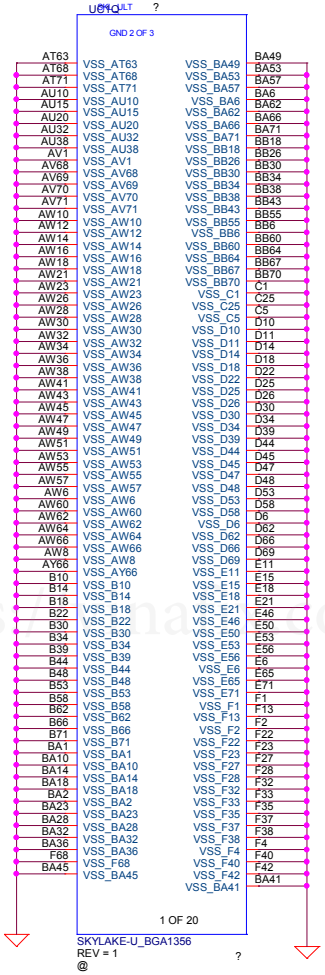
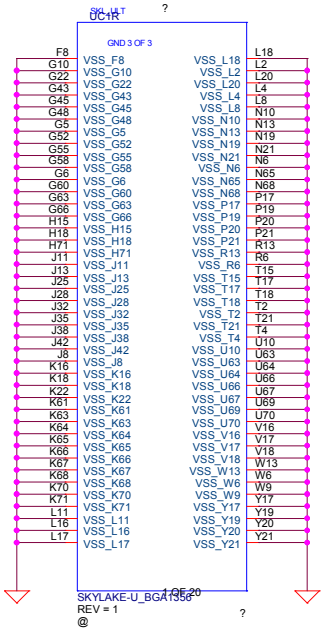
Title: MCP (PCH PWR)

Size: Custom	Document Number: GS44B/GS54B	Rev: 1.0
Date: Wednesday, May 29, 2019	Sheet 14 of 60	







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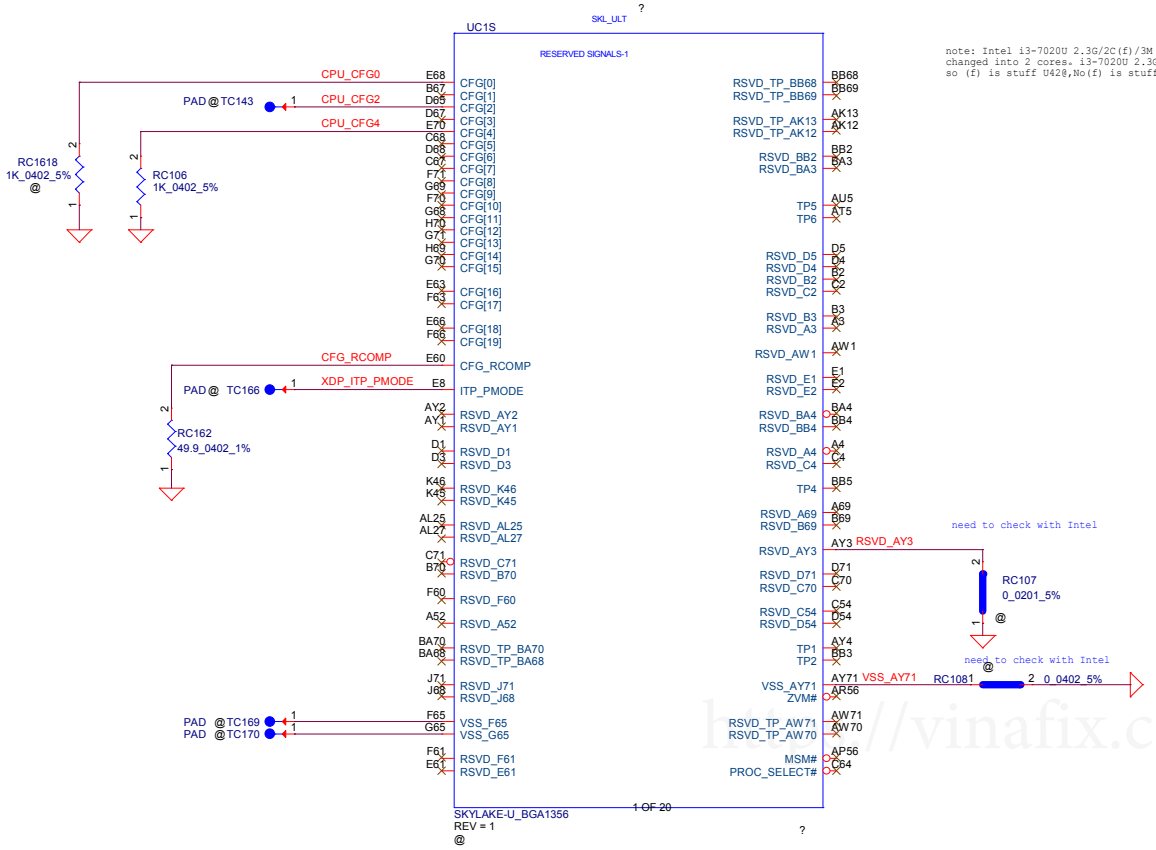
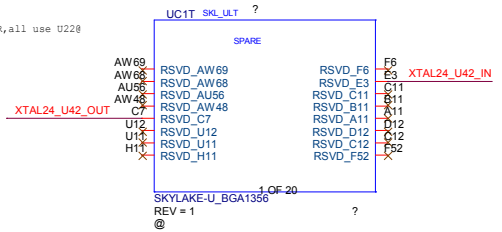
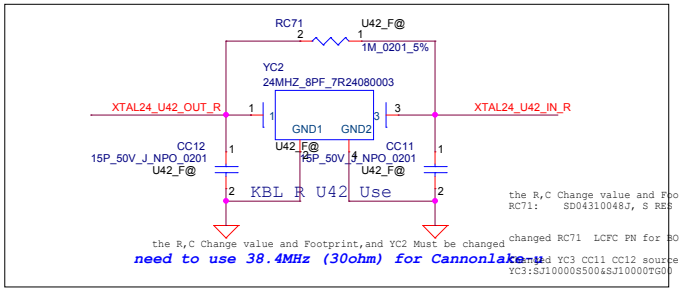
Title: **MCP (VSS)**

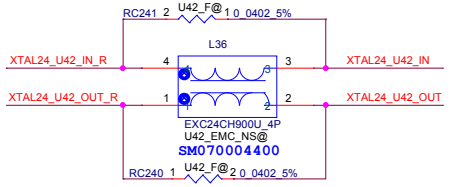
Size: Custom	Document Number: GS44B/GS54B	Rev: 1.0
Date: Wednesday, May 29, 2019	Sheet 15 of 60	



note: Intel i3-7020U 2.3G/2C(f)/3M is 4 Cores original and changed into 2 cores. i3-7020U 2.3G/2C/3M is 2 cores. so (f) is stuff U42@,No(f) is stuff U22. and power use 1 VR,all use U22@







L36 Co-layer w/ RC241,RC240

Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	–1 = eDP Disabled –0 = eDP Enabled ★	1

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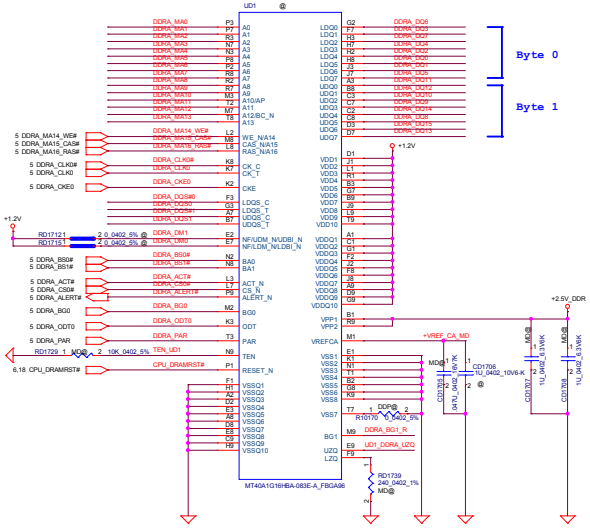
Issued Date	2015/08/20	Deciphered Date	2016/08/20

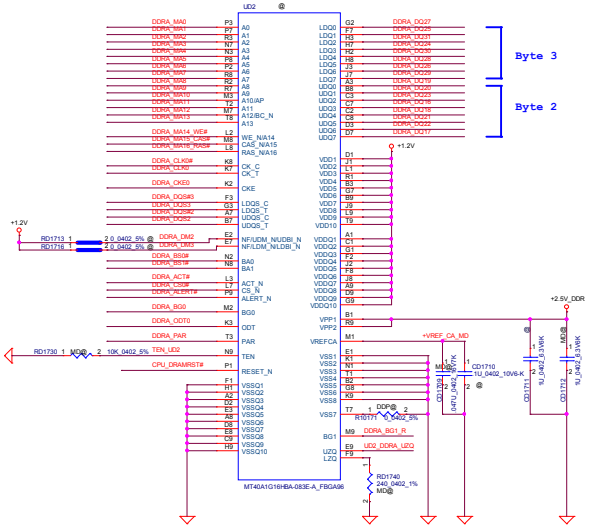
Title: **MCP (CFG,RESERVED)**

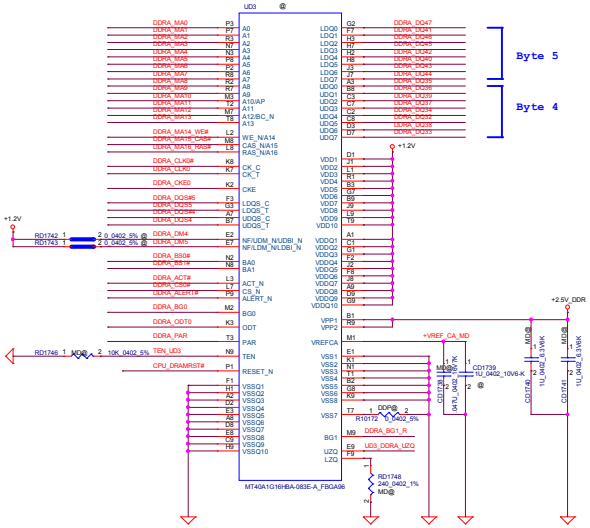
Size	Document Number	Rev
Custom	GS44B/GS54B	1.0

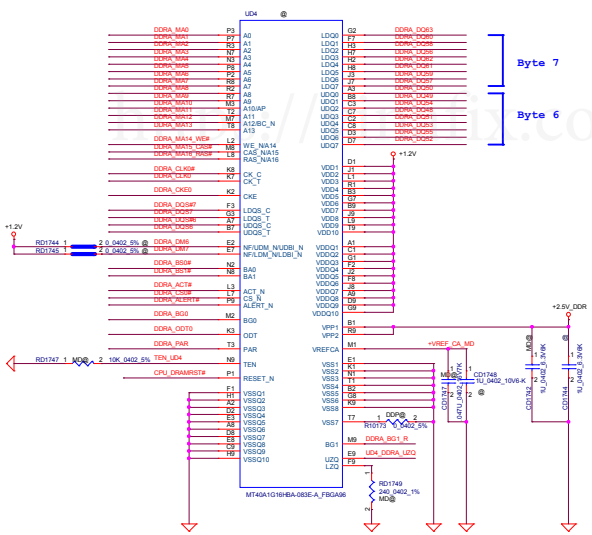
Date: Wednesday, May 29, 2019 Sheet 16 of 60

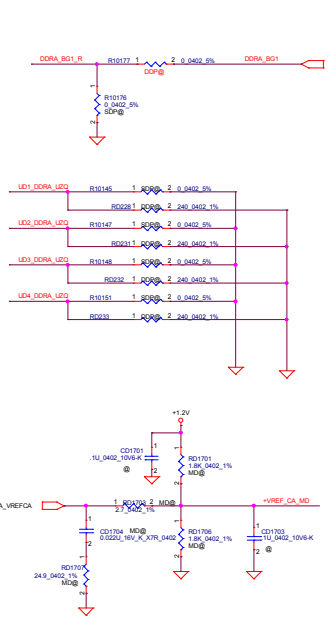
Apply X76 BOM to control DDP Memory Down stuff components!



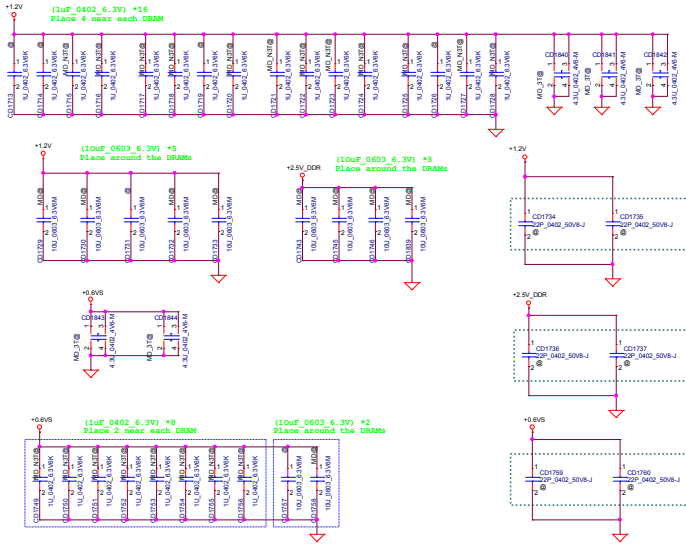








The ALERT signal must be routed in the opposite direction to the address/command bus.
For example, the alert signal must first connect to the last device that the address/command bus is connected to.



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Title: DDR4 Memory Down

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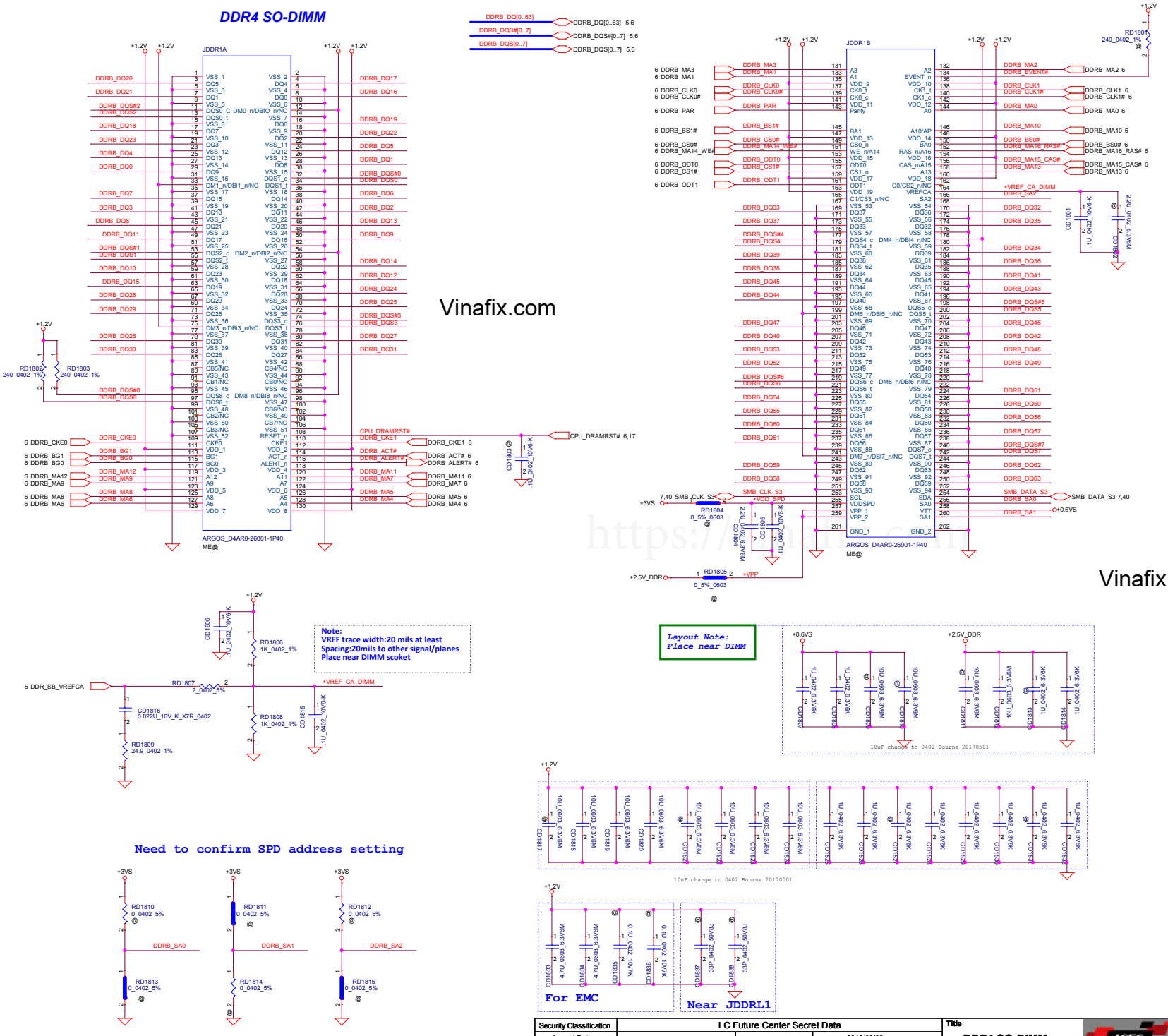
Date: Wednesday, May 29, 2019 | Sheet 17 of 61

DDR4 SO-DIMM



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: DDR4 SO-DIMM

Size: Custom | Document Number: GS44B/GS54B | Rev: 0.1

Date: Wednesday, May 29, 2019 | Sheet 18 of 61

N16x GPIO

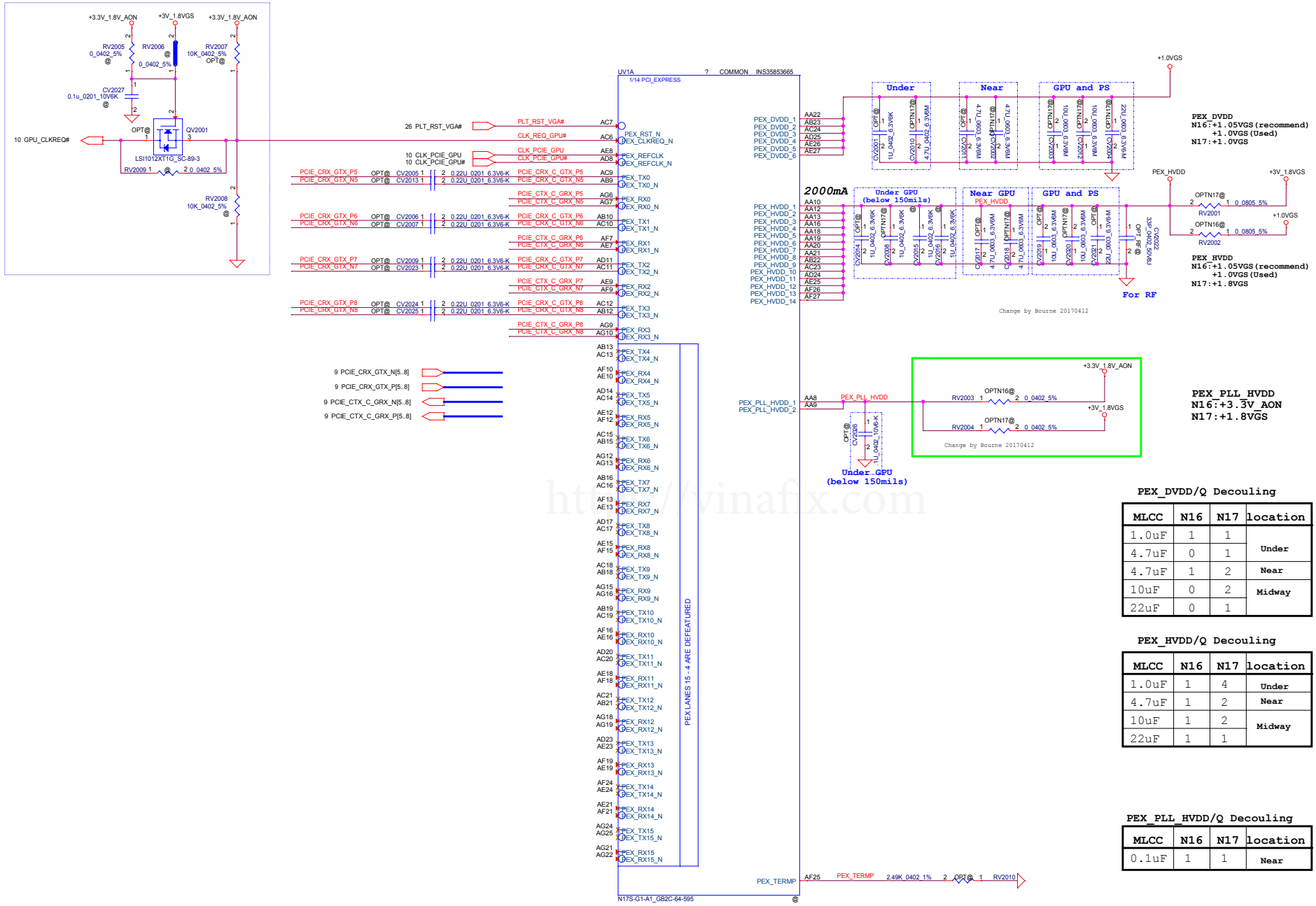
GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				



PEX_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	Near
10uF	0	2	Midway
22uF	0	1	

PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

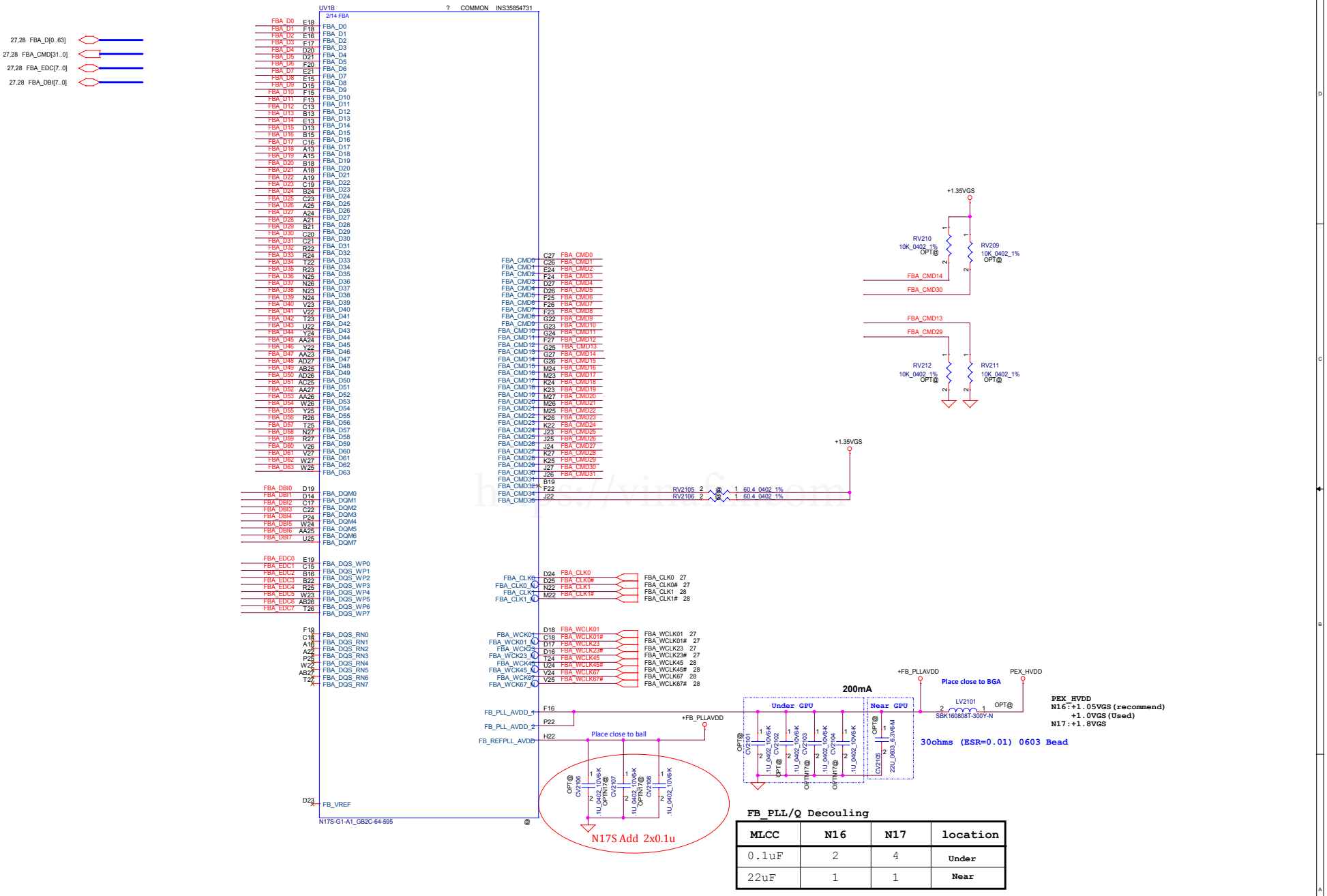
MLCC	N16	N17	location
0.1uF	1	1	Near

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_PCIE Interface**

Size: C | Document Number: **GS44B/GS54B** | Rev: 0.1

Date: Wednesday, May 29, 2019 | Sheet 20 of 61



FB_PLL/Q Decoupling

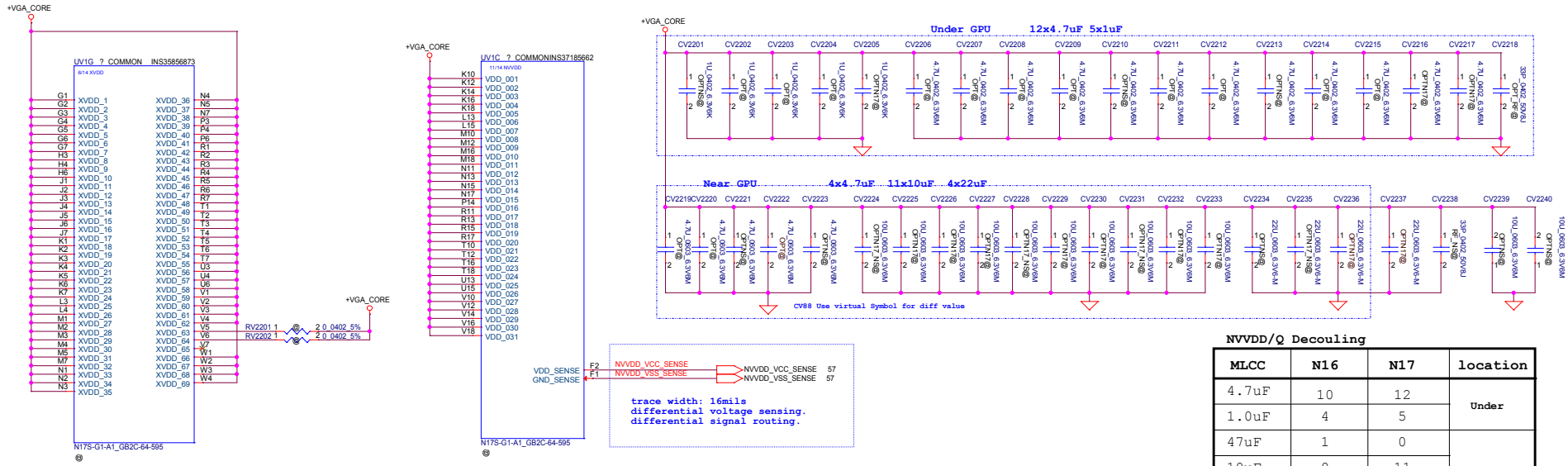
MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_MEM Interface**

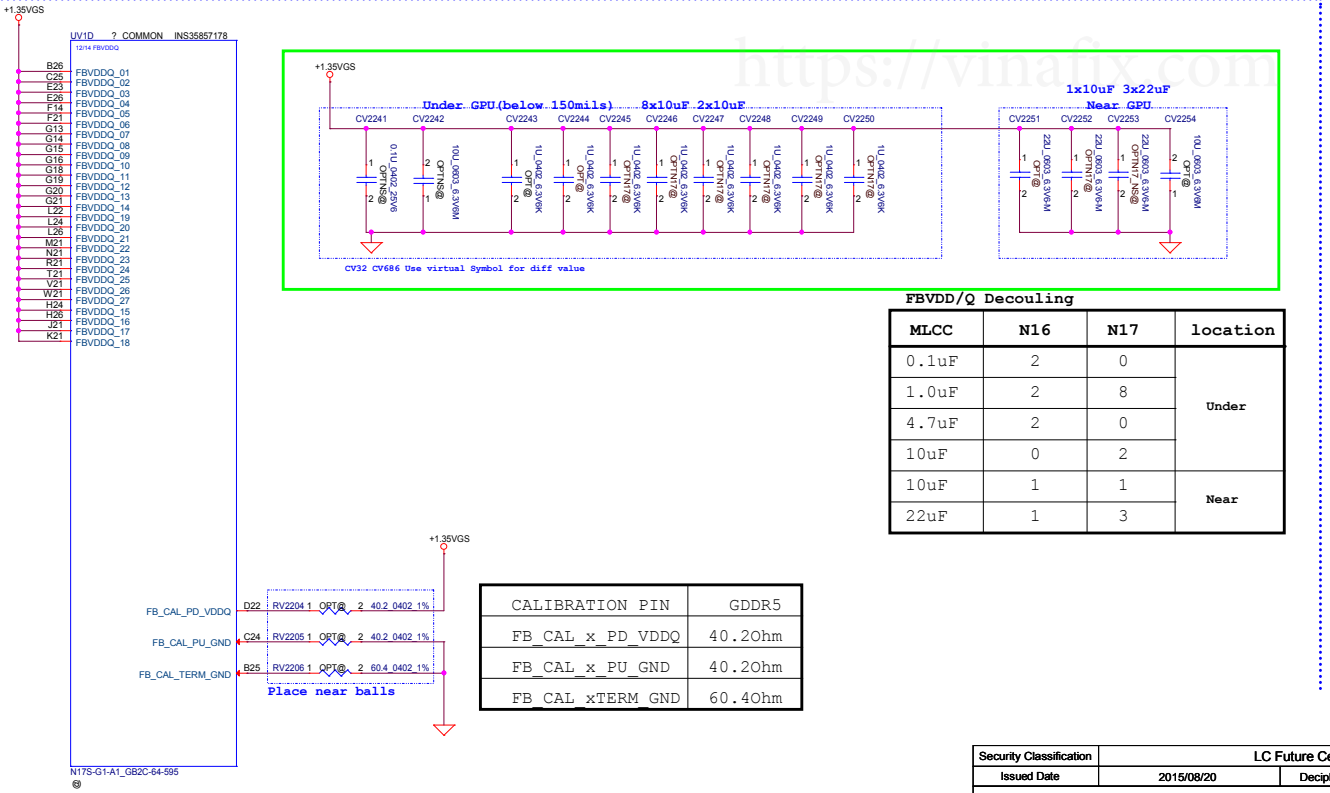
Size	Document Number	Rev
C	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 21 of 61



NVVDD/Q Decoupling

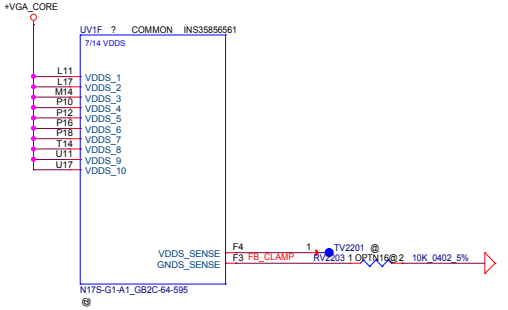
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

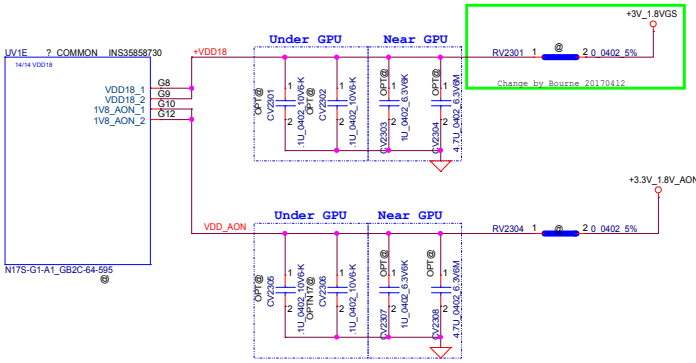


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_+VGA_CORE,FBVDDQ

Size	Document Number	Rev
C	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 22 of 61



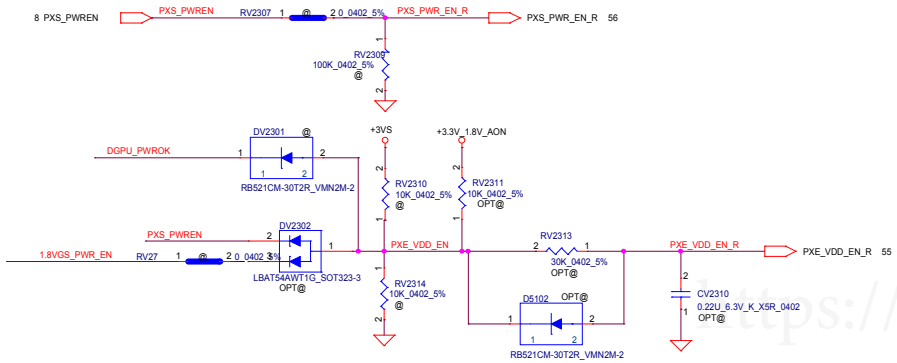
N16 3V3_MAIN(N17 VDD_18) Decouling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

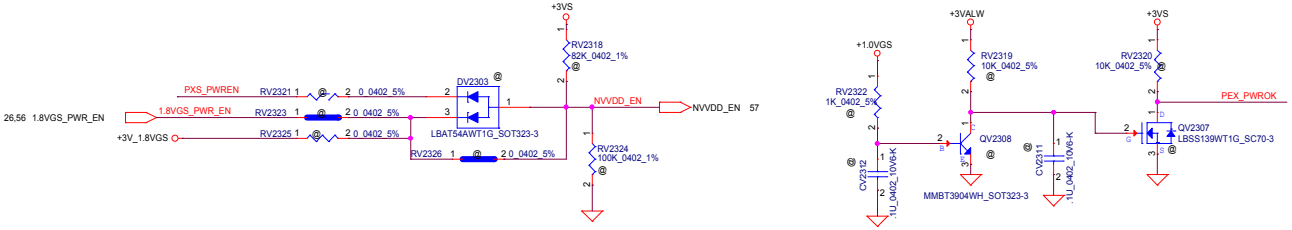
N16 3V3_AON(N17 1V8_AON) Decouling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

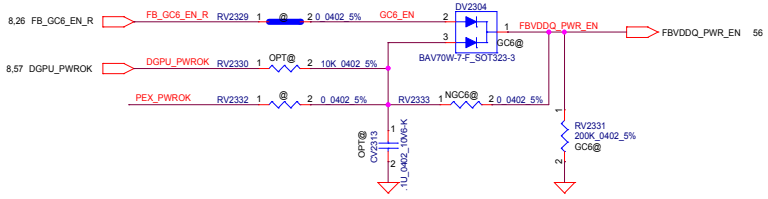
PXE_VDD & 1V8_AON



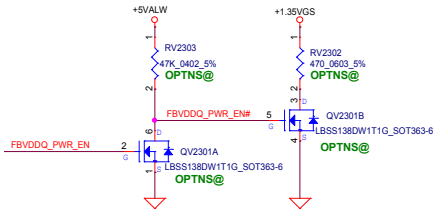
+1.8VG_AON TO +1.8VGS

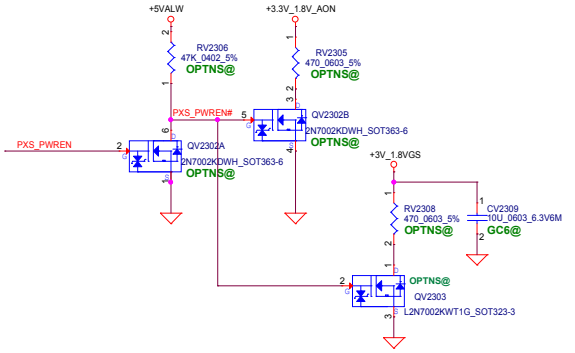


Vinafix.com

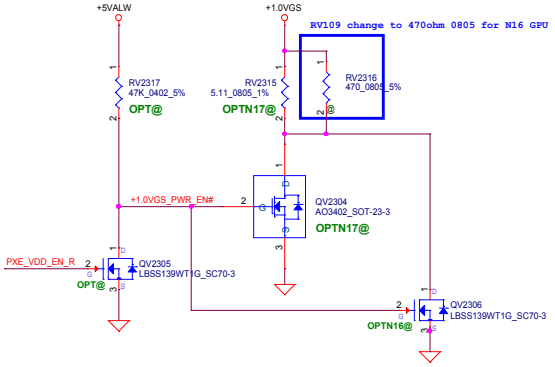


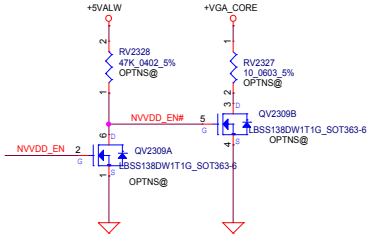
Discharge





RV2316 建虚拟料号,N16=470 ohm,N17=5.11 ohm



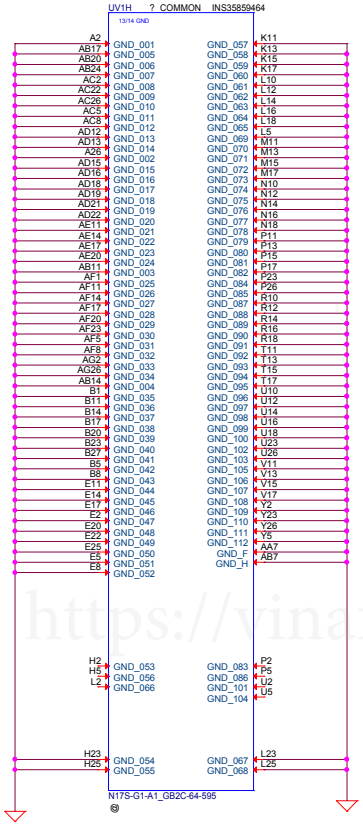


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_AON/MAIN PWR/SEQ

Size	Document Number	Rev
C	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 23 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **GPU_GND**

Size	Document Number	Rev
C	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 24 of 61

PEX_PLLVDD/Q Decouling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	

PEX_PLLVDD
N16:+1.0VGS(recommend)
N17:NC

PEX_SVDD_3V3
N16:+3.3V_AON(recommend)
N17:NC

PEX_SVDD/Q Decouling

MLCC	N16	N17	location
4.7uF	2	NA	Near

PEX_HVDD
N16:+1.05VGS(recommend)
+1.0VGS(Used)
N17:+1.8VGS

XS_PLLVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

SP_PLLVDD & VID_PLLVDD/Q Decouling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

GPCPLL_AVDD/Q Decouling

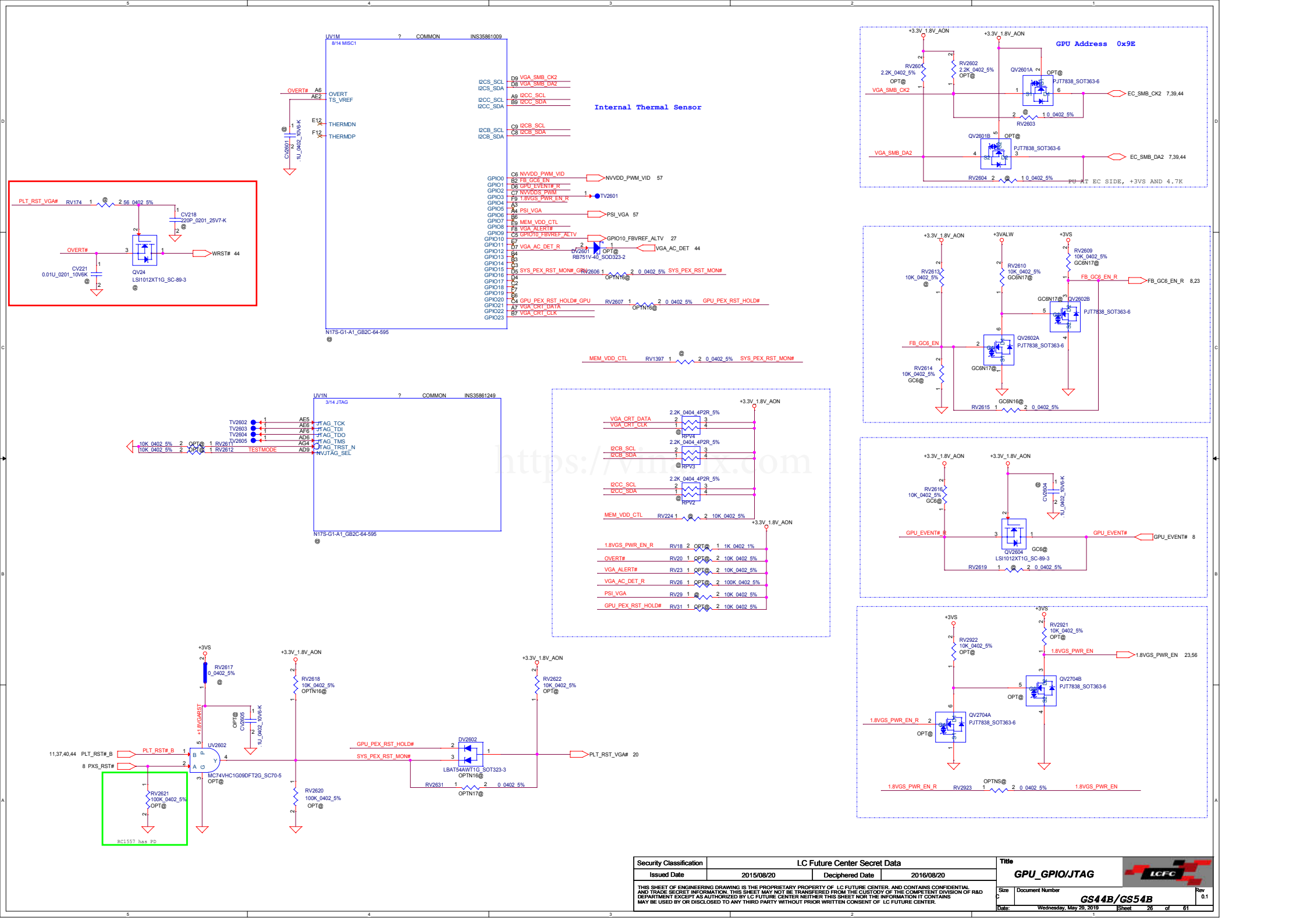
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: GPU_STRAP/DP/HDMI

Size: C | Document Number: GS44B/GS54B | Rev: 0.1

Date: Wednesday, May 29, 2019 | Sheet 25 of 61


UV1M
8/14 MISC1
COMMON
INS35861009
OVERT#
OVERT
TS_VREF
THERMDN
THERMDP
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
Internal Thermal Sensor
GPIO0 NVVDD_PWM_VID
GPIO1 FB_GC6_EN
GPIO2 GPU_EVENT#_R
GPIO3 NVVDDS_PWM
GPIO4 1.8VGS_PWR_EN_R
GPIO5 PSI_VGA
GPIO6 MEM_VDD_CTL
GPIO7 VGA_ALERT#
GPIO8 GPIO10_FBVREF_ALTV
GPIO9 VGA_AC_DET_R
GPIO10 SYS_PEX_RST_MON#_GPU
GPIO11 GPU_PEX_RST_HOLD#_GPU
GPIO12 VGA_CRT_DATA
GPIO13 VGA_CRT_CLK
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
N17S-G1-A1_GB2C-64-595
NVVDD_PWM_VID 57
TV2601
PSI_VGA 57
GPIO10_FBVREF_ALTV 27
VGA_AC_DET 44
DV2601 RB751V-40_SOD323-2
RV2606 0_0402_5%
SYS_PEX_RST_MON#
RV2607 0_0402_5%
GPU_PEX_RST_HOLD#
MEM_VDD_CTL
RV1397 0_0402_5%
SYS_PEX_RST_MON#
PLT_RST_VGA#
RV174 56_0402_5%
CV218 220P_0201_25V7-K
OVERT#
CV221 0.01U_0201_10V6K
QV24 LSI1012XT1G_SC-89-3
WRST# 44
UV1N
3/14 JTAG
TV2602
TV2603
TV2604
TV2605
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
NVJTAG_SEL
RV2611 10K_0402_5%
RV2612 10K_0402_5%
TESTMODE
N17S-G1-A1_GB2C-64-595
+3.3V_1.8V_AON
VGA_CRT_DATA
VGA_CRT_CLK
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
MEM_VDD_CTL
RPV4 2.2K_0404_4P2R_5%
RPV3 2.2K_0404_4P2R_5%
RPV2 2.2K_0404_4P2R_5%
RV224 10K_0402_5%
1.8VGS_PWR_EN_R RV18 1K_0402_1%
OVERT# RV20 10K_0402_5%
VGA_ALERT# RV23 10K_0402_5%
VGA_AC_DET_R RV26 100K_0402_5%
PSI_VGA RV29 10K_0402_5%
GPU_PEX_RST_HOLD# RV31 10K_0402_5%
GPU Address 0x9E
RV2601 2.2K_0402_5%
RV2602 2.2K_0402_5%
QV2601A PJT7838_SOT363-6
QV2601B PJT7838_SOT363-6
VGA_SMB_CK2
VGA_SMB_DA2
EC_SMB_CK2 7,39,44
EC_SMB_DA2 7,39,44
RV2603 10_0402_5%
RV2604 10_0402_5%
PU AT EC SIDE, +3VS AND 4.7K
+3VALW
RV2609 10K_0402_5%
RV2610 10K_0402_5%
RV2613 10K_0402_5%
RV2614 10K_0402_5%
QV2602A PJT7838_SOT363-6
QV2602B PJT7838_SOT363-6
FB_GC6_EN_R
FB_GC6_EN_R 8,23
FB_GC6_EN
RV2615 0_0402_5%
RV2616 10K_0402_5%
CV2604 1U_0402_10V6-K
QV2604 LSI1012XT1G_SC-89-3
GPU_EVENT# 8
RV2619 0_0402_5%
+3VS
RV2921 10K_0402_5%
RV2922 10K_0402_5%
QV2704A PJT7838_SOT363-6
QV2704B PJT7838_SOT363-6
1.8VGS_PWR_EN
1.8VGS_PWR_EN 23,56
1.8VGS_PWR_EN_R
RV2923 0_0402_5%
RV2617 0_0402_5%
RV2618 10K_0402_5%
RV2620 100K_0402_5%
RV2621 100K_0402_5%
RV2622 10K_0402_5%
CV2605 1U_0402_10V6-K
+1.8VGARST
UV2602 MC74VHC1G09DFT2G_SC70-5
11,37,40,44 PLT_RST#_B
8 PXS_RST#
DV2602 LBAT54AWT1G_SOT323-3
RV2631 0_0402_5%
PLT_RST_VGA# 20
RC1557 has PD
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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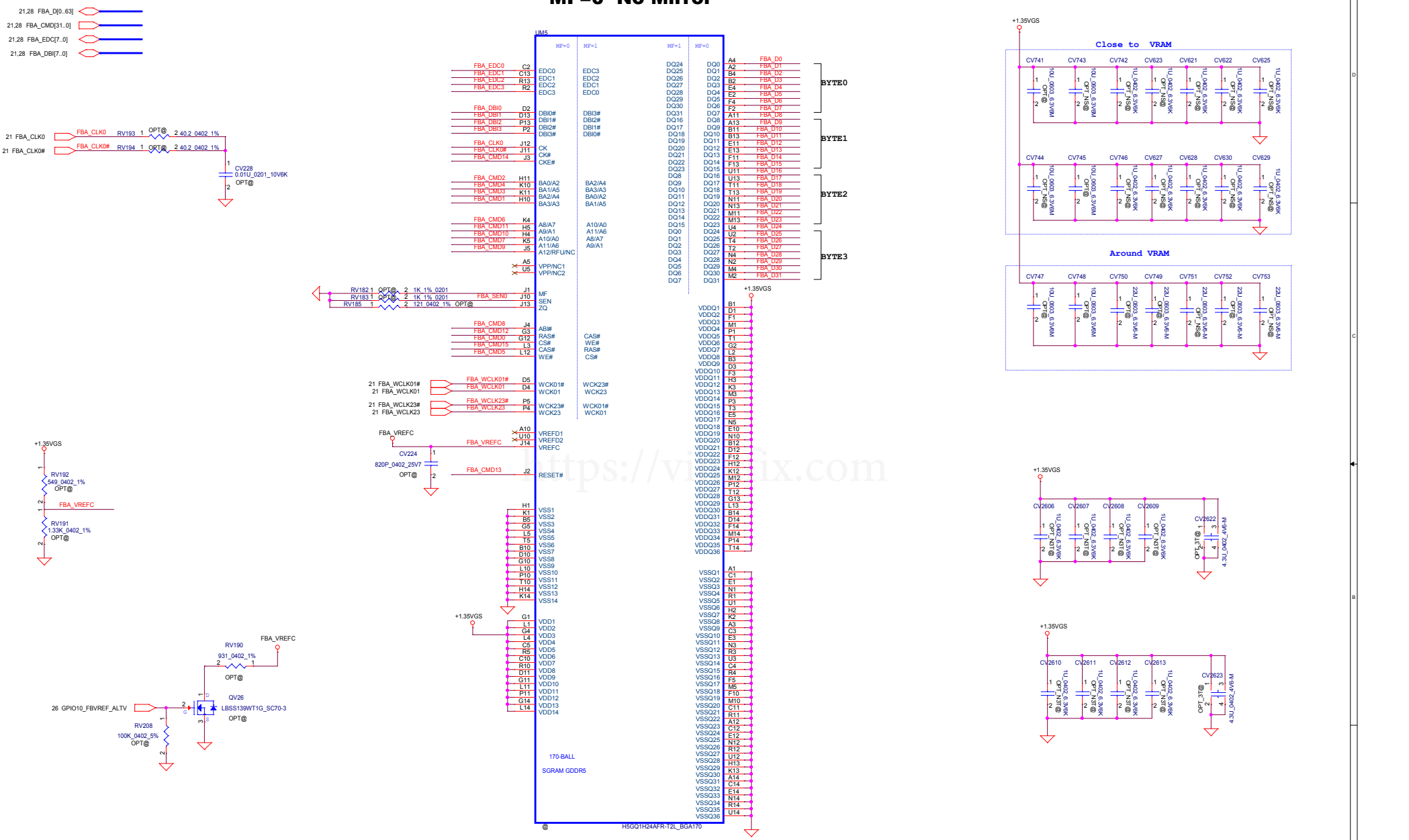
Title
GPU_GPIO/JTAG
Size C
Document Number
GS44B/GS54B
Rev 0.1
Date: Wednesday, May 29, 2019
Sheet 26 of 61

Lower 32 bits

MF=0 No Mirror



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

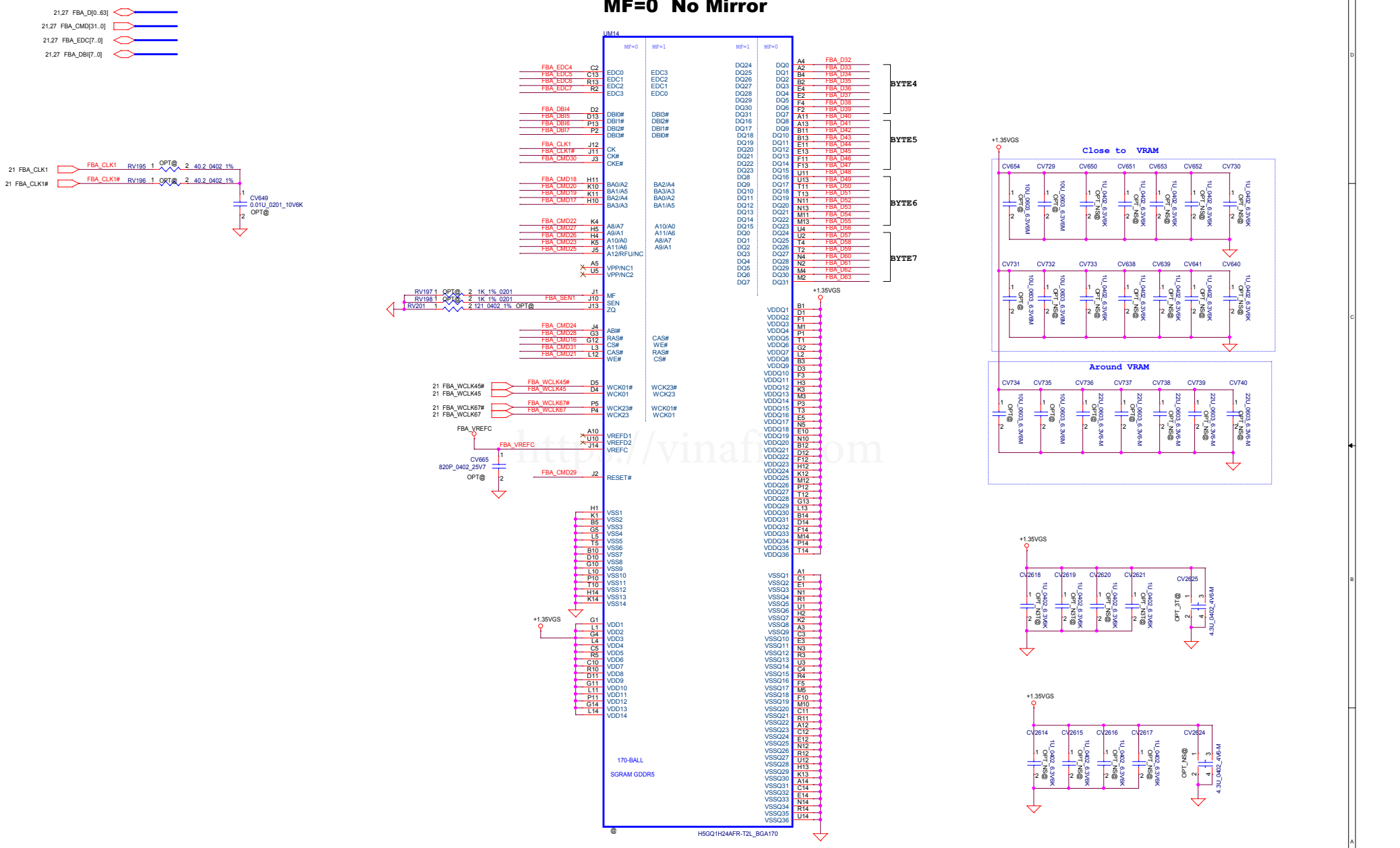
Title: GPU_GDDR5_Rank0_[31:0]

Size: C | Document Number: teknisi GS44B/GS54B | Rev: 0.1

Date: Wednesday, May 29, 2019 | Sheet 27 of 61

upper 32 bits

MF=0 No Mirror

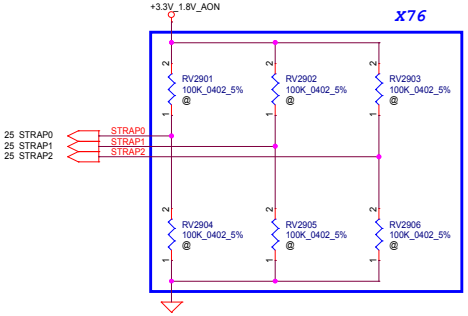


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

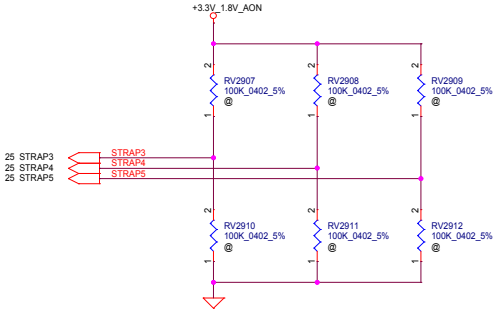
Title: GPU_GDDR5_Rank0_[64:32]

Size	Document Number	Rev
C	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 28 of 61



GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L



Strap5 is NC pin on N16

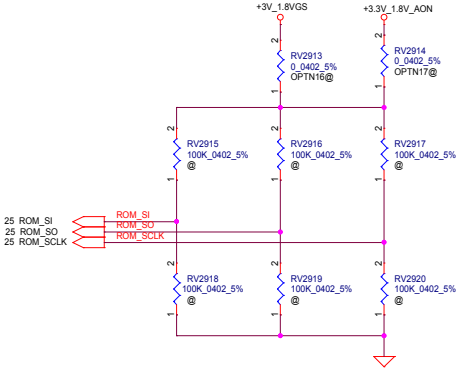
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

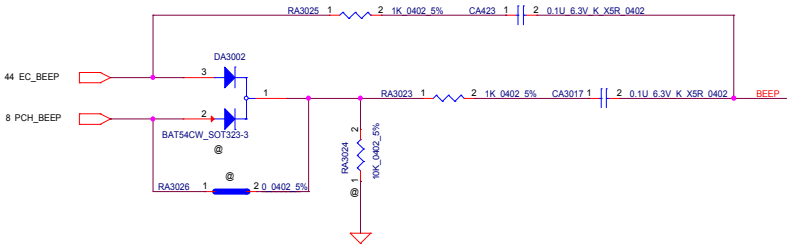
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

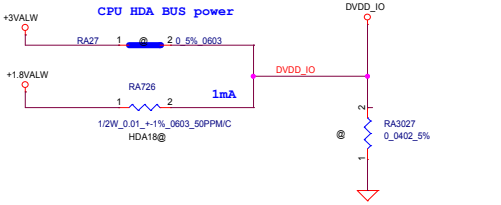
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

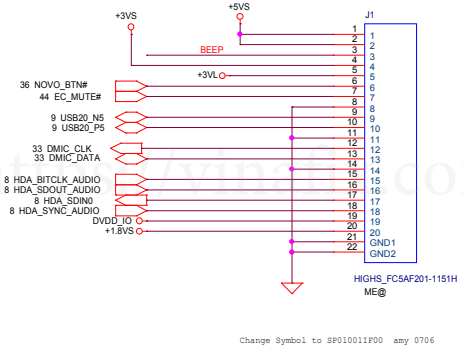
Title: GPU_MISC

Size	Document Number	Rev
C	GS44B/GS54B	0.1

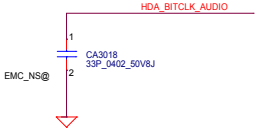
Date: Wednesday, May 29, 2019 Sheet 29 of 61







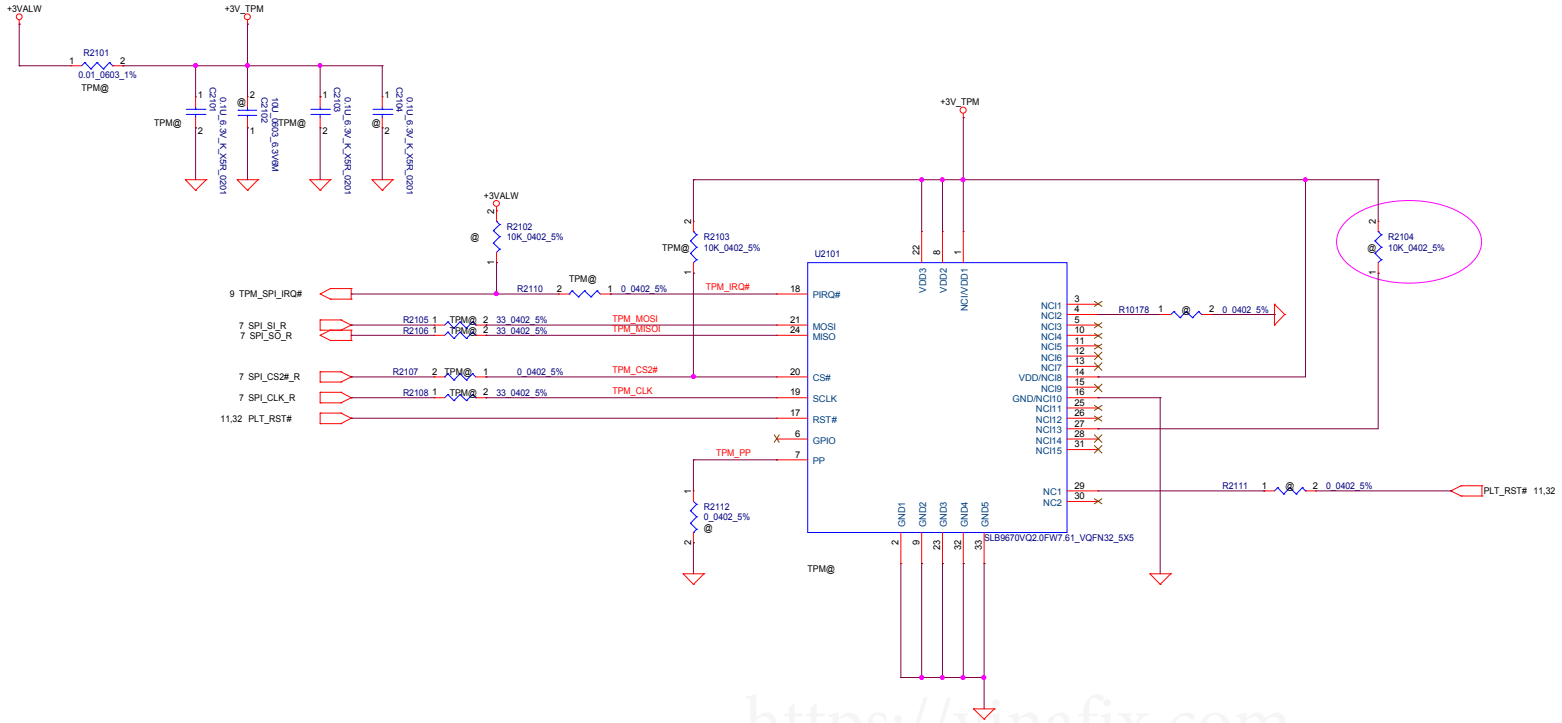
20Pin CONN



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	IO board		
Size	Document Number		Rev
C	GS44B/GS54B		0.1
Date:	Wednesday, May 29, 2019	Sheet	30 of 61

Title	<Title>	
Size A	Document Number GS44B/GS54B	Rev 0.1
Date: Wednesday, May 29, 2019	Sheet 31 of 61	

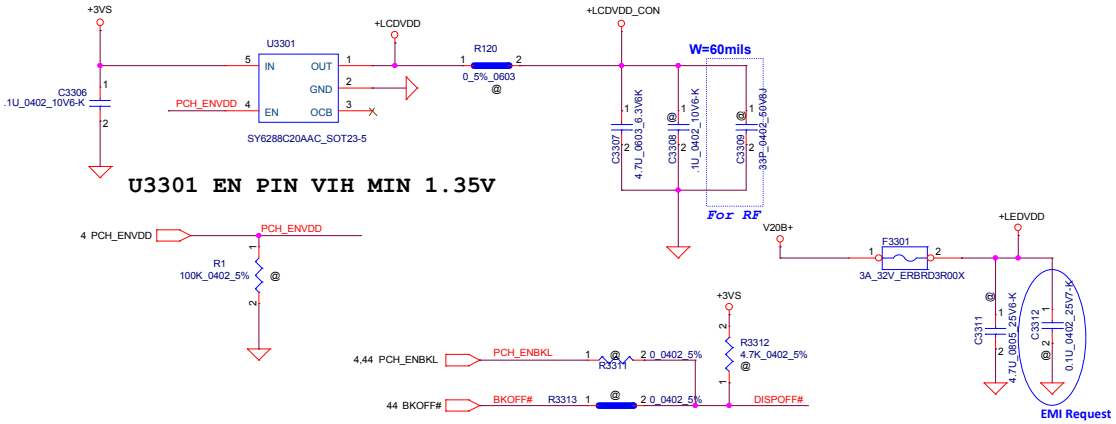


TABLE

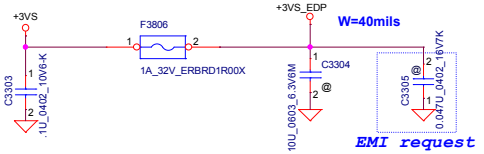
Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z32H330TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	GND	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

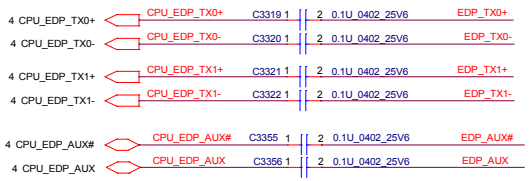
Title			
TPM			
Size C	Document Number GS44B/GS54B		Rev 0.1
Date: Wednesday, May 29, 2019		Sheet 32 of 61	

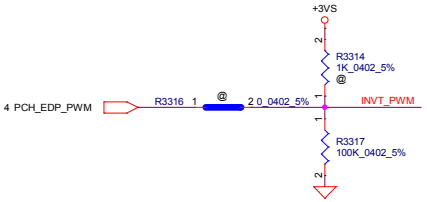
LCD POWER CIRCUIT

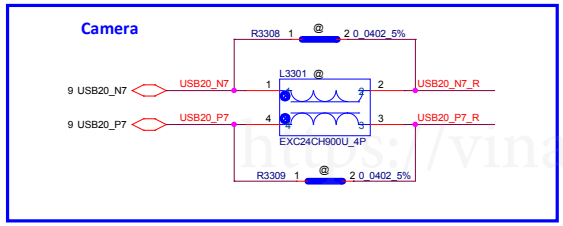


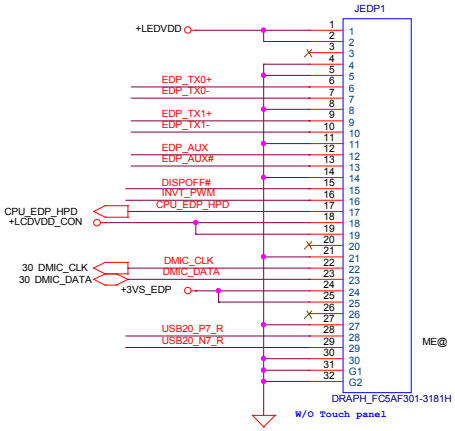
CMOS Camera

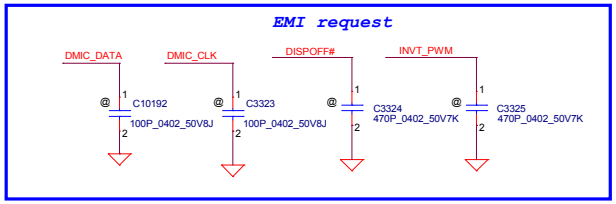




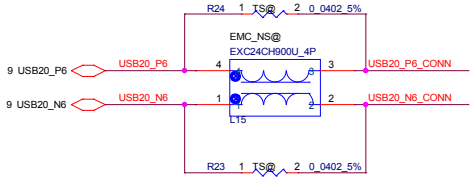


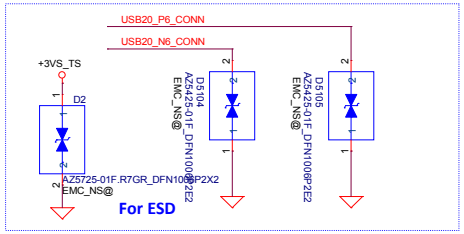


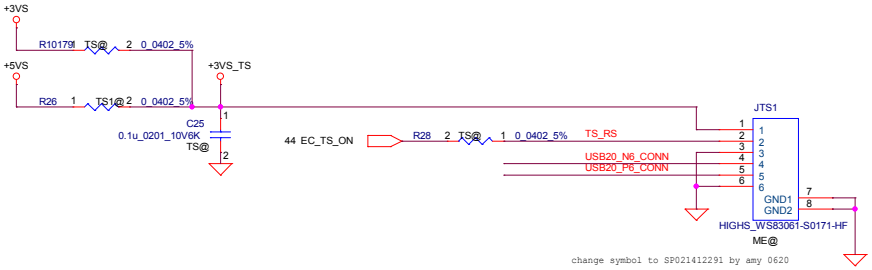




Touch Screen

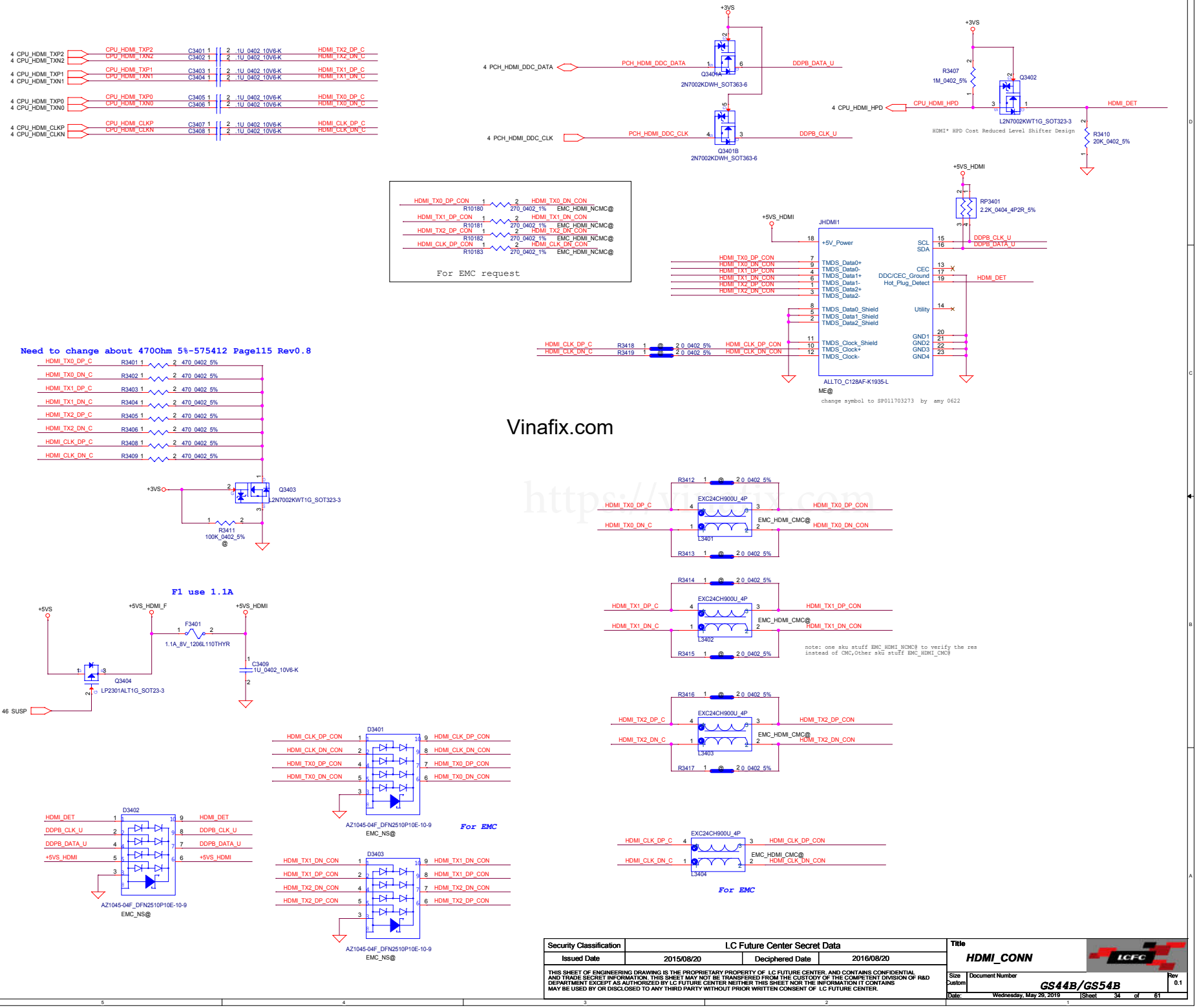






Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	eDP/CAMERA.		
Size: Custom	Document Number: GS44B/GS54B		Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 33 of 61		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	HDMI_CONN		
Size	Document Number		Rev
Custom	GS44B/GS54B		0.1
Date:	Wednesday, May 29, 2019	Sheet	34 of 61

1.1.8VGS_PWR_EN_R pull high RV18----P26

2.ON/OFFBTN# add diode D25-----P36

3.del

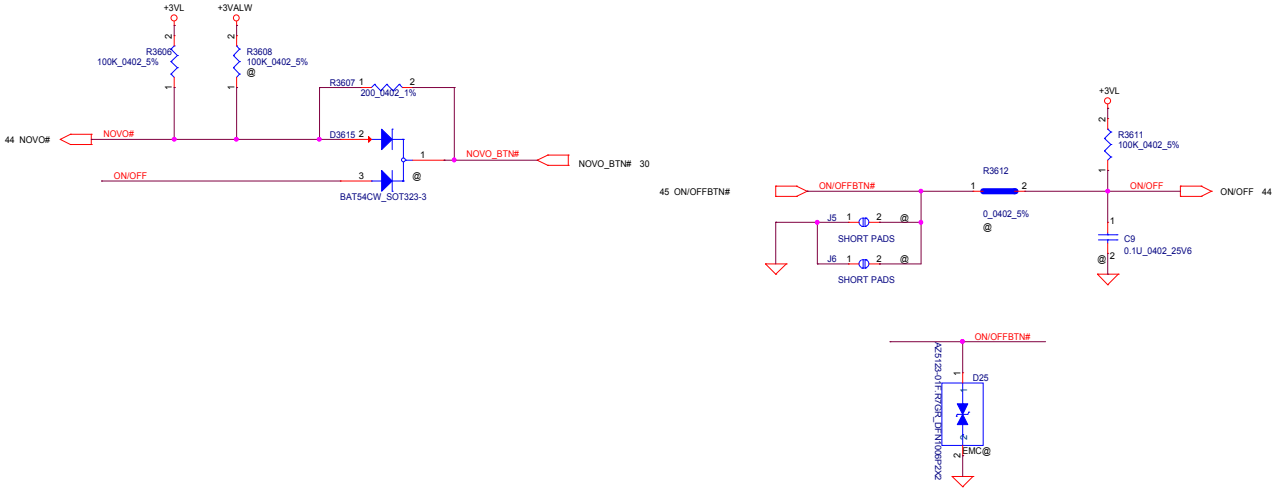
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Blank***

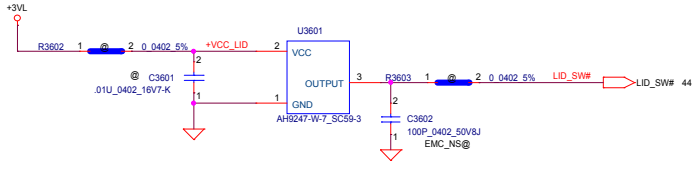
Size	Document Number	Rev
B	***GS44B/GS54B***	0.1

Date: Wednesday, May 29, 2019 Sheet 35 of 61

ON/OFF switch



LID switch

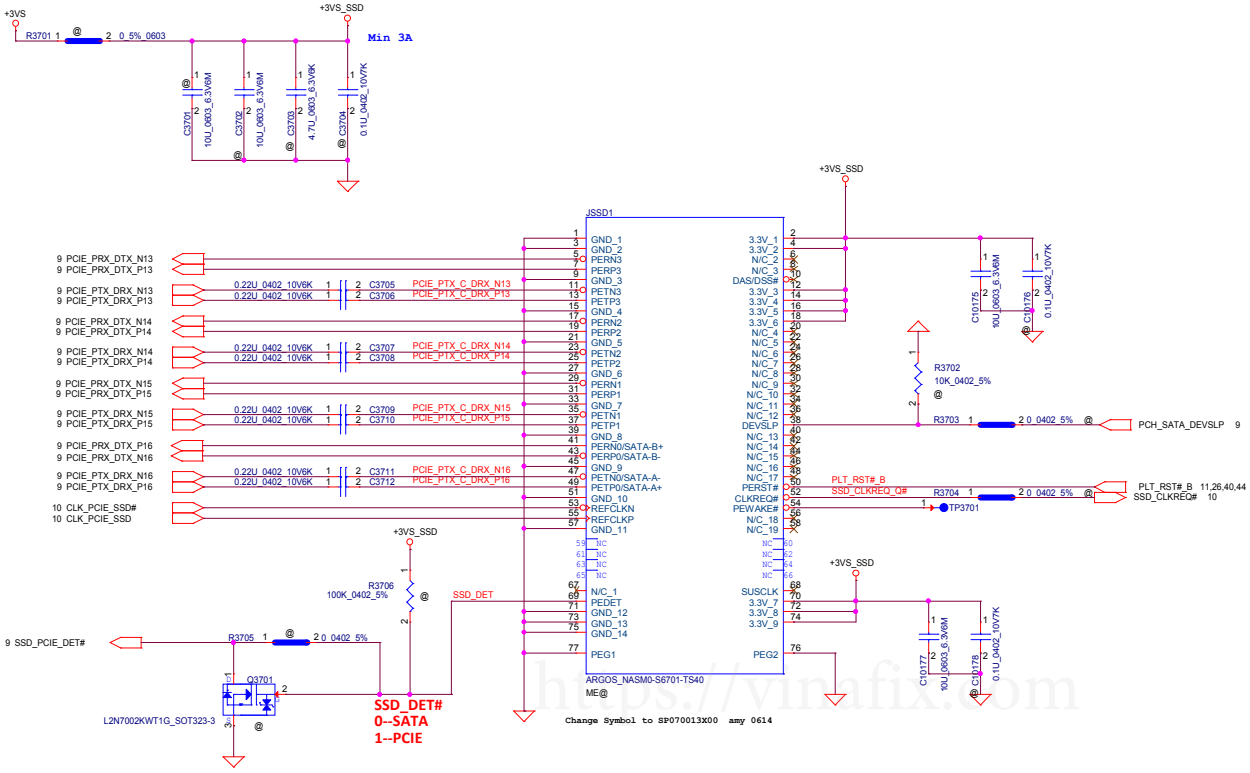


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **HALL Sensor**

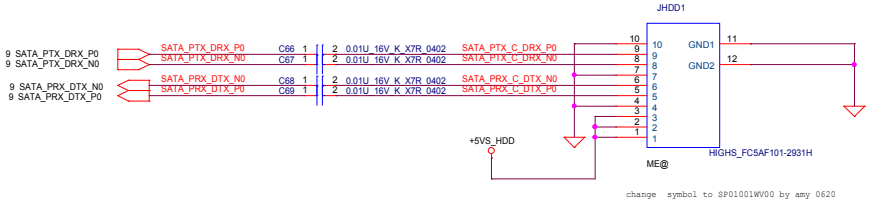
Size	Document Number	Rev
Custom	GS44B/GS54B	0.1

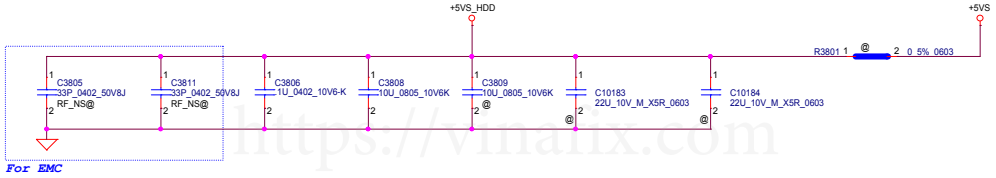
Date: Wednesday, May 29, 2019 | Sheet 36 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	NGFF_SSD_1	
Size: C	Document Number: GS44B/GS54B	Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 37 of 61	





Vinafix.com

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

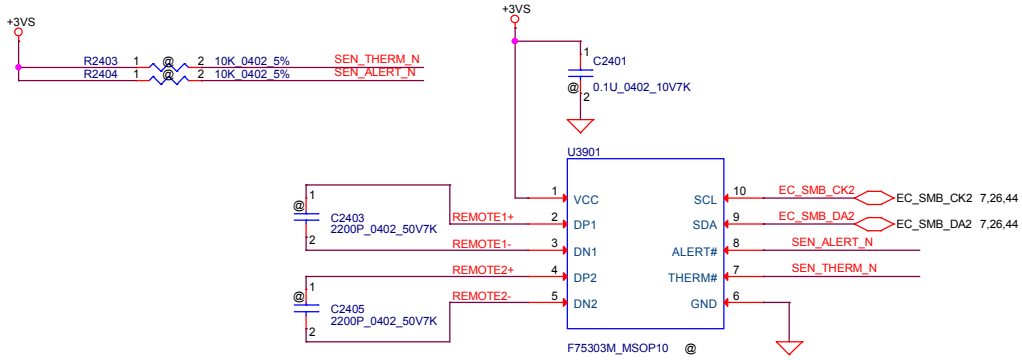
Title: **SATA HDD CONN**

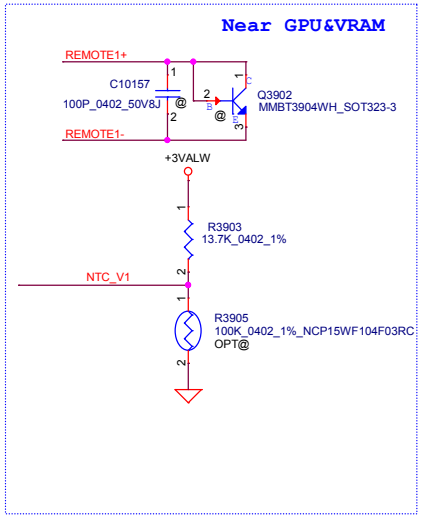
Size	Document Number	Rev
C	GS44B/GS54B	0.1

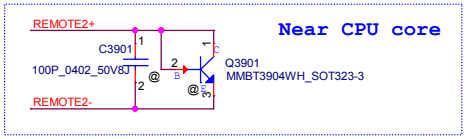
Date: Wednesday, May 29, 2019 Sheet 38 of 61

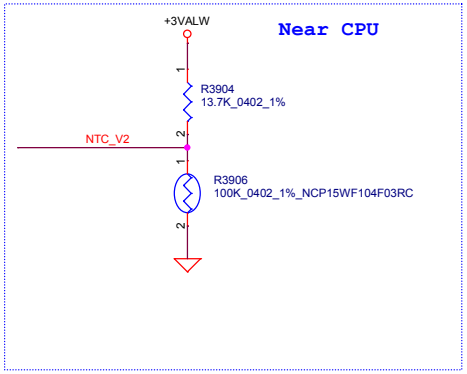
SMSC thermal sensor placed near DIMM

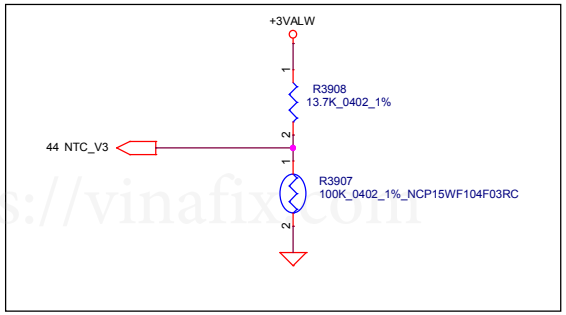
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



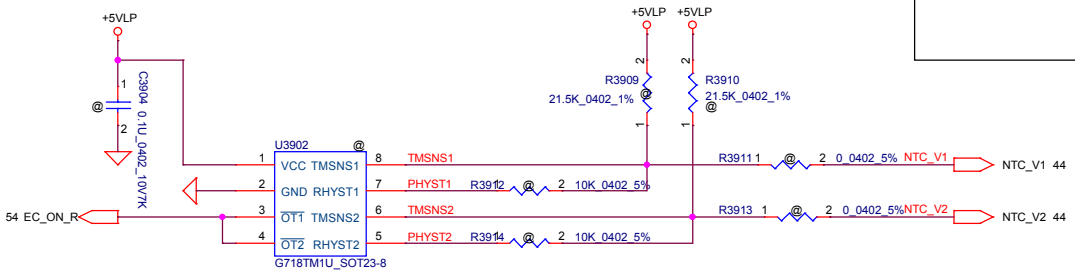




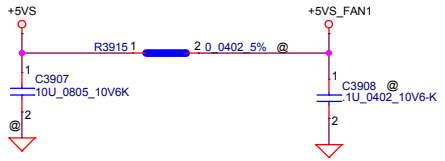




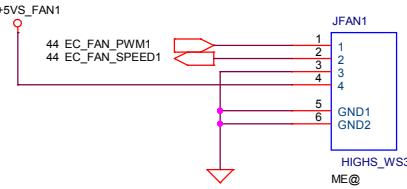
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C



FAN Conn

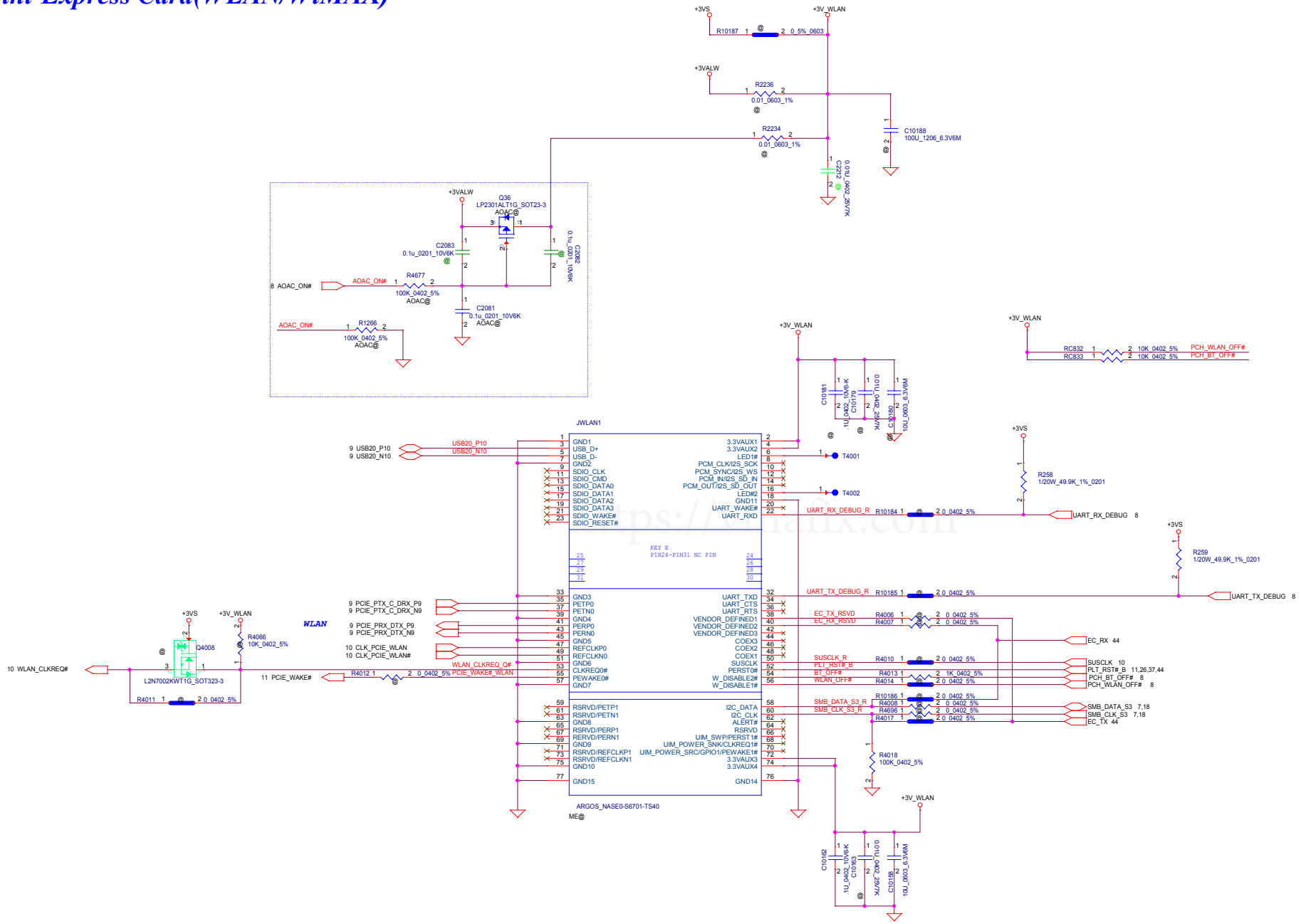


Change Symbol to SP021410082 amy 0614

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Thermal sensor/FAN CONN		
Size: Custom	Document Number: GS44B/GS54B		Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 39 of 61		

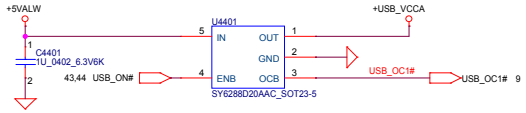
Mini-Express Card(WLAN/WiMAX)



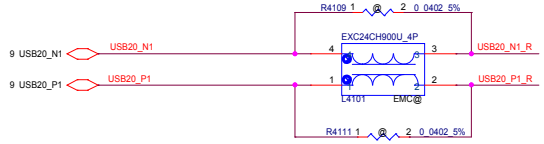
Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

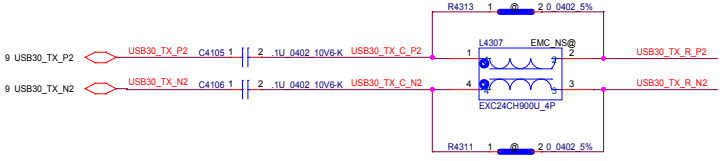
Title	NGFF_WLAN		
Size	Document Number		Rev
C	GS44B/GS54B		0.1
Date:	Wednesday, May 29, 2019	Sheet	40 of 61

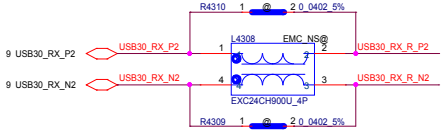
RIGHT SIDE USB3.0 PORT x1

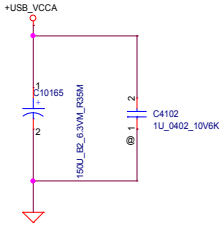


Low Active 2A

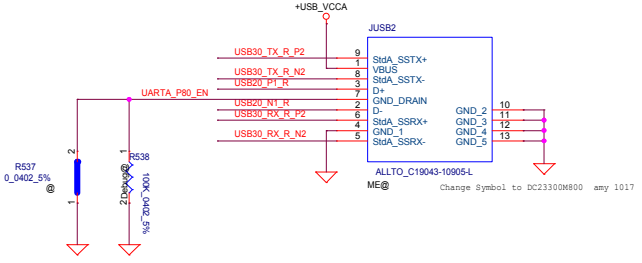


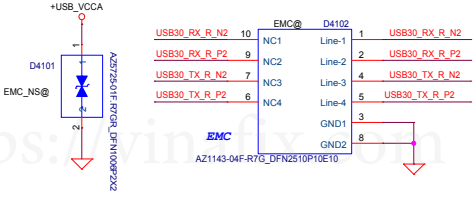


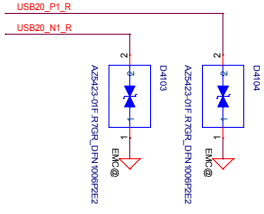




C4102 close to USB Conn







For USB Debug Function

USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **USB3 PORT_LEFT**

Size	Document Number	Rev
Custom	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 41 of 61

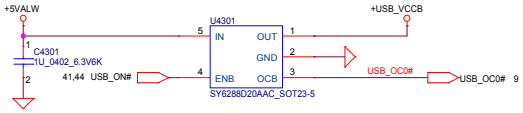
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: ***Blank***

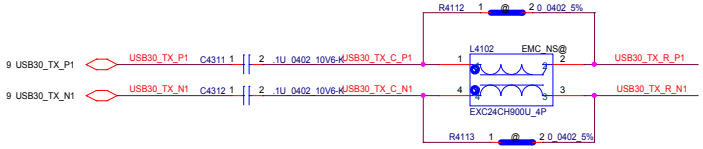
Size: A3 | Document Number: ***GS44B/GS54B*** | Rev: 0.1

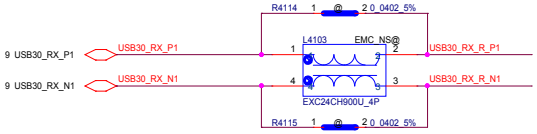
Date: Wednesday, May 29, 2019 | Sheet 42 of 61

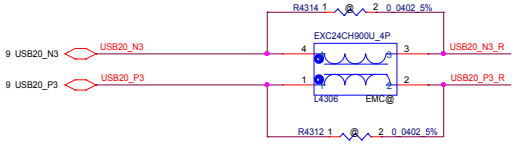
Right SIDE USB3.0 PORT

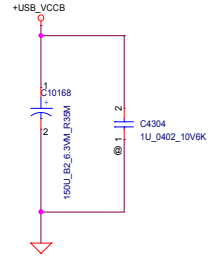


Low Active 2A

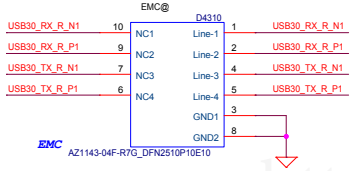


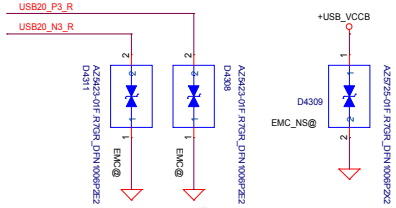


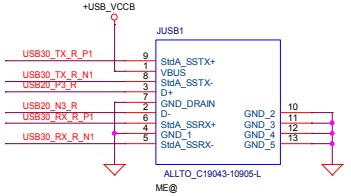




C4304 close to USB Conn



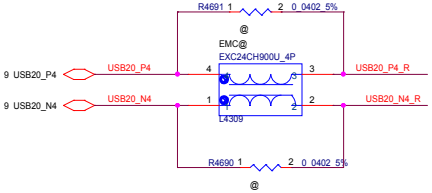


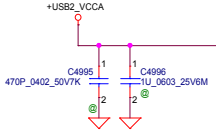


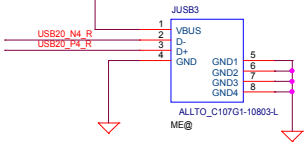
Change Symbol to SP011703284 amy 0614

D4308 and D4311 (SC400006510):due to CIS source cant use,so need change to SC400008800, S DIO_ESD AZ5423-01F.R7GR DFN1006P2E

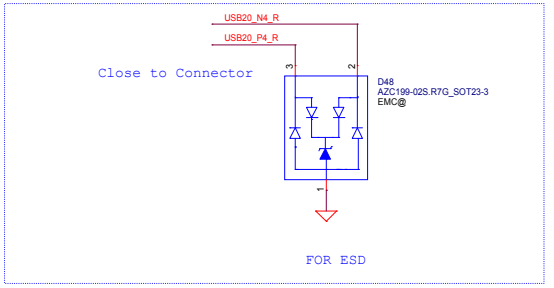
USB2.0 PORT x1

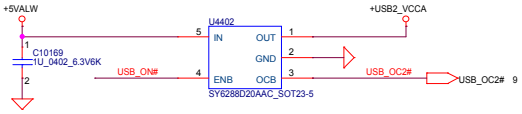




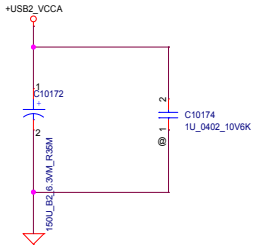


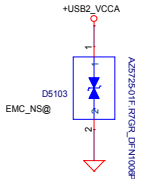
change symbol to SP011807041 amy 0710





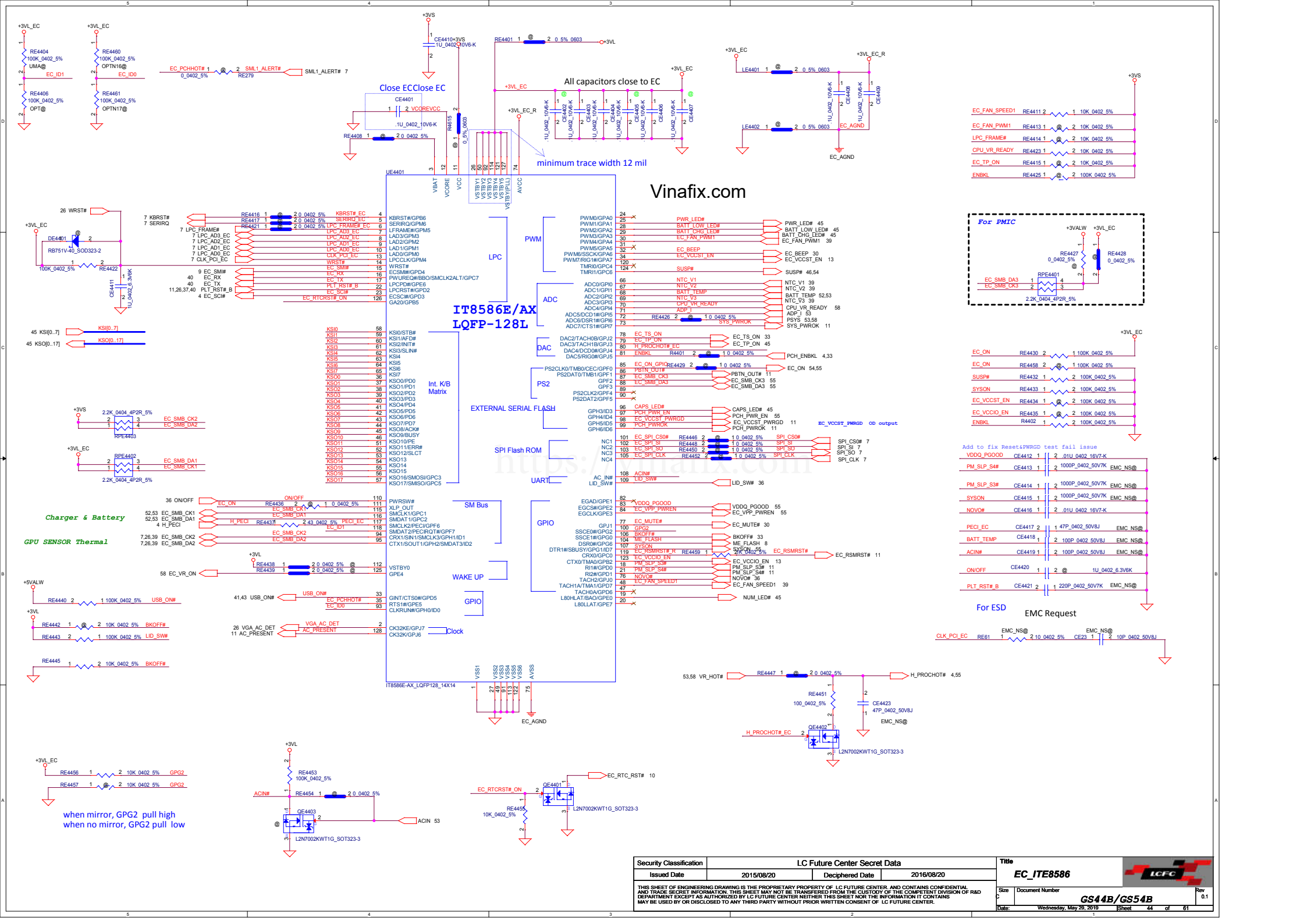
Low Active 2A





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

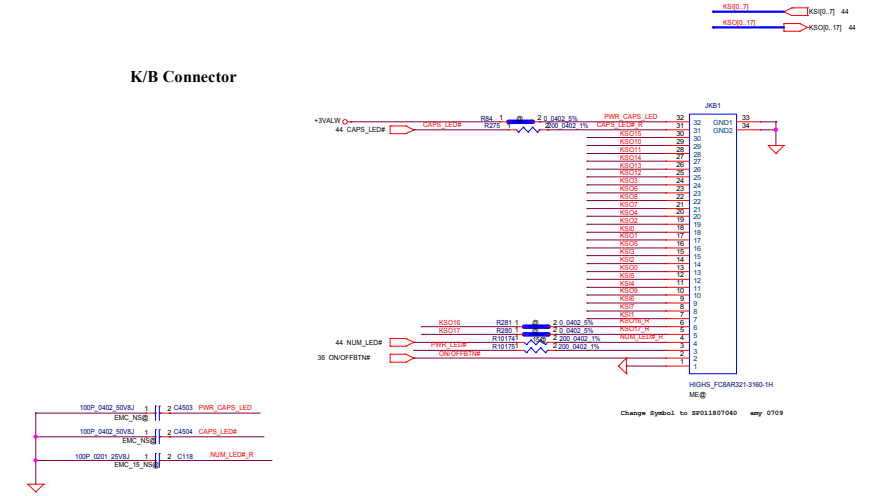
Title	USB3 Port_Right & USB2.0		
Size C	Document Number GS44B/GS54B		Rev 0.1
Date: Wednesday, May 29, 2019		Sheet 43 of 61	

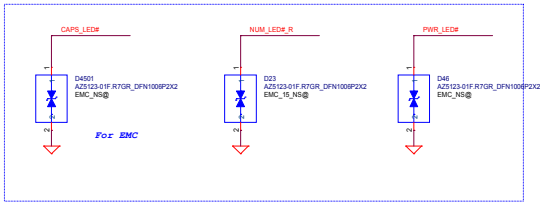


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

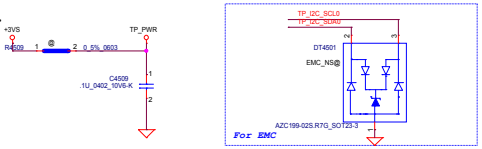
Title	EC_ITE8586		
Size	Document Number		Rev
C	GS44B/GS54B		0.1
Date:	Wednesday, May 29, 2019	Sheet	44 of 61

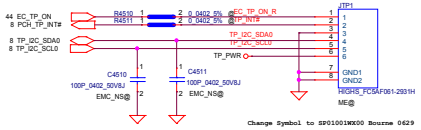
K/B Connector

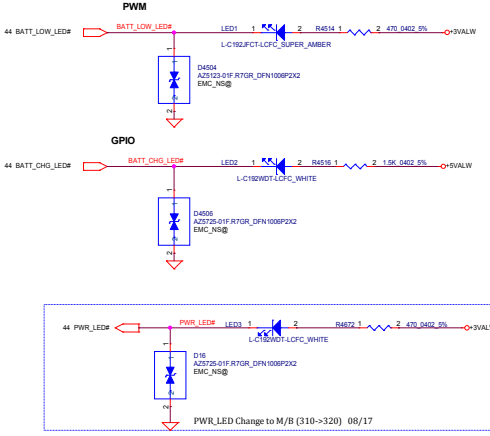




TP/B Connector





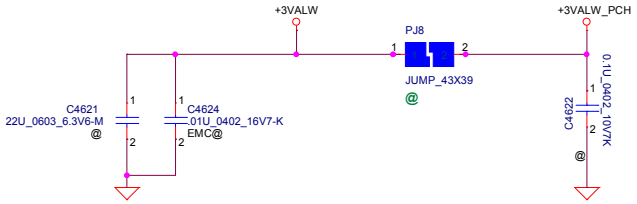


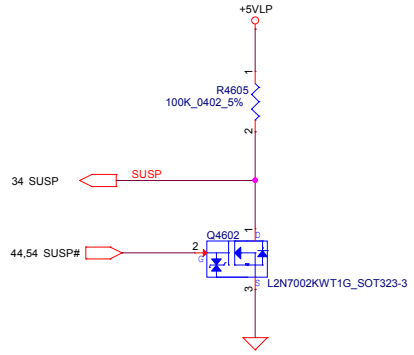
LED	Stute	LED Behavior
Power Button	System on	White_on(battery: 21%~100%)
		Amber_on(battery: 0%~20%)
	Standby LID closed	White_on(battery: 21%~100%)
		Amber_Blink_3S(battery: 0%~20%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_on(battery: 1%~90%)
		White_on(battery: 91%~100%)

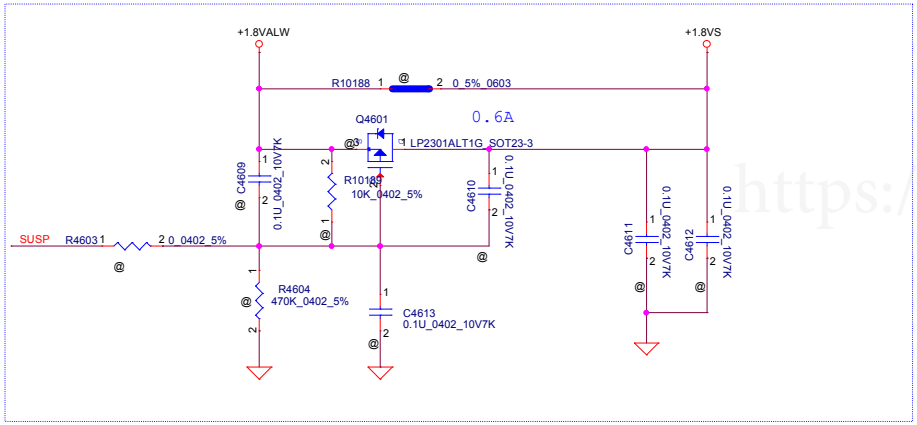
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: KB/TP_CONN.

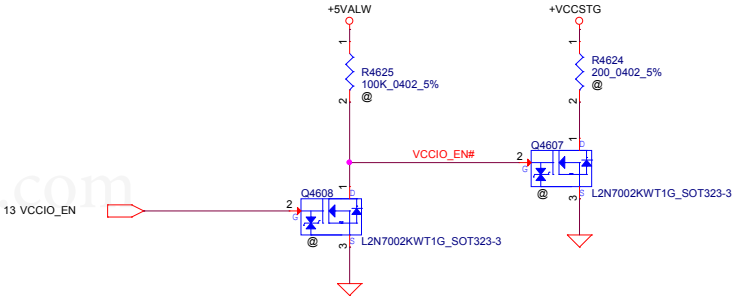
Size: Custom	Document Number: GS44B/GS54B		Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 45 of 61		

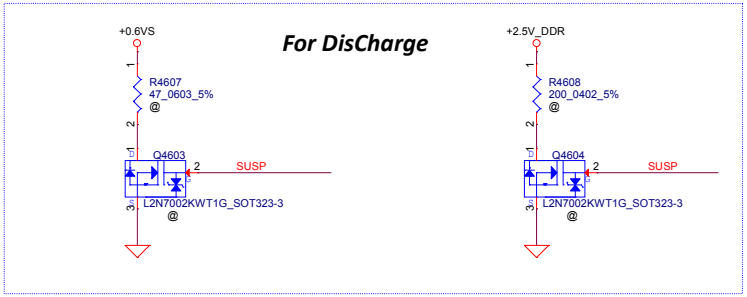






Reserve for VCCSGT discharge



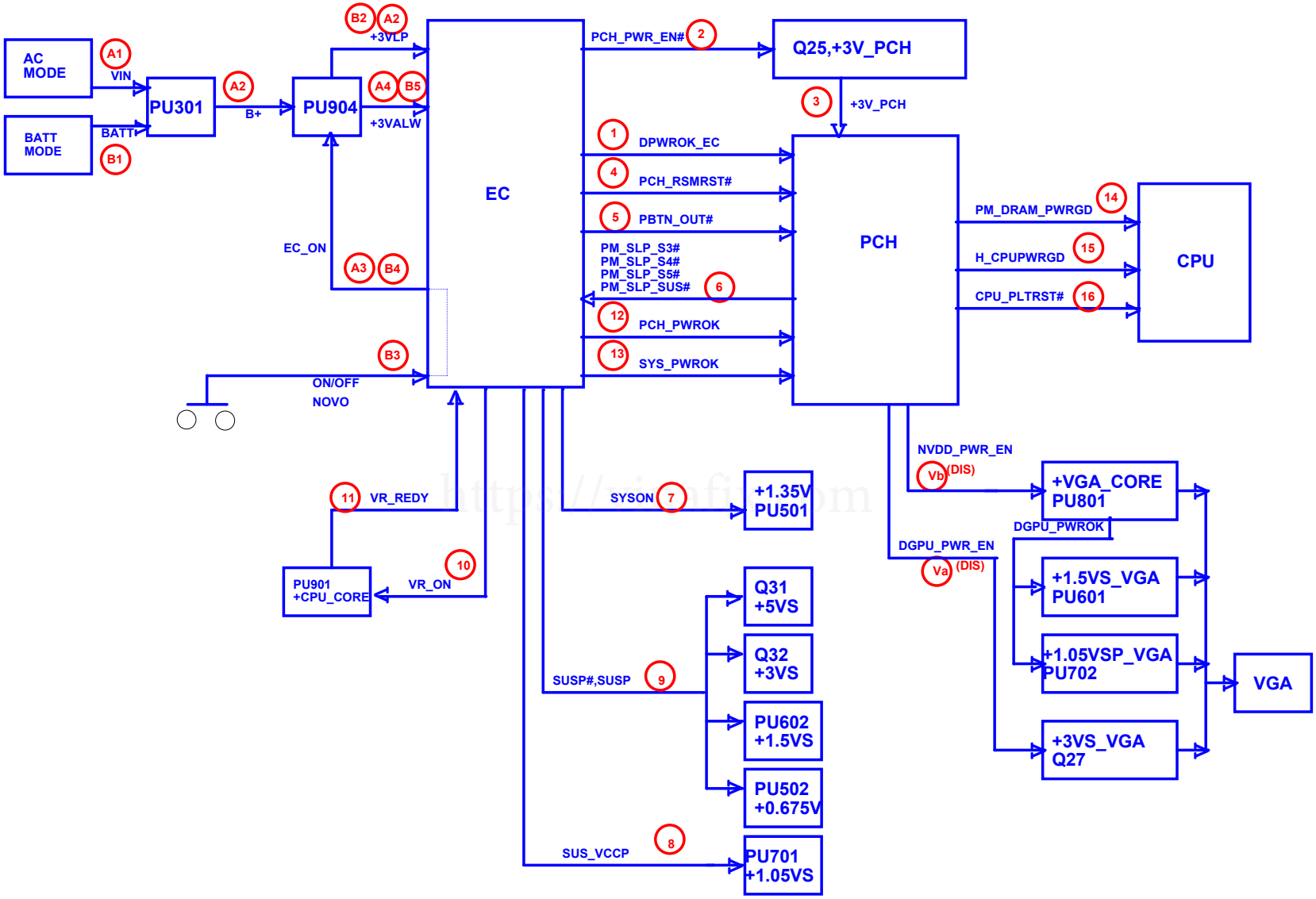


08/29: Need double check enable signal and the resistance

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **DC V TO VS INTERFACE**

Size: Custom	Document Number: GS44B/GS54B	Rev: 0.1
Date: Wednesday, May 29, 2019	Sheet 46 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	GS44B/GS54B	0.1

Date: Wednesday, May 29, 2019 Sheet 47 of 61

Hole

H2
HOLEA
PAD_C10P0D8P0

PCB Fedical Mark PAD

FD4901 FD4902 FD4903 FD4904 FD4905 FD4906

MD Shielding

SH1 SPRING_FINGER_6.2X1.64
SH2 SPRING_FINGER_6.2X1.64
SH3 SPRING_FINGER_6.2X1.64
SH4 SPRING_FINGER_6.2X1.64
SH5 SPRING_FINGER_6.2X1.64
SH6 SPRING_FINGER_6.2X1.64

H3 HOLEA PAD_CT7P0B6P0D3P2
H4 HOLEA PAD_CT7P0B6P0D3P2
H5 HOLEA PAD_CT7P0B6P0D3P2
H6 HOLEA PAD_CT7P0B6P0D3P2
H7 HOLEA PAD_CT7P0B6P0D3P2
H8 HOLEA PAD_CT7P0B6P0D3P2

H9 HOLEA PAD_C7P0D4P0
H10 HOLEA PAD_C7P0D4P0

H17 HOLEA PAD_O2P5X3P0D2P5X3P0N
H18 HOLEA PAD_O2P5X3P0D2P5X3P0N

SODIMM Shielding

SH10 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 SHIELDING_SUL-35A2M_9P2X3P3_1P

H11 HOLEA PAD_C7P0D2P8
H12 HOLEA PAD_C7P0D2P8
H13 HOLEA PAD_C7P0D2P8

H14 HOLEA PAD_C7P0D2P4

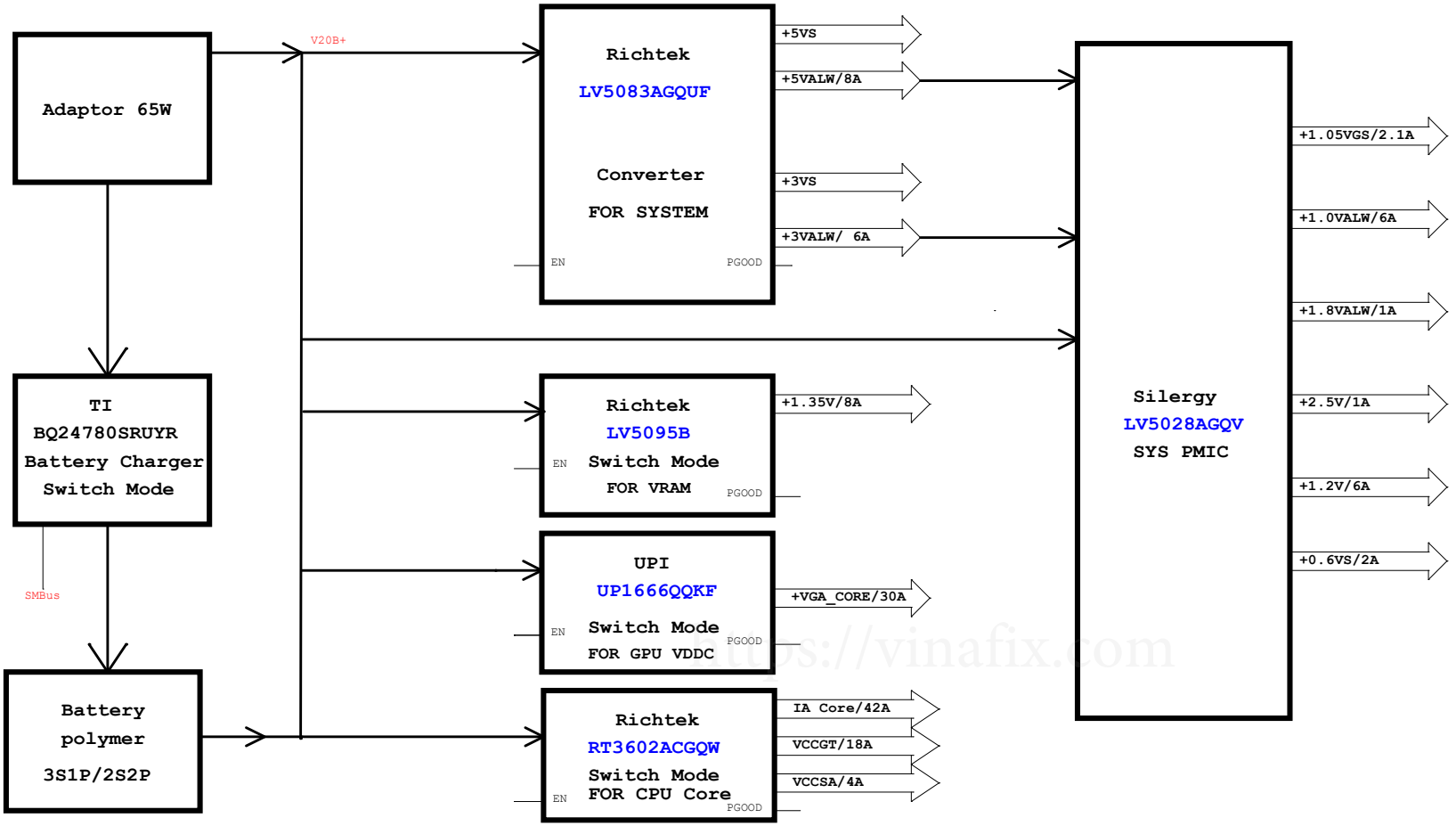
H15 HOLEA PAD_CT7P0B10P0D4P0
H16 HOLEA PAD_CT7P0B10P0D4P0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Hole

Size: B | Document Number: FS441/FS540 | Rev: 0.1

Date: Wednesday, May 29, 2019 | Sheet 49 of 61

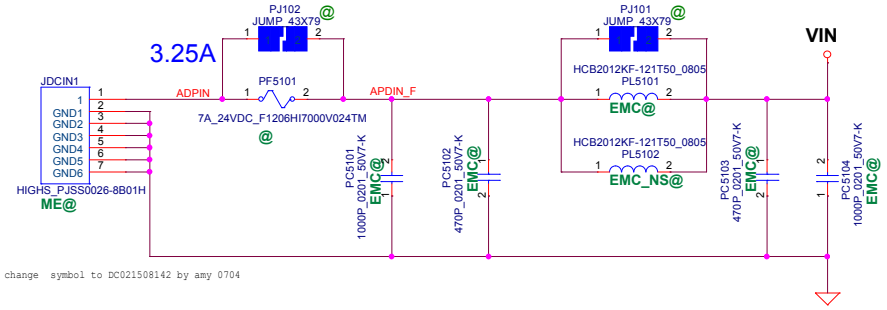


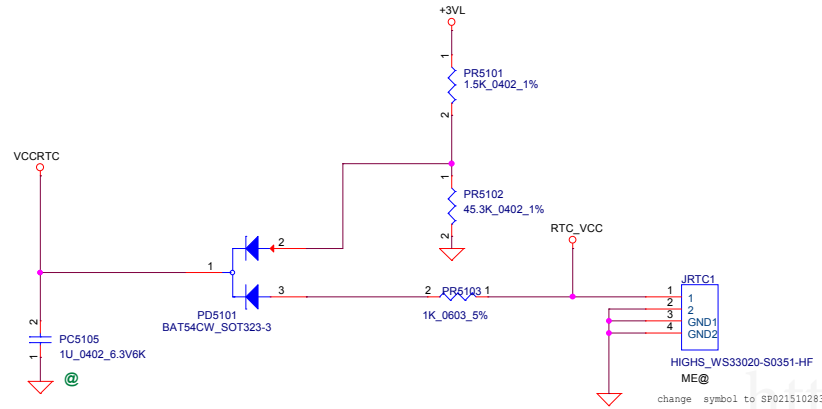
Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: **PWR-Power Diagram**

Size	Document Number	Rev
C	140S-WHL	0.3

Date: Wednesday, May 29, 2019 Sheet 50 of 61



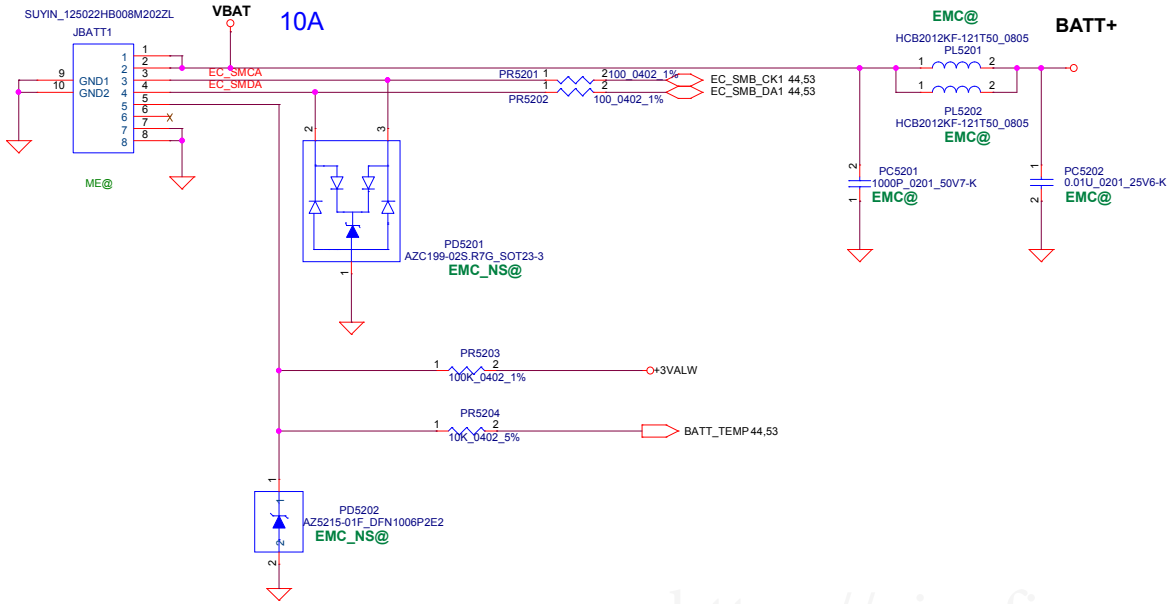


RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-DCIN / RTC charger

Size: Custom	Document Number: 140S-WHL	Rev: 0.3
Date: Wednesday, May 29, 2019	Sheet 51 of 61	



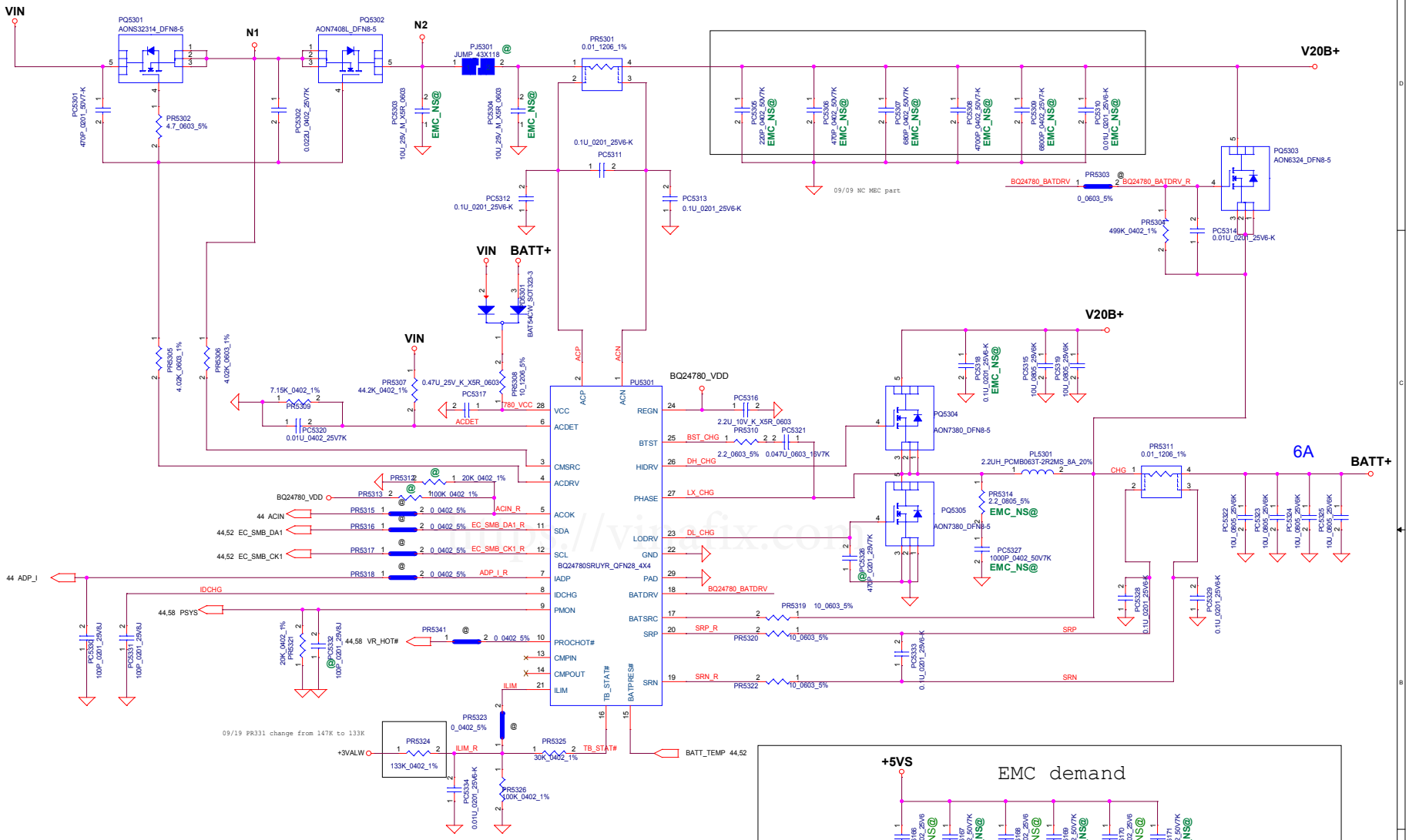
2S1P polymer battery voltage level: +5.5V ~ 8.8 V

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	140S-WHL	0.3

Date: Wednesday, May 29, 2019 Sheet 52 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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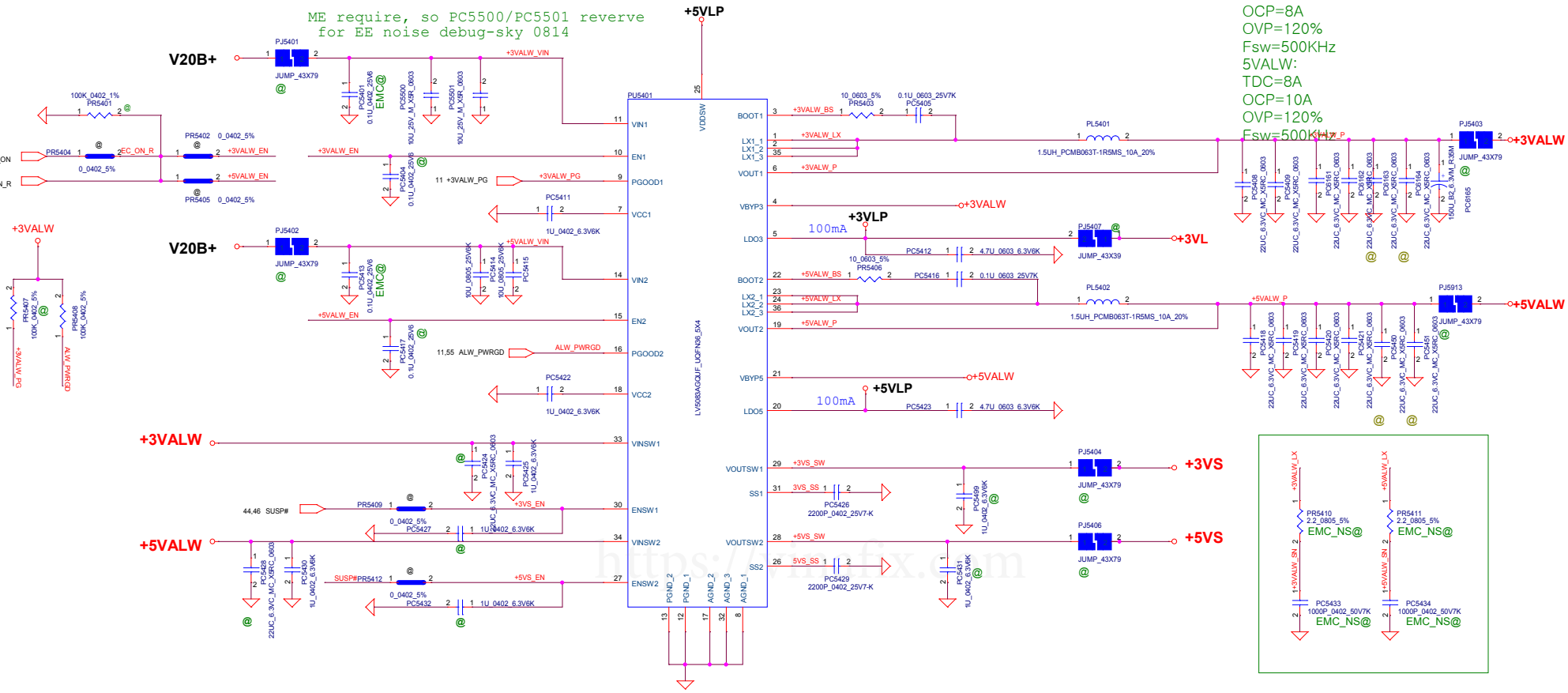
Title	PWR-CHARGER		
Size	Document Number		Rev
C	140S-WHL		0.3
Date:	Wednesday, May 29, 2019	Sheet	53 of 61

EC_ON pull high reserve at EC,
no need USM enable=1.57V USM

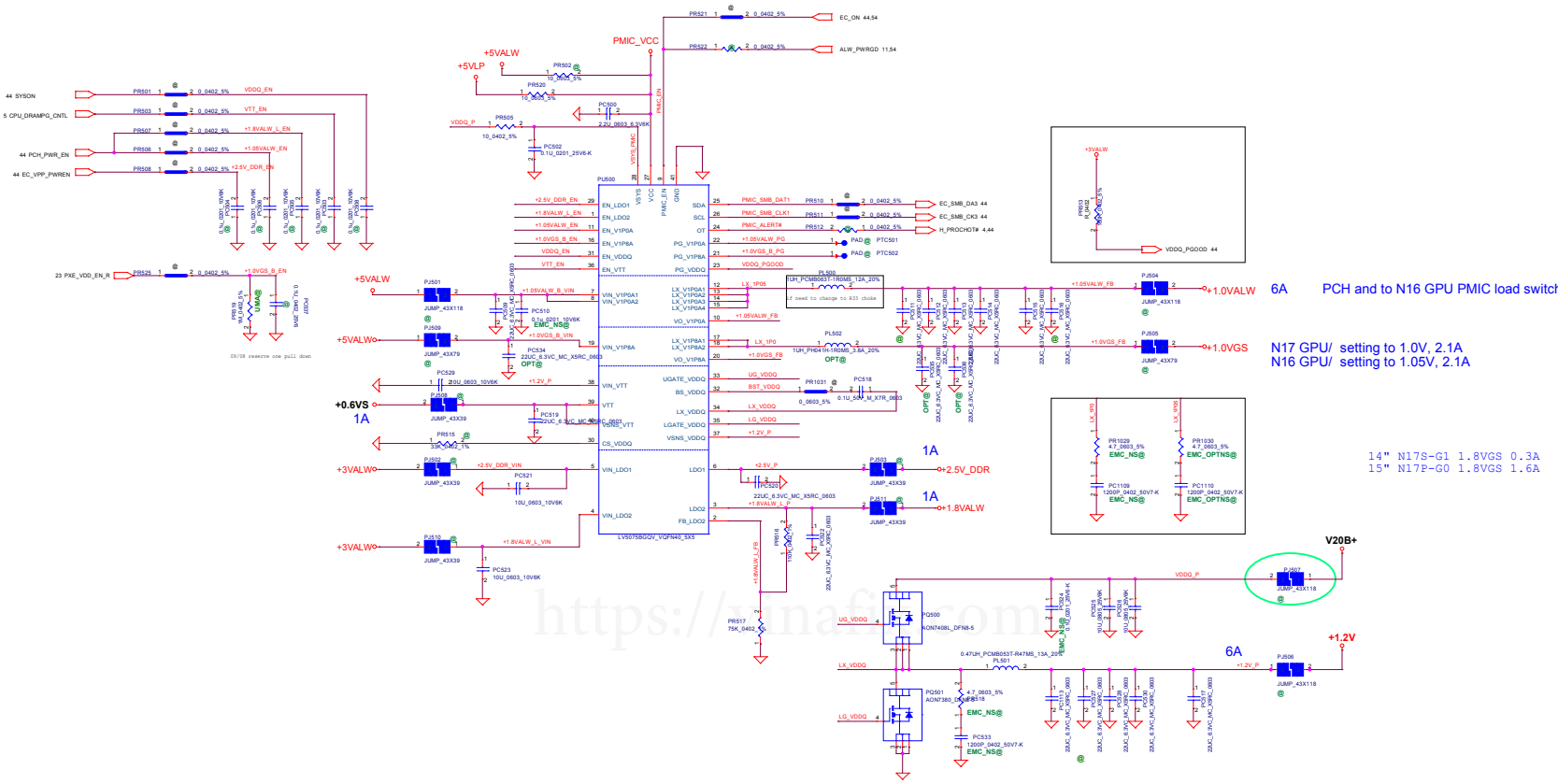
ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814

3VALW:
TDC=6A
OCP=8A
OVP=120%
Fsw=500KHz
5VALW:
TDC=8A
OCP=10A
OVP=120%
Fsw=500KHz



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	140S-WHL		0.2
Date:	Wednesday, May 29, 2019	Sheet	54 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

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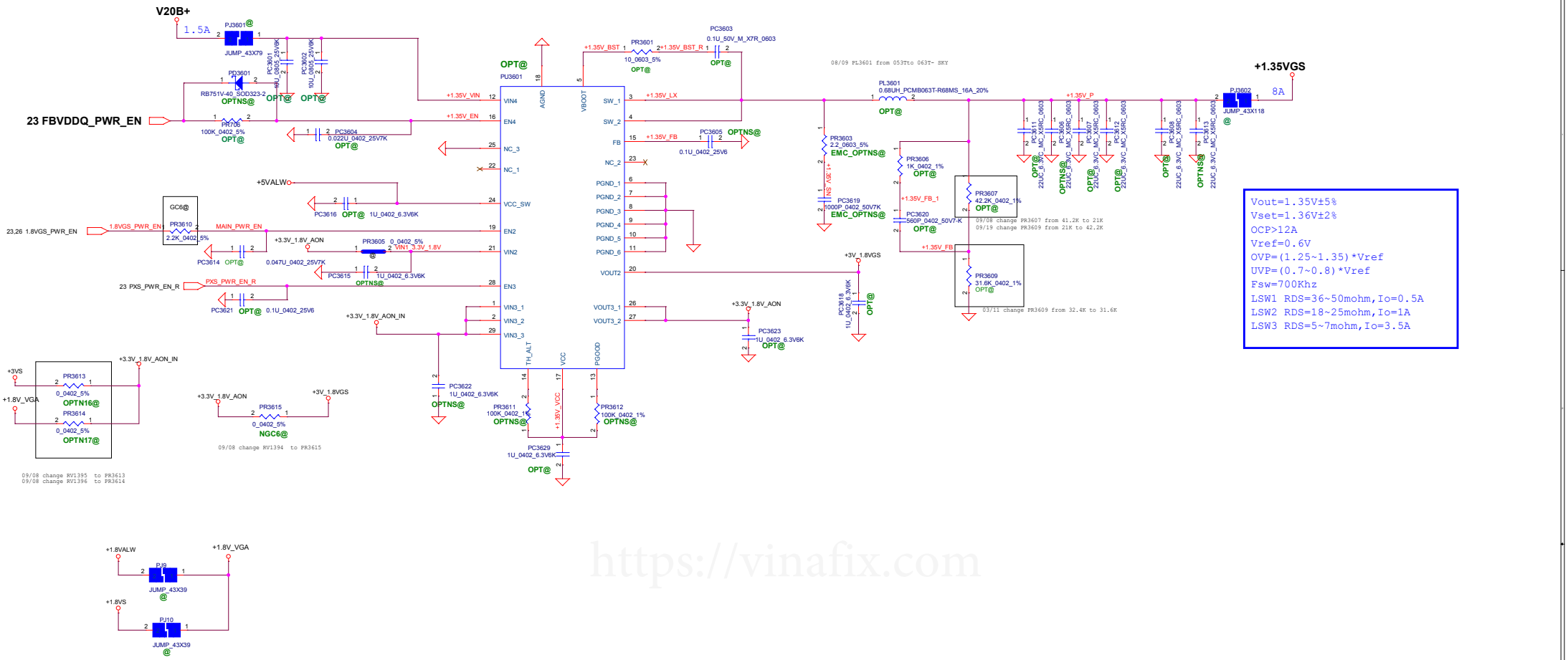
Title: PWR PMIC-DDR4/1.0ALW/1.8VALW

Size	Document Number	Rev
Custom	14OS-WHL	0.3

Date: Wednesday, May 29, 2019 Sheet 55 of 61

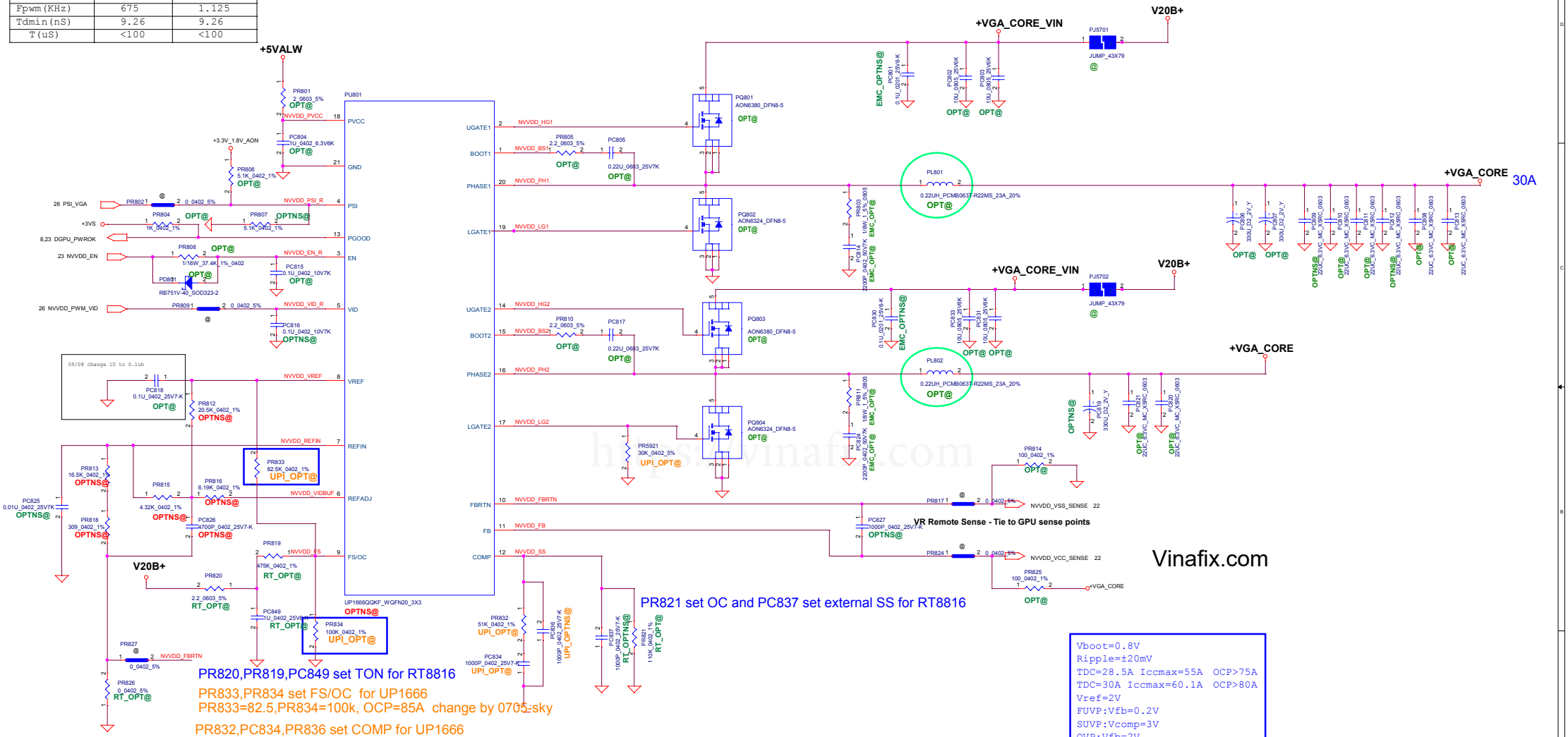


Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-VGA-PMIC
Size: Custom	Document Number: 140S-WHL
Rev	0.3
Date:	Wednesday, May 29, 2019
Sheet	56 of 61

PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



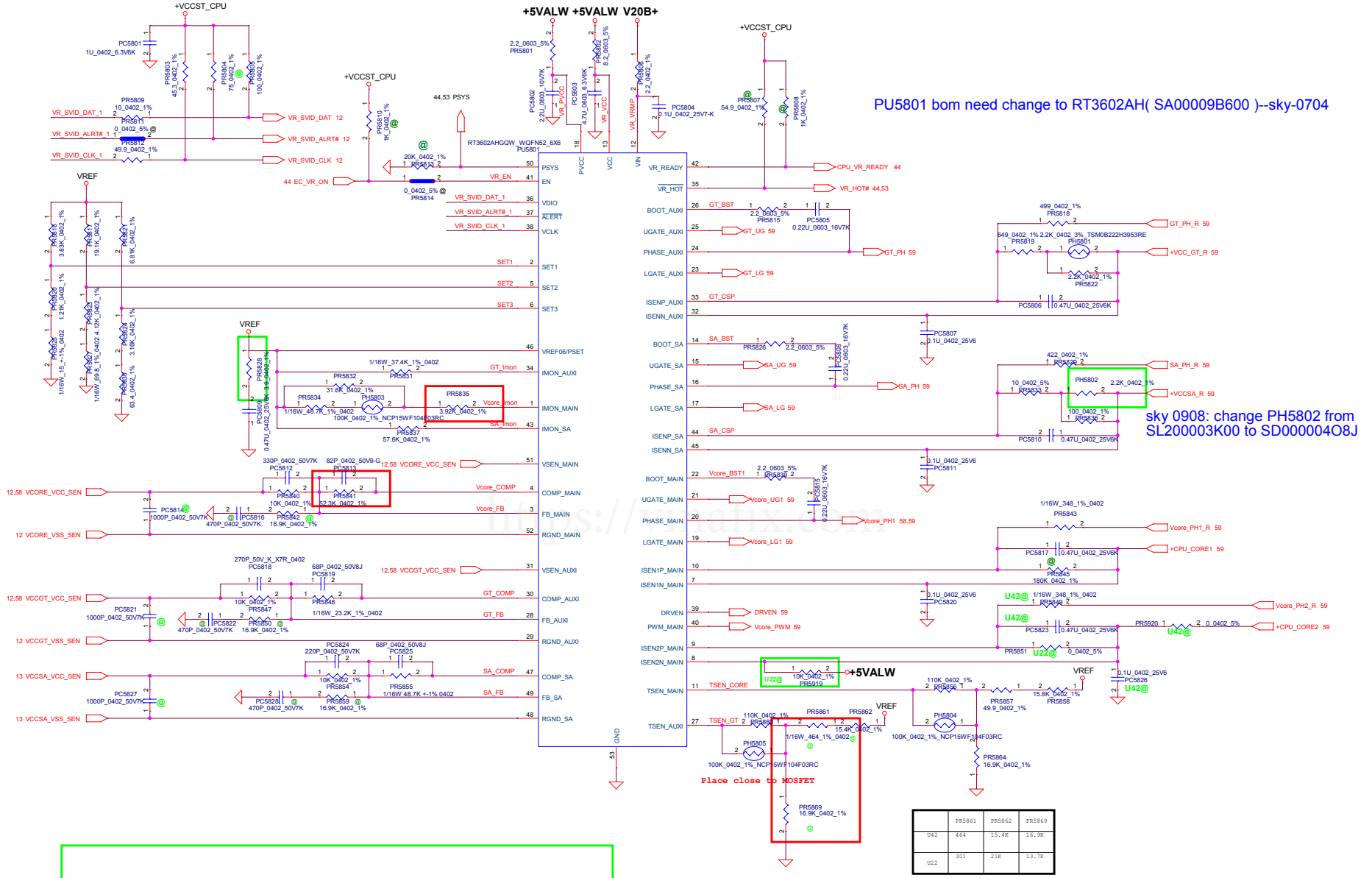
PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(KΩ)	PR816	6.19	20
R2(KΩ)	PR812	20.5	20
R3(KΩ)	PR815	4.32	2
R4(KΩ)	PR813	16.5	18
R5(KΩ)	PR818	0.309	0
C(nF)	PC826	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title	PWR-VGA_CORE		
Size: Custom	Document Number: 140S-WHL		Rev: 0.3
Date: Wednesday, May 29, 2019	Sheet 57 of 60		



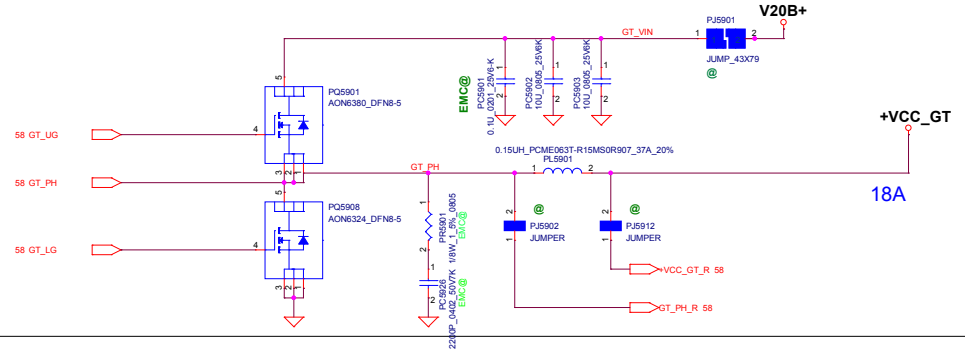
	PR5861	PR5862	PR5869
U42	464	15.4K	16.9K
U22	301	21K	13.7K

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

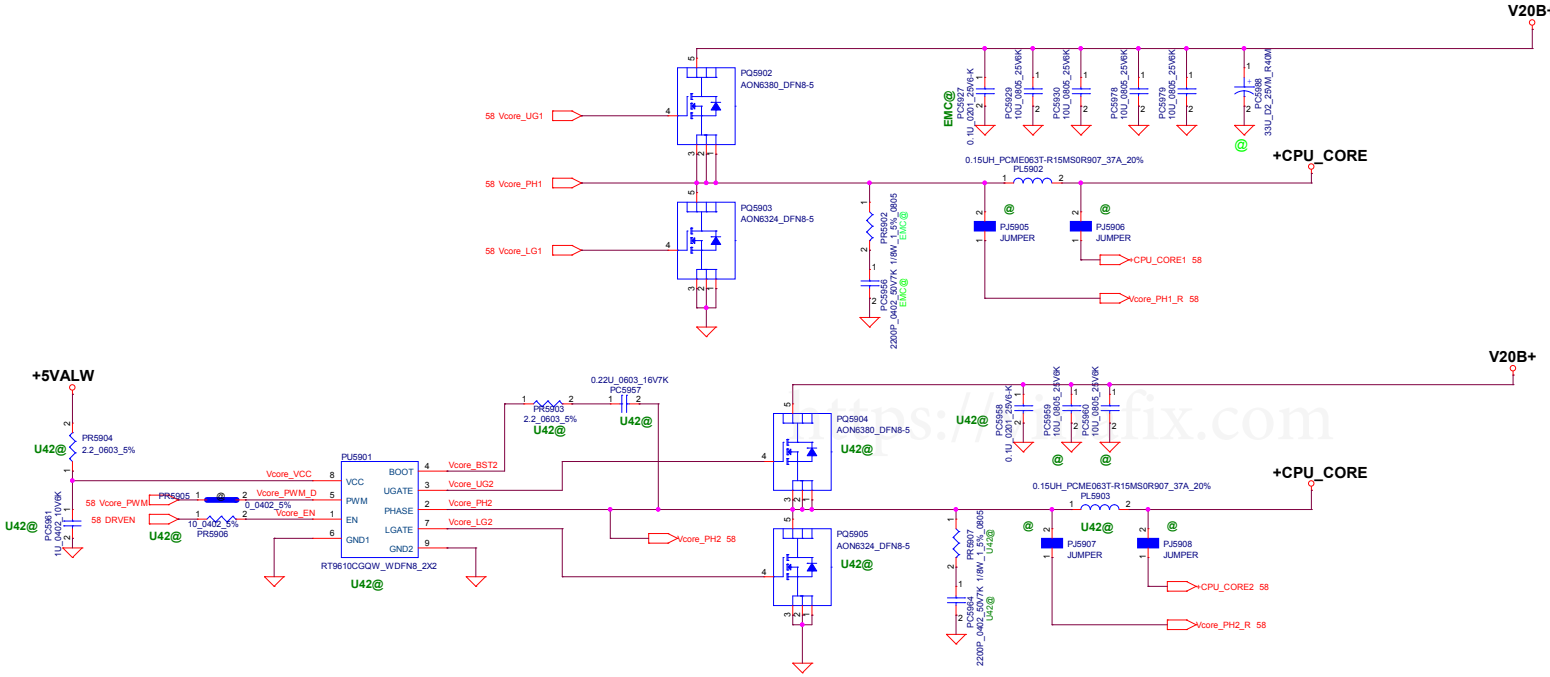
Title: PWR-CPU-CORE-1

Size: A2 | Document Number: 140S-WHL | Rev: 0.3

Date: Wednesday, May 29, 2019 | Sheet 58 of 61



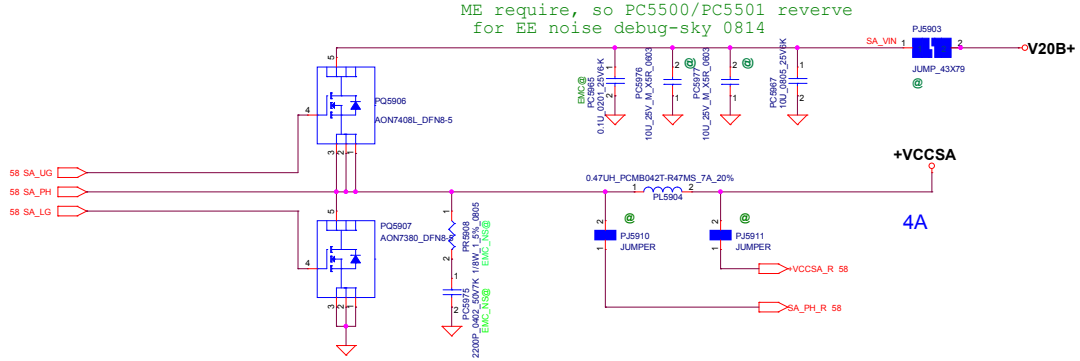
Vboot=0V Loadline=3.1mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=18A Iccmax=31A OCP=37A
OVP=VID+370mV~VID+430mV
Max Overshoot:70mv/10us
UVP=VID-370mV~VID-225mV
Fsw=550Khz



U22 :21A
U42: 48A

Vboot=0V Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=21A/48A Iccmax=32A/70A
OCP=37A / 74A
Max Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz

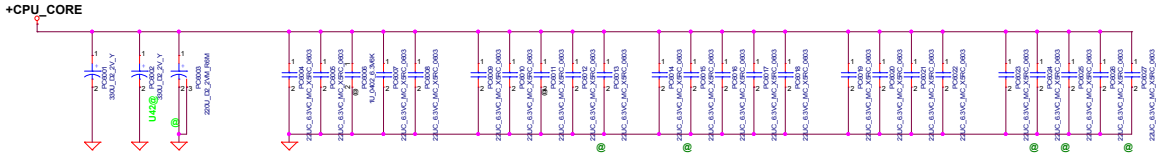
ME require, so PC5500/PC5501 reverve
for EE noise debug-sky 0814



Vboot=0V Loadline=10.3Ω
Ripple=+30mV/-10mV(0A~0.5A)
Ripple=±10mV(0.5A~TDC)
Ripple=±15mV(TDC~Iccmax)
TDC=4A Iccmax=4.5A OCP=7A
Max Overshoot:70mv/10us
OVP=VID+370mV~VID+430mV
UVP=VID-370mV~VID-225mV
Fsw=550Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2018/07/10	Deciphered Date	2018/07/10

Title: PWR-CPU-CORE-2
Size: A2
Document Number: 140S-WHL
Rev: 0.3
Date: Wednesday, May 29, 2019
Sheet 59 of 61

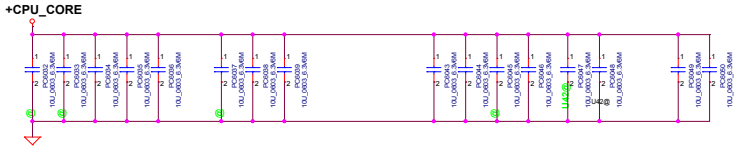


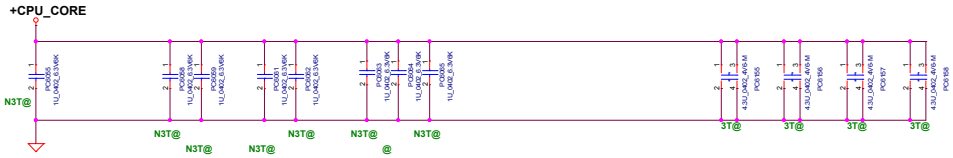
CPU_CORE: 2PCS_330U_D2_2V+1PCS_220U_D2_2V
+13PCS_22U_0603_6V+18PCS_10U_0402_6V
+16PCS_1U_0201_6V=

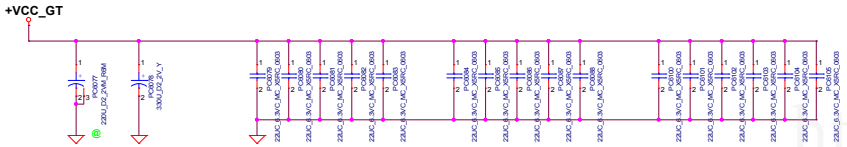
Vender modify_20180705
PC6003 @ and stuff 6 pcs 22U/0603

sky modify_20180709
change 10U/0402 to 10U/0603, 1U/0201 to 1U/0402

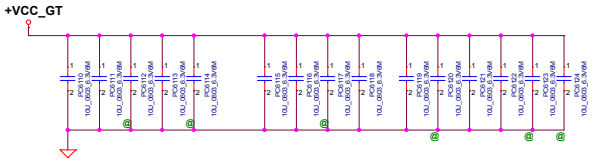
sky modify_20180925
layout change PC6024/PC6025 to PC6036/PC6046

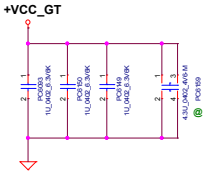


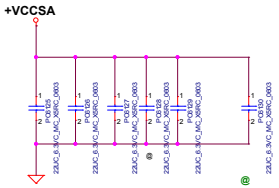


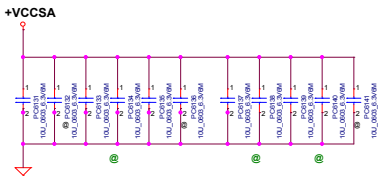


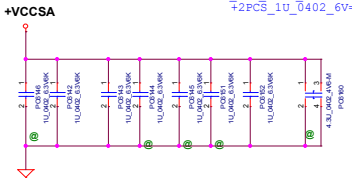
VCCGT: 1PCS_330U_D2_2V+1PCS_220U_D2_2V
+10PCS_22U_0603_6V+9PCS_9U_0603_6V
+2PCS_1U_0402_6V= sky_07_09











VCCSA:5PCS_22U_0603_6V+6PCS_10U_0603_6V
+2PCS_1U_0402_6V=07-09 sky

Security Classification	LC Future Center Secret Data		
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Title: PWR-CPU Decoupling Cap

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Date: Wednesday, May 29, 2019	Sheet 69 of 81	