

# LCFC Confidential


## BMWC1&C2 M/B Schematics Document

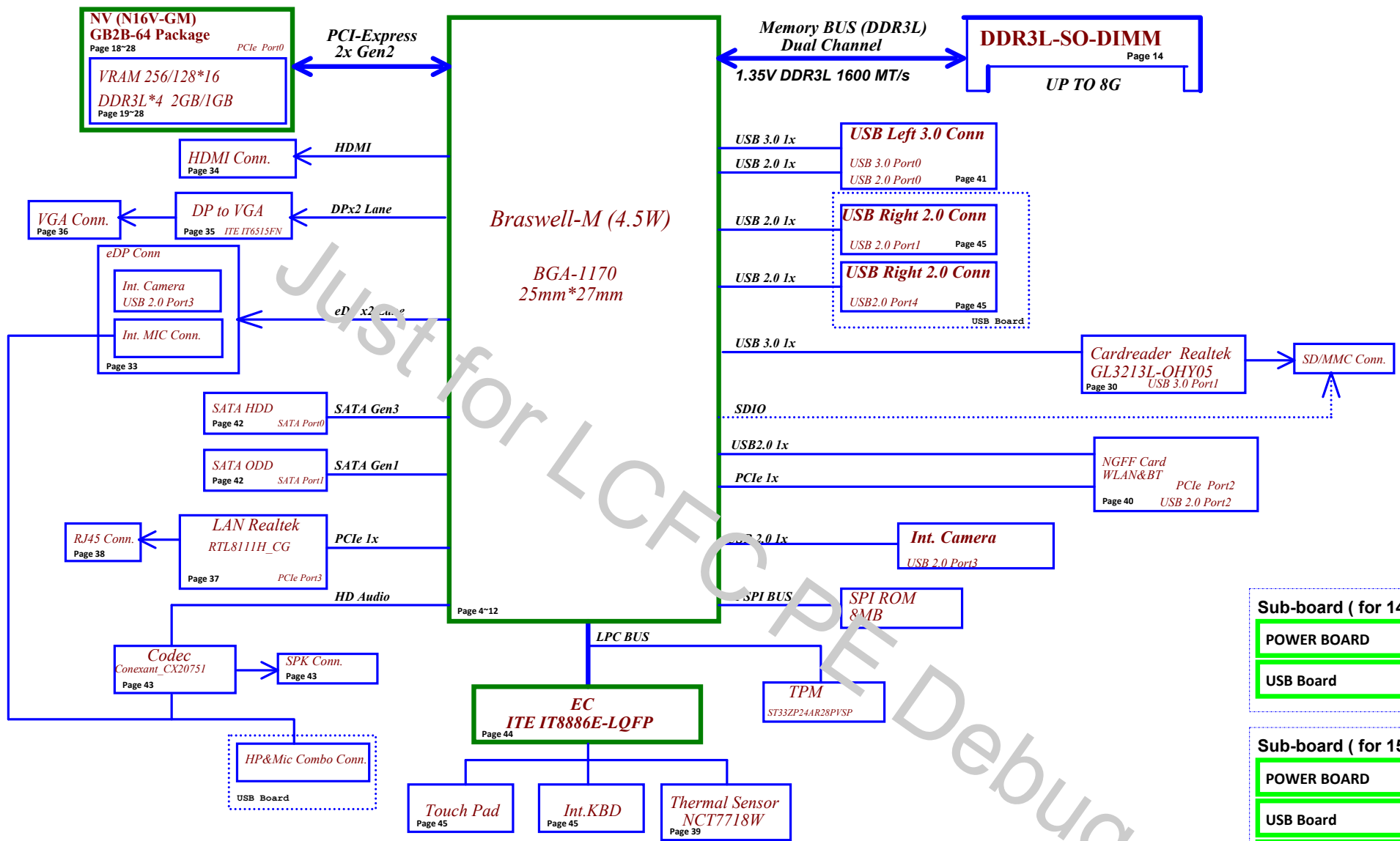
NM-A471 REV:0.4

Intel Braswell M-Processor with DDR3L + NV (N16V-GM) GPU

2015-03-23

REV: 0.4

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Power Plane \ State	B+	+3VALW +3VL	+3VALW_SOC +1.0VALW +5VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS  +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	GPU Part
UMA@	UMA SKU ID part
14@	For 14" part
15@	For 15" part
100M@	100M LAN part
N15SGT@	N15SGT Part
N15VGM@	N15GSM Part
GIGA@	GIGA LAN Part
GC6@	GPU GC6 Part
TS@	Touch Screen part
RANKA@	GPU VRAM RANKA PART
RANKB@	GPU VRAM RANKB PART
ME@	Connector
CD@	COST DOWN
@	Not stuff
H4T@	Hynix VRAM Part
M4T@	Micron VRAM Part
S4T@	Samsung VRAM Part

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1	EC		V	V	X	X	X	X	X	V
EC_SMB_DA1	+3VALW	X	V	+3VALW	X	X	X	X	X	V
EC_SMB_CK2	EC	V		V	X	X	V	X	X	X
EC_SMB_DA2	+3VS	+3VGS	X	+3VS	X	X	+3VS	X	X	X
PCH_SMB_CLK	PCH				V	V	X	V	X	X
PCH_SMB_DATA	+3VALW_PCH	X	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X

PCIe PORT LIST

Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Address
Smart Battery	0001 011X b
Charger	need to update
Thermal Sensor EMC1403-2	1001_100xb(reserve)
VGA	0x9E(base on NV default)

Device	Address
DDR DIMMA	1010 000Xb
Wlan	Rsvd
TP	need to update

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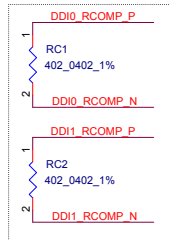
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Title: Notes List

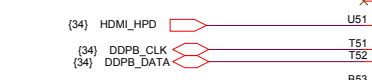
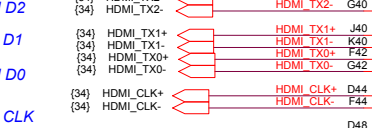
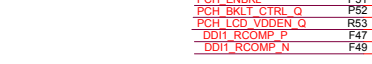
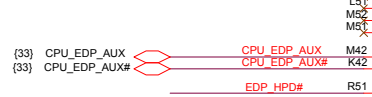
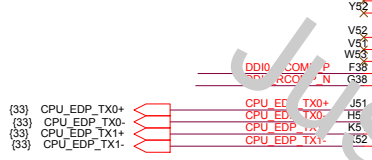
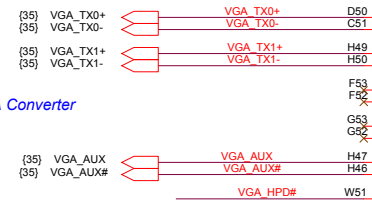
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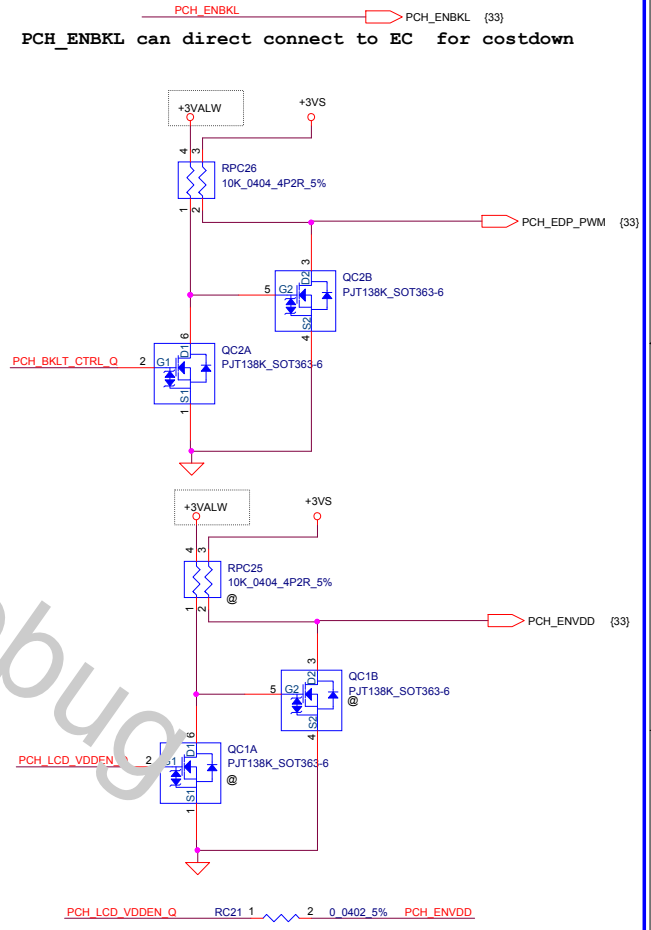
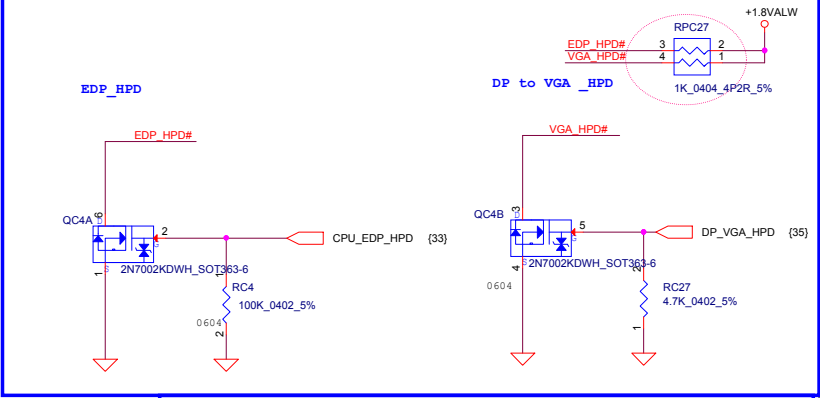
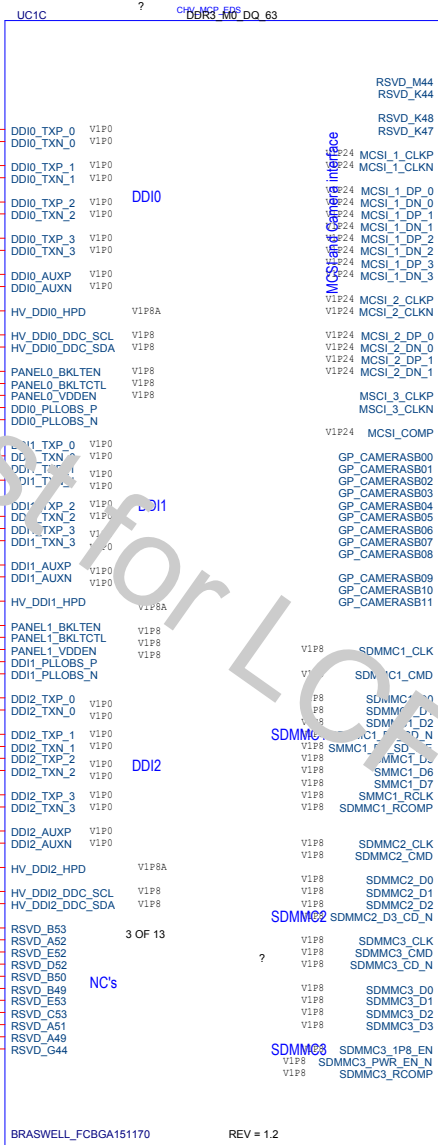
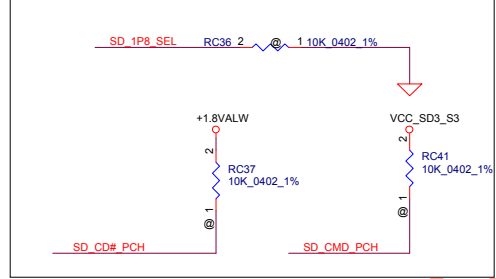


DP TO VGA Converter



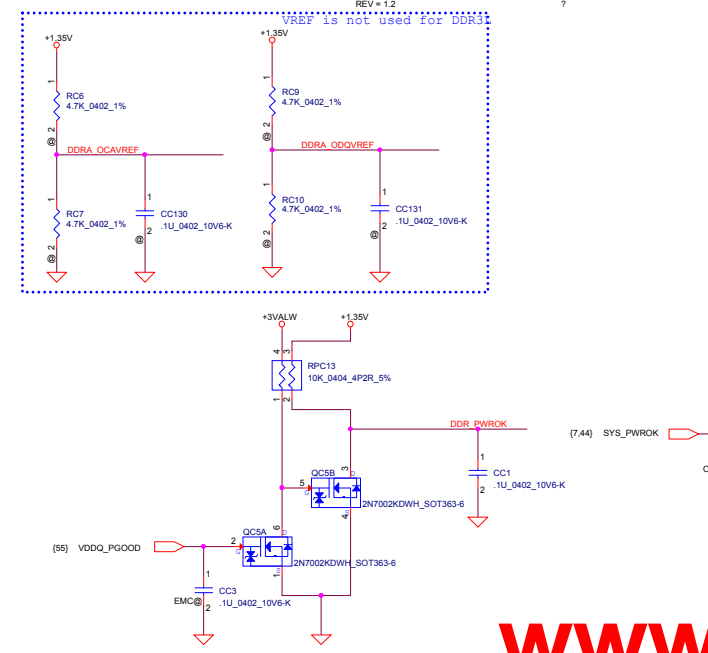
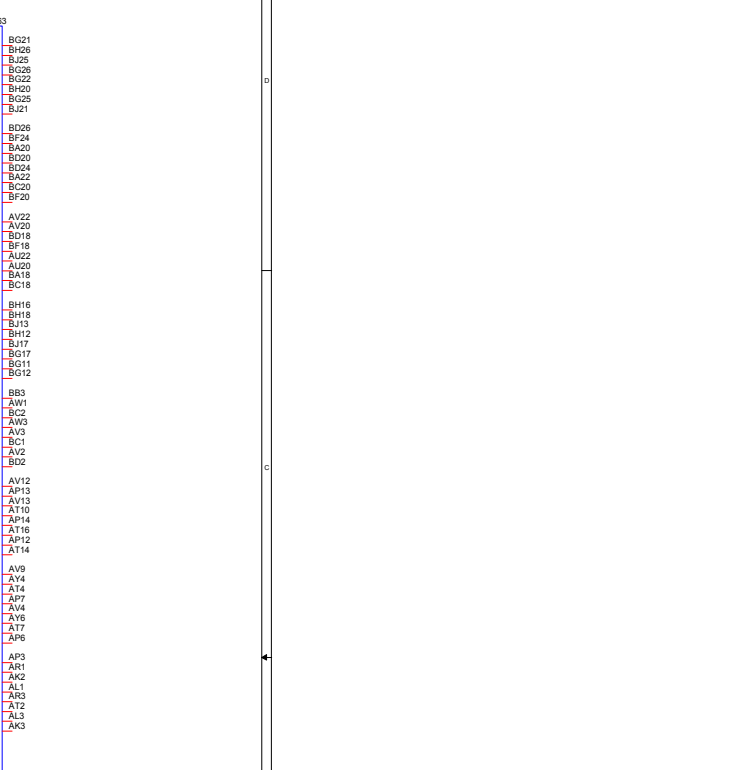
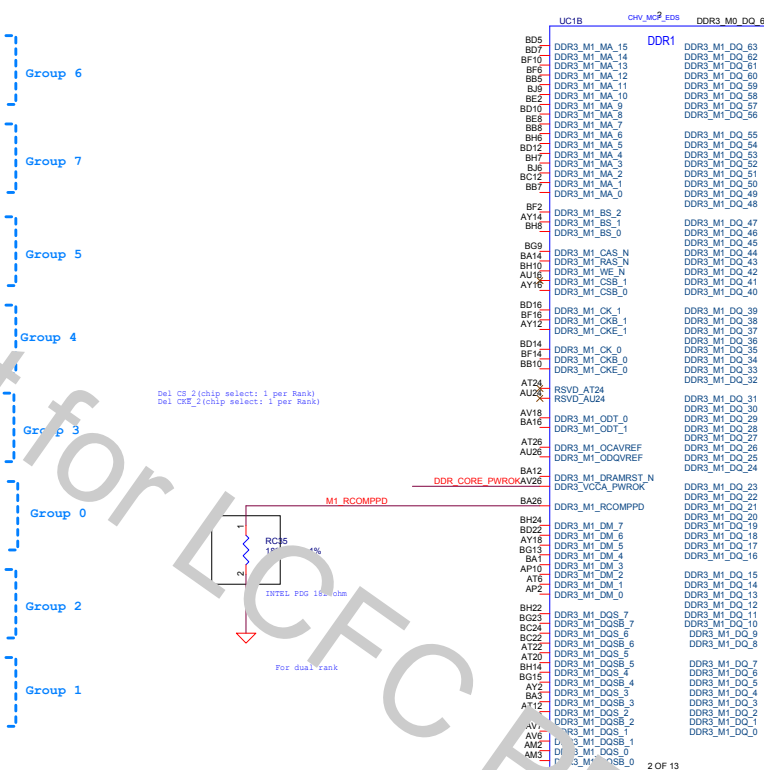
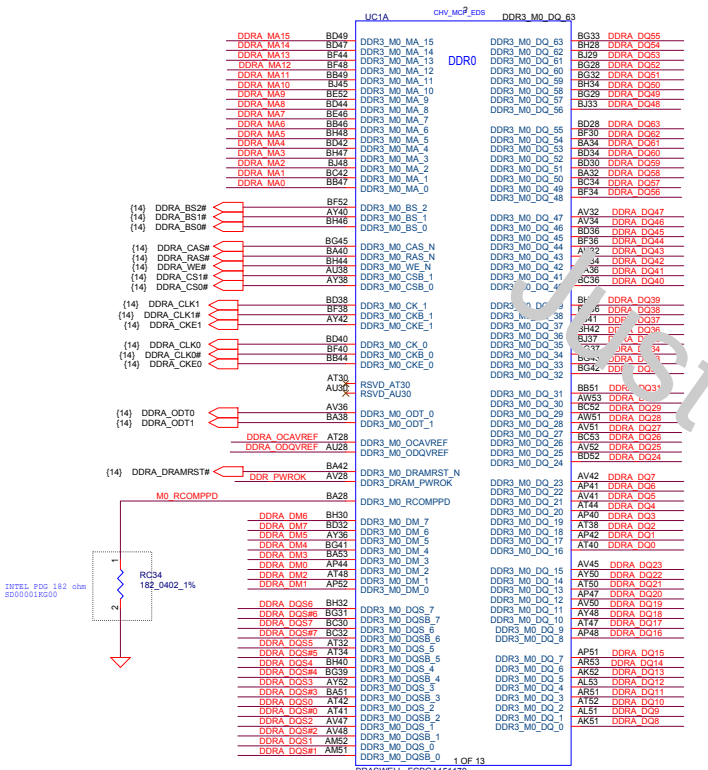
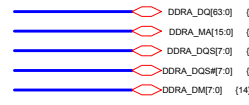
DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI



PCH LCD VDDEN\_Q VOH min is 1.8-0.45=1.35V, need level shift

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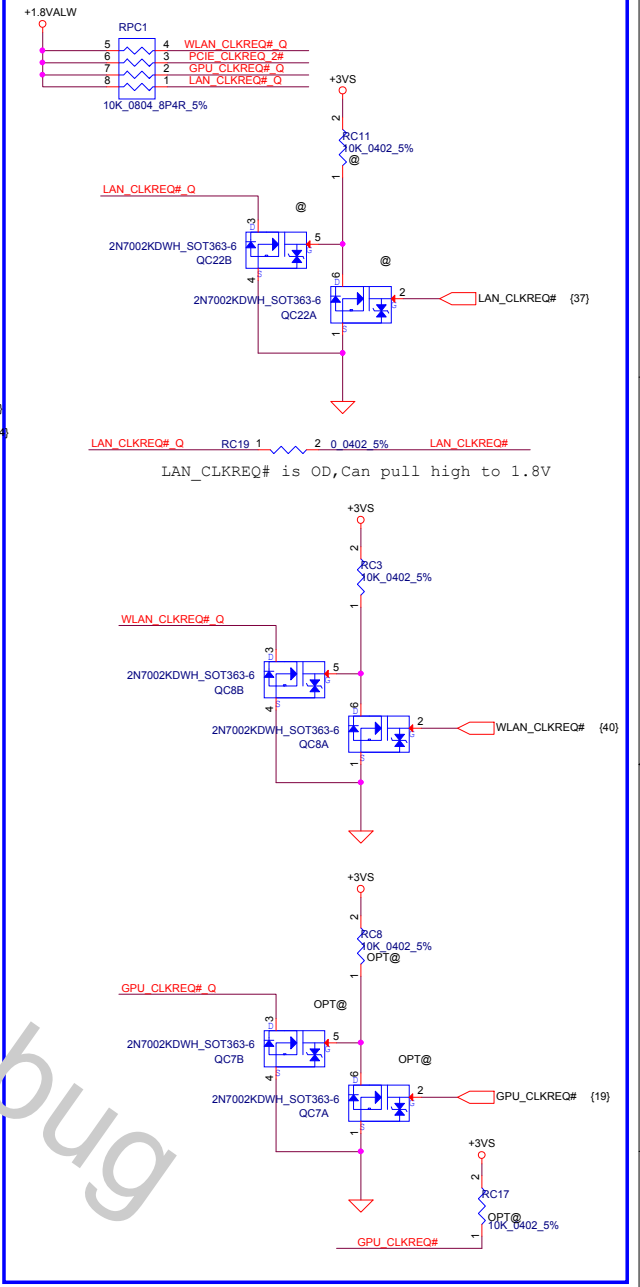
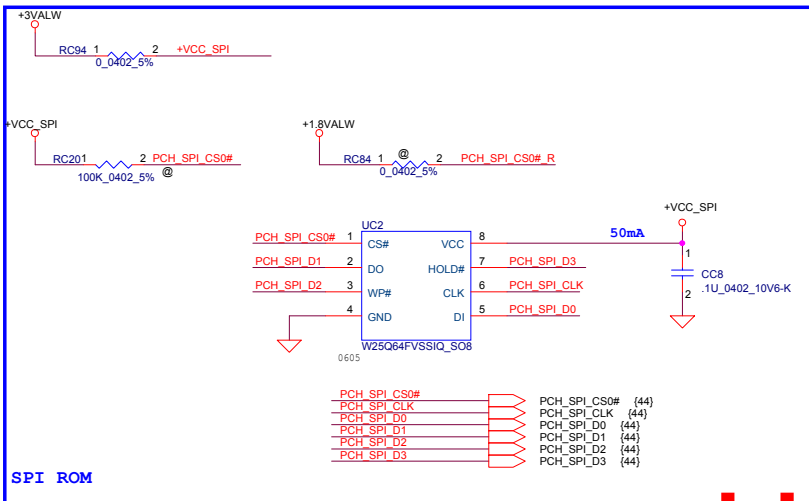
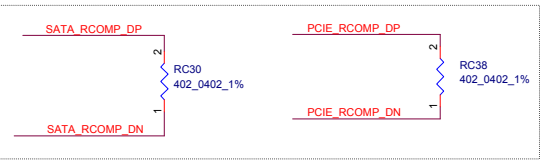
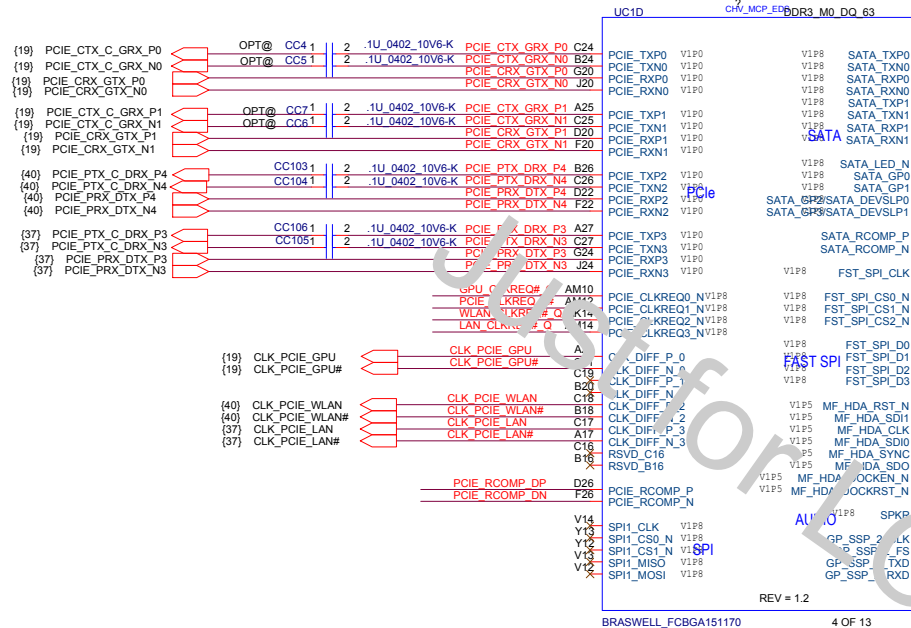


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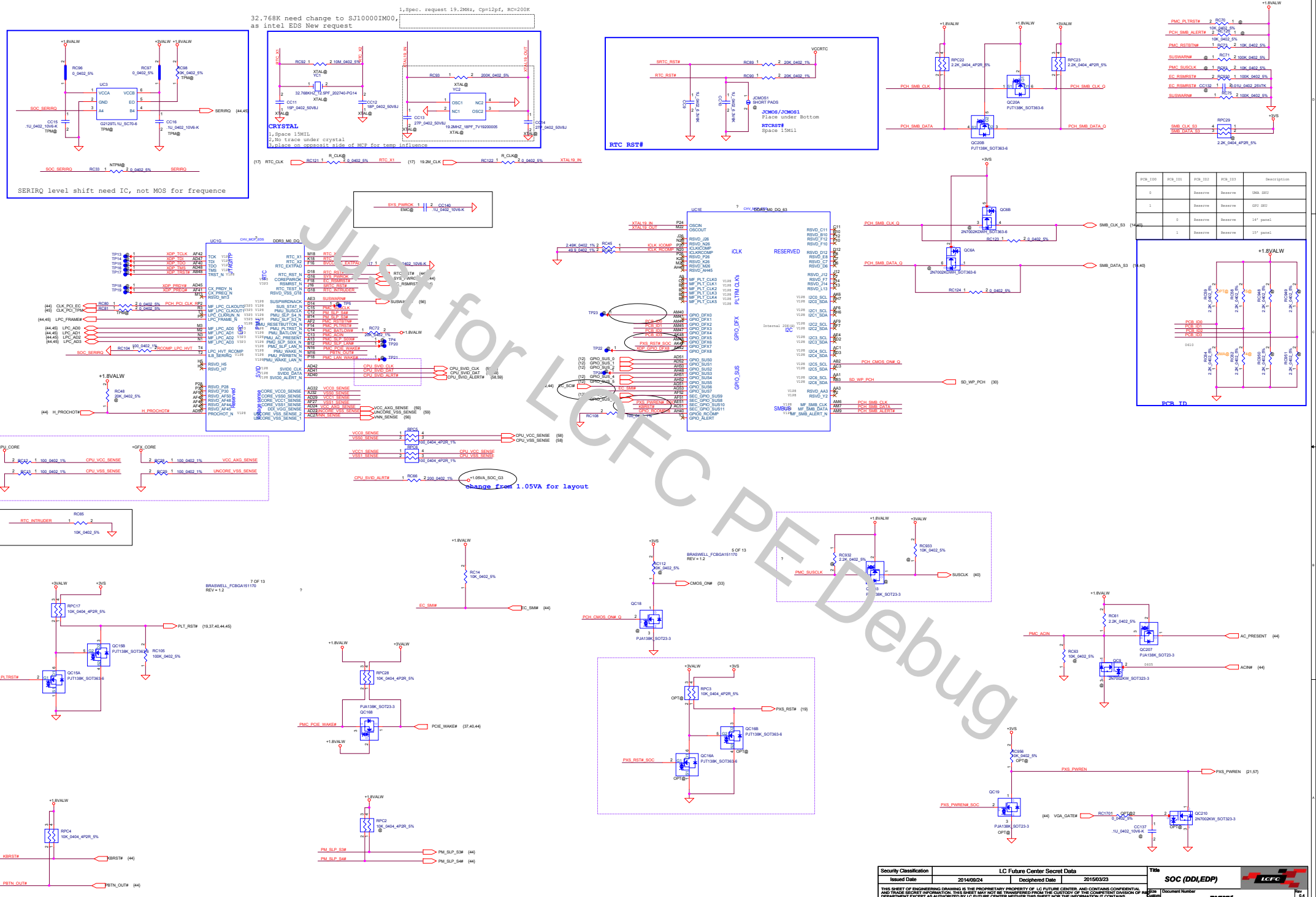
dGPU

WLAN

LAN



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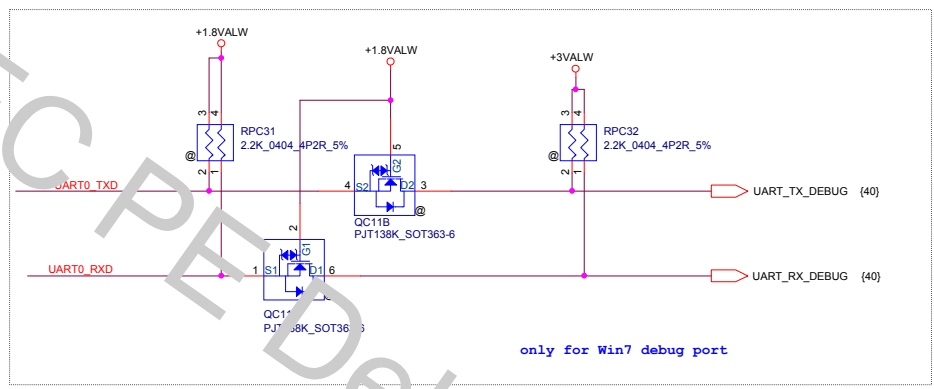
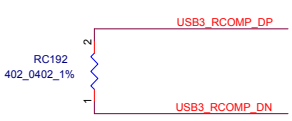
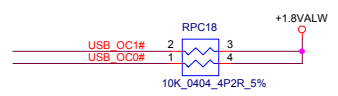
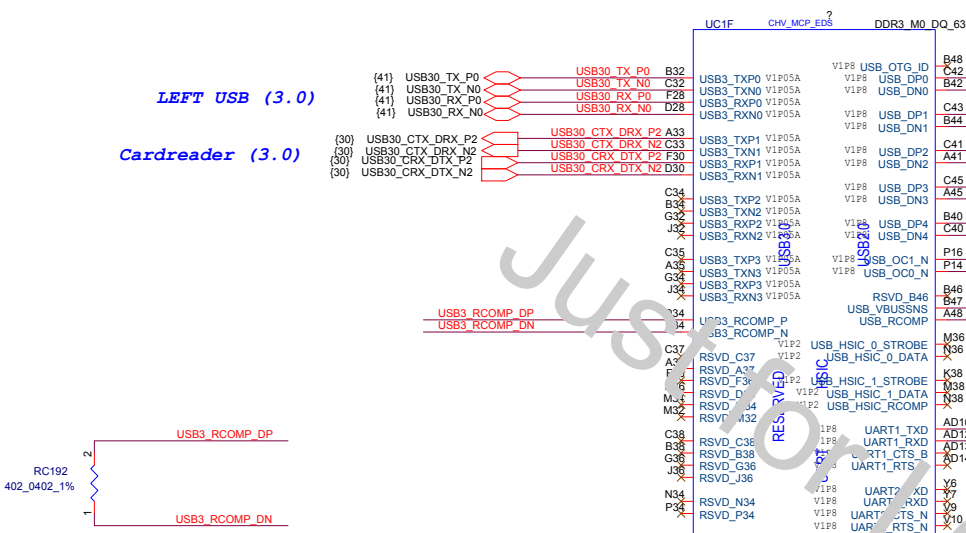
32.768K need change to SJ100001M00,  
as intel BDS New request

change from 1.05VA for layout

PCB_100	PCB_101	PCB_102	PCB_103	Description
0	Reserved	Reserved	Reserved	00K_000
1	Reserved	Reserved	Reserved	020_000
2	Reserved	Reserved	Reserved	147_pascal
3	Reserved	Reserved	Reserved	157_pascal

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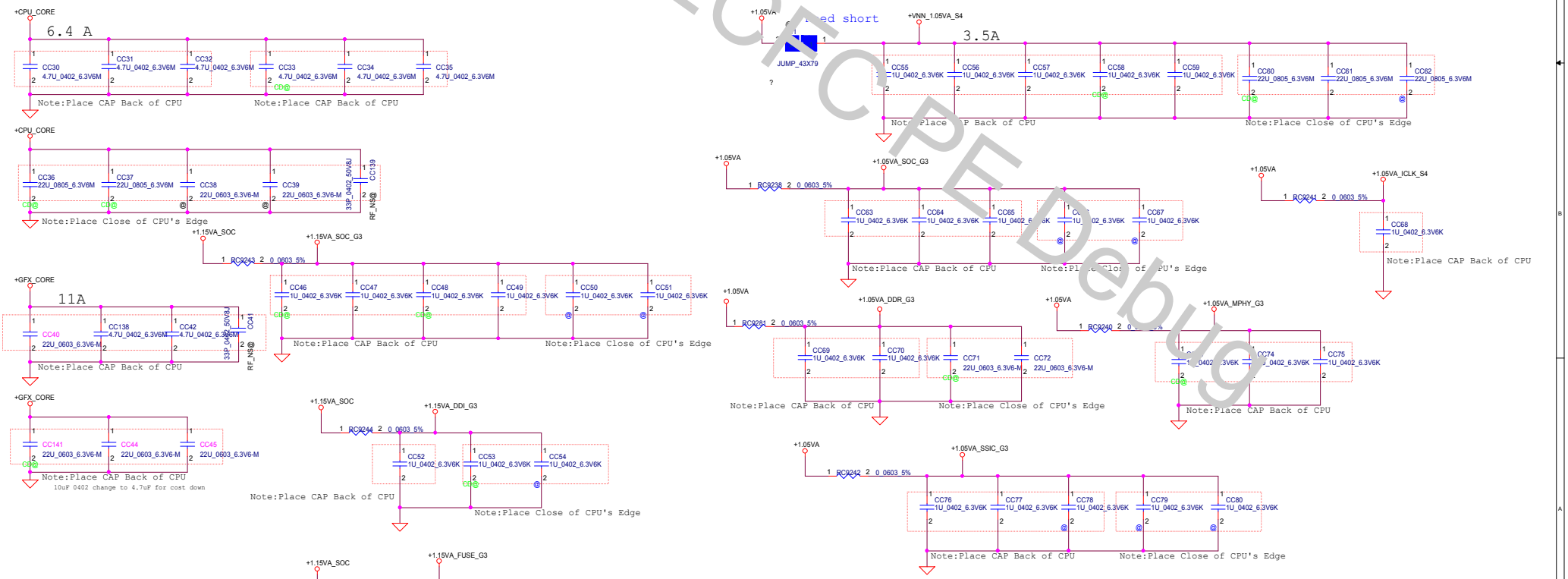
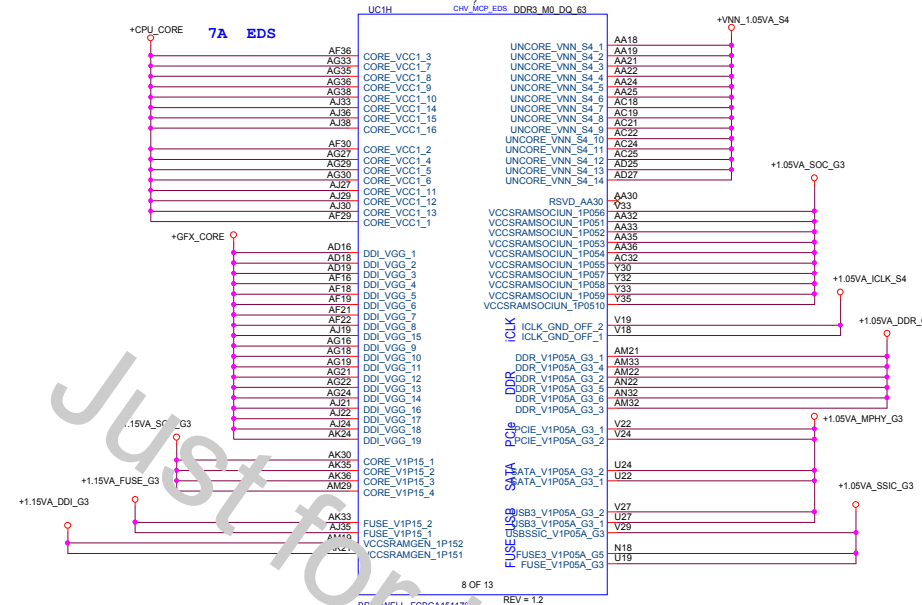


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BRASWELL\_FCBGA151170  
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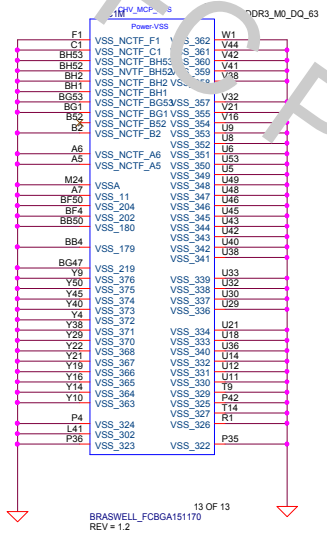
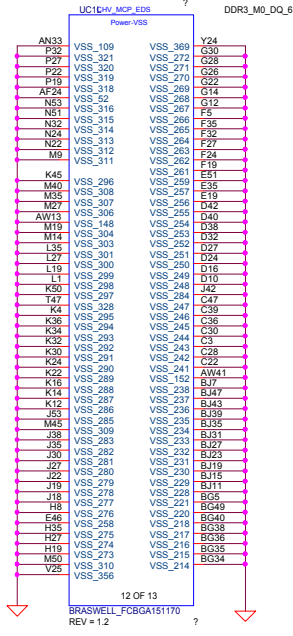
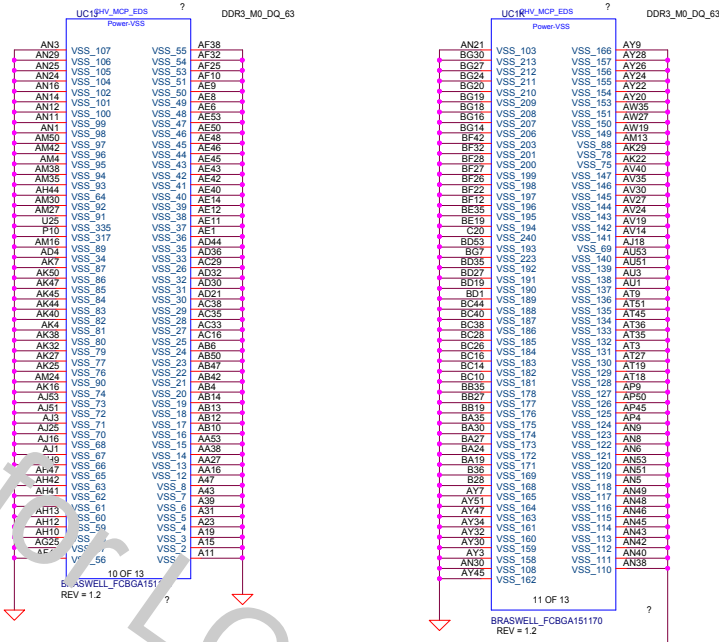




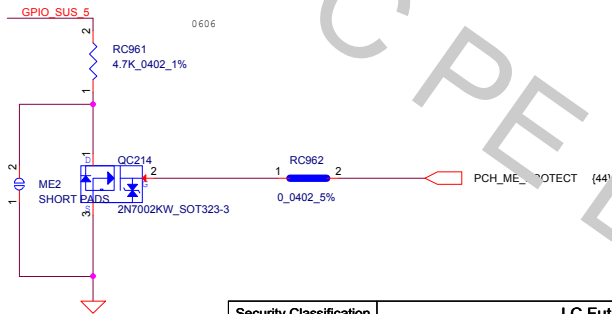
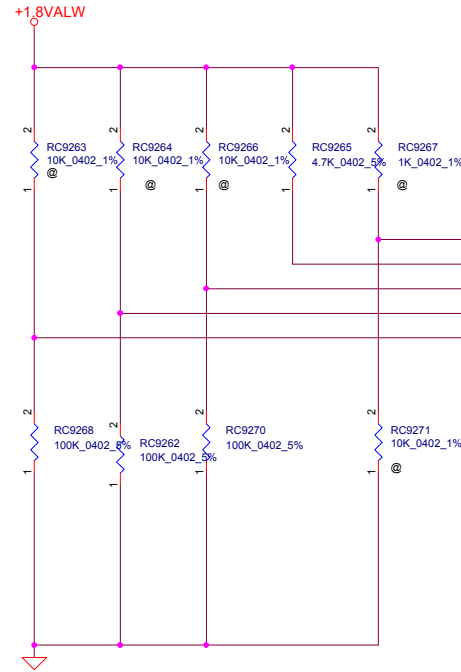
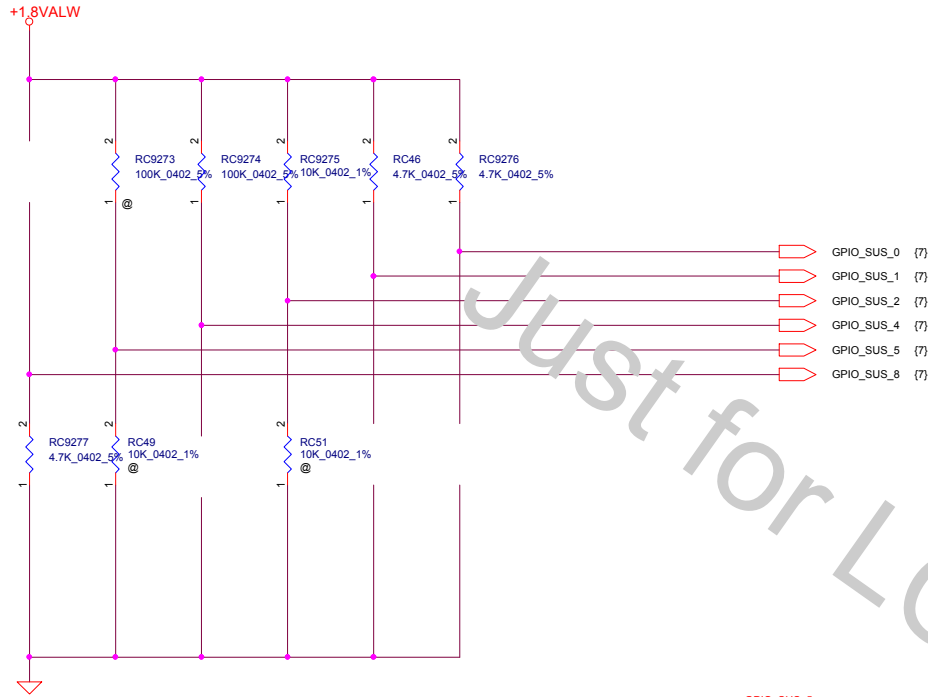
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**Hardware STRAPS  
(Follow up CRB)**




- GPIO\_SUS\_9 {7}
- EC\_SCI# {7,44}
- GPIO\_CAM\_8 {4}
- GPIO\_CAM\_9 {4}
- GPIO\_CAM\_11 {4}

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak Internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak Internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak Internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak Internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected <b>Note:</b> DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak Internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak Internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak Internal (20k PU)	1 = Normal Operation <b>Note:</b> This strap <b>MUST</b> be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak Internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak Internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak Internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak Internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak Internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

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Just for LCFC PE Debug

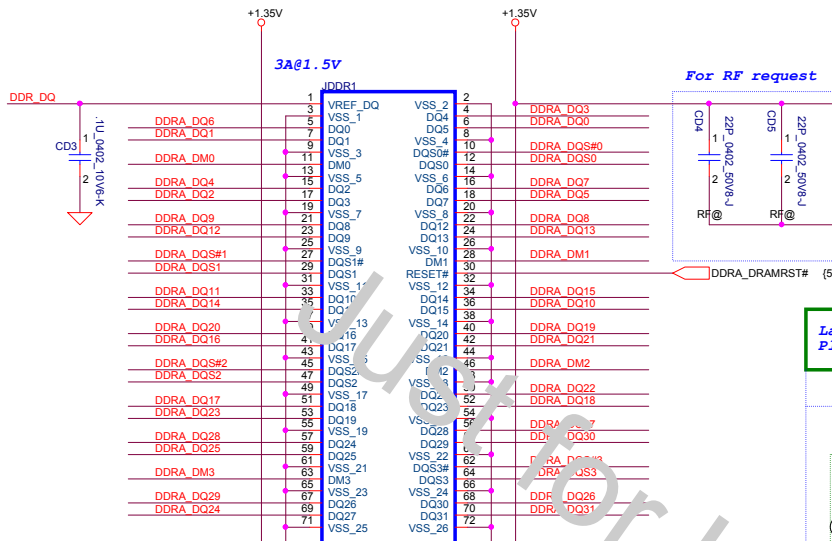
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# DDR3 SO-DIMM A

DDR Mapping table

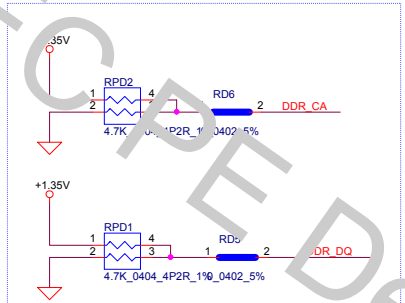
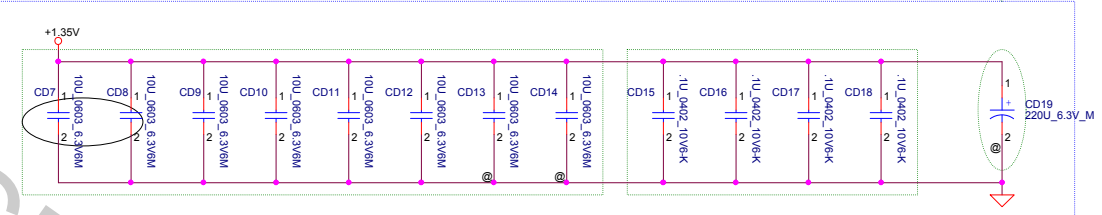
DDR3 Pin	DDR3 Signal	DDR3 Pin	DDR3 Signal
1	VREF_DQ	2	VSS_2
2	VSS_1	3	DQ0
3	DQ0	4	DQ5
4	DQ5	5	VSS_4
5	VSS_4	6	DQ10
6	DQ10	7	DQ15
7	DQ15	8	DQ20
8	DQ20	9	DQ25
9	DQ25	10	DQ30
10	DQ30	11	DQ35
11	DQ35	12	DQ40
12	DQ40	13	DQ45
13	DQ45	14	DQ50
14	DQ50	15	DQ55
15	DQ55	16	DQ60
16	DQ60	17	DQ65
17	DQ65	18	DQ70
18	DQ70	19	DQ75
19	DQ75	20	DQ80
20	DQ80	21	DQ85
21	DQ85	22	DQ90
22	DQ90	23	DQ95
23	DQ95	24	DQ100
24	DQ100	25	DQ105
25	DQ105	26	DQ110
26	DQ110	27	DQ115
27	DQ115	28	DQ120
28	DQ120	29	DQ125
29	DQ125	30	DQ130
30	DQ130	31	DQ135
31	DQ135	32	DQ140
32	DQ140	33	DQ145
33	DQ145	34	DQ150
34	DQ150	35	DQ155
35	DQ155	36	DQ160
36	DQ160	37	DQ165
37	DQ165	38	DQ170
38	DQ170	39	DQ175
39	DQ175	40	DQ180
40	DQ180	41	DQ185
41	DQ185	42	DQ190
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- DDR3\_A1[0..7] (5)
- DDR3\_A2[0..7] (5)
- DDR3\_A3[0..15] (5)
- DDR3\_A4[7..0] (5)

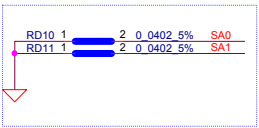
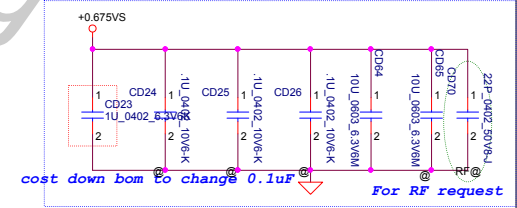
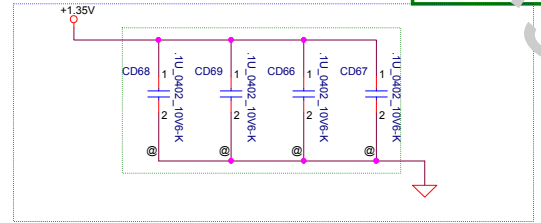
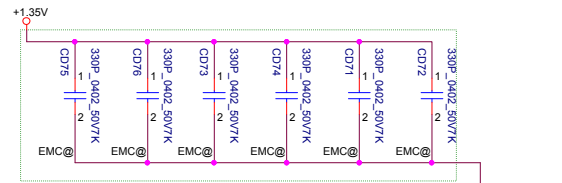


Layout Note:  
Place near DIMM

OSCON (220uF\_6.3V\_4.2L\_ESR17m)\*1=(SF00002Y00)  
(10uF\_0603\_6.3V)\*8  
(0.1uF\_402\_10V)\*4



Layout Note:  
Place near DIMM



Security Classification	LC Future Center Secret Data
Issued Date	2014/09/24
Deciphered Date	2015/03/23

Title	DDR3 SO-DIMM A
Document Number	BMWC1
Date	Tuesday, April 07, 2015
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Just for LCFC PE Debug

Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR8_DQ17
7	DQ1	DDR8_DQ23
15	DQ2	DDR8_DQ18
17	DQ3	DDR8_DQ21
4	DQ4	DDR8_DQ16
6	DQ5	DDR8_DQ22
16	DQ6	DDR8_DQ19
18	DQ7	DDR8_DQ20
10	DQS#0	DDR8_DQS#2
12	DQS0	DDR8_DQS2
21	DQ8	DDR8_DQ3
23	DQ9	DDR8_DQ5
33	DQ10	DDR8_DQ6
35	DQ11	DDR8_DQ1
22	DQ12	DDR8_DQ2
24	DQ13	DDR8_DQ4
34	DQ14	DDR8_DQ0
36	DQ15	DDR8_DQ7
27	DQS#1	DDR8_DQS#0
29	DQS1	DDR8_DQS0
39	DQ16	DDR8_DQ8
41	DQ17	DDR8_DQ10
51	DQ18	DDR8_DQ14
53	DQ19	DDR8_DQ15
40	DQ20	DDR8_DQ13
42	DQ21	DDR8_DQ12
50	DQ22	DDR8_DQ9
52	DQ23	DDR8_DQ11
45	DQS#2	DDR8_DQS#1
47	DQS2	DDR8_DQS1
57	DQ24	DDR8_DQ27
59	DQ25	DDR8_DQ26
67	DQ26	DDR8_DQ28
69	DQ27	DDR8_DQ24
56	DQ28	DDR8_DQ31
58	DQ29	DDR8_DQ30
68	DQ30	DDR8_DQ29
70	DQ31	DDR8_DQ25
62	DQS#3	DDR8_DQS#3
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142	DQ39	DDR8_DQ34
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165	DQ49	DDR8_DQ51
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166	DQ53	DDR8_DQ53
174	DQ54	DDR8_DQ54
176	DQ55	DDR8_DQ55
169	DQS#6	DDR8_DQS#6
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181	DQ56	DDR8_DQ62
183	DQ57	DDR8_DQ57
191	DQ58	DDR8_DQ59
193	DQ59	DDR8_DQ63
180	DQ60	DDR8_DQ56
182	DQ61	DDR8_DQ61
192	DQ62	DDR8_DQ58
194	DQ63	DDR8_DQ60
186	DQS#7	DDR8_DQS#7
188	DQS7	DDR8_DQS7

0.65A#0.75V


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Issued Date	2014/09/24	Deciphered Date	2015/03/23
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Date: Tuesday, April 07, 2015			Rev 0.4

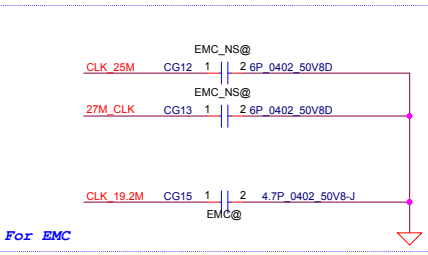
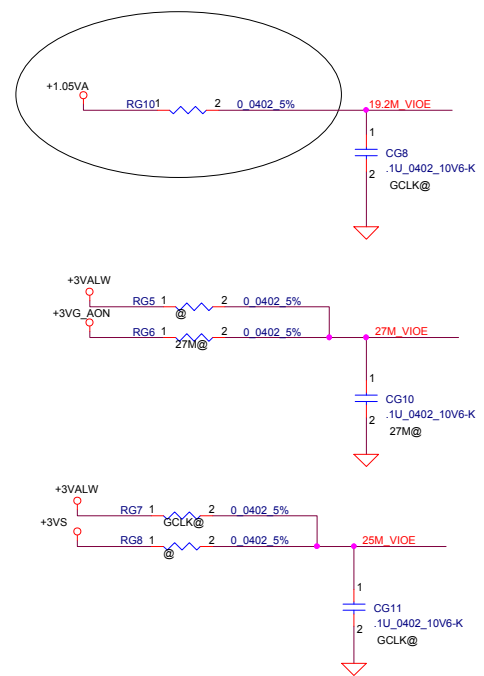
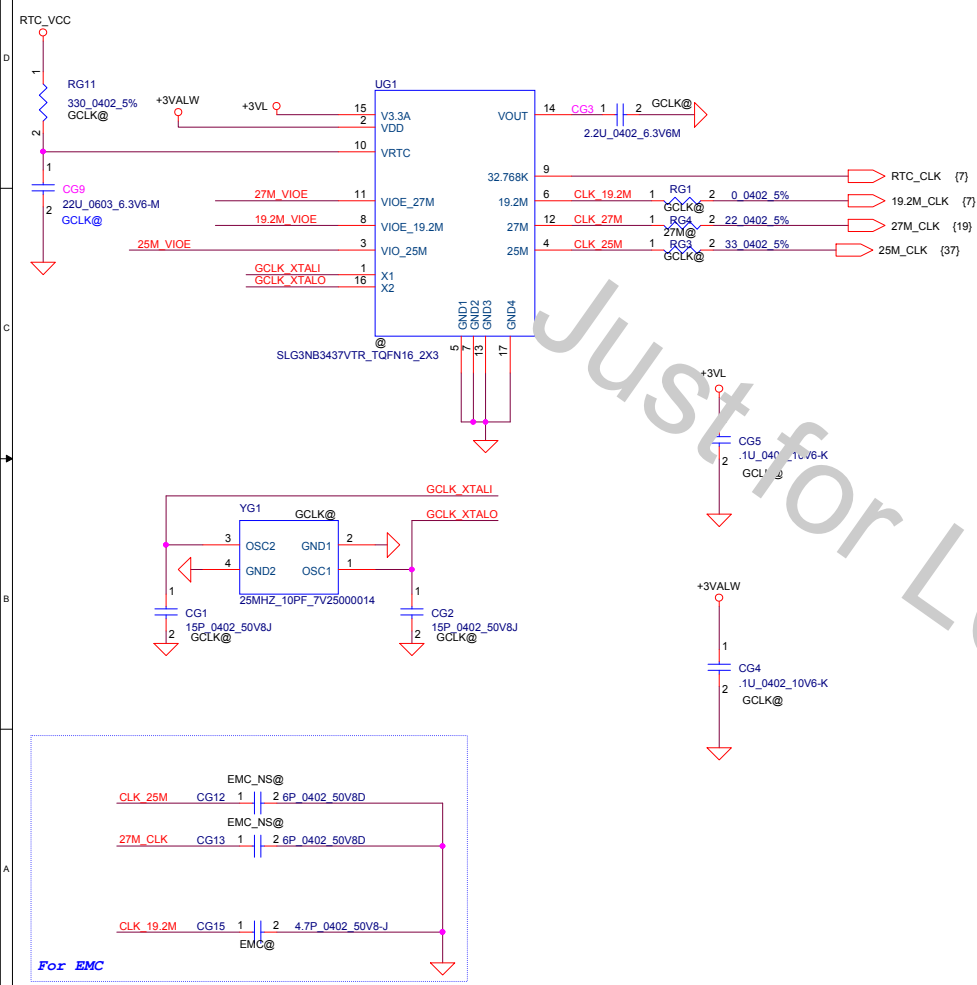


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Issued Date	2014/09/24	Deciphered Date	2015/03/23	Document Number	<b>BMWC1</b>	Rev	0.4
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Issued Date	2014/09/24	Deciphered Date	2015/03/23	Size	Document Number
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			Date:	Tuesday, April 07, 2015	Sheet 17 of 60

## N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System safe Power reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K Pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

## Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

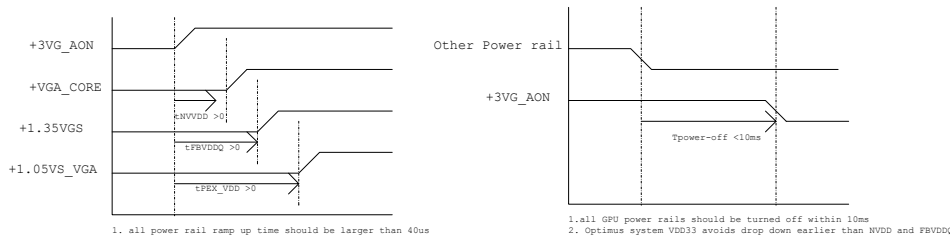
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## N15x Multi-level Straps

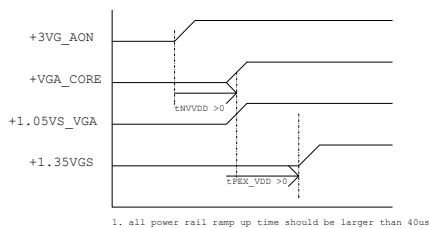
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMB_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Max GPU usage)

## N15V-GM Power Sequence



## N15S-GT Power Sequence

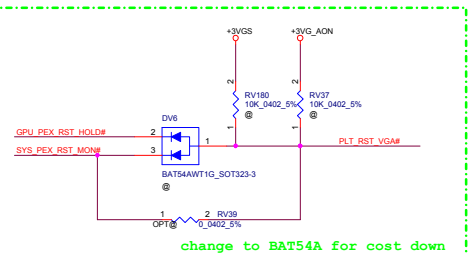
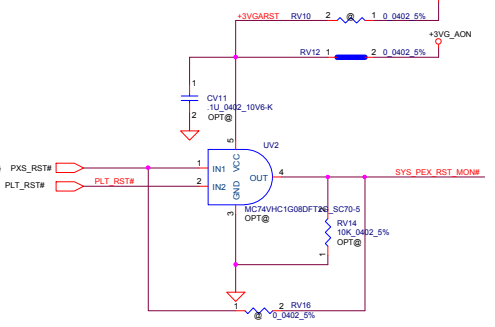
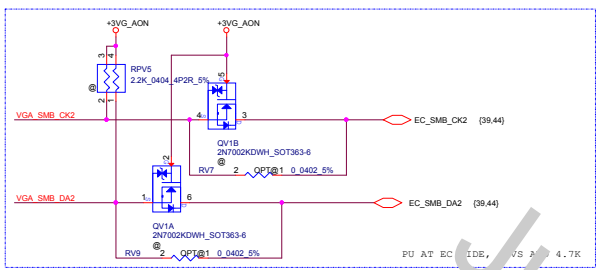


## N15x Binary Straps

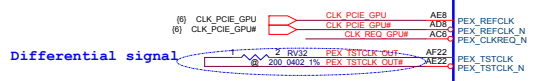
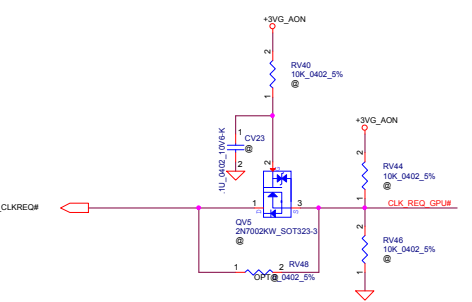
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

RV1 2 0.0402 5% FB\_GCB\_EN\_R  
 RV2 2 0.0402 5% GPU\_EVENT#

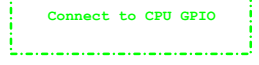
- (6) PCIe\_CRX\_GTX\_N0..1
- (6) PCIe\_CRX\_GTX\_P0..1
- (6) PCIe\_CTX\_C\_GRX\_N0..1
- (6) PCIe\_CTX\_C\_GRX\_P0..1



change to BAT54A for cost down



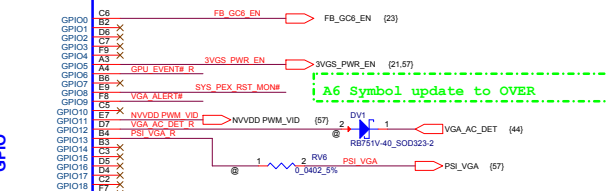
Differential signal



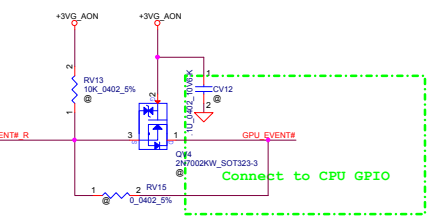
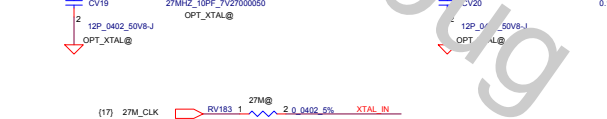
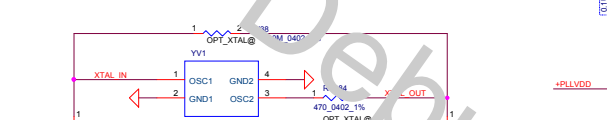
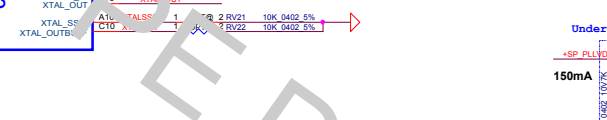
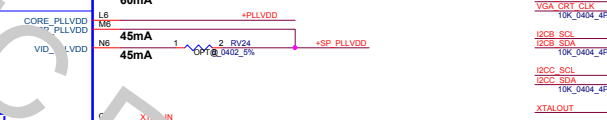
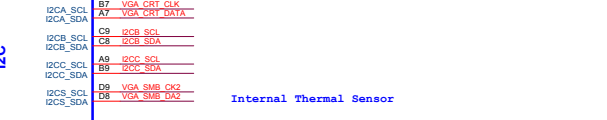
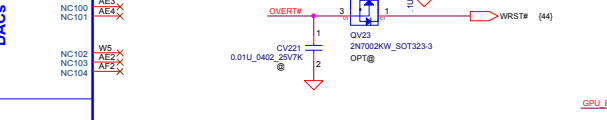
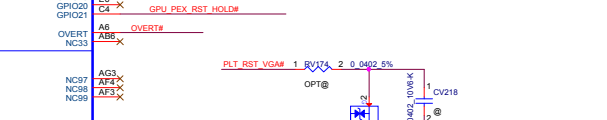
Connect to CPU GPIO

Part 1 of 6

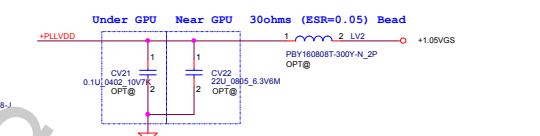
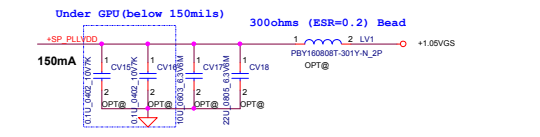
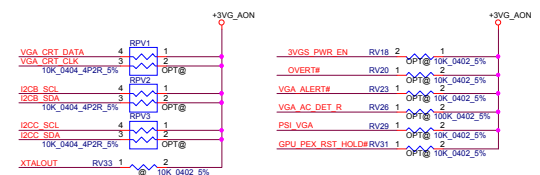
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PCIE CTX C GRX N0	AD7	PEX_RX0_N	AD8	PCIE CRX C GTX N0	AB6	PEX_TX0_N
PCIE CTX C GRX P1	AF7	PEX_RX1	AF8	PCIE CRX C GTX P1	AB10	PEX_TX1
PCIE CTX C GRX N1	AE9	PEX_RX1_N	AE8	PCIE CRX C GTX N1	AC10	PEX_TX1_N
	AF9	PEX_RX2	AF8		AD11	PEX_TX2
	AD9	PEX_RX2_N	AD8		AD12	PEX_TX2_N
	AE9	PEX_RX3	AE8		AD13	PEX_TX3
	AD9	PEX_RX3_N	AD8		AD14	PEX_TX3_N
	AE9	PEX_RX4	AE8		AD15	PEX_TX4
	AD9	PEX_RX4_N	AD8		AD16	PEX_TX4_N
	AE9	PEX_RX5	AE8		AD17	PEX_TX5
	AD9	PEX_RX5_N	AD8		AD18	PEX_TX5_N
	AE9	PEX_RX6	AE8		AD19	PEX_TX6
	AD9	PEX_RX6_N	AD8		AD20	PEX_TX6_N
	AE9	PEX_RX7	AE8		AD21	PEX_TX7
	AD9	PEX_RX7_N	AD8		AD22	PEX_TX7_N
	AE9	PEX_RX8	AE8		AD23	PEX_TX8
	AD9	PEX_RX8_N	AD8		AD24	PEX_TX8_N
	AE9	PEX_RX9	AE8		AD25	PEX_TX9
	AD9	PEX_RX9_N	AD8		AD26	PEX_TX9_N
	AE9	PEX_RX10	AE8		AD27	PEX_TX10
	AD9	PEX_RX10_N	AD8		AD28	PEX_TX10_N
	AE9	PEX_RX11	AE8		AD29	PEX_TX11
	AD9	PEX_RX11_N	AD8		AD30	PEX_TX11_N
	AE9	PEX_RX12	AE8		AD31	PEX_TX12
	AD9	PEX_RX12_N	AD8		AD32	PEX_TX12_N
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	AD9	PEX_RX14_N	AD8		AD36	PEX_TX14_N
	AE9	PEX_RX15	AE8		AD37	PEX_TX15
	AD9	PEX_RX15_N	AD8		AD38	PEX_TX15_N
	AE9	PEX_RX16	AE8		AD39	PEX_TX16
	AD9	PEX_RX16_N	AD8		AD40	PEX_TX16_N
	AE9	PEX_RX17	AE8		AD41	PEX_TX17
	AD9	PEX_RX17_N	AD8		AD42	PEX_TX17_N
	AE9	PEX_RX18	AE8		AD43	PEX_TX18
	AD9	PEX_RX18_N	AD8		AD44	PEX_TX18_N
	AE9	PEX_RX19	AE8		AD45	PEX_TX19
	AD9	PEX_RX19_N	AD8		AD46	PEX_TX19_N
	AE9	PEX_RX20	AE8		AD47	PEX_TX20
	AD9	PEX_RX20_N	AD8		AD48	PEX_TX20_N
	AE9	PEX_RX21	AE8		AD49	PEX_TX21
	AD9	PEX_RX21_N	AD8		AD50	PEX_TX21_N
	AE9	PEX_RX22	AE8		AD51	PEX_TX22
	AD9	PEX_RX22_N	AD8		AD52	PEX_TX22_N
	AE9	PEX_RX23	AE8		AD53	PEX_TX23
	AD9	PEX_RX23_N	AD8		AD54	PEX_TX23_N
	AE9	PEX_RX24	AE8		AD55	PEX_TX24
	AD9	PEX_RX24_N	AD8		AD56	PEX_TX24_N
	AE9	PEX_RX25	AE8		AD57	PEX_TX25
	AD9	PEX_RX25_N	AD8		AD58	PEX_TX25_N
	AE9	PEX_RX26	AE8		AD59	PEX_TX26
	AD9	PEX_RX26_N	AD8		AD60	PEX_TX26_N
	AE9	PEX_RX27	AE8		AD61	PEX_TX27
	AD9	PEX_RX27_N	AD8		AD62	PEX_TX27_N
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	AD9	PEX_RX28_N	AD8		AD64	PEX_TX28_N
	AE9	PEX_RX29	AE8		AD65	PEX_TX29
	AD9	PEX_RX29_N	AD8		AD66	PEX_TX29_N
	AE9	PEX_RX30	AE8		AD67	PEX_TX30
	AD9	PEX_RX30_N	AD8		AD68	PEX_TX30_N
	AE9	PEX_RX31	AE8		AD69	PEX_TX31
	AD9	PEX_RX31_N	AD8		AD70	PEX_TX31_N
	AE9	PEX_RX32	AE8		AD71	PEX_TX32
	AD9	PEX_RX32_N	AD8		AD72	PEX_TX32_N
	AE9	PEX_RX33	AE8		AD73	PEX_TX33
	AD9	PEX_RX33_N	AD8		AD74	PEX_TX33_N
	AE9	PEX_RX34	AE8		AD75	PEX_TX34
	AD9	PEX_RX34_N	AD8		AD76	PEX_TX34_N
	AE9	PEX_RX35	AE8		AD77	PEX_TX35
	AD9	PEX_RX35_N	AD8		AD78	PEX_TX35_N
	AE9	PEX_RX36	AE8		AD79	PEX_TX36
	AD9	PEX_RX36_N	AD8		AD80	PEX_TX36_N
	AE9	PEX_RX37	AE8		AD81	PEX_TX37
	AD9	PEX_RX37_N	AD8		AD82	PEX_TX37_N
	AE9	PEX_RX38	AE8		AD83	PEX_TX38
	AD9	PEX_RX38_N	AD8		AD84	PEX_TX38_N
	AE9	PEX_RX39	AE8		AD85	PEX_TX39
	AD9	PEX_RX39_N	AD8		AD86	PEX_TX39_N
	AE9	PEX_RX40	AE8		AD87	PEX_TX40
	AD9	PEX_RX40_N	AD8		AD88	PEX_TX40_N
	AE9	PEX_RX41	AE8		AD89	PEX_TX41
	AD9	PEX_RX41_N	AD8		AD90	PEX_TX41_N
	AE9	PEX_RX42	AE8		AD91	PEX_TX42
	AD9	PEX_RX42_N	AD8		AD92	PEX_TX42_N
	AE9	PEX_RX43	AE8		AD93	PEX_TX43
	AD9	PEX_RX43_N	AD8		AD94	PEX_TX43_N
	AE9	PEX_RX44	AE8		AD95	PEX_TX44
	AD9	PEX_RX44_N	AD8		AD96	PEX_TX44_N
	AE9	PEX_RX45	AE8		AD97	PEX_TX45
	AD9	PEX_RX45_N	AD8		AD98	PEX_TX45_N
	AE9	PEX_RX46	AE8		AD99	PEX_TX46
	AD9	PEX_RX46_N	AD8		AD100	PEX_TX46_N



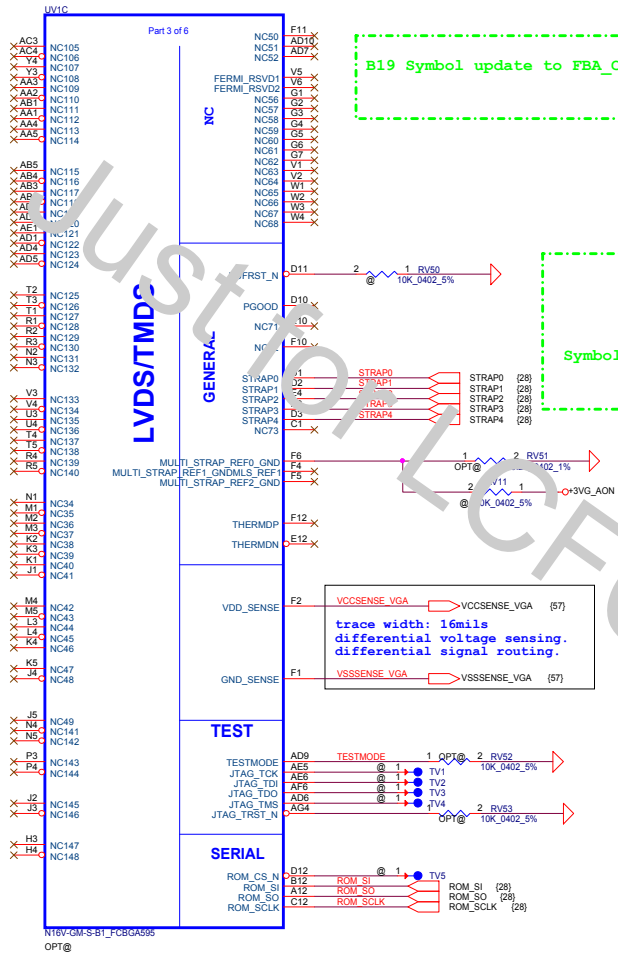
A6 Symbol update to OVER



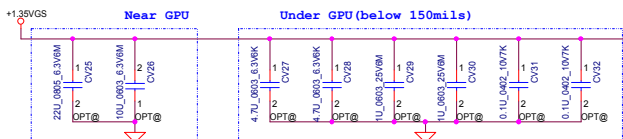
Connect to CPU GPIO



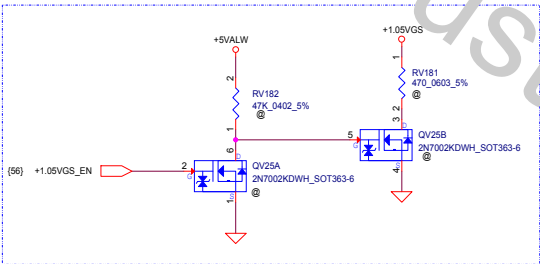
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			Document Number BMWC1
			Rev 0.4
			Date Tuesday, April 07, 2016
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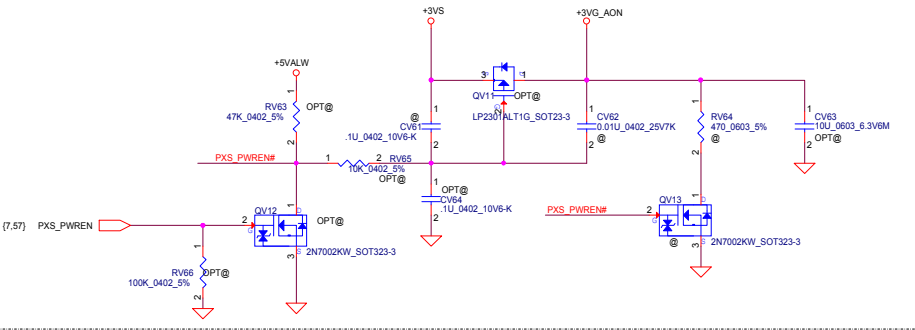
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Issued Date	2014/09/24	Deciphered Date	2015/03/23	N16X_LVDS/ HDM/ THERM	
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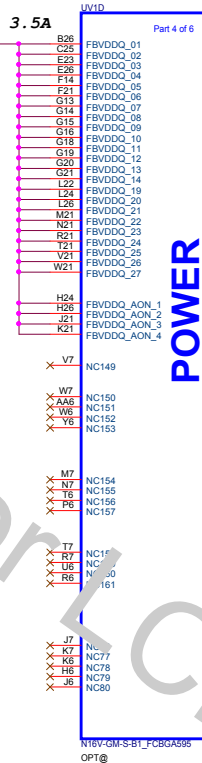
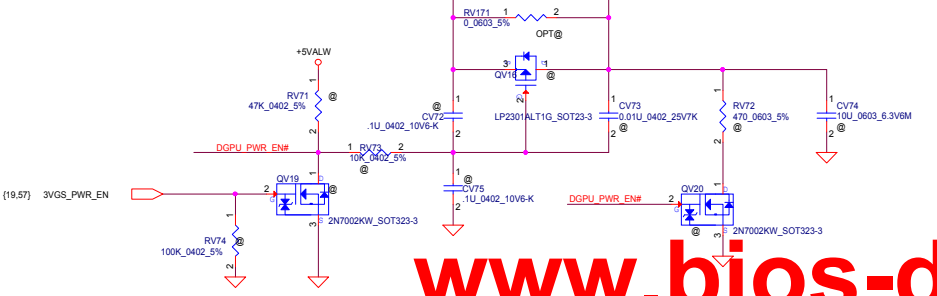
Symbol update to FBVDDQ\_AON  
H24/H26/J21/K21



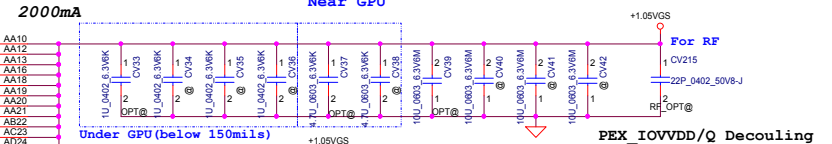
+3.3VS TO +3VG\_AON



+3.3VS TO +3VGS

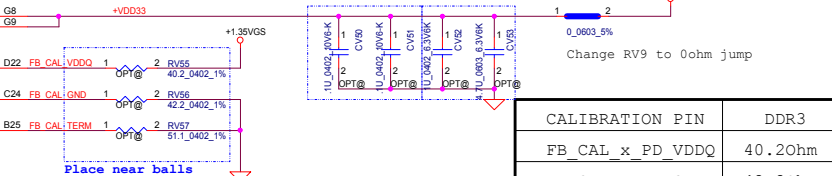
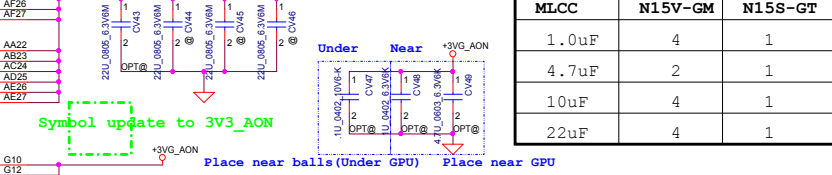


POWER



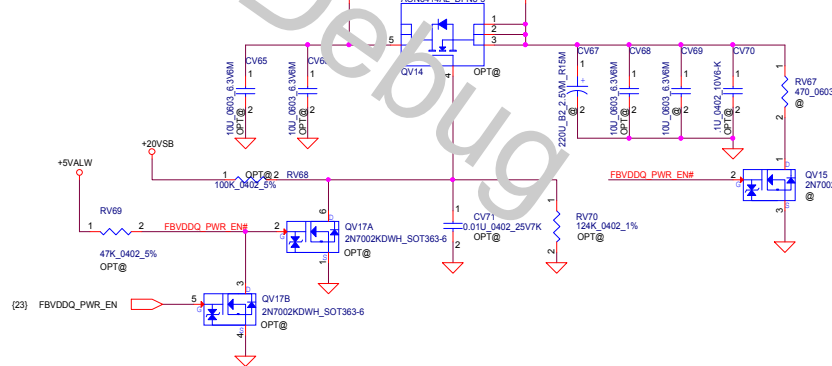
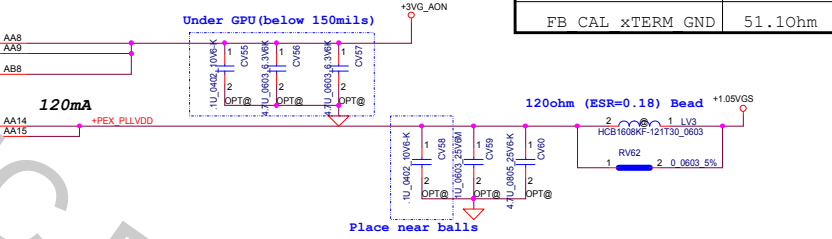
PEX\_IOVDD/Q Decoupling

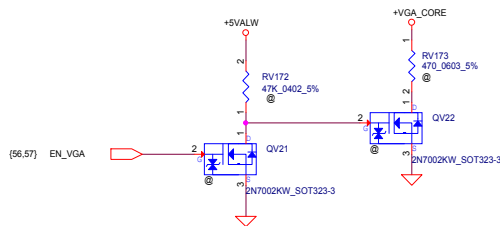
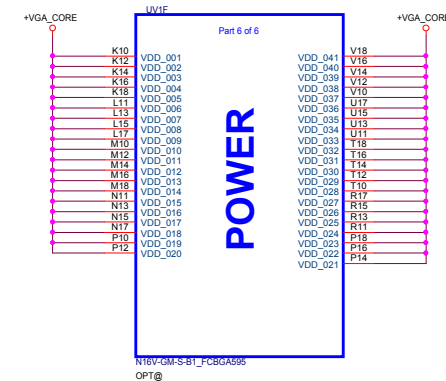
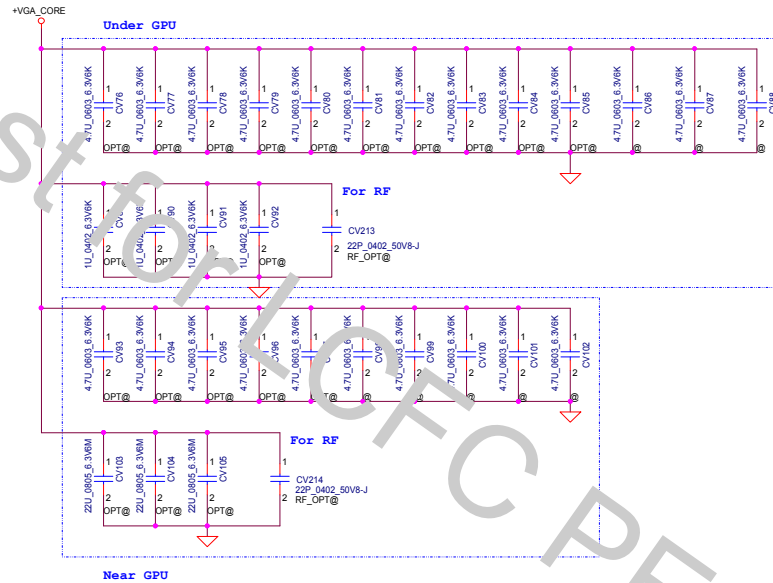
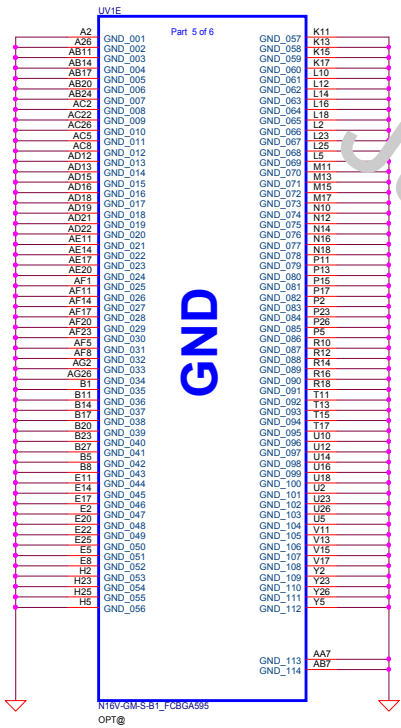
MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1



CALIBRATION PIN

CALIBRATION PIN	DDR3
FB_CAL x PD_VDDQ	40.2ohm
FB_CAL x PU_GND	42.2ohm
FB_CAL xTERM_GND	51.1ohm





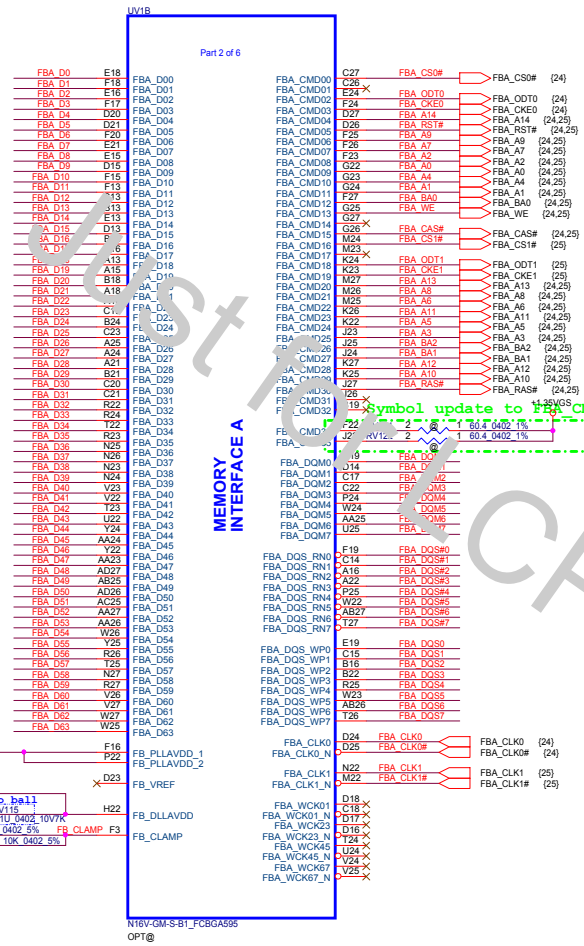
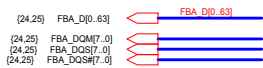
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Issued Date	2014/09/24	Deciphered Date
		2015/03/23

Title	
N16X_+VGA CORE, GND	

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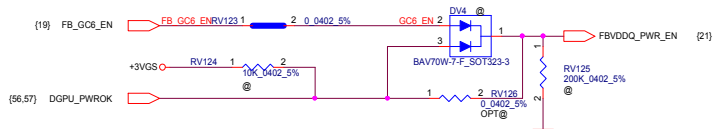
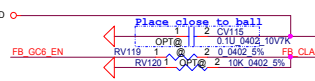
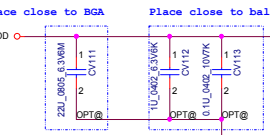
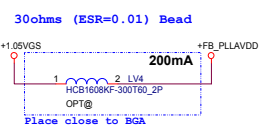
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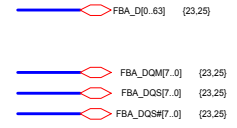
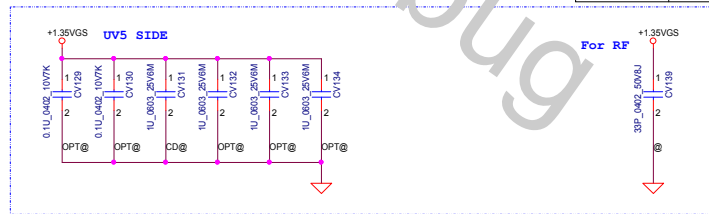
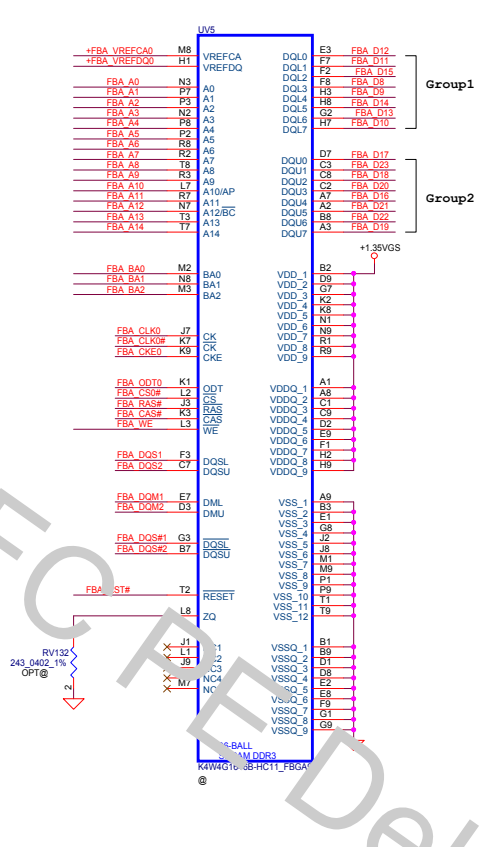
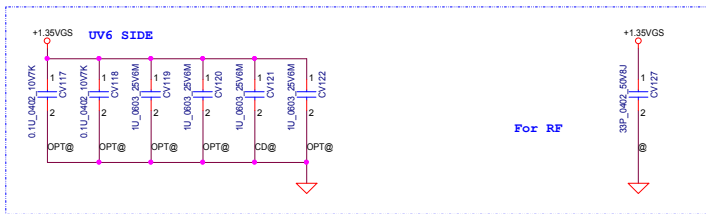
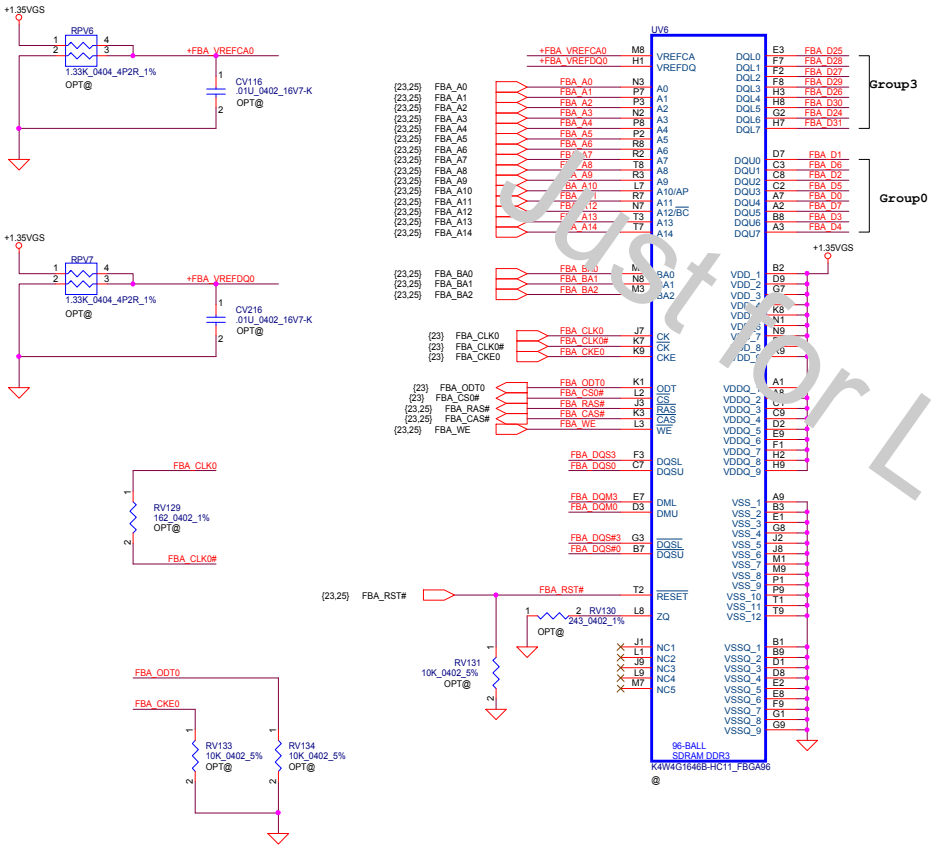


CMD mapping mod Mode D

Address	Rank0	
	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT0	
FBx_CMD3	CKE0	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE	WE
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS1#
FBx_CMD17		
FBx_CMD18	ODT1	
FBx_CMD19	CKE1	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		
FBx_CMD32		
FBx_CMD33		
FBx_CMD34	DBG0	
FBx_CMD35	DBG1	



at least 16 mils width(optimal)  
20 mils spacing to other signals /planes

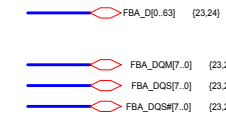
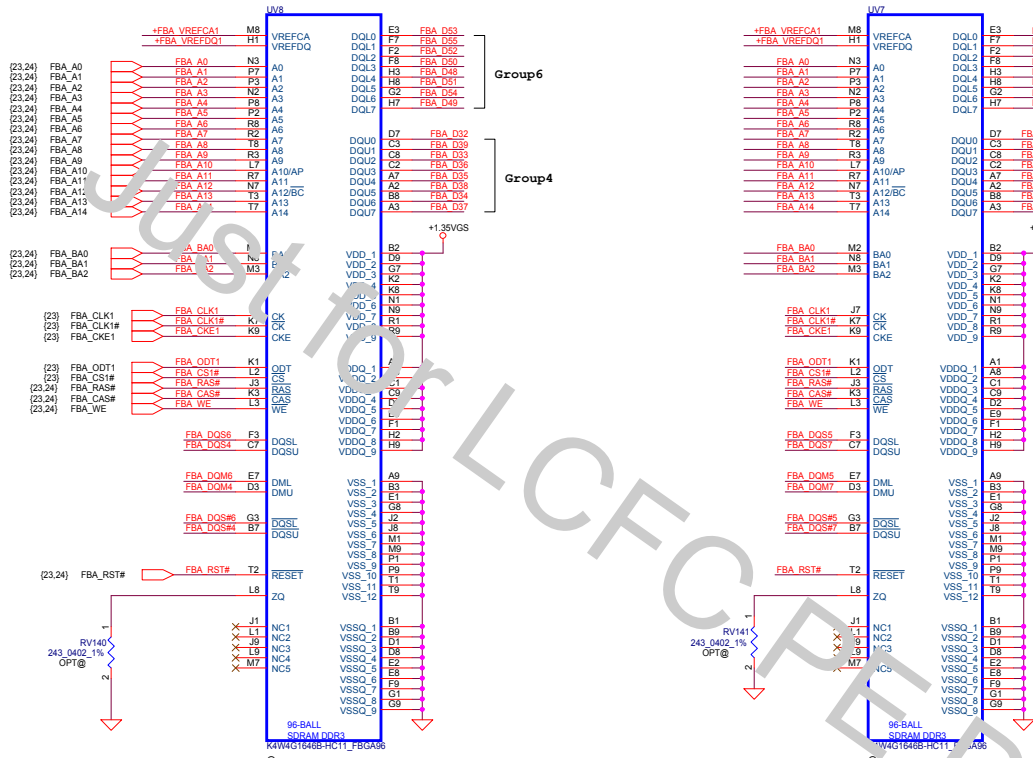
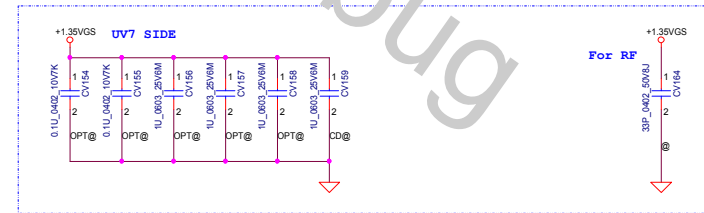
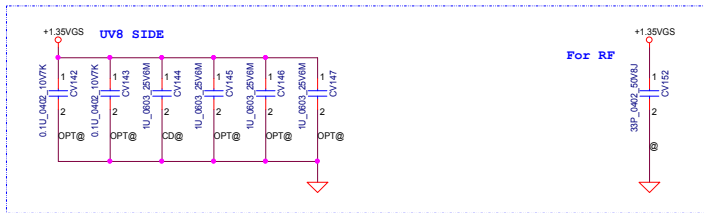
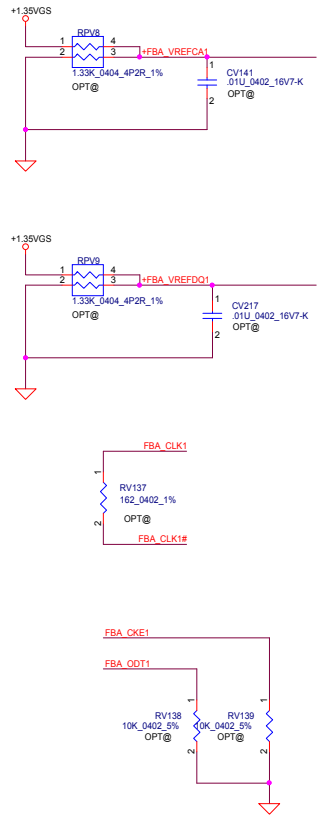


**CMD mapping mod Mode D**

Address	Rank0	
	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT0	
FBx_CMD3	CKE0	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE	WE
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CSI#	
FBx_CMD17		
FBx_CMD18		
FBx_CMD19	CKE1	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		
FBx_CMD32		
FBx_CMD33		
FBx_CMD34	DBG0	
FBx_CMD35	DBG1	

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at least 16 mils width(optimal)  
20 mils spacing to other signals /planes




CMD mapping mod Mode D

Address	Rank0	Rank1	Rank2
FBx_CMD0	CS0#	32..63	
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16		CS1#	
FBx_CMD17			
FBx_CMD18		ODT1	
FBx_CMD19		CKE1	
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		


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Just for LCFC PE Debug

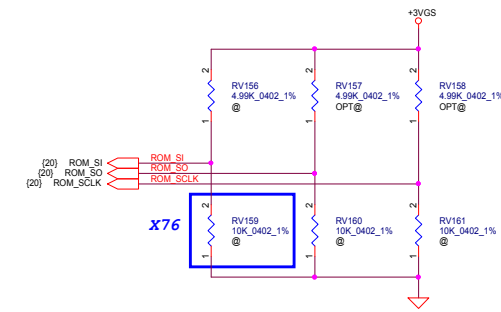
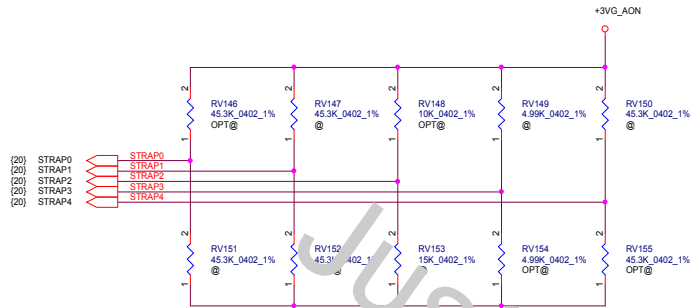
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				Date:	Tuesday, April 07, 2015	Sheet 26 of 60

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Just for LCFC PE Debug

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			<b>BMWC1</b>	0.4
			date: Tuesday, April 07, 2015	Sheet 27 of 60

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS				
STRAP2	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K SD03449918J	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K SD03449928J	1100	0100
30.1K SD03449912AJ	1101	0101
34.8K SD03449922AJ	1110	0110
45.3K SD034499328J	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)


Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16V-GM	H5TC4G63AFR-11C	0xE							
	Hynix 900MHz 256M x 16 0xE	PU 34.8K							
	MT41J256M16HA-093G:E	0xD							
	Micron 900MHz 256M x 16 0xD	PU 30.1K							
	H5TC2G63FPR-11C	0xB	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K
	Hynix 900MHz 128M x 16 0xB	PU 20K							
	MT41J128M16JT-093G	0x8							
	Micron 900MHz 128M x 16 0x8	PU 4.99K							
	K4W2G1646Q-BC1A	0x7							
	Samsung 900MHz 128M x 16 0x7	PD 45.3K							

VRAM	X76	VRAM 2/N
Samsung	X7606012101	SA00005SH40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00

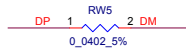
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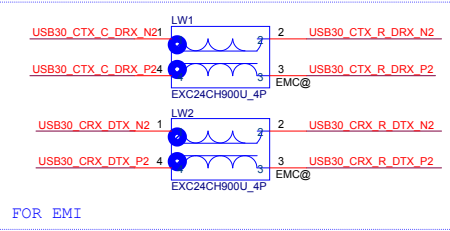
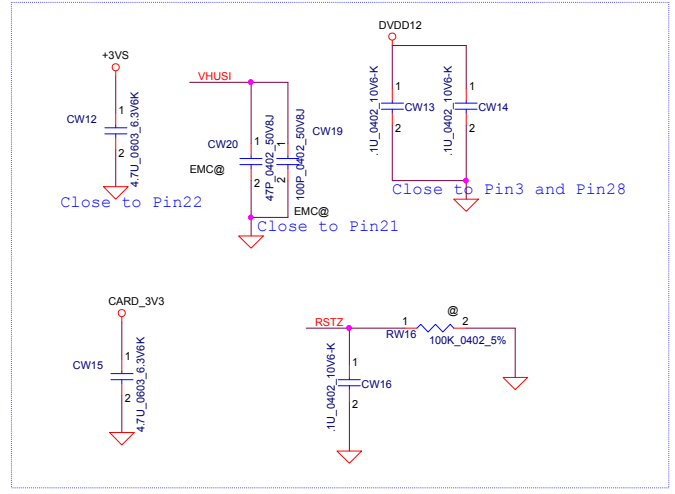
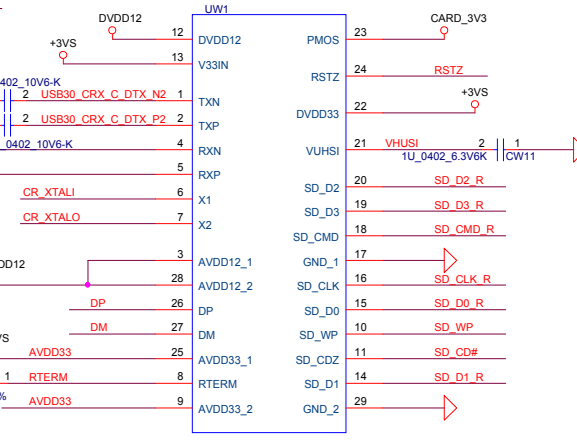


(8) USB30\_CTX\_DRX\_N2 1U\_0402\_10V6-K CW25 1 2 USB30\_CTX\_C\_DRX\_N2 1 RW1 @ 2 0\_0402\_5% USB30\_CTX\_R\_DRX\_N2  
 (8) USB30\_CTX\_DRX\_P2 1U\_0402\_10V6-K CW26 1 2 USB30\_CTX\_C\_DRX\_P2 1 RW2 @ 2 0\_0402\_5% USB30\_CTX\_R\_DRX\_P2

(8) USB30\_CRX\_DTX\_N2 USB30\_CRX\_DTX\_N2 RW3 1 @ 2 0\_0402\_5% USB30\_CRX\_R\_DTX\_N2  
 (8) USB30\_CRX\_DTX\_P2 USB30\_CRX\_DTX\_P2 RW4 1 @ 2 0\_0402\_5% USB30\_CRX\_R\_DTX\_P2

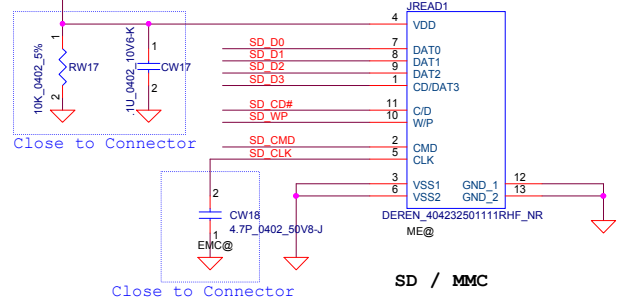
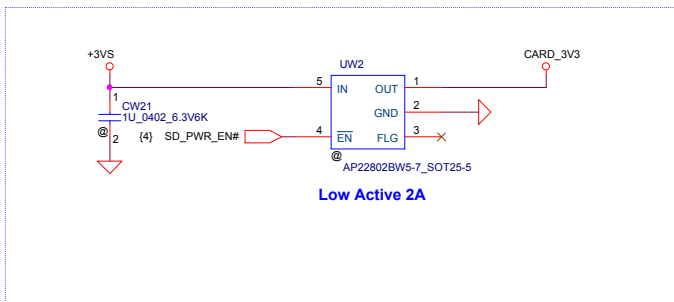
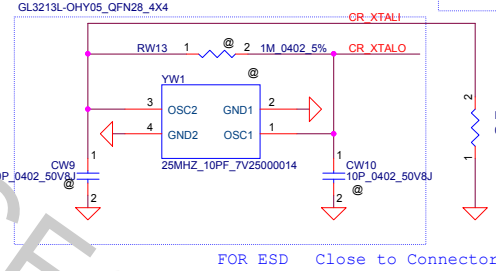


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 USB30\_CTX\_R\_DRX\_N2 1U\_0402\_10V6-K  
 USB30\_CTX\_R\_DRX\_P2




FOR EMI

(4) SD\_D0\_PCH SD\_D0\_R RW6 2 EMC@ 1 33\_0402\_5% SD\_D0  
 SD\_D0\_PCH RW37 2 @ 1 10\_0402\_1% CW3 1 2 4\_7P\_0402\_V8-J  
 (4) SD\_D1\_PCH SD\_D1\_R RW7 2 EMC@ 1 33\_0402\_5% SD\_D1  
 SD\_D1\_PCH RW38 2 @ 1 10\_0402\_1% CW4 1 2 4\_7P\_0402\_V8-J  
 (4) SD\_D2\_PCH SD\_D2\_R RW8 2 EMC@ 1 33\_0402\_5% SD\_D2  
 SD\_D2\_PCH RW39 2 @ 1 10\_0402\_1% CW5 1 2 4\_7P\_0402\_50V8-J  
 (4) SD\_D3\_PCH SD\_D3\_R RW9 2 EMC@ 1 33\_0402\_5% SD\_D3  
 SD\_D3\_PCH RW40 2 @ 1 10\_0402\_1% CW6 1 2 4\_7P\_0402\_50V8-J  
 (4) SD\_CMD\_PCH SD\_CMD\_R RW10 1 EMC@ 2 22\_0402\_5% SD\_CMD  
 SD\_CMD\_PCH RW41 2 @ 1 10\_0402\_1% CW7 1 2 4\_7P\_0402\_50V8-J  
 (4) SD\_CLK\_PCH SD\_CLK\_R RW11 1 EMC@ 2 22\_0402\_5% SD\_CLK  
 SD\_CLK\_PCH RW42 1 @ 2 0\_0402\_5% CW8 1 2 4\_7P\_0402\_50V8-J  
 (4) SD\_CLK\_PCH RW43 1 @ 2 0\_0402\_5% SD\_CLK  
 SD\_CLK\_PCH RW44 1 @ 2 0\_0402\_5% SD\_CLK  
 (7) SD\_WP\_PCH SD\_CD#\_PCH RW43 1 @ 2 0\_0402\_5% SD\_CD#  
 SD\_WP\_PCH RW44 1 @ 2 0\_0402\_5% SD\_WP




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			Date:	Tuesday, April 07, 2015	Sheet 30 of 59

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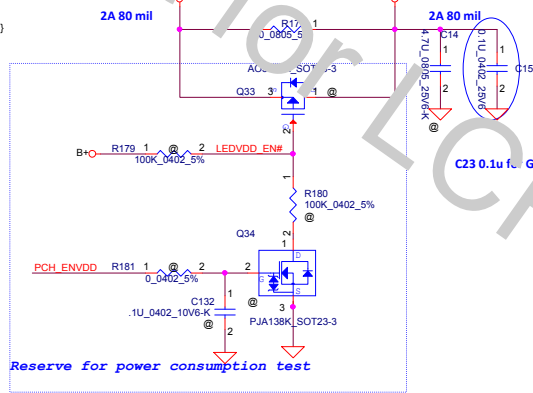
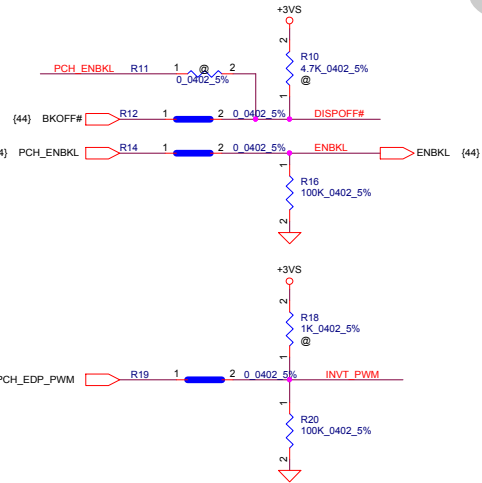
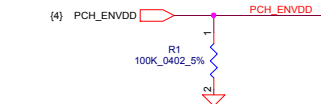
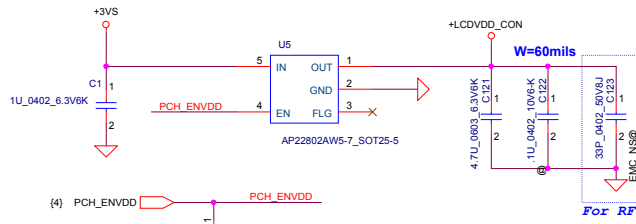
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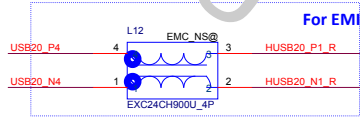
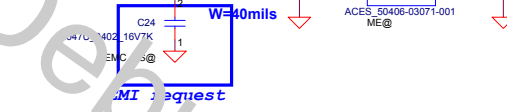
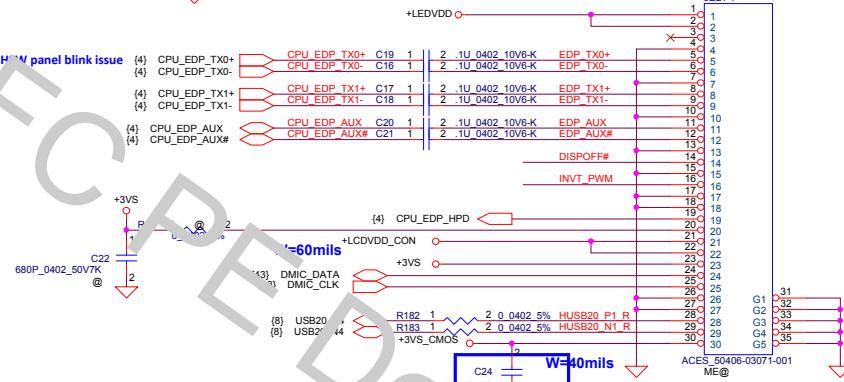
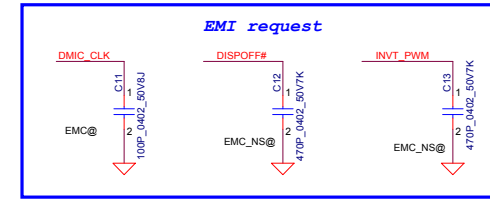
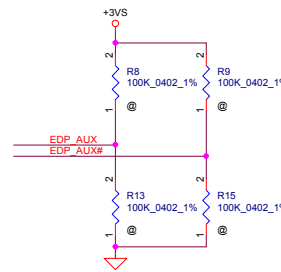
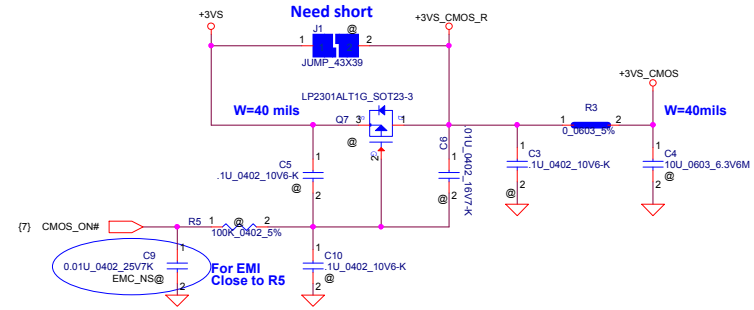
# LCD POWER CIRCUIT

W=60mils



# CMOS Camera

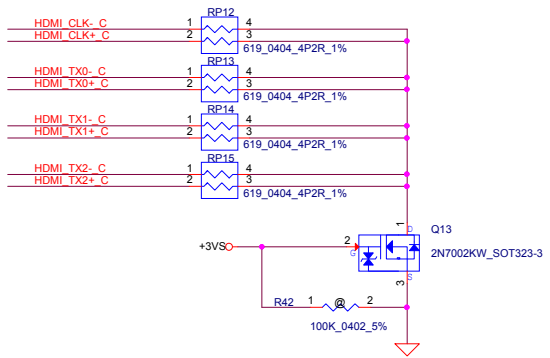
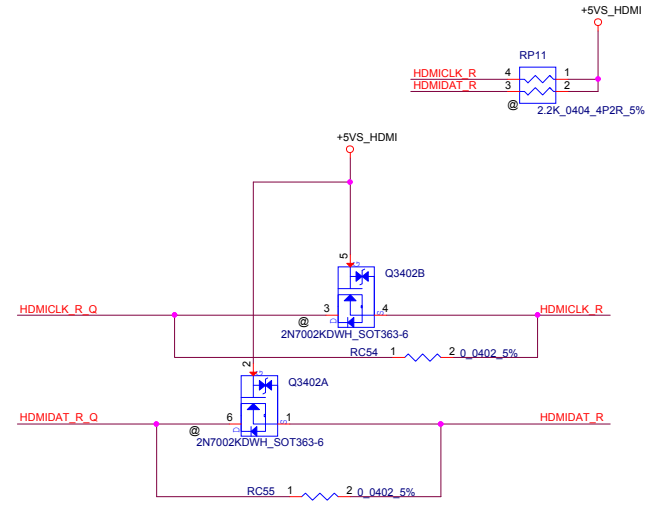
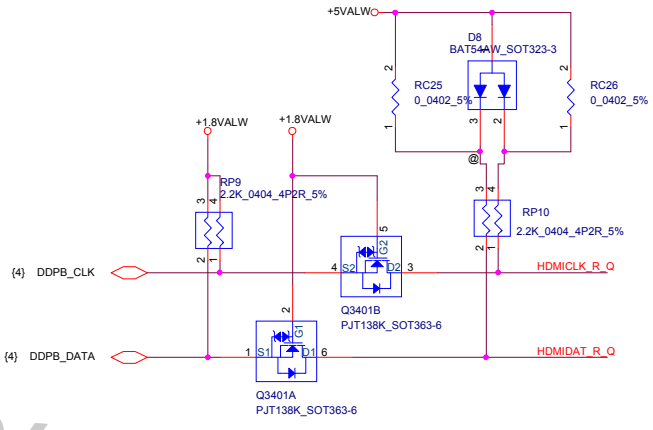
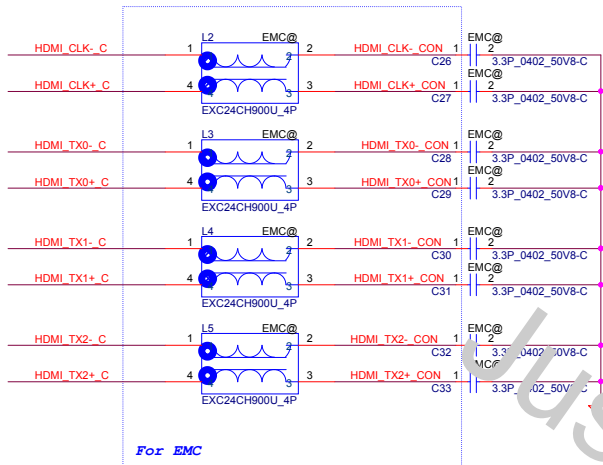
Need short



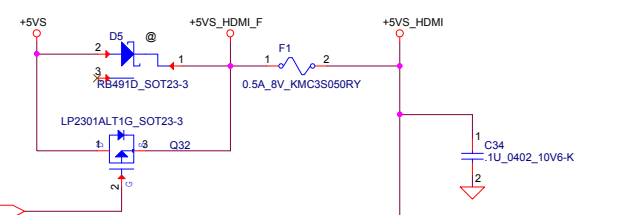
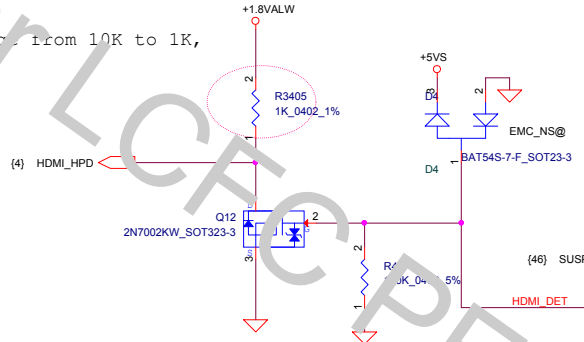
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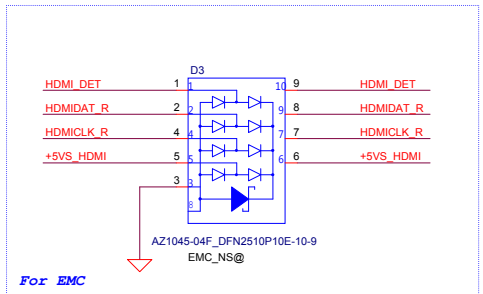
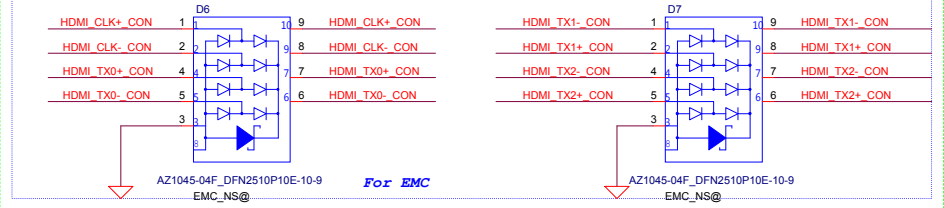


R4602 changed from 10K to 1K, as Vienna

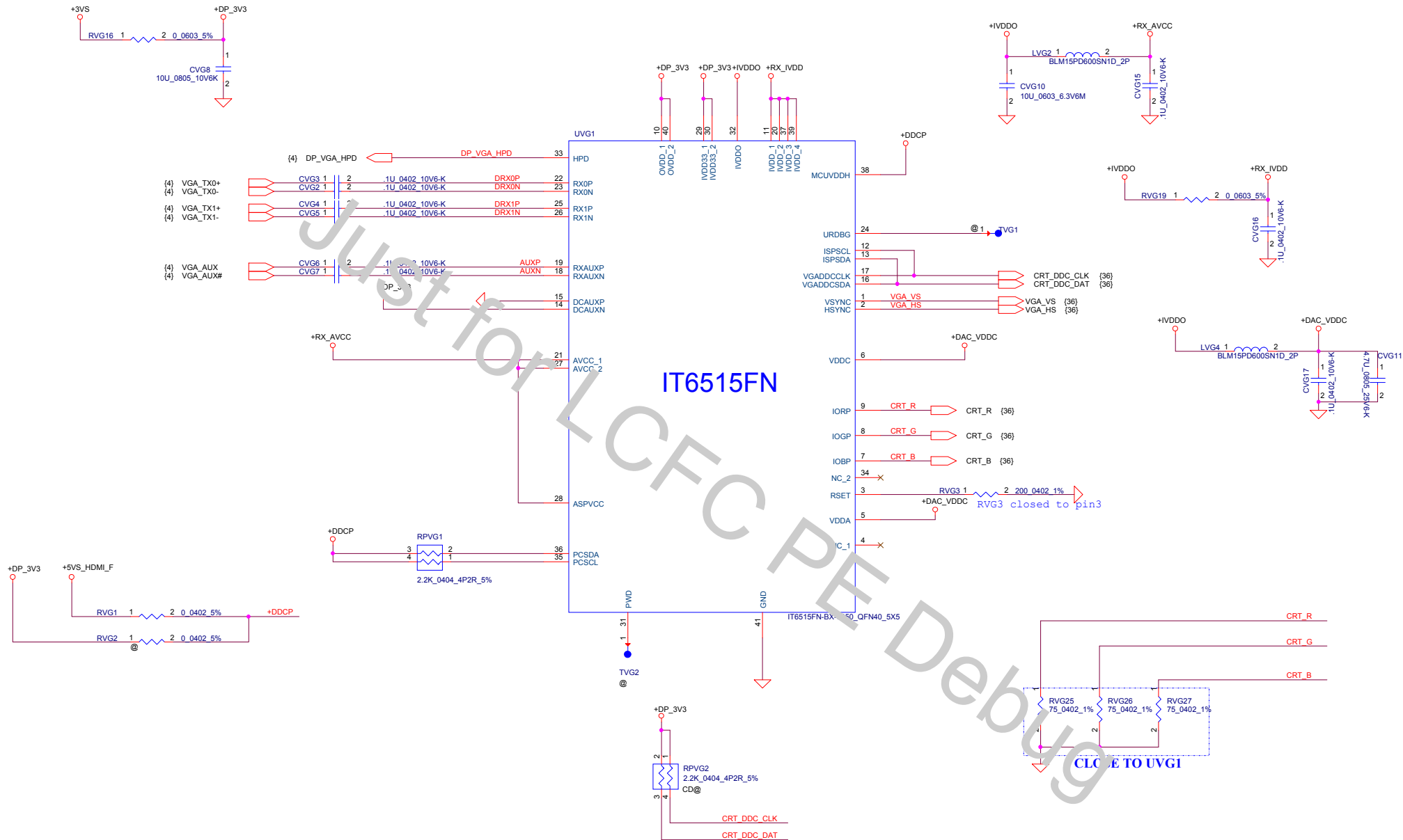


(4) HDMI_CLK-	HDMI_CLK-	C35	1	1.1U	0402	10V6-K	HDMI_CLK- C	R432	@	1	0	0402	5%	HDMI_CLK- CON
(4) HDMI_CLK+	HDMI_CLK+	C36	2	1.1U	0402	10V6-K	HDMI_CLK+ C	R442	@	1	0	0402	5%	HDMI_CLK+ CON
(4) HDMI_TX0-	HDMI_TX0-	C37	2	1.1U	0402	10V6-K	HDMI_TX0- C	R452	@	1	0	0402	5%	HDMI_TX0- CON
(4) HDMI_TX0+	HDMI_TX0+	C38	2	1.1U	0402	10V6-K	HDMI_TX0+ C	R462	@	1	0	0402	5%	HDMI_TX0+ CON
(4) HDMI_TX1-	HDMI_TX1-	C39	2	1.1U	0402	10V6-K	HDMI_TX1- C	R472	@	1	0	0402	5%	HDMI_TX1- CON
(4) HDMI_TX1+	HDMI_TX1+	C40	2	1.1U	0402	10V6-K	HDMI_TX1+ C	R482	@	1	0	0402	5%	HDMI_TX1+ CON
(4) HDMI_TX2-	HDMI_TX2-	C41	2	1.1U	0402	10V6-K	HDMI_TX2- C	R492	@	1	0	0402	5%	HDMI_TX2- CON
(4) HDMI_TX2+	HDMI_TX2+	C42	2	1.1U	0402	10V6-K	HDMI_TX2+ C	R502	@	1	0	0402	5%	HDMI_TX2+ CON

Close to JHDMI1



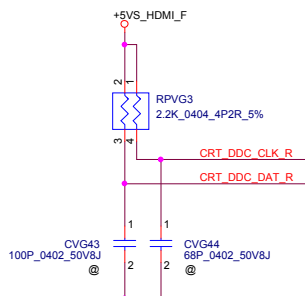
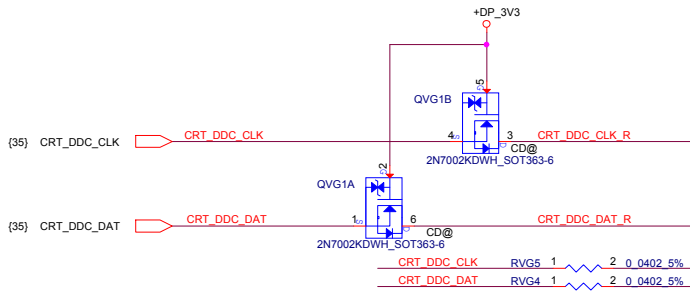
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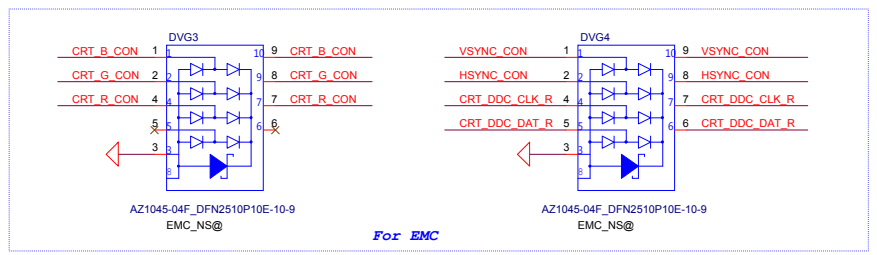
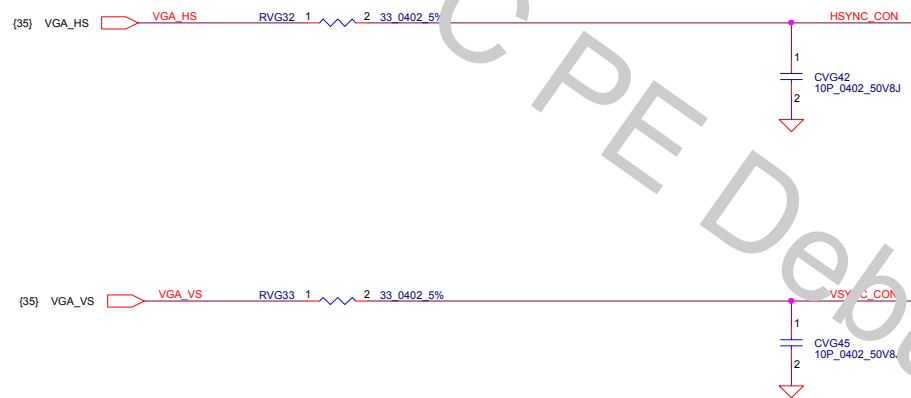
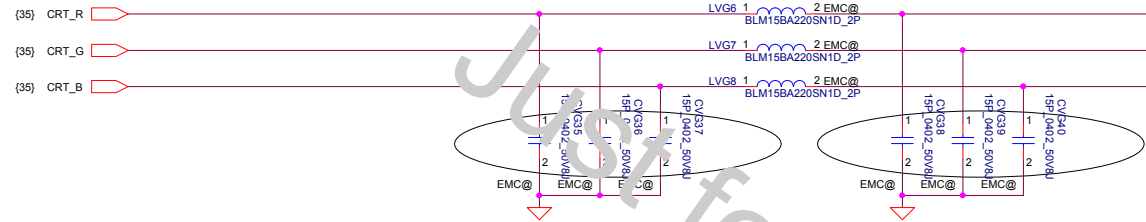
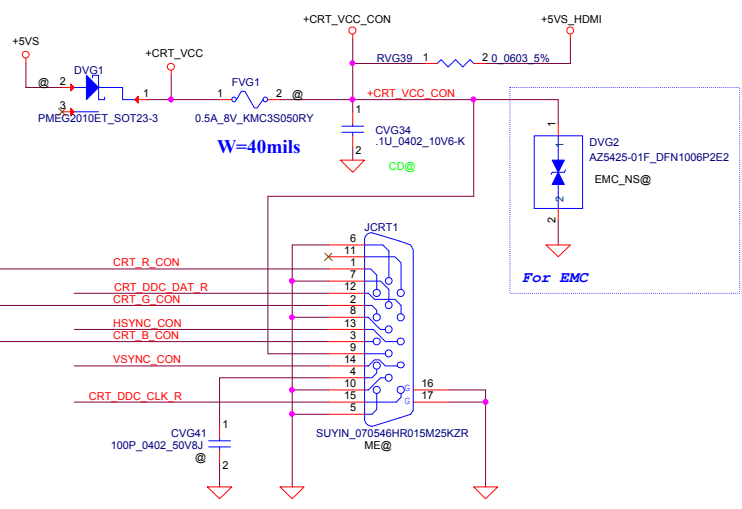
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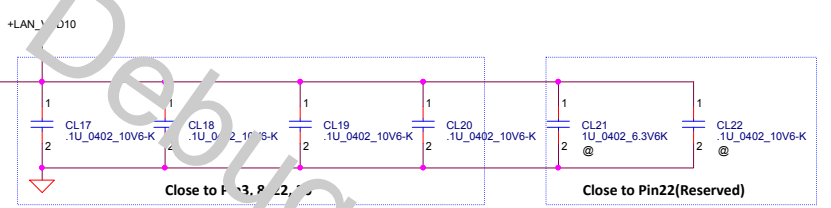
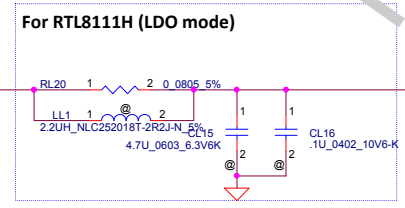
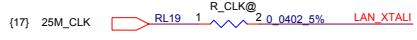
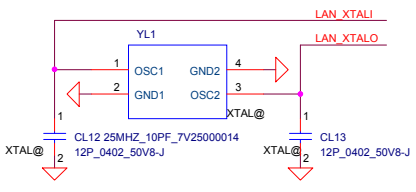
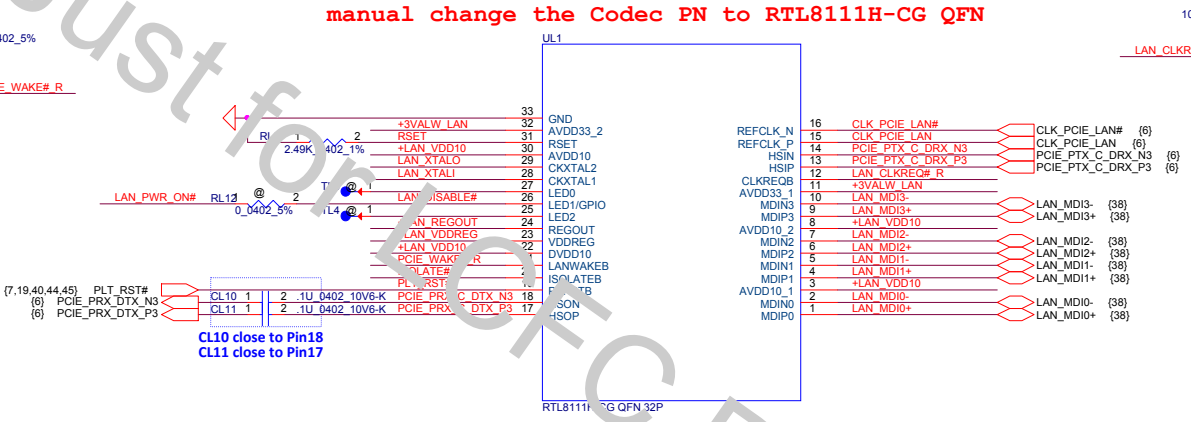
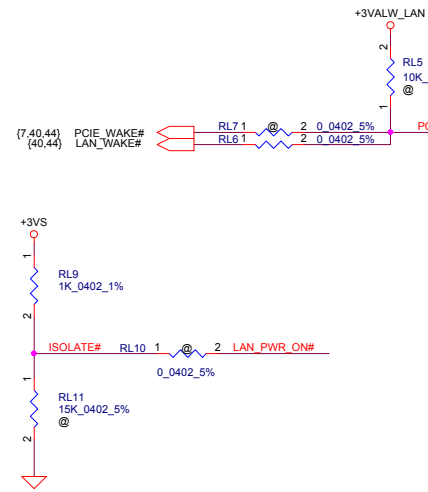
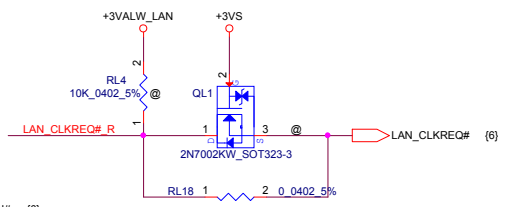
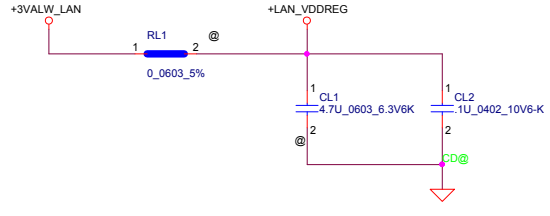
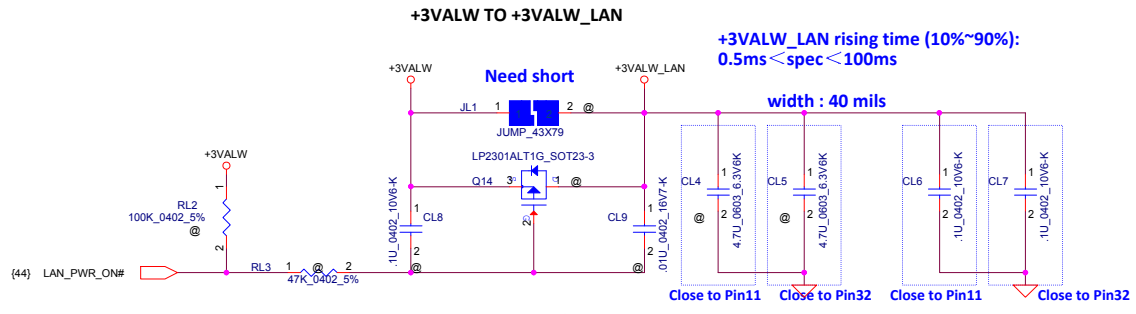


### CRT Connector



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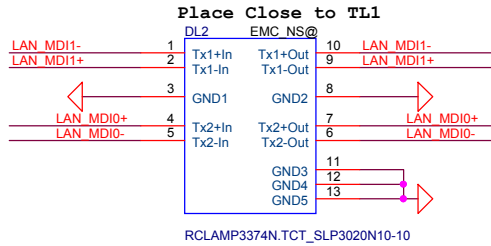
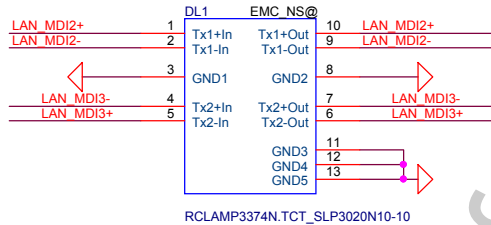


Layout Note: LL1 must be within 200mil to Pin24,  
CL15, CL16 must be within 200mil to L1  
+LAN\_REGOUT: Width =60mil

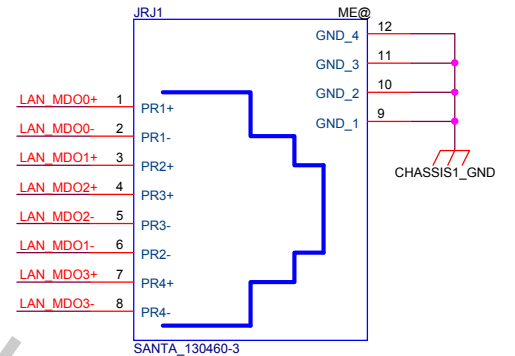
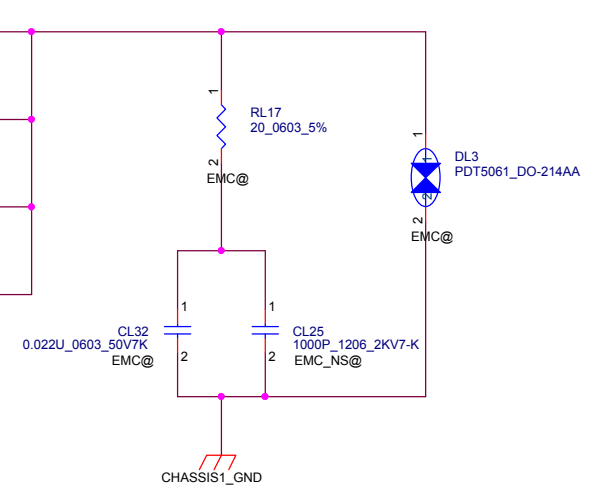
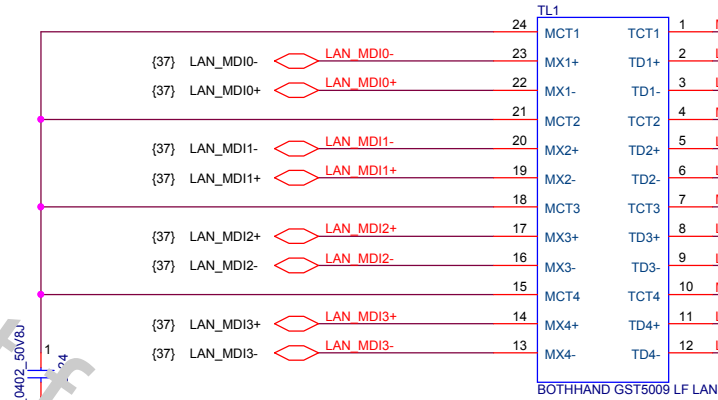
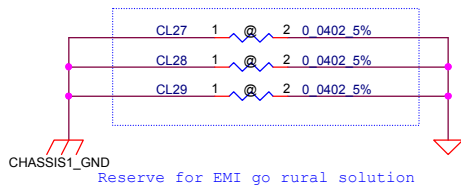
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DL1/DL2  
1'S PN:SC400007R00

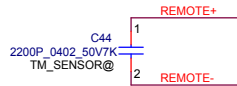


Place Close to TL2



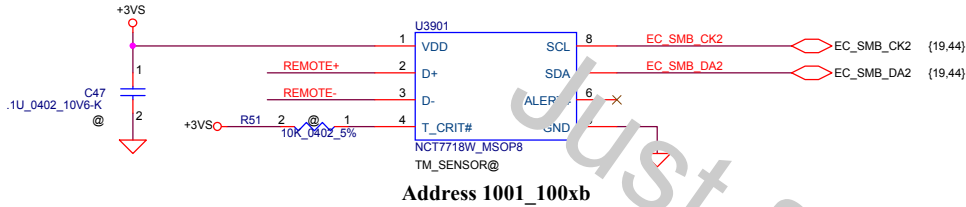
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**Close to U3901**

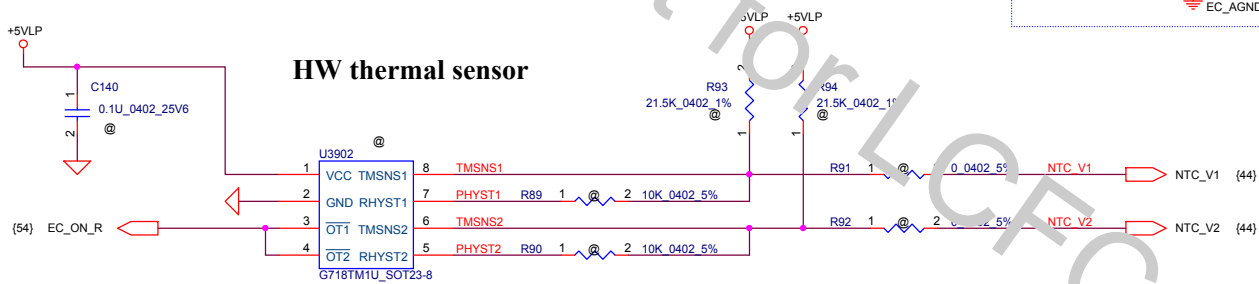


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

**SMSC thermal sensor placed near DIMM**

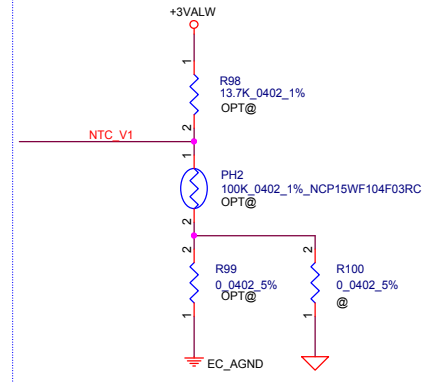


**HW thermal sensor**

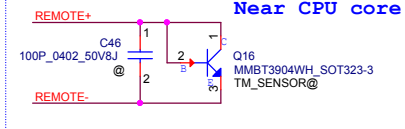


over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML) / (3\*RTML-RSET)  
56+/-30C

**Near GPU&VRAM**

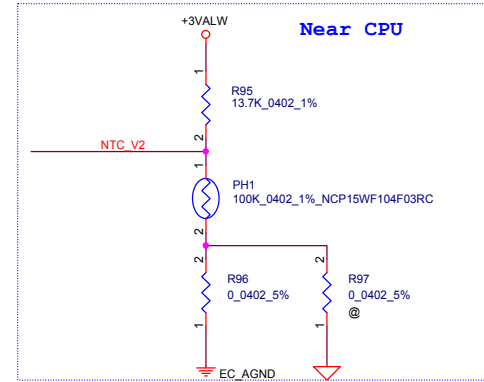


**Near CPU core**

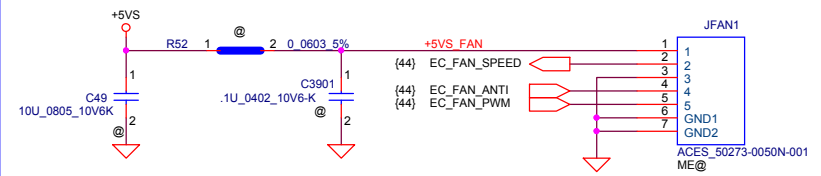


Baytrail SOC use thermal sensor to read the thermal, Baytrail don't has PECI signal

**Near CPU**



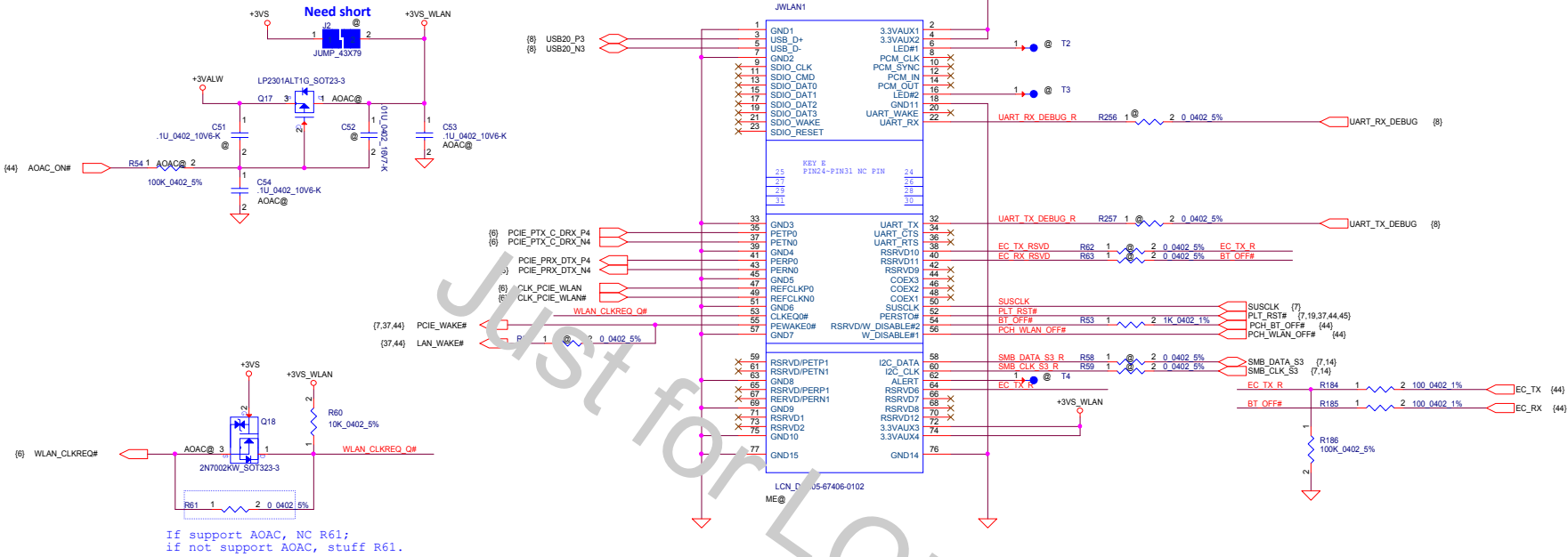
**FAN Conn**



JFAN1 Pin defin need check other G

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Custom		0.4		
Date	Tuesday, April 07, 2015	Sheet	39	of 60

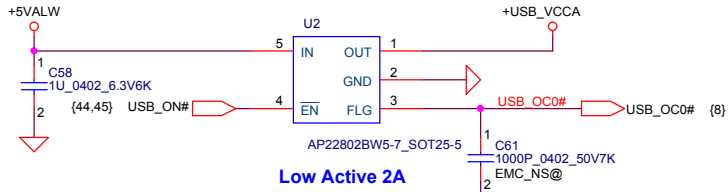
# Mini-Express Card(WLAN/WiMAX)



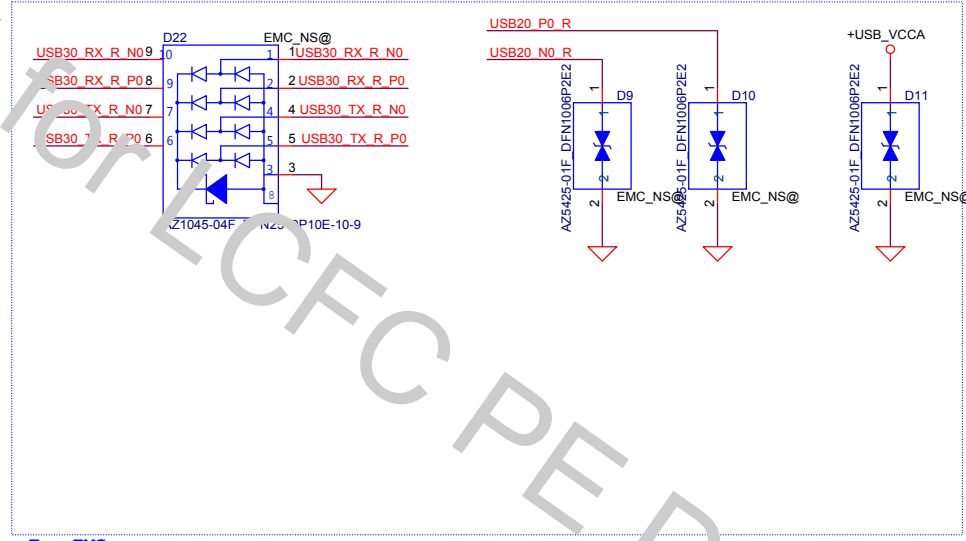
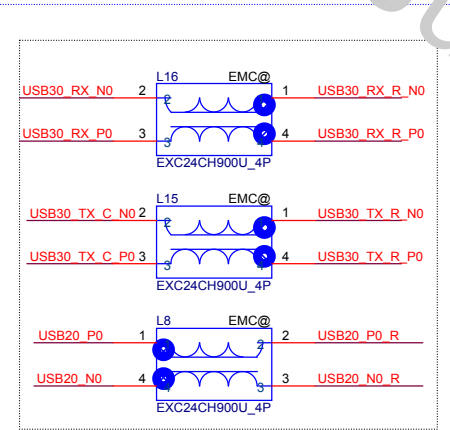
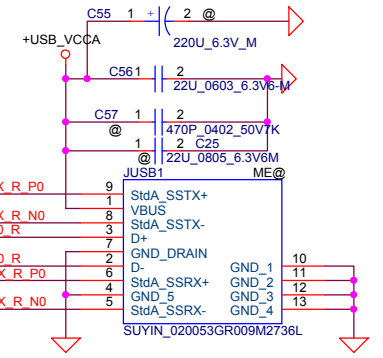
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<small>DATE: 2014/09/24</small> <small>DESIGNER: [Name]</small> <small>CHECKER: [Name]</small> <small>APPROVER: [Name]</small>			NGFF WLAN	0.4
<small>DATE: 2014/09/24</small> <small>DESIGNER: [Name]</small> <small>CHECKER: [Name]</small> <small>APPROVER: [Name]</small>			40	of 60

[www.bios-downloads.com](http://www.bios-downloads.com)

# LEFT SIDE USB3.0 PORT X1

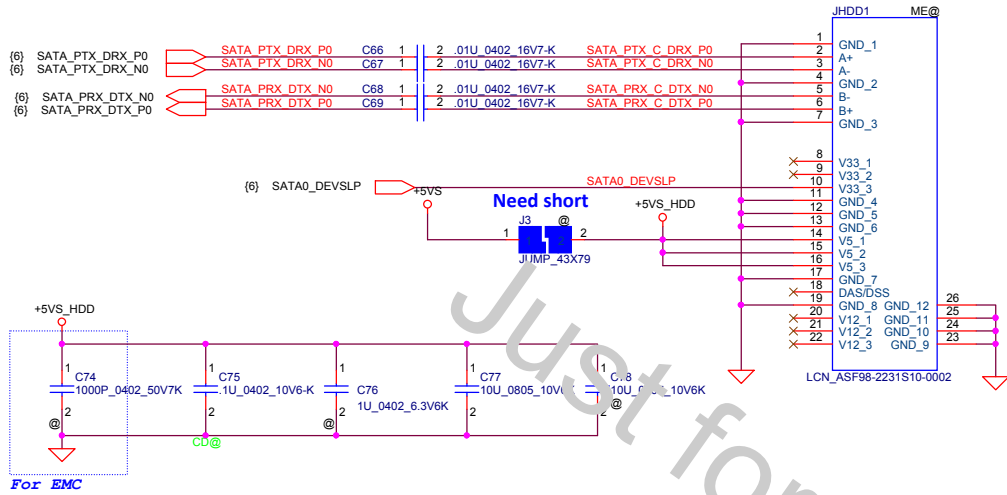


- {8} USB30\_TX\_P0 <math>\leftrightarrow</math> USB30 TX P0 C59 1 2 .1U\_0402\_10V6-K USB30 TX C P0 R46141 @ 2 0 0.0402 5% USB30 TX R P0
- {8} USB30\_TX\_N0 <math>\leftrightarrow</math> USB30 TX N0 C60 1 2 .1U\_0402\_10V6-K USB30 TX C N0 R46121 @ 2 0 0.0402 5% USB30 TX R N0
- {8} USB20\_P0 <math>\leftrightarrow</math> USB20 P0 R46151 @ 2 0 0.0402 5% USB20 P0 R
- {8} USB20\_N0 <math>\leftrightarrow</math> USB20 N0 R46131 @ 2 0 0.0402 5% USB20 N0 R
- {8} USB30\_RX\_P0 <math>\leftrightarrow</math> USB30 RX P0 R46111 @ 2 0 0.0402 5% USB30 RX R P0
- {8} USB30\_RX\_N0 <math>\leftrightarrow</math> USB30 RX N0 R46101 @ 2 0 0.0402 5% USB30 RX R N0

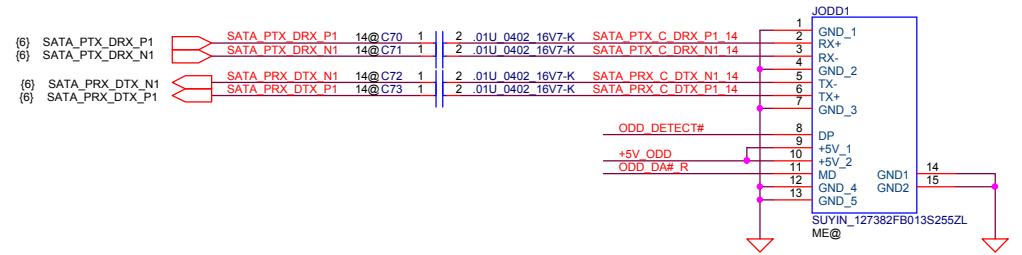


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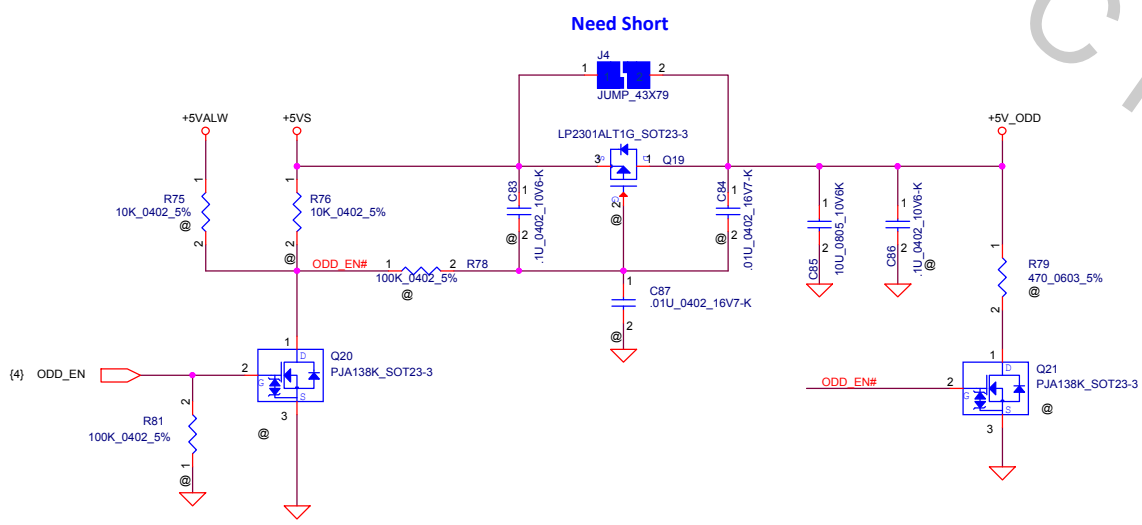
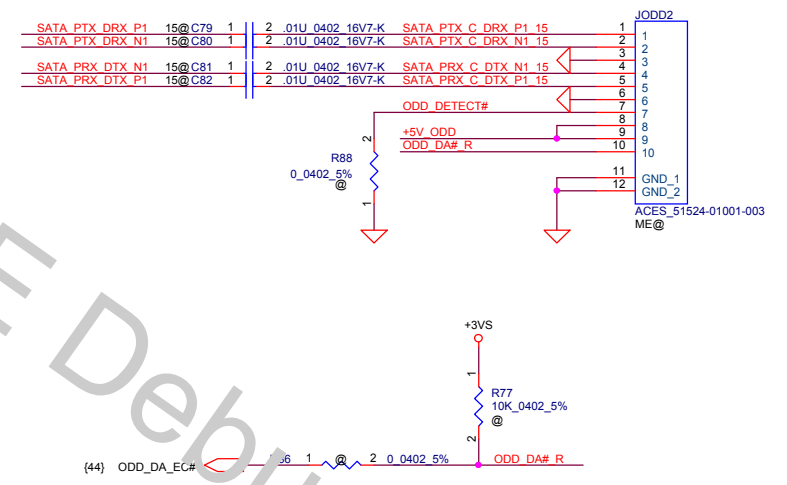
### SATA HDD Conn.



### FOR 14" SATA ODD Conn.

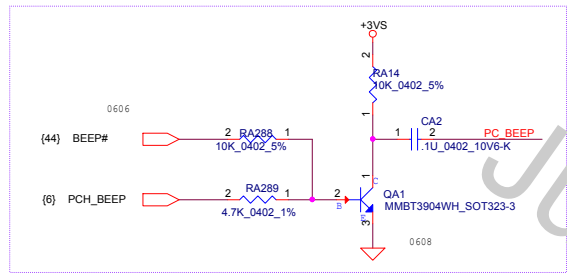


### FOR 15" SATA ODD FFC Conn

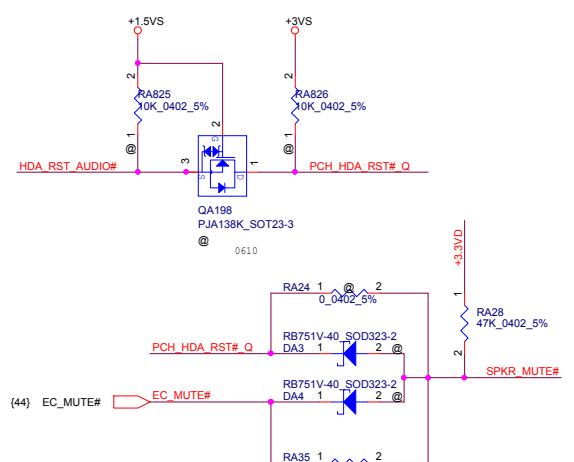
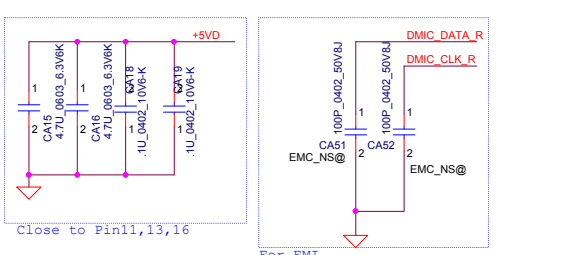
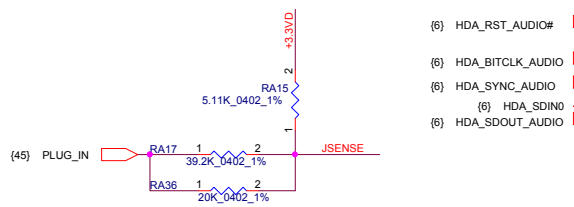


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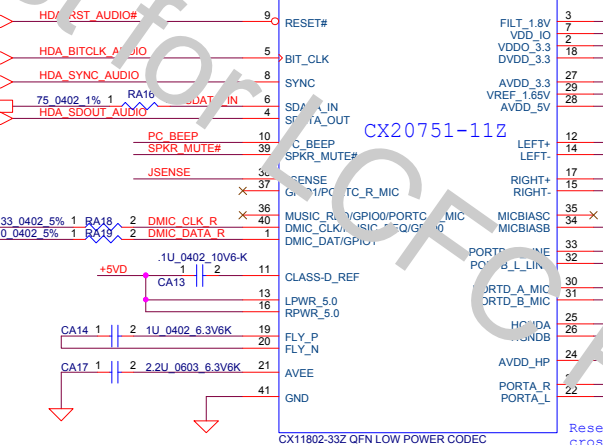
Same as Vienna



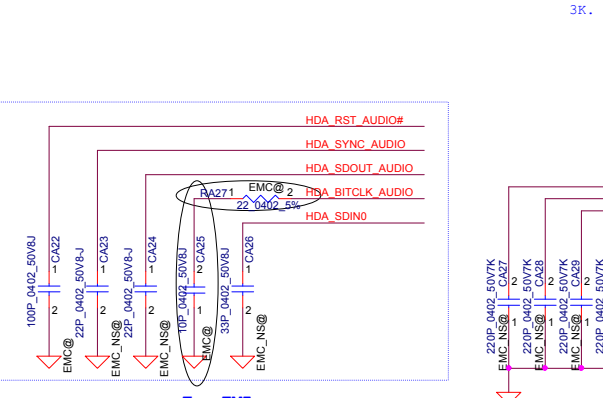
manually change the Codec PN to CX11802-33Z



manually change the Codec PN to CX11802-33Z

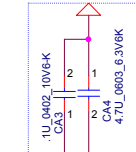


Reserve RA2 to prevent cross-talk between HPOUT\_R/L, HPOUT\_B. RA37/RA38 need change to 3K.

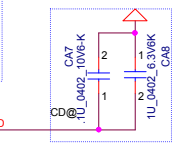


For EMI

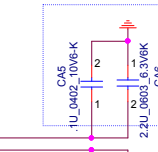
Close to Pin3



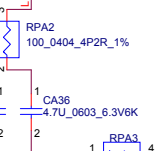
CA16 close to Pin18  
CA17 close to Pin2



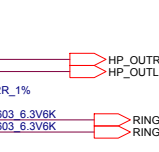
Close to Pin27



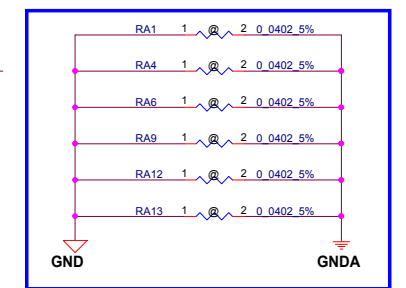
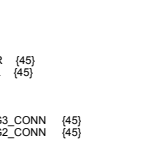
Close to Pin29



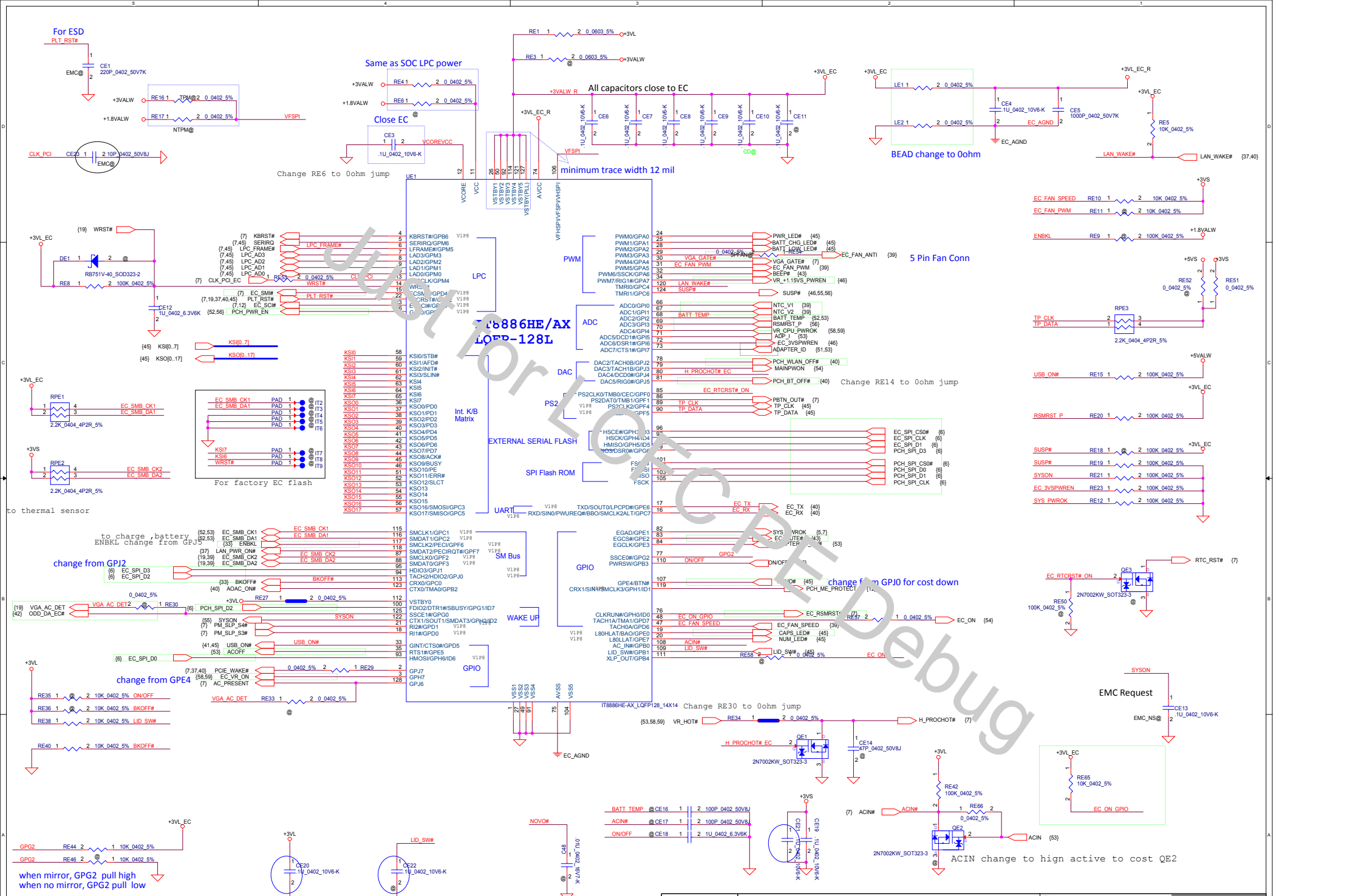
Close to Pin28



Close to Pin24

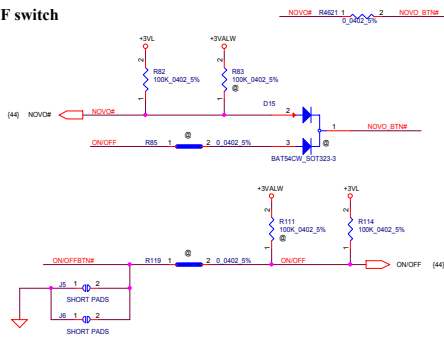


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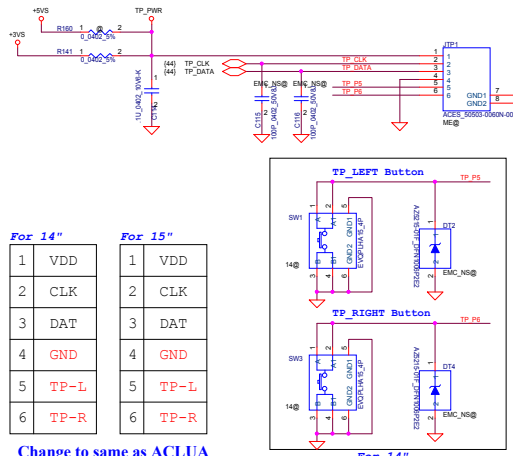




**ON/OFF switch**

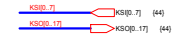


**TP/B Connector**

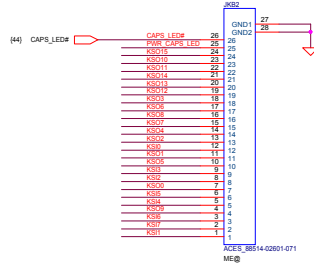


Change to same as ACLUA

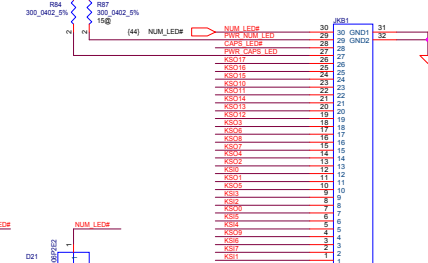
**K/B Connector**



**14"**

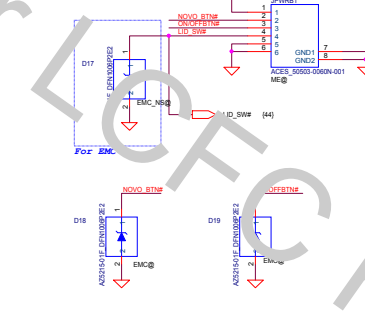


**15"**

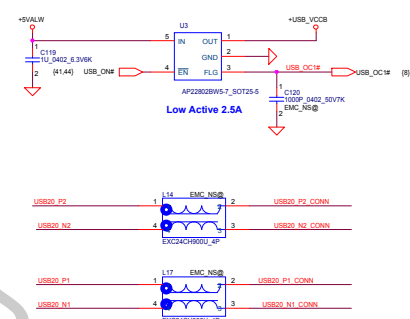


	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS15_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS04_14	KS03_15
KB_13	KS02_14	KS012_15
KB_14	KS04_14	KS011_15
KB_15	KS07_14	KS014_15
KB_16	KS09_14	KS011_14
KB_17	KS06_14	KS010_15
KB_18	KS012_14	KS016_15
KB_19	KS013_14	KS017_15
KB_20	KS014_14	KB_LED_PWR_5
KB_21	KS014_14	CAPS_LED#_15
KB_22	KS010_14	VDD_15
KB_23	KS010_14	NOM_LED#_15
KB_24	KS015_14	

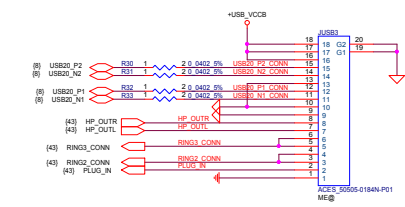
**PWR/B Connector**



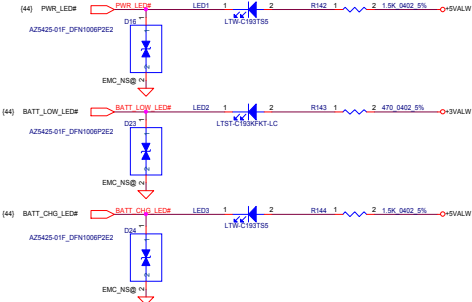
**Right Side USB2.0 Port X 2 (USB/B)**



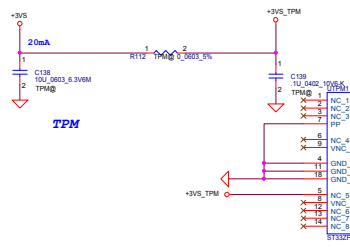
**USB I/O Connector**



**LED**

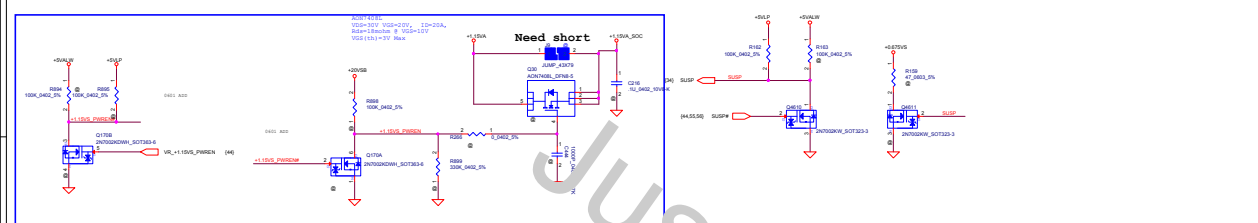
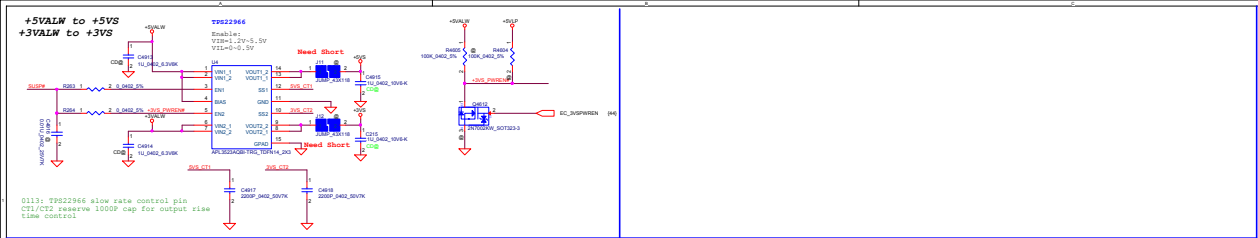


check LED location and BOM structure when placement and Load BOM, PWR\_LED and BATT\_LED have the same location on 14"/15" 02/26



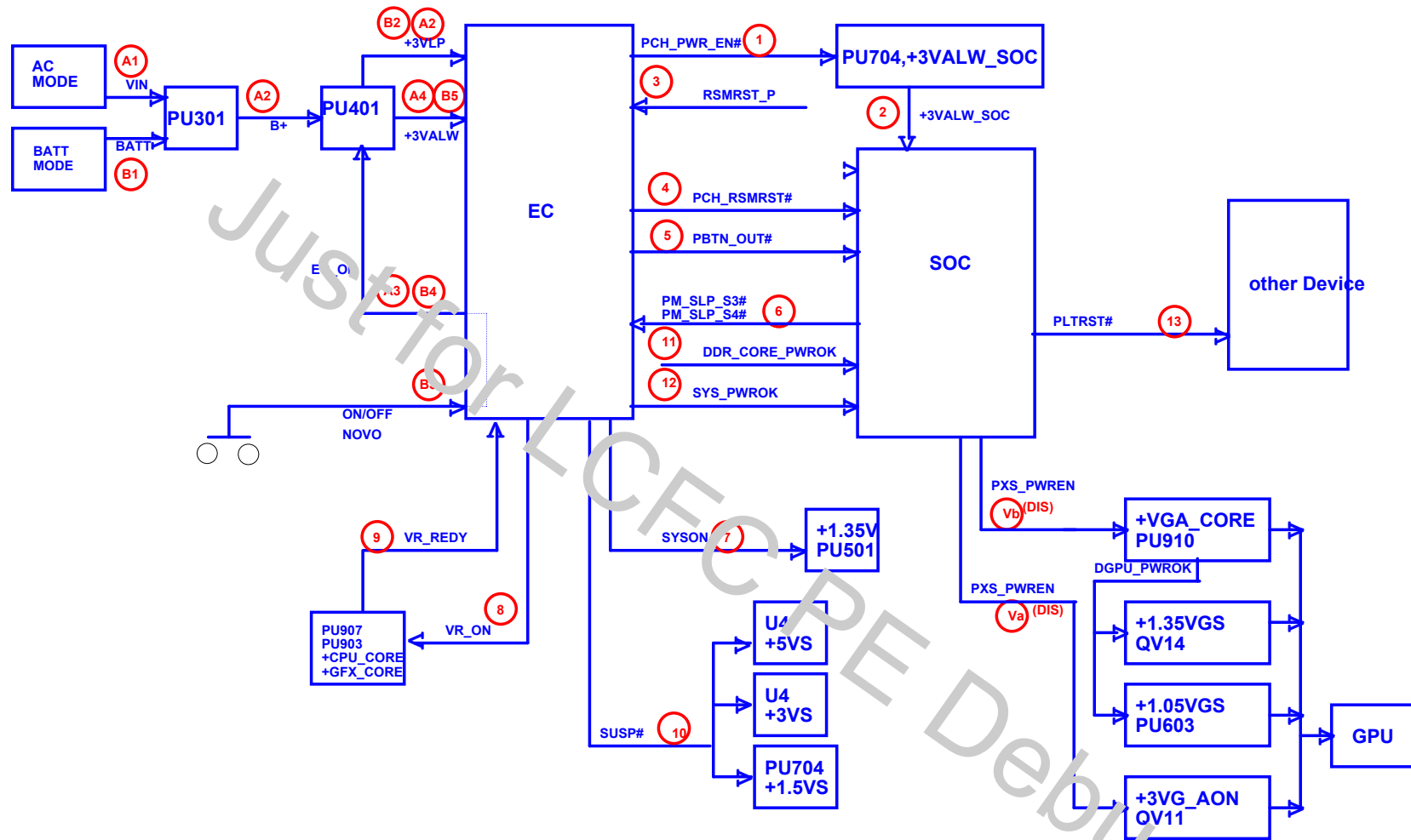
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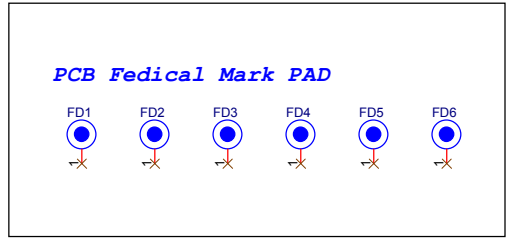
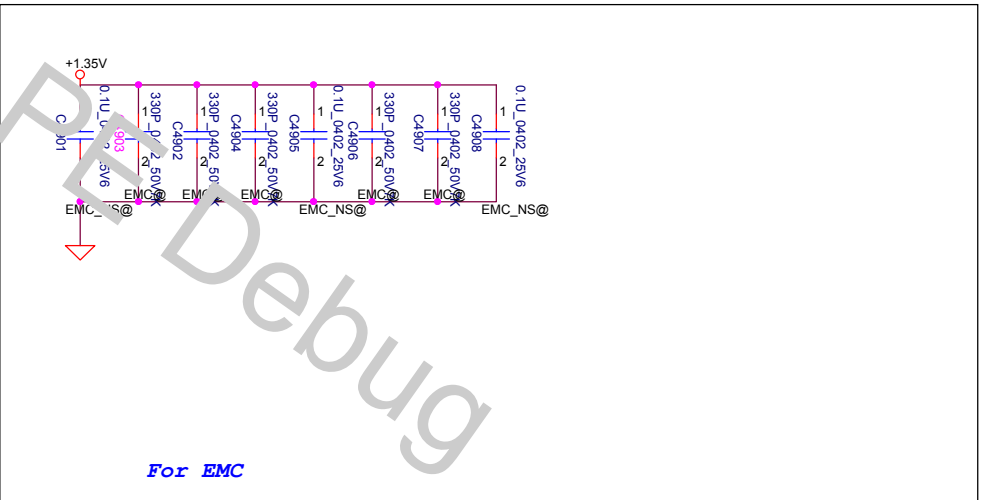
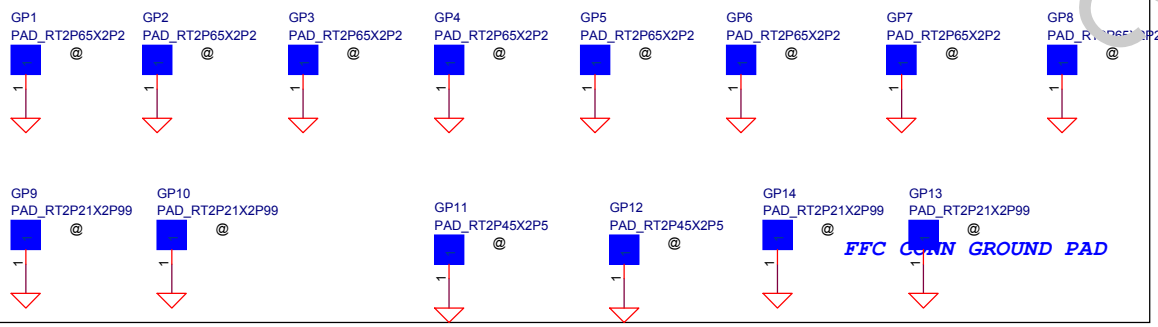
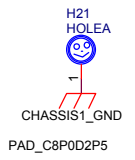
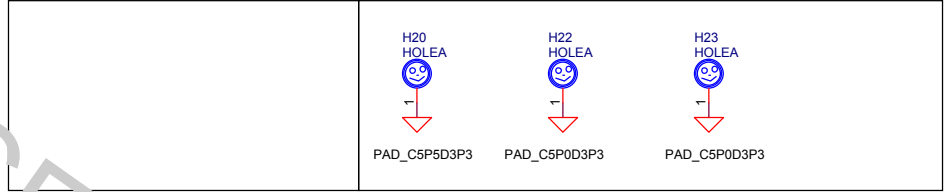
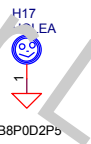
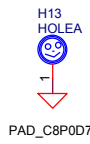
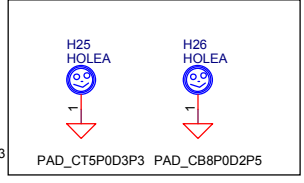
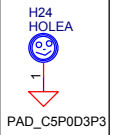
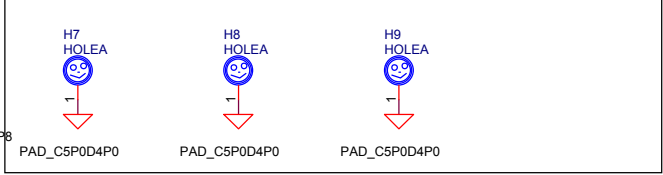
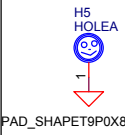
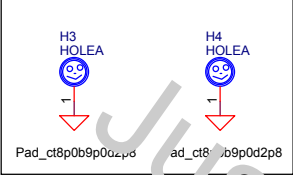
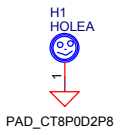
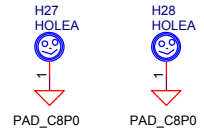
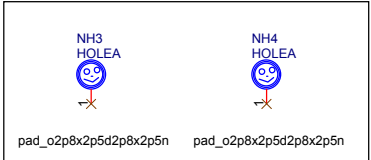
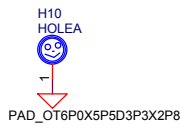
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Issued Date	20140924	Discontinued Date	20150623	
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			Custom	BMWC1	0.4
			Date:	Tuesday, April 07, 2015 1 Sheet 47 of 60	

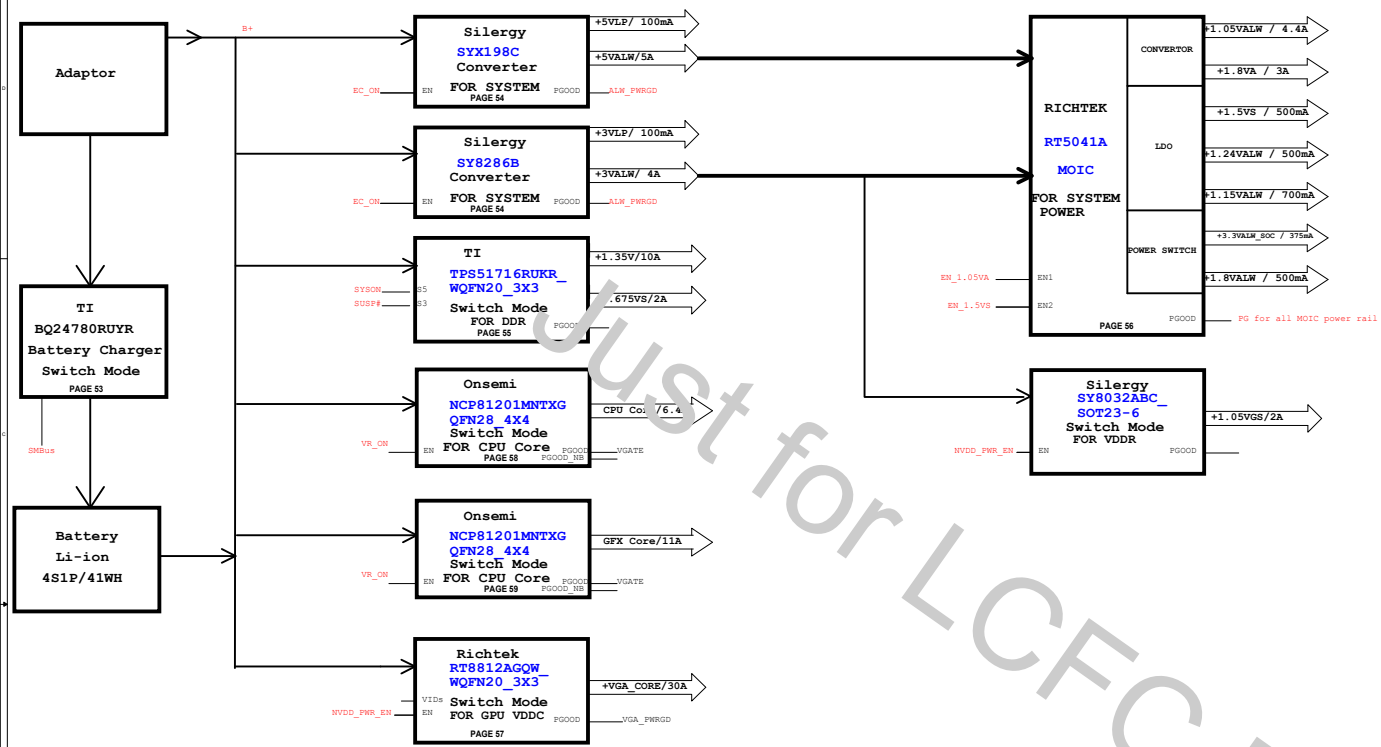
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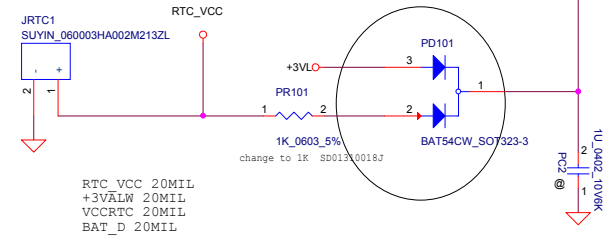
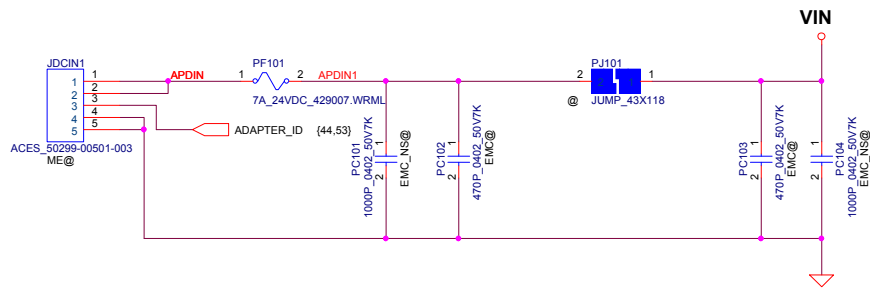
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Rev	0.4	




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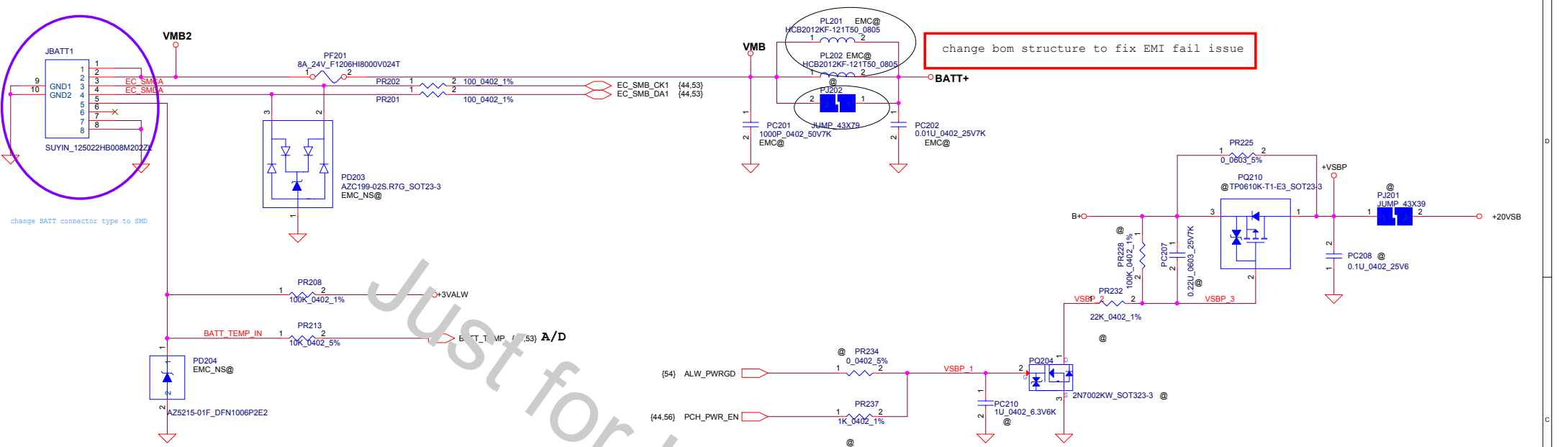
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Issued Date	20140924	Disciplined Date	20150323	
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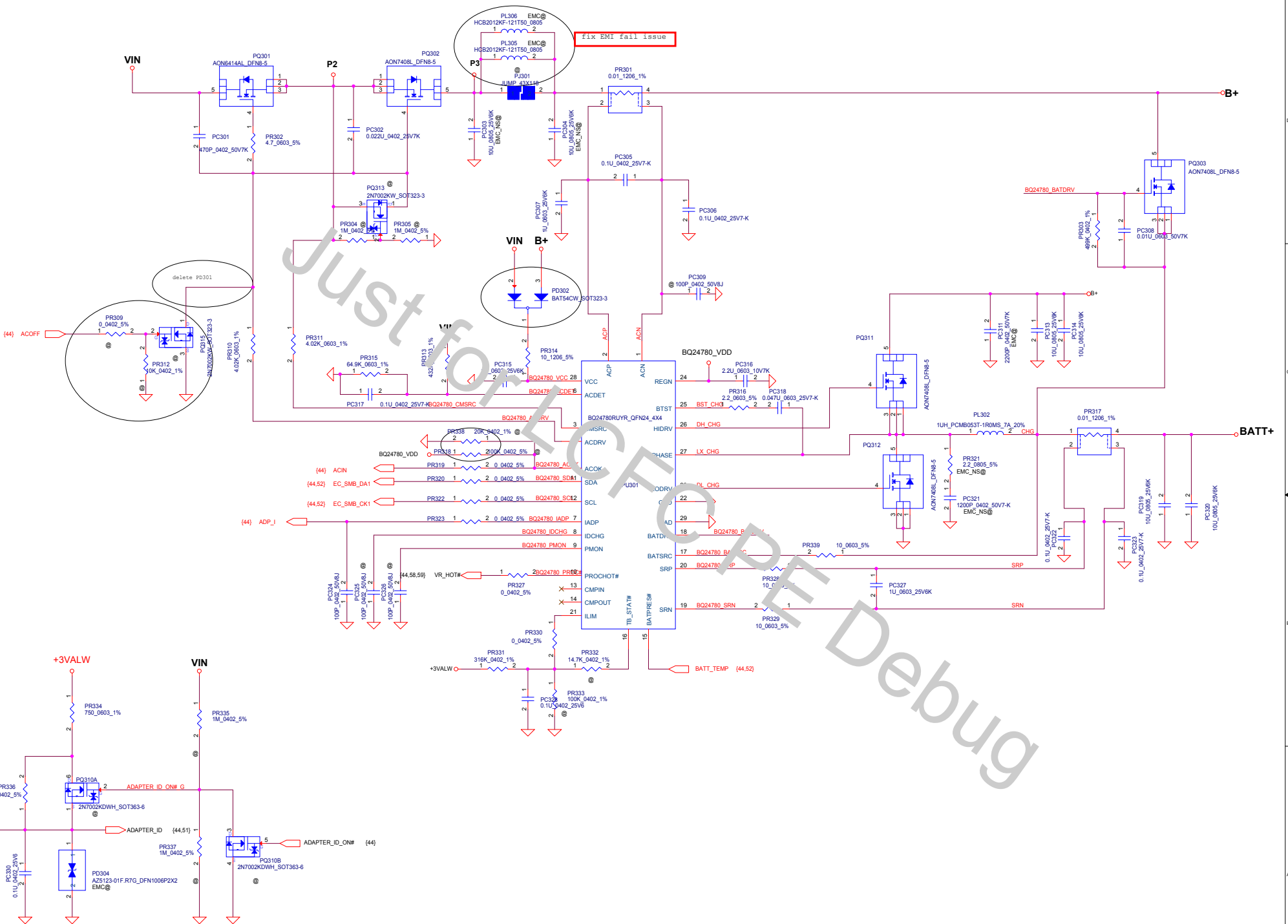
change BATT connector type to SMD




change bom structure to fix EMI fail issue

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				Sheet	52 of 59

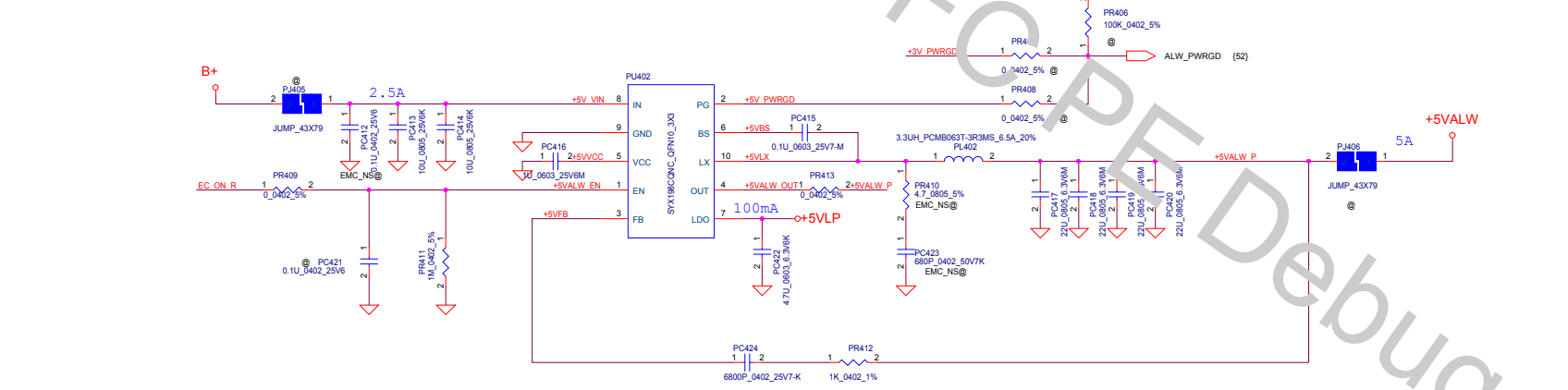
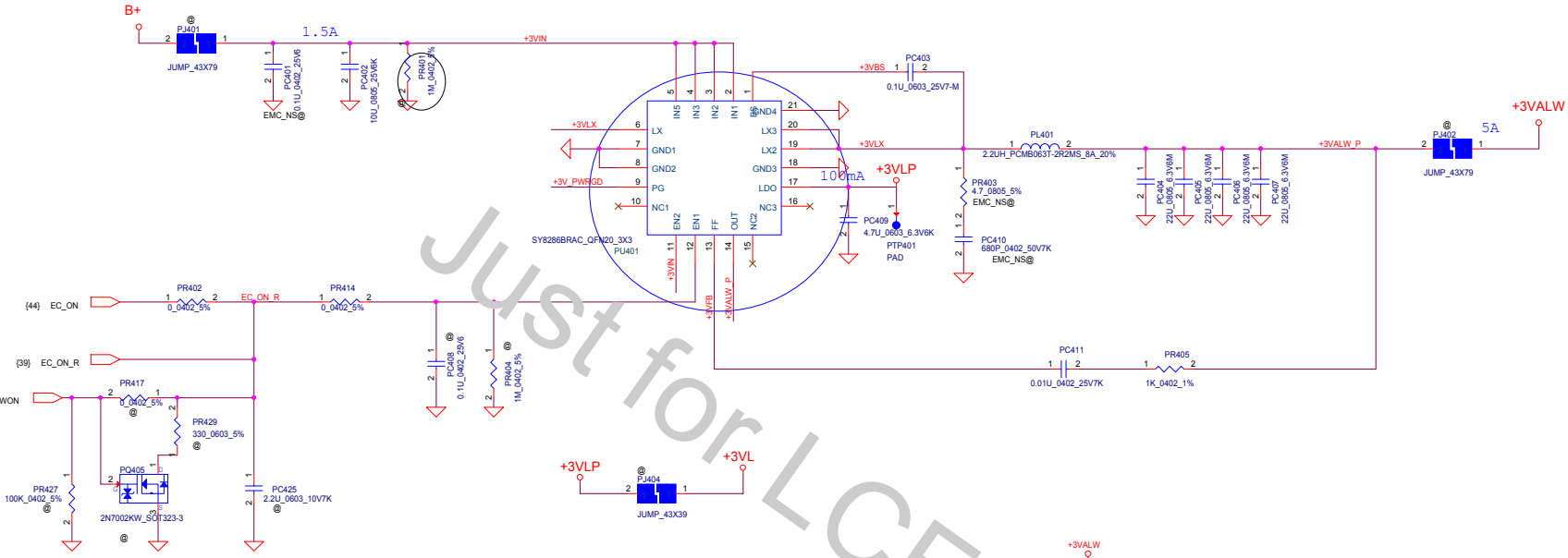
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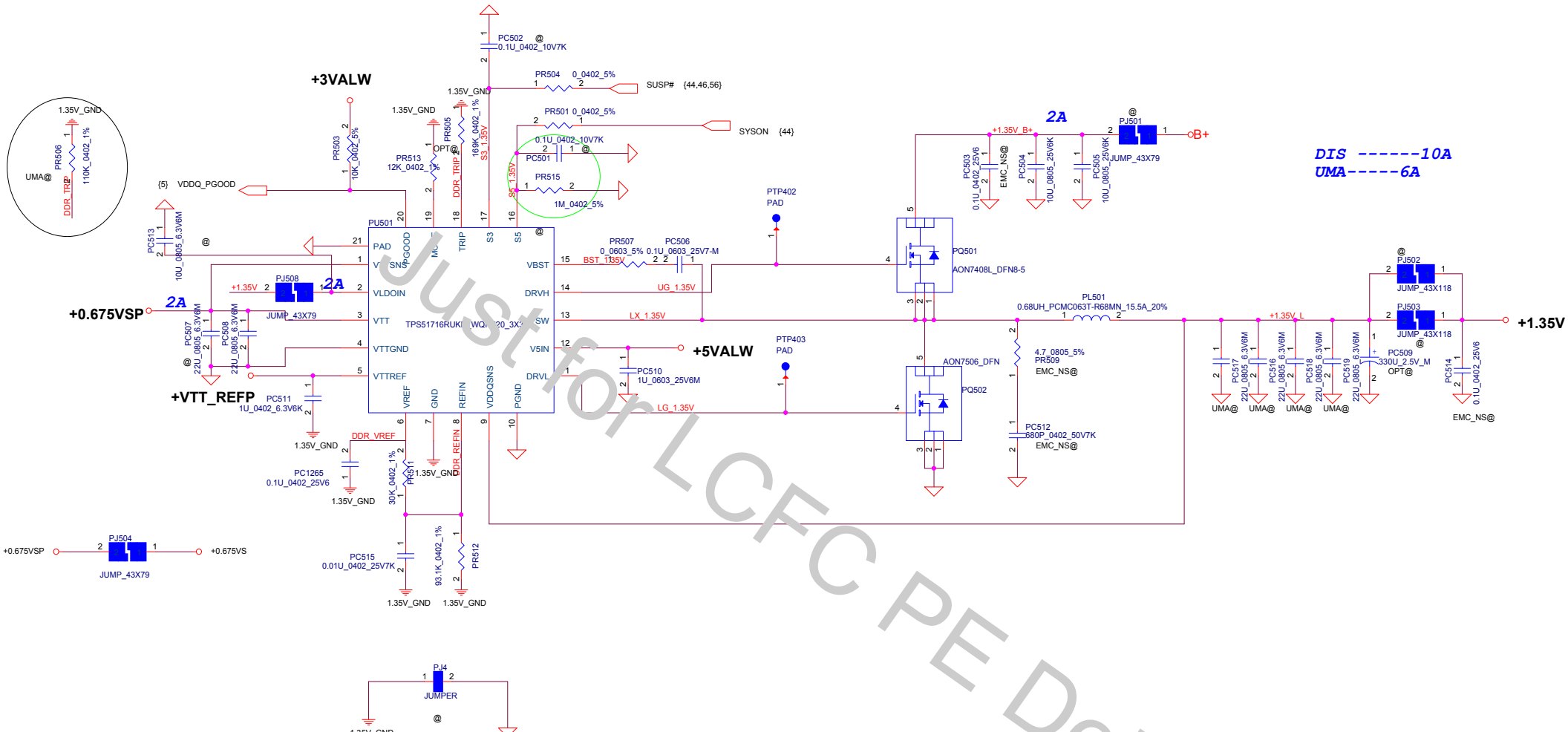
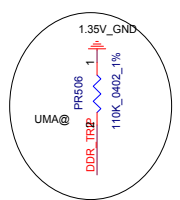




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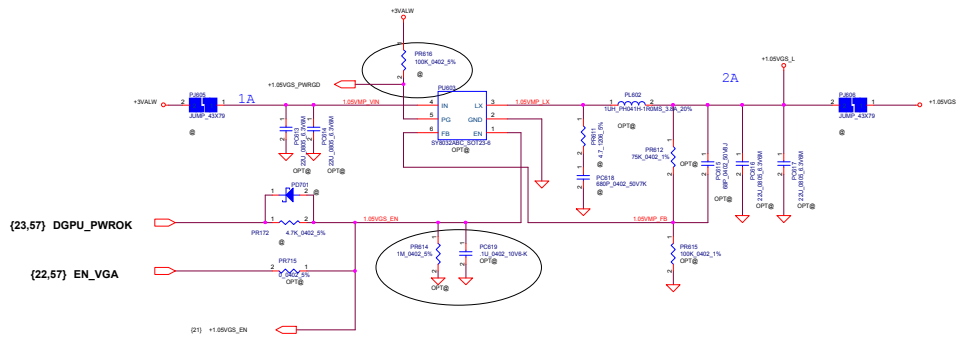
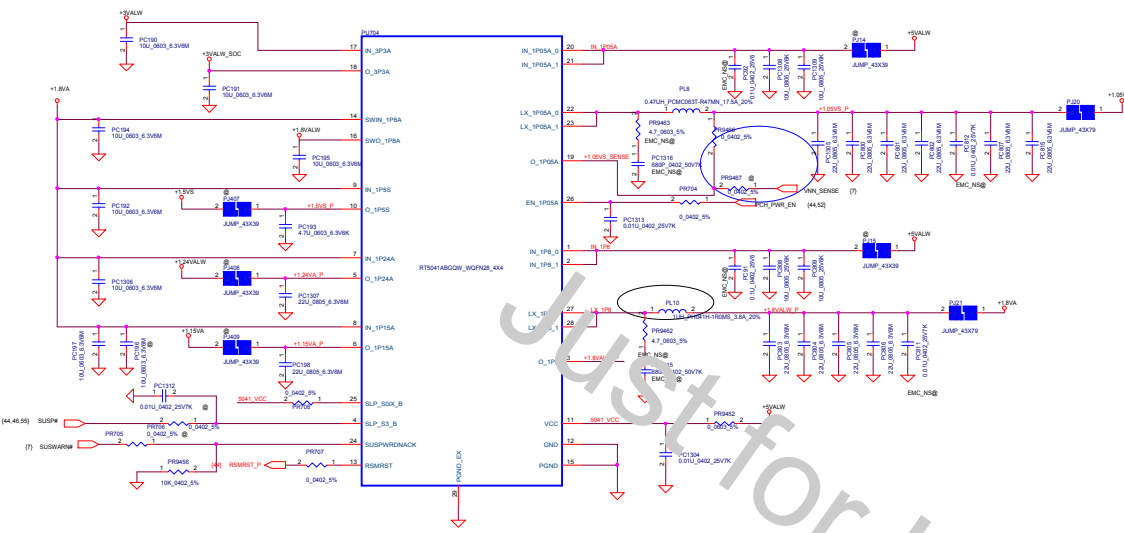
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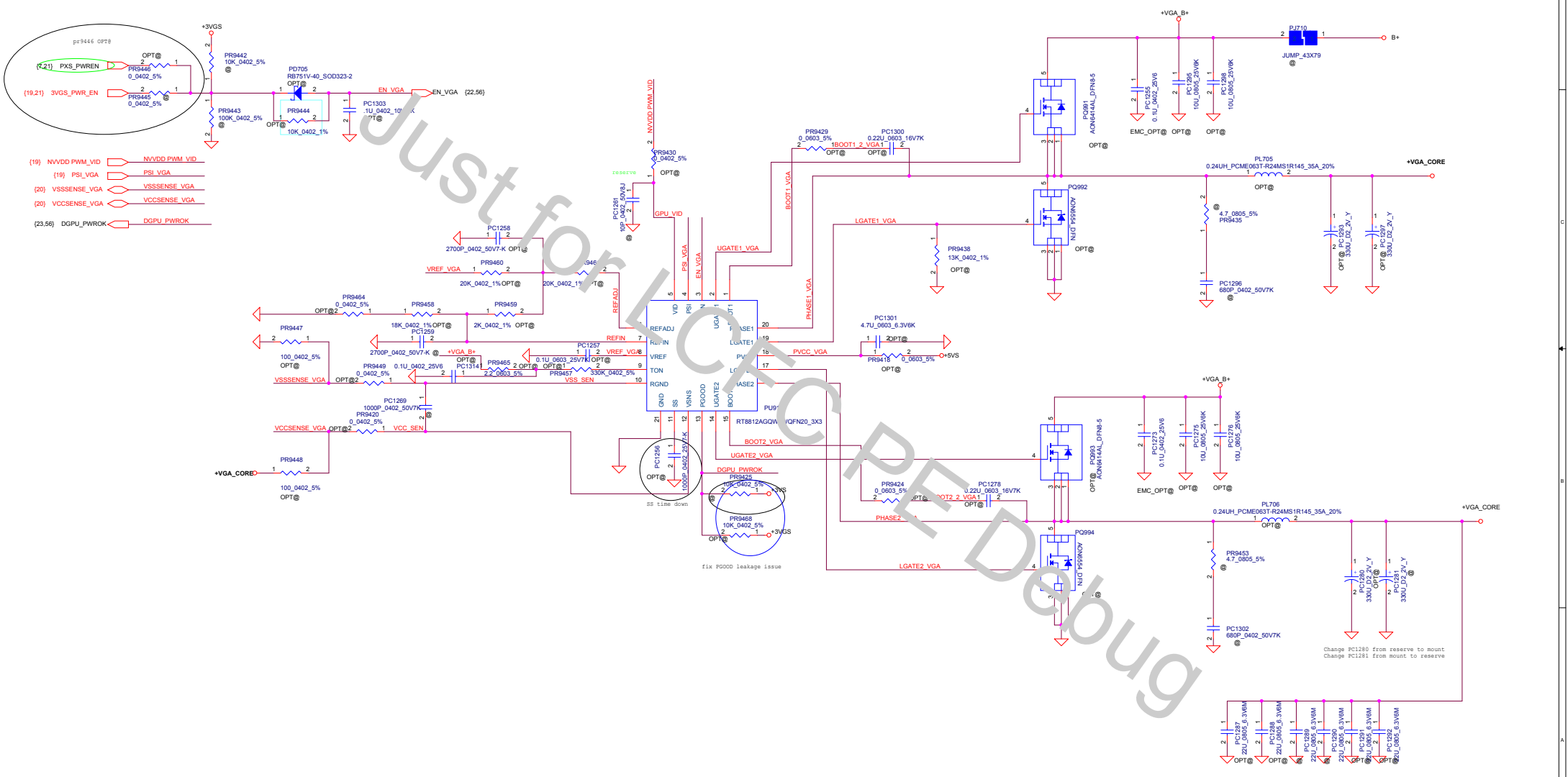
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		BMWC1	0.4

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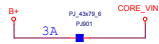
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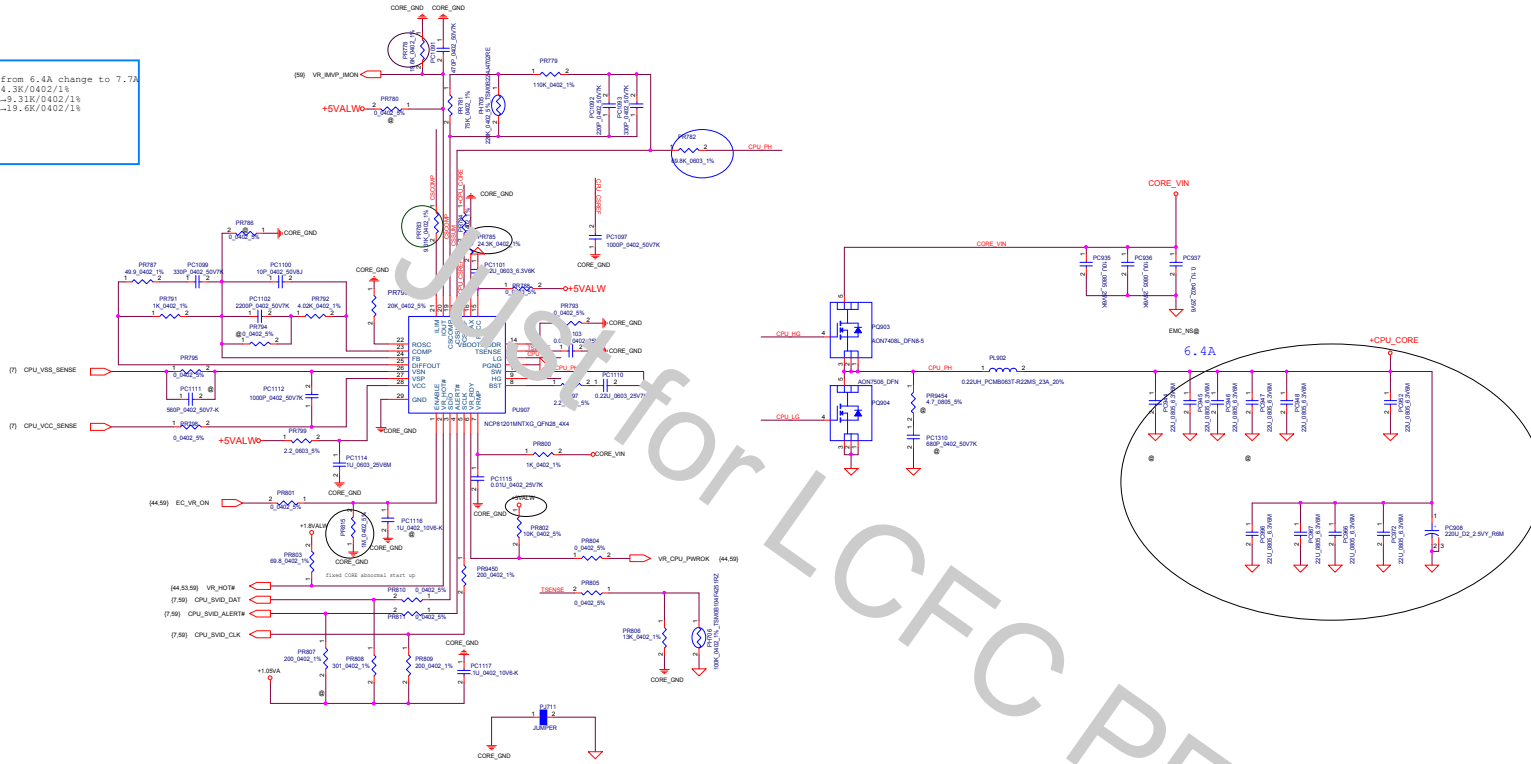


- (19) NVVDD\_PWM\_VID <-> NVVDD\_PWM\_VID
- (19) PSI\_VGA <-> PSI\_VGA
- (20) VSSSENSE\_VGA <-> VSSSENSE\_VGA
- (20) VCCSENSE\_VGA <-> VCCSENSE\_VGA
- (23.56) DGPU\_PWROK <-> DGPU\_PWROK

Security Classification	LC Future Center Secret Data		Title	 <b>PWR-VGA_CORE</b>
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for CPU TDC from 6.4A change to 7.7A  
 PR785: 23.5K-24.3K/0.402/1%  
 PR783: 7.68K-9.31K/0.402/1%  
 PR778: 20.5K-19.6K/0.402/1%



LCFC PE Debug

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