LCFC Confidential

SOLO/LANDO

EL480/580

NM-B461 Rev0.1 Schematic

Intel KabyLake/KabyLake-R Processor with DDR4 + PCH

AMD R17M-M1-70

2017-04-19 Rev0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	COVER PAGE	
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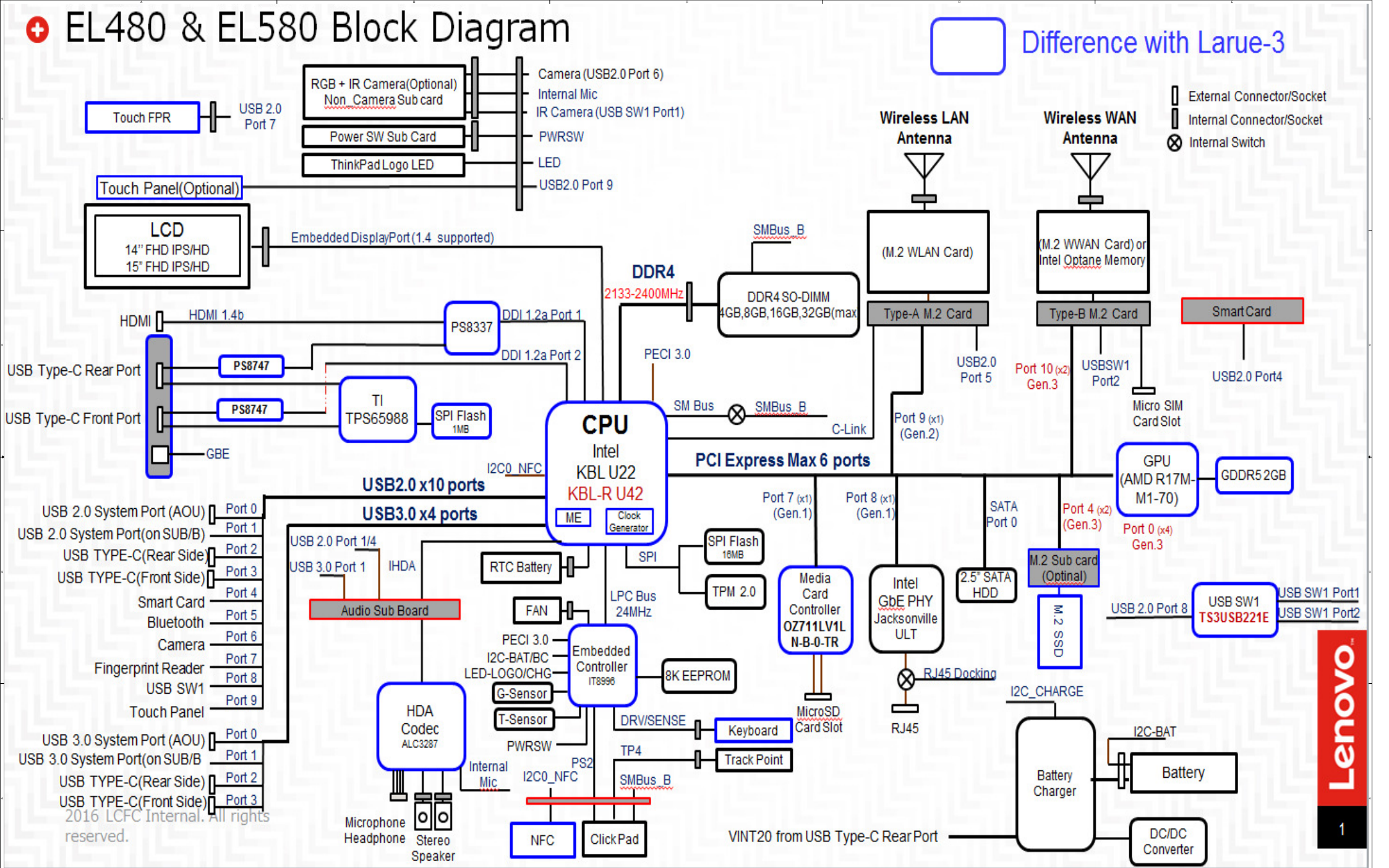
EL480 & EL580 Block Diagram



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Title: BLOCK DIAGRAM

Size: C | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

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Voltage Rails

O --> Means ON
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

	SIGNAL						
STATE	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	PCH	EC	GPU	TYPE-C	BATT	Charge	DIMM-A	DIMM-B	G-Sensor	Thermal	CLICK Pad	LAN
EC_SMB_CK1 EC_SMB_DA1	X	V +3VL_EC	X	X	V +3VL_EC	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	X	V VCC3_LDO_PD	X	V VCC3_LDO_PD	X	X	X	X	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	V +3VALW_PCH	X	X	X	X	X	V +3VS	V +3VS	X	X	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	V +3VALW_PCH	X	X	X	X	X	X	X	X	X	X	V +3VALW
PCH_SML1_CLK PCH_SML1_DAT	V +3VALW_PCH	V +3VS	V +3VS_VGA	X	X	X	X	X	V +3VS	V +3VS	X	X
CLK_PD DATA_PD	V +1.8VALW	X	X	V VCC3_LDO_PD	X	X	X	X	X	X	X	X

HSIO Port

Port	HIGH Speed	Device
1	USB3 1	Syetem Port(AOU)
2	USB3 2/SSIC	System Port on SUB/B
3	USB3 3	TYPE-C(Rear Side)
4	USB3 4	TYPE-C(Front Side)
5	USB3 5/PCIE 1	PCIE (GPU) Lane 0
6	USB3 6/PCIE 2	PCIE (GPU) Lane 1
7	PCIE 3 (GbE)	PCIE (GPU) Lane 2
8	PCIE 4 (GbE	PCIE (GPU) Lane 3
9	PCIE 5 (GbE)	PCIe 0 (Storage)
10	PCIE 6	PCIe 1 (Storage)
11	PCIE 7/SATA 0	SATA 0 (Storage)
12	PCIE 8/SATA 1A	PCIE Media Card Reader
13	PCIE 9 (GbE)	GbE PHY
14	PCIE 10 (GbE)	PCIE (WLAN)
15	PCIE 11/SATA 1B	PCIe 1(Optane)
16	PCIE 12/SATA 2	PCIe 0(Optane)/SATA 2/WWAN

USB2.0 Port

Port	Device
1	System Port(AOU)
2	System Port on SUB/B
3	TYPE-C(Rear Side)
4	TYPE-C(Front Side)
5	Smart Card
6	Bluetooth
7	Camera
8	Finger Printer
9	WWAN/IR Camera (USB Switch)
10	Touch Panel

USB Switch

USB Switch Port1	WWAN (option)
USB Switch Port2	IR USB CAMERA (option)

Title: SYSTEM LIST

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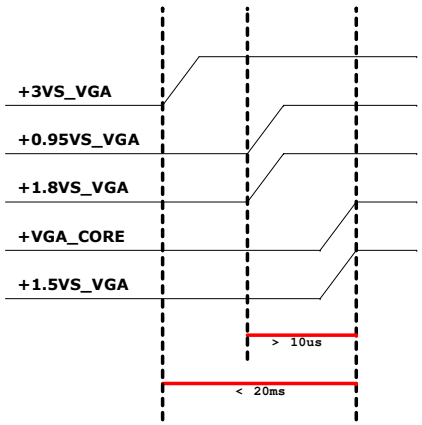
VGA GPIO (EXO-PRO-S3)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN		GPIO5_AC_BATT
GPIO6	IN		GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	N/A	GPIO8_ROMSO
GPIO9	OUT	N/A	GPIO9_ROMSI
GPIO10	OUT	N/A	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN		SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN		SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

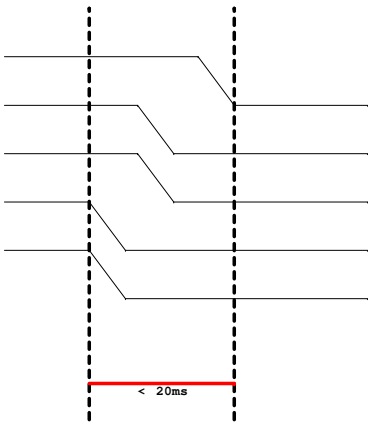
BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)
KBL@	For KBL-R SKU
KBLR@	For KBL SKU

GPU POWER UP sequence



GPU POWER DOWN sequence



	Device ID
EXO-pro	6660

GPU		EXO-Pro-S3	
VRAM (GDDR3)		PS_3 (RV104)	PS_3 (RV105)
Samsung 1000MHz			
	K4W4G1646E-BC1A (2G)	PH 3.4K	PD 10K
Hynix 1000MHz			
	H5TC4G63CFR-N0C (2G)	PH 4.75K	NC
Micro 1000MHz			
	MT41J256M16HA-093G:E (2G)	PH 3.24K	PD 5.62K

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Title: BOM LIST

Size	Document Number	Rev
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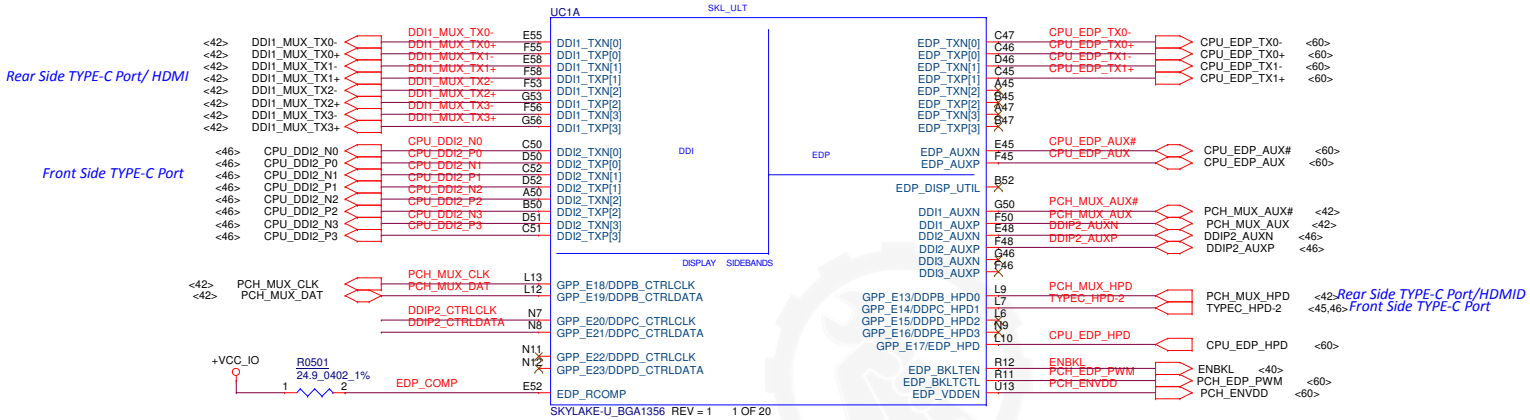
+3VS +3VS <9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>

DP port	Enable	Disable
DDPB_CTRLDATA	pull-high	no connect
DDPC_CTRLDATA	pull-high	no connect



EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP
Trace Width=20mil, Spacing=25mil, Max length=100mil

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Title: KBL(A)_DDI/eDP

Size	Document Number	Rev
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+3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>
+2.5V <23,24,25,26,95>
+3VALW <9,10,12,15,19,39,40,43,45,46,49,52,58,60,62,63,64,65,67,72,83,84,85,96>
+1.2V <7,18,23,24,25,26,86>

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71 AL68 AN68 AN69 AL70 AL69 AN70 AR71 AR70 AR68 AU71 AU68 AR71 AR69 AU70 AU69	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]
Block 2	BB65 AW65 AW63 AY63 BA65 AY65 BA63 BB63 BA61 BB59 AW59 BB61 AY61 BA59 AY59	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]
Block 4	AY39 AW39 AY37 AW37 BB39 BA39 BA37 BB37 AY35 AW35 AY33 AW33 BB35 BA35 BA33 BB33	DDR0_DQ[32] DDR0_DQ[33] DDR0_DQ[34] DDR0_DQ[35] DDR0_DQ[36] DDR0_DQ[37] DDR0_DQ[38] DDR0_DQ[39] DDR0_DQ[40] DDR0_DQ[41] DDR0_DQ[42] DDR0_DQ[43] DDR0_DQ[44] DDR0_DQ[45] DDR0_DQ[46] DDR0_DQ[47]	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]
Block 6	AY31 AW31 AY29 AW29 BB31 BA31 BA29 BB29 AY27 AW27 AY25 AW25 BB27 BA27 BA25 BB25	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[62] DDR0_DQ[63]	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46] DDR1_DQ[47]

LOGIC

TABLE

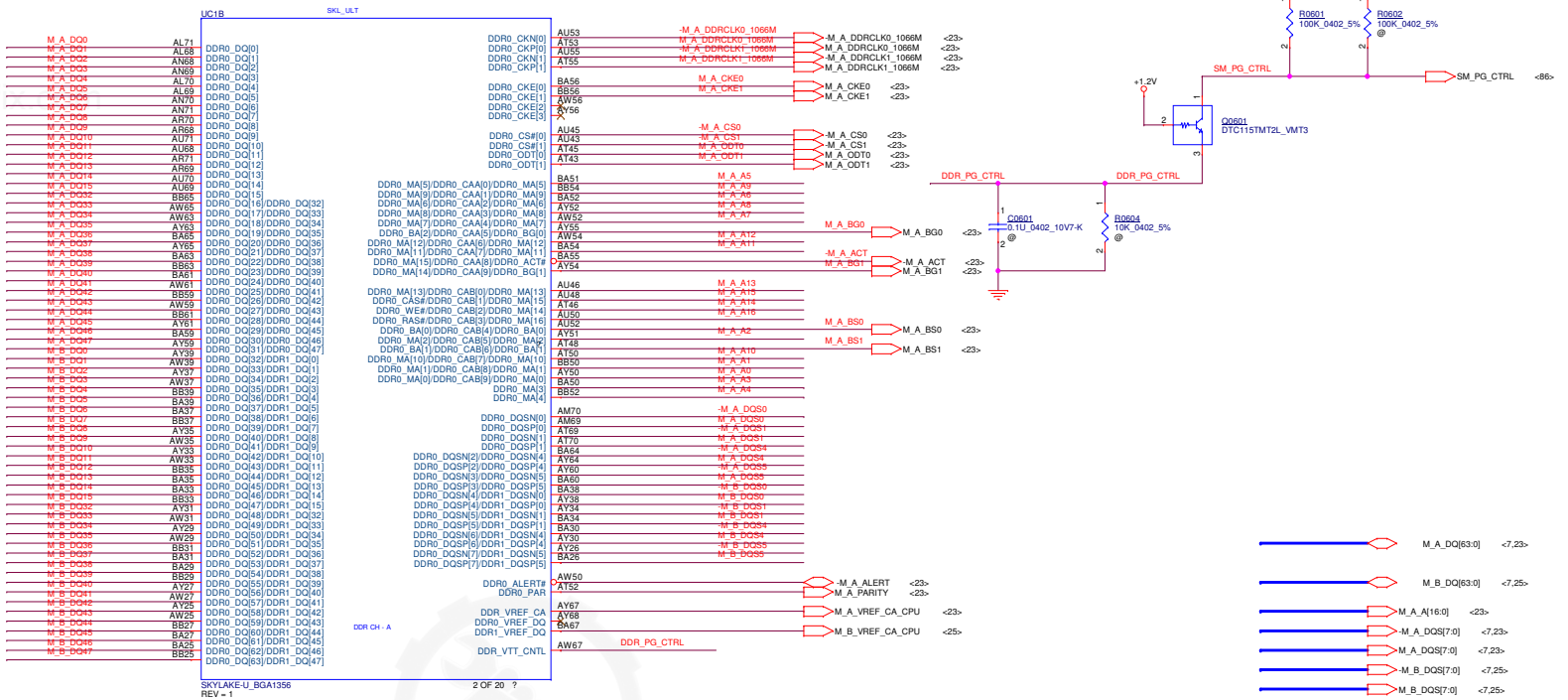
	Pin	Interleave	Non-Interleave
Block 0	AM70 AM69 AT69 AT70	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]
Block 2	BA64 AY64 AY60 BA60	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
Block 4	BA38 AY38 AY34 BA34	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]
Block 6	BA30 AY30 AY26 BA26	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]

LOGIC

TABLE

Pin	DDR4
BA51 BB54 BA52 AY52 AW52 AY55 AW54 BA54 BA55 AY54	DDR0_MA[5] DDR0_MA[9] DDR0_MA[6] DDR0_MA[8] DDR0_MA[7] DDR0_BG[0] DDR0_MA[12] DDR0_MA[11] DDR0_ACT# DDR0_BG[1]
AU46 AU48 AT46 AU50 AU52 AY51 AT48 AT50 BB50 AY50 BA50 BB52	DDR0_MA[13] DDR0_MA[15] DDR0_MA[14] DDR0_MA[16] DDR0_BA[0] DDR0_MA[2] DDR0_BA[1] DDR0_MA[10] DDR0_MA[1] DDR0_MA[0] DDR0_MA[3] DDR0_MA[4]

LOGIC



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Title: KBL(B)_DDR4 CH.A

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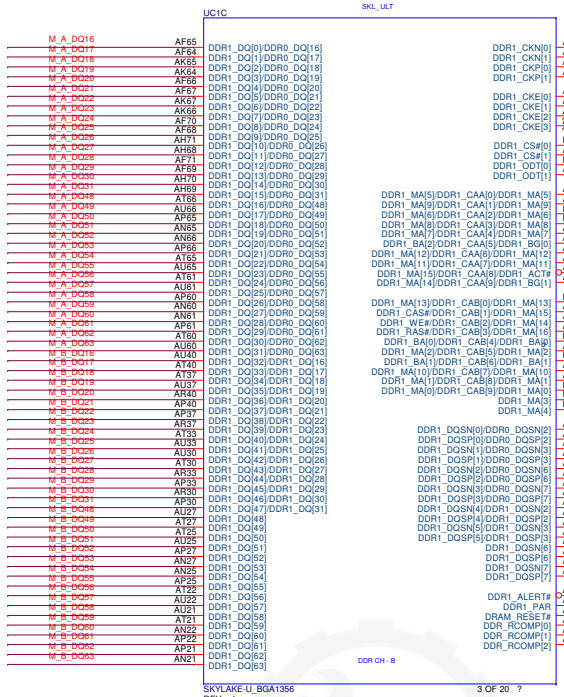
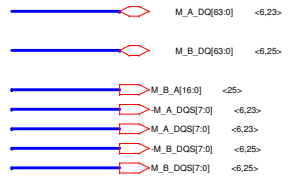
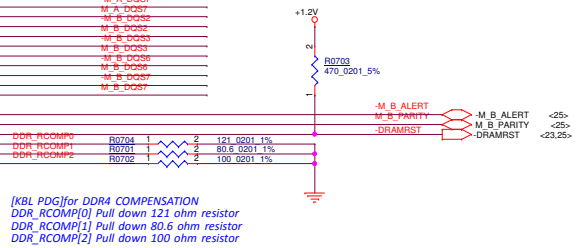
+1.2V +1.2V <6,18,23,24,25,26,86>

+3VS +3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>







[KBL PDG]for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65 AF64 AK65 AK64 AF66 AF67 AK67 AK66 AF70 AF68 AH71 AH68 AF71 AF69 AH70 AH69	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]
Block 3	AT66 AU66 AP65 AN65 AN66 AP66 AT65 AU65 AT61 AU61 AP60 AN60 AN61 AP61 AT60 AU60	DDR1_DQ[16] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30] DDR1_DQ[31]	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61] DDR0_DQ[62] DDR0_DQ[63]
Block 5	AU40 AT40 AT37 AU37 AR40 AP40 AP37 AR37 AT33 AU33 AU30 AT30 AR33 AP33 AR30 AP30	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46] DDR1_DQ[47]	DDR1_DQ[16] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30] DDR1_DQ[31]
Block 7	AU27 AT27 AT25 AU25 AP27 AN27 AN25 AP25 AT22 AU22 AU21 AT21 AN22 AP22 AP21 AN21	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] DDR1_DQ[63]	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] DDR1_DQ[63]

LOGIC

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66 AH65 AG69 AG70	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]
Block 3	AR66 AR65 AR61 AR60	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]
Block 5	AT38 AR38 AT32 AR32	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]
Block 7	AR25 AR27 AR22 AR21	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR4
AY48 AP50 BA48 BB48 AP48 AP52 AN50 AN48 AN53 AN52	DDR1_MA[5] DDR1_MA[9] DDR1_MA[6] DDR1_MA[8] DDR1_MA[7] DDR1_BG[0] DDR1_MA[12] DDR1_MA[11] DDR1_ACT# DDR1_BG[1]
BA43 AY43 AY44 AW44 BB44 AY47 BA44 AW46 AY46 BA46 BB46 BA47	DDR1_MA[13] DDR1_MA[15] DDR1_MA[14] DDR1_MA[16] DDR1_BA[0] DDR1_MA[2] DDR1_BA[1] DDR1_MA[10] DDR1_MA[1] DDR1_MA[0] DDR1_MA[3] DDR1_MA[4]

LOGIC

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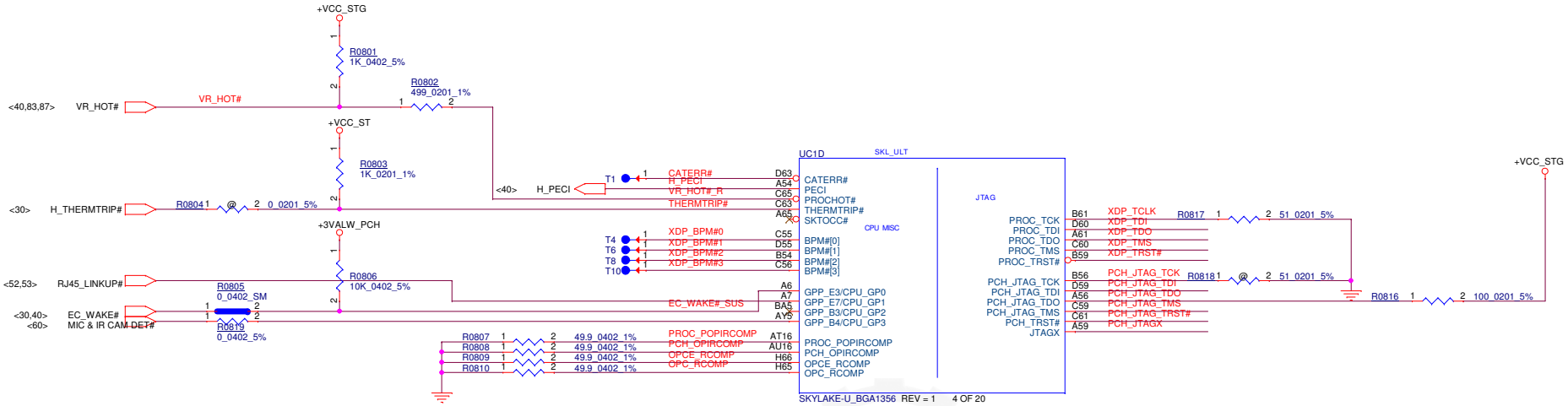
+VCC_ST +VCC_ST <15,16,18,21,71,87>

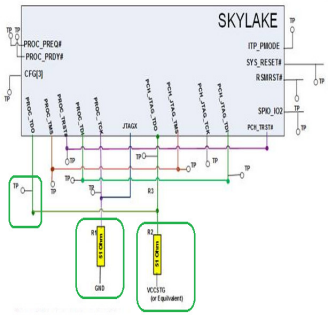
+VCC_STG +VCC_STG <16,18,71>

+3VALW_PCH +3VALW_PCH <9,10,11,12,19>



XDP_TCLK	R0811 1 DCI@ 2 0_0201_5%	PCH_JTAGX
XDP_TDI	R0812 1 DCI@ 2 0_0201_5%	PCH_JTAG_TDI
XDP_TDO	R0813 1 DCI@ 2 0_0201_5%	PCH_JTAG_TDO
XDP_TMS	R0814 1 DCI@ 2 0_0201_5%	PCH_JTAG_TMS
XDP_TRST#	R0815 1 DCI@ 2 0_0201_5%	PCH_JTAG_TRST#

[KBL PDG FOR DCL DEBUG]



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Title: KBL(D)_MISC/ JTAG

Size	Document Number	Rev
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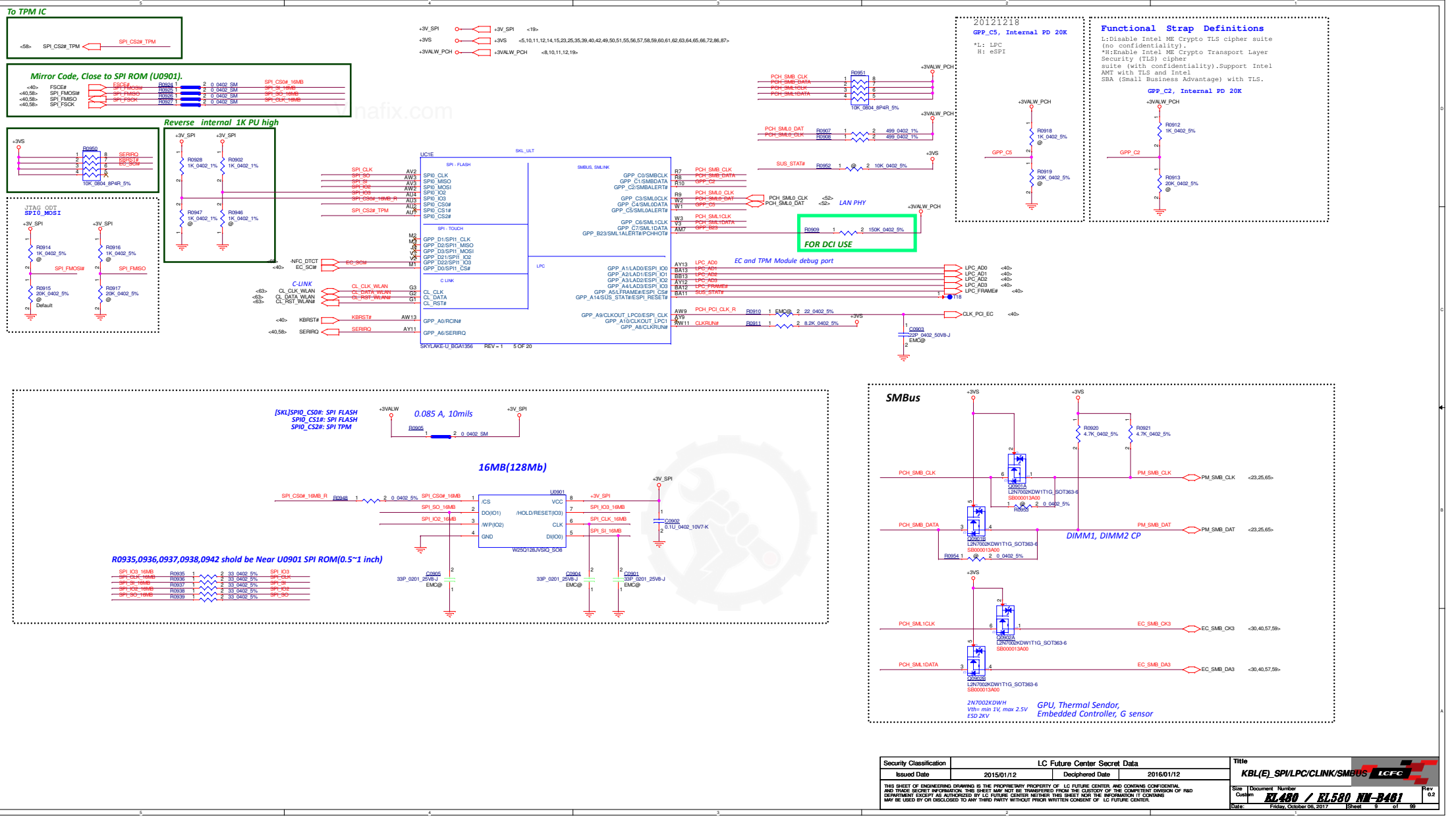

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

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Title	KBL(E)_SPI/LPC/CLINK/SMBUS		
Size: Custom	Document Number: EL480 / EL580 NM-B461		Rev: 0.2
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+3VALW_PCH +3VALW_PCH <8,9,11,12,19>

+3VS +3VS <5,9,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>

+3VALW +3VALW <6,9,12,15,19,39,40,43,45,46,49,52,58,60,62,63,64,65,67,72,83,84,85,96>

GPP_B18, Internal PD 20K

*L: Disable " No Reboot" mode
H: Enable " No Reboot" mode

+3VALW_PCH
R1008 1K_0402_5% @
GPP_B18
R1009 20K_0402_5% @

GPP_B22, Internal PD 20K

*L: SPI
H: LPC

+3VS
R1010 20K_0402_5% @
GPP_B22
R1011 20K_0402_5% @

+3VALW_PCH
R1001 10K_0402_5% @
RF_OFF#
+3VS
R1002 10K_0402_5%

+3VALW_PCH +3VS
R1003 10K_0402_5% VGA_ON
R1004 4.7K_0402_5% BT_ON
R1007 10K_0402_5% DGPU_HOLD_RST#

UC1F SKL_ULT

LPSS

<63> RF_OFF#	RF_OFF#	AN8	GPP_B15/GSPI0_CS#
<66> NFC_DLREQ	NFC_DLREQ	AP7	GPP_B16/GSPI0_CLK
<50> HP_JACK_IN	HP_JACK_IN	AP8	GPP_B17/GSPI0_MISO
	GPP_B18	AR7	GPP_B18/GSPI0_MOSI
		AM5	GPP_B19/GSPI1_CS#
	PLANARID0	AN7	GPP_B20/GSPI1_CLK
<63> BT_ON	BT_ON	AP5	GPP_B21/GSPI1_MISO
	GPP_B22	AN5	GPP_B22/GSPI1_MOSI
		AB1	GPP_C8/UART0_RXD
<60> S_L_CTL	S_L_CTL	AB2	GPP_C9/UART0_TXD
	PLANARID1	W4	GPP_C10/UART0_RTS#
	PLANARID2	AB3	GPP_C11/UART0_CTS#
<49,63> UART2_RX	UART2_RX	AD1	GPP_C20/UART2_RXD
<49,63> UART2_TX	UART2_TX	AD2	GPP_C21/UART2_TXD
	PLANARID4	AD3	GPP_C22/UART2_RTS#
<60> TPNL_EN	TPNL_EN	AD4	GPP_C23/UART2_CTS#
<64> WWAN_IR_SW	WWAN_IR_SW	U7	GPP_C16/I2C0_SDA
<30,38,39,92> VGA_ON	VGA_ON	U6	GPP_C17/I2C0_SCL
<38,92> DGPU_PWROK	DGPU_PWROK	U8	GPP_C18/I2C1_SDA
<35> DGPU_HOLD_RST#	DGPU_HOLD_RST#	U9	GPP_C19/I2C1_SCL
<66> I2C0_DATA		AH9	GPP_F4/I2C2_SDA
<66> I2C0_CLK		AH10	GPP_F5/I2C2_SCL
	DATA_PD	AH11	GPP_F6/I2C3_SDA
	CLK_PD	AH12	GPP_F7/I2C3_SCL
<62> PCH_WWAN_RST#	PCH_WWAN_RST#	AF11	GPP_F8/I2C4_SDA
		AF12	GPP_F9/I2C4_SCL

ISH

		P2	GPP_D9
-LID_CLOSE	LID_CLOSE	P3	GPP_D10
PAD_DISABLE	PAD_DISABLE	P4	GPP_D11
TP_RESET	TP_RESET	P1	GPP_D12
		M4	GPP_D5/ISH_I2C0_SDA
-PD_I2C_INT		N3	GPP_D6/ISH_I2C0_SCL
		N1	GPP_D7/ISH_I2C1_SDA
WWANRF_DISABLE#	WWANRF_DISABLE#	N2	GPP_D8/ISH_I2C1_SCL
		AD11	GPP_F10/I2C5_SDA/ISH_I2C2_SDA
		AD12	GPP_F11/I2C5_SCL/ISH_I2C2_SCL
		U1	GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
		U2	GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
		U3	GPP_D15/ISH_UART0_RTS#
MUX_SW_PCH	MUX_SW_PCH	U4	GPP_D16/ISH_UART0_CTS#/SML0BALERT#
		AC1	GPP_C12/UART1_RXD/ISH_UART1_RXD
F1_LED#	F1_LED#	AC2	GPP_C13/UART1_TXD/ISH_UART1_TXD
F4_LED#	F4_LED#	AC3	GPP_C14/UART1_RTS#/ISH_UART1_RTS#
	GPP_C15	AB4	GPP_C15/UART1_CTS#/ISH_UART1_CTS#
		AY8	GPP_A18/ISH_GP0
		BA8	GPP_A19/ISH_GP1
		BB7	GPP_A20/ISH_GP2
		BA7	GPP_A21/ISH_GP3
		AY7	GPP_A22/ISH_GP4
		AW7	GPP_A23/ISH_GP5
		AP13	GPP_A12/BM_BUSY#/ISH_GP6

SKYLAKE-U_BGA1356 REV = 1 6 OF 20

TP4313 TP4314

+3VS
R1026 10K_0402_5% GPP_C15
R1027 10K_0402_5% F1_LED#
R1028 10K_0402_5% F4_LED#
R1036 10K_0402_5% WWANRF_DISABLE#

+3VALW
R1035 10K_0402_5%
R1034 10K_0402_5%
WWAN_CFG1 <62>
WWAN_CFG2 <62>
WWAN_CFG3 <62>
WWAN_CFG0 <62>

+1.8VALW
R1037 10K_0201_5%
R1038 10K_0201_5%
<45,46> I2C_DATA_PD
DATA_PD
Q1002 LBSS138LT1G_SOT-23-3
<45,46> I2C_CLK_PD
CLK_PD
Q1001 LBSS138LT1G_SOT-23-3

Project/SKU ID

	PLANARID3 GPP_C11	PLANARID2 GPP_C10	PLANARID0 GPP_B20	PLANARID1 (GPP_C9)	PLANARID4 (GPP_22)
SDV	0	0	0	0:UMA (R1024) 1:DIS(R1023)	0:KBLR(R1030) 1:KBL(R1031)
FVT	0	0	1	0:UMA (R1024) 1:DIS(R1023)	0:KBLR(R1030) 1:KBL(R1031)
SIT	0	1	0	0:UMA (R1024) 1:DIS(R1023)	0:KBLR(R1030) 1:KBL(R1031)
SVT	0	1	1	0:UMA (R1024) 1:DIS(R1023)	0:KBLR(R1030) 1:KBL(R1031)

+3VS
R1019 @ 10K_0402_5%
R1021 10K_0402_5%
R1023 10K_0402_5% DIS@
R1031 10K_0402_5% KBL@
R1032 10K_0402_5%
PLANARID0
PLANARID1
PLANARID2
PLANARID3
PLANARID4
R1020 10K_0402_5%
R1022 10K_0402_5% @
R1024 10K_0402_5% UMA@
R1030 10K_0402_5% KBLR@
R1033 10K_0402_5%

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Title: KBL(F)_GPIO

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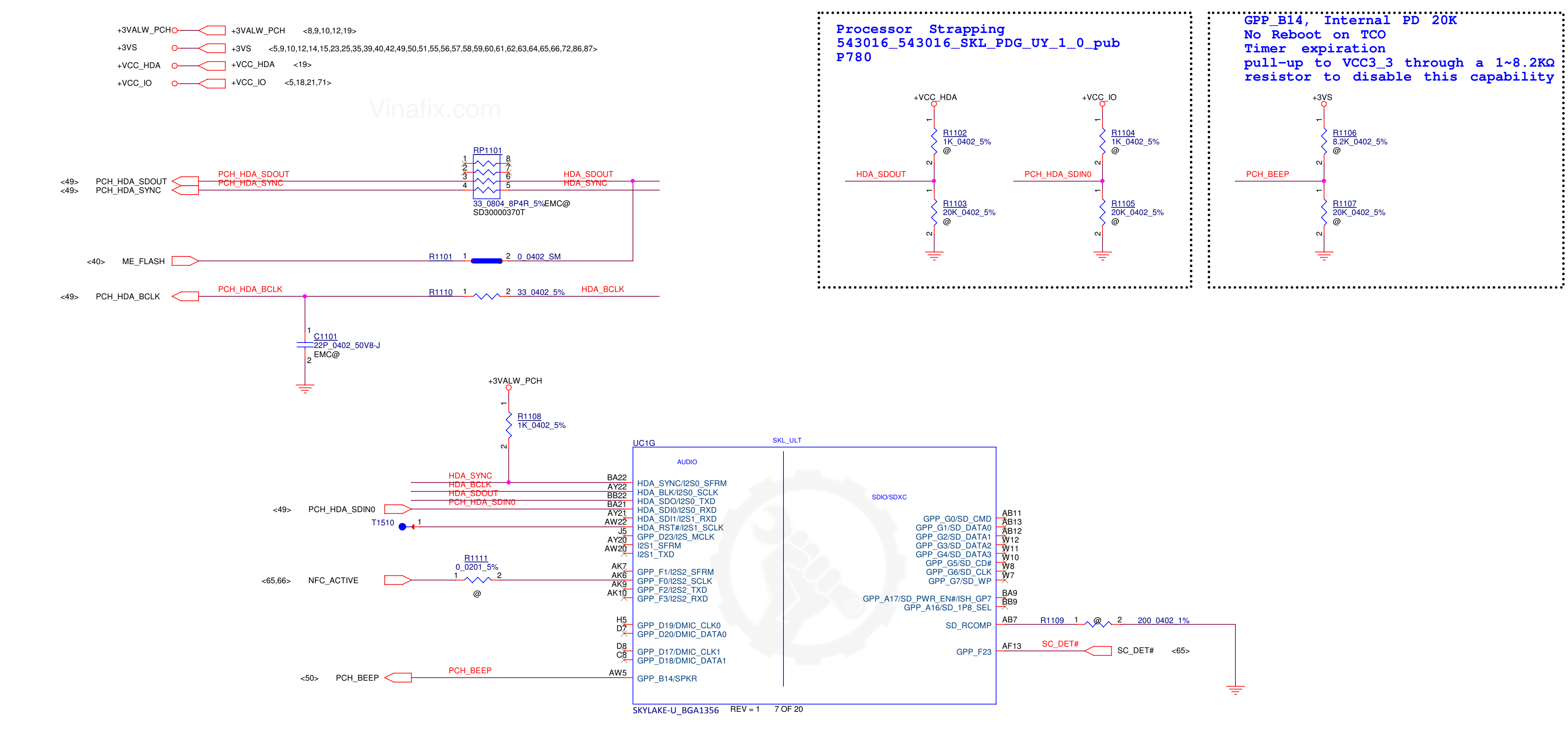

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Title: KBL(G)_HDA/ GPIO

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

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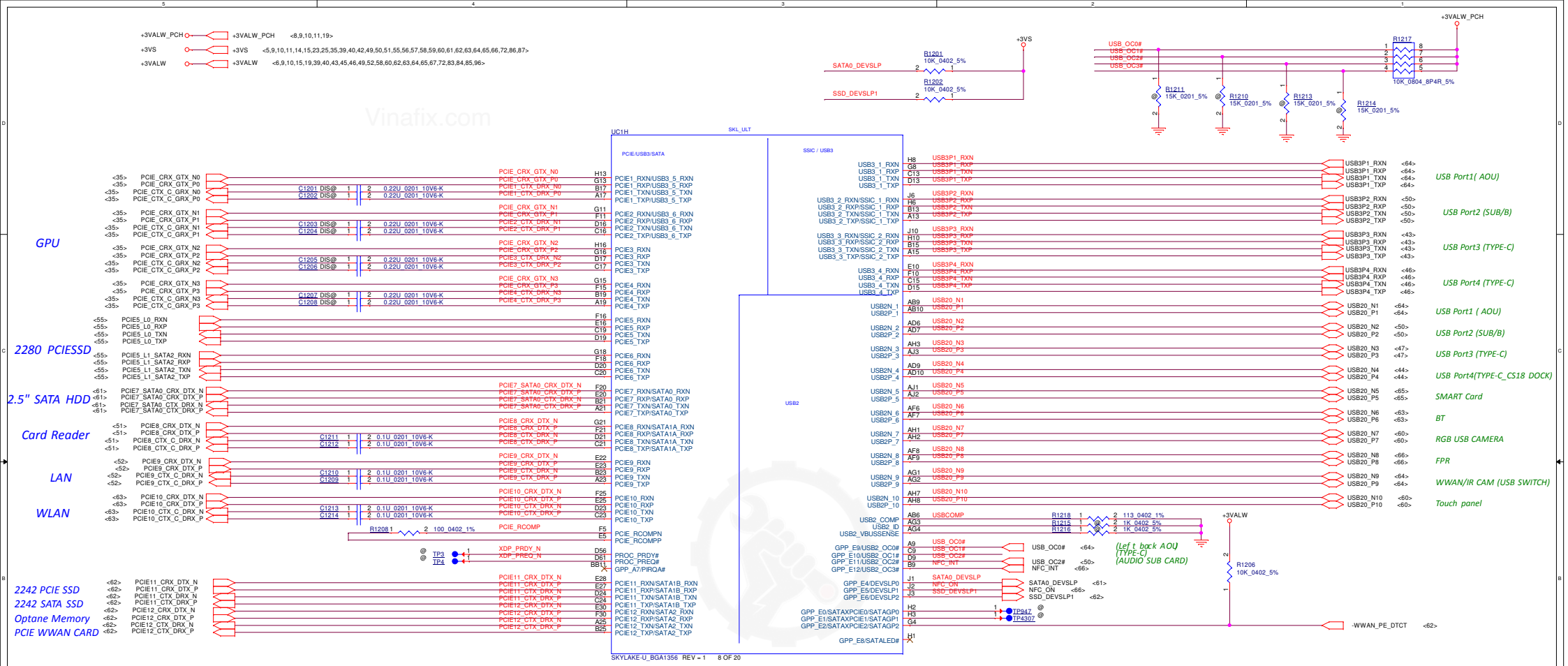
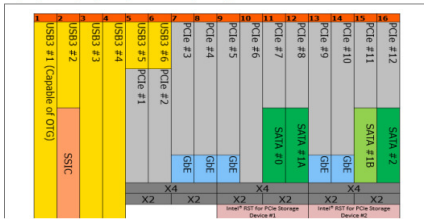


Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP



Pin.	USB3.0 Port NO.	USB2.0 Port NO.	Default Port Mapping
USB_OC0#	Port 1	Port 1	System Port(AOU)
USB_OC1#	Unused.	Unused.	Unused.
USB_OC2#	port 2	port 2	System Port on SUB/B
USB_OC3#	Unused.	Unused.	Unused.

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Title: KBL(H)_PCIE/ SATA/ USB30

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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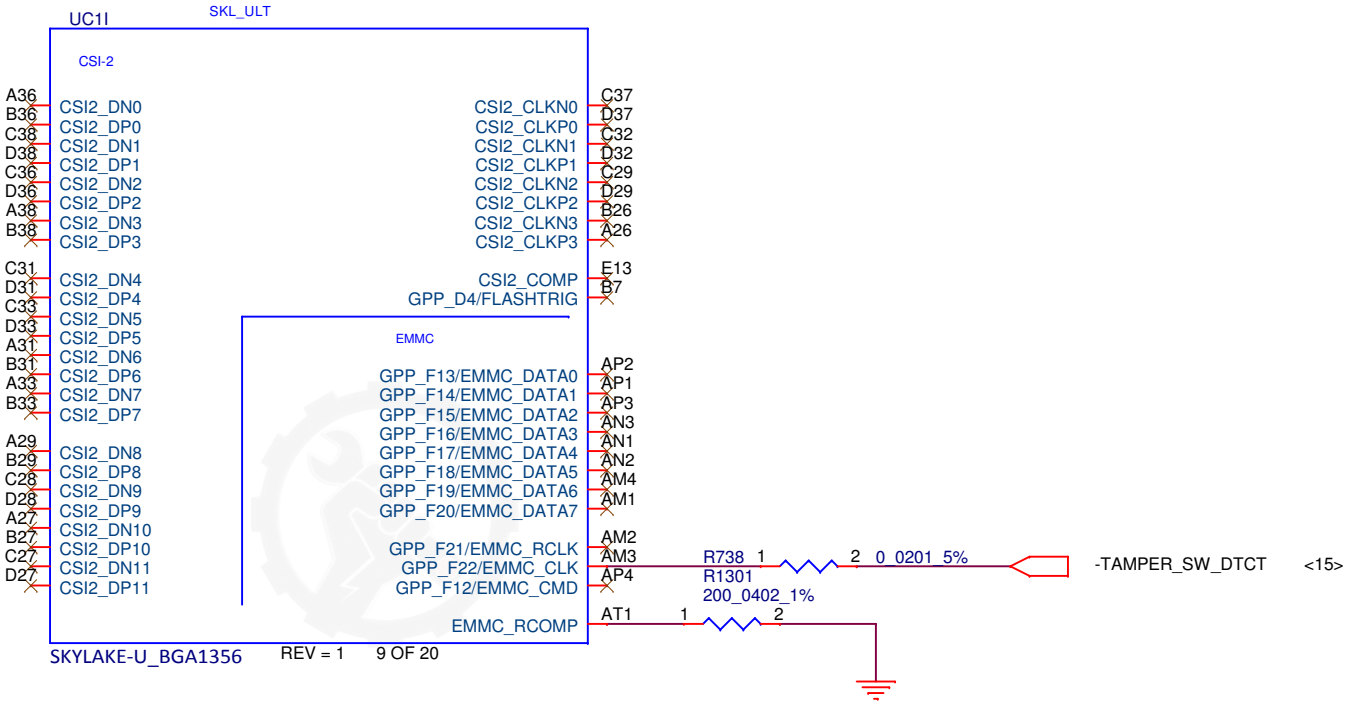

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **KBL(I)_CS12/ EMMC**

Size	Document Number	Rev
A4	EL480 / EL580 NM-B461	0.2

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+RTCBATT +RTCBATT <66,80>
+RTCVCC +RTCVCC <15,19>
+3VS +3VS <5,9,10,11,12,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>
+1VALW +1VALW <19,39,71,96>

RTC External Circuit

+RTCBATT, +RTCVCC
Trace width = 20mils

+RTCBATT
+RTCVCC
R1401 1 2 0_0402_SM
C1401 0.1U_0402_10V6-K
near CC59 for layout

+RTCVCC
R1402 20K_0402_5% PCH_RTCRST# JCMOS1 @ C1402 1U_0402_10V6-K
R1403 20K_0402_5% PCH_SRTCRST# JME1 @ C1403 1U_0402_10V6-K

RTC Crystal

1. Space > 15mils
2. No trace under crystal
3. Place on oppsosit side of MCP for temp inf l uence

PCH_RTCX1
R1404 10M_0402_5%
PCH_RTCX2
YC3 32.768KHZ_9PF_9H03280012
C1404 5.6P_0402_50V8-D
C1405 5.6P_0402_50V8-D

+3VS
R1406 10K_0402_5% UMA@ CLKREQ_PCIE4_VGA#
R1407 10K_0402_5% DIS@

+3VS
RP1401 10K_0804_8P4R_5%
CLKREQ_PCIE2_WLAN#
CLKREQ_PCIE3_LAN#
CLKREQ_PCIE1_SSD#
CLKREQ_PCIE5_CR#

UC1J SKL_ULT
CLOCK SIGNALS

HDD	<56>	CLK_PCIE_HDD#	CLK_PCIE_HDD#	D42	CLKOUT_PCIE_N0
	<56>	CLK_PCIE_HDD	CLK_PCIE_HDD	C42	CLKOUT_PCIE_P0
	<56>	CLKREQ_PCIE0_HDD#	CLKREQ_PCIE0_HDD#	AR10	GPP_B5/SRCCLKREQ0#
M.2 SSD	<62>	CLK_PCIE_SSD#	CLK_PCIE_SSD#	B42	CLKOUT_PCIE_N1
	<62>	CLK_PCIE_SSD	CLK_PCIE_SSD	A42	CLKOUT_PCIE_P1
	<62>	CLKREQ_PCIE1_SSD#	CLKREQ_PCIE1_SSD#	AT7	GPP_B6/SRCCLKREQ1#
WLAN	<63>	CLK_PCIE_WLAN#	CLK_PCIE_WLAN#	D41	CLKOUT_PCIE_N2
	<63>	CLK_PCIE_WLAN	CLK_PCIE_WLAN	C41	CLKOUT_PCIE_P2
	<63>	CLKREQ_PCIE2_WLAN#	CLKREQ_PCIE2_WLAN#	AT8	GPP_B7/SRCCLKREQ2#
LAN	<52>	CLK_PCIE_LAN#	CLK_PCIE_LAN#	D40	CLKOUT_PCIE_N3
	<52>	CLK_PCIE_LAN	CLK_PCIE_LAN	C40	CLKOUT_PCIE_P3
	<52>	CLKREQ_PCIE3_LAN#	CLKREQ_PCIE3_LAN#	AT10	GPP_B8/SRCCLKREQ3#
GPU	<35>	CLK_PCIE_VGA#	CLK_PCIE_VGA#	B40	CLKOUT_PCIE_N4
	<35>	CLK_PCIE_VGA	CLK_PCIE_VGA	A40	CLKOUT_PCIE_P4
	<30>	CLKREQ_PCIE4_VGA#	CLKREQ_PCIE4_VGA#	AU8	GPP_B9/SRCCLKREQ4#
CR	<51>	CLK_PCIE_CR#	CLK_PCIE_CR#	E40	CLKOUT_PCIE_N5
	<51>	CLK_PCIE_CR	CLK_PCIE_CR	E38	CLKOUT_PCIE_P5
	<51>	CLKREQ_PCIE5_CR#	CLKREQ_PCIE5_CR#	AU7	GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43 CLKOUT_ITPXDP_N → T56
CLKOUT_ITPXDP_P E43 CLKOUT_ITPXDP_P → T57
GPD8/SUSCLK BA17 SUSCLK_32K → SUSCLK_32K <63> to WLAN
XTAL24_IN E37 PCH_XTAL24_IN_KBL
XTAL24_OUT E35 PCH_XTAL24_OUT_KBL
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 PCH_RTCX1
RTCX2 AM20 PCH_RTCX2
SRTCRST# AN18 PCH_SRTCRST#
RTCRST# AM16 PCH_RTCRST#
+1VALW
R1409 2.71K_0402_0.5% SD00001LB1T

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Need close CPU For KBL-R U42 and KBL U22 control

PCH_XTAL24_IN_KBL R1413 1 KBL@ 2 0_0201_5% PCH_XTAL24_IN_KBL_R
PCH_XTAL24_OUT_KBL R1414 1 KBL@ 2 0_0201_5% PCH_XTAL24_OUT_KBL_R
R1412 KBL@ 1M_0402_5%
YC2 KBL@ 24MHZ_10PF_8Y24000011 GND1 GND2
C1414 KBL@ 10P_0402_50V8-J
C1415 KBL@ 10P_0402_50V8-J

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Title: KBL(J)_RTC/ CLK
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+3VALW +3VALW <6,9,10,12,19,39,40,43,45,46,49,52,58,60,62,63,64,65,67,72,83,84,85,96>

+3VALW_PRIM +3VALW_PRIM <19>

+3VS +3VS <5,9,10,11,12,14,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>

+RTCVCC +RTCVCC <14,19>

Reserved for HW control

+3VALW

RP1501 10K_0804_8P4R_5% SD300002P0T

1 AC_PRESENT
2 BATLOW#
3 PCIE_WAKE#
4

+3VALW *For vPRO LAN WAKE#*

R1501 1 2 10K_0402_5% EC_WAKE#_DSW

R1502 1 @ 2 10K_0402_5% PM_SLP_S5#

R1532 1 @ 2 10K_0201_5% PCH_SLP_WLAN#

R1533 1 @ 2 10K_0402_5% PCH_SLP_LAN#

+3VS

R1528 1 2 20K_0402_1% GPP_A11

R1505 1 @ 2 10K_0402_5% SYS_RESET#

+3VALW_PRIM

R1506 1 2 10K_0402_5%

R1507 1 2 10K_0402_5% EC_RSMRST#

R1508 1 @ 2 10K_0201_5% H_CPUPWRGD

R1525 1 2 10K_0402_5% PCH_PWROK

R1526 1 @ 2 10K_0402_5% PCH_SYSPWROK

R1527 1 @ 2 10K_0402_5% AC_PRESENT

+VCC_ST

R1513 1K_0402_5%

<40> VCCST_PG_EC R1509 1 2 0_0402_5% VCCST_PWRGD

+3VALW

R1514 4.7K_0402_5%

<40> PCH_PWROK R1515 1 2 0_0402_SM

<40,87> VGATE R1516 1 @ 2 0_0402_5%

<30> GPU_WAKE# R1530 1 @ 2 0_0402_5%

<52> PCH_LAN_WAKE# R1529 1 2 0_0402_5%

FOR VPRO LAN WAKE#

VCCST_PWRGD R1519 1 2 60.4_0402_1%

EC_RSMRST# R1520 1 2 0_0402_SM

R1521 1 2 0_0402_SM

<35> PCH_PLT_RST#
<40> EC_RSMRST#
H_CPUPWRGD
PCH_SYSPWROK
<40,66> PCH_SYSPWROK
SUSWARN#
SUSACK#
<62,63> PCIE_WAKE#
PCIE_WAKE#_DSW
LANPHYPC
<52> LANPHYPC

UC1K SKL_ULT

SYSTEM POWER MANAGEMENT

PCH_PLT_RST#	AN10
SYS_RESET#	B5
EC_RSMRST#	AY17
GPP_B13/PLTRST#	
SYS_RESET#	
RSMRST#	
H_CPUPWRGD	A68
PROCPWRGD	B65
VCCST_PWRGD	
PCH_SYSPWROK	B6
SYS_PWROK	
PCH_PWROK	BA20
DSW_PWROK	BB20
GPP_A13/SUSWARN#/SUSPWRDNACK	AR13
GPP_A15/SUSACK#	AP11
WAKE#	BB15
GPD2/LAN_WAKE#	AM15
GPD11/LANPHYPC	AW17
GPD7/RSVD	AT15

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PM_SLP_S3# T1501
PM_SLP_S4# T1502
PM_SLP_S5# T1503

GPP_B12/SLP_S0#	AT11 PM_SLP_S0# T1504
GPD4/SLP_S3#	AP15 PM_SLP_S3# → PM_SLP_S3# <40>
GPD5/SLP_S4#	BA16 PM_SLP_S4# → PM_SLP_S4# <40>
GPD10/SLP_S5#	AY16 PM_SLP_S5# → PM_SLP_S5# <40>
SLP_SUS#	AN15 PCH_SLP_SUS#
SLP_LAN#	AW15 PCH_SLP_LAN# TP4306 @
GPD9/SLP_WLAN#	BB17 PCH_SLP_WLAN# → PCH_SLP_LAN# <40> / PCH_SLP_WLAN# <40>
GPD6/SLP_A#	AN16 PM_SLP_A# → PM_SLP_A# <40>
GPD3/PWRBTN#	BA15 PBTN_OUT#
GPD1/ACPRESENT	AY15 AC_PRESENT → PBTN_OUT# <40> / AC_PRESENT <40>
GPD0/BATLOW#	AU13 BATLOW#
GPP_A11/PME#	AU11 GPP_A11
INTRUDER#	AP16 PCH_INTRUDER#
GPP_B11/EXT_PWR_GATE#	AM10 EXT_PWR_GATE# T1508
GPP_B2/VRALERT#	AM11 VRALERT# T1507

1. must be always pulled-up to VCCRTC.
2. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on product i on boar ds.

+RTCVCC

R1522 1 2 1M_0402_5%

C1501 @ 2 1 1000P_0201_25V7-K

R1523 1 2 0_0402_SM

U1501 @ TC7SG17FE_SON5

1 NC
2 IN_A
3 GND
5 VCC
4 OUT_Y

+3VALW

PCH_PLT_RST#

R1524 100K_0402_5%

C7214 0.1U_0402_16V7-K EMC_NS@

PLT_RST# PLT_RST# <35,40,51,52,56,58,62,63>

<13> -TAMPER_SW_DTCT

S3 SPVR310100_4P

R1531 1 2 0_0201_5%

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Title: KBL(K)_SYS PM

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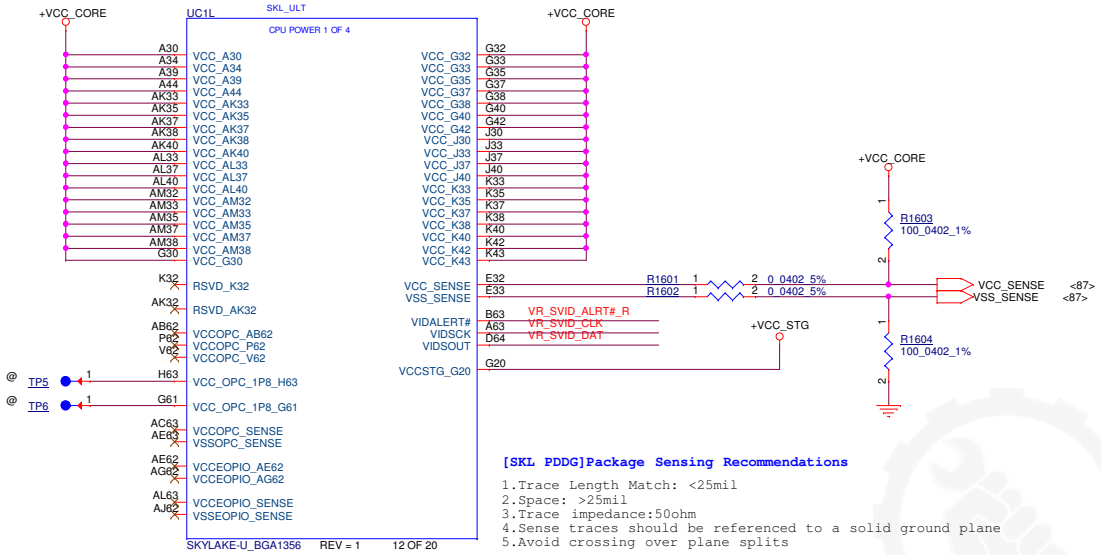
+VCC_CORE +VCC_CORE <17,27,88,91>

+VCC_ST +VCC_ST <8,15,18,21,71,87>

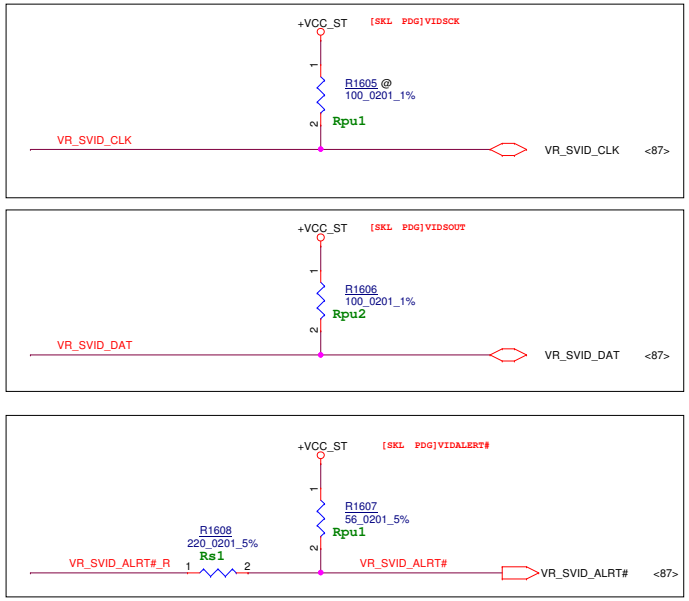


[SKL PDDG]Package Sensing Recommendations

1.Trace Length Match: <25mil
2.Space: >25mil
3.Trace impedance:50ohm
4.Sense traces should be referenced to a solid ground plane
5.Avoid crossing over plane splits

[SKL PDG]SVID

1.Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(L)_PW-VCCCORE

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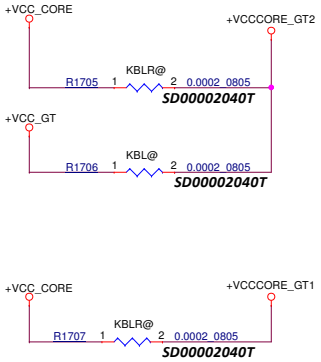
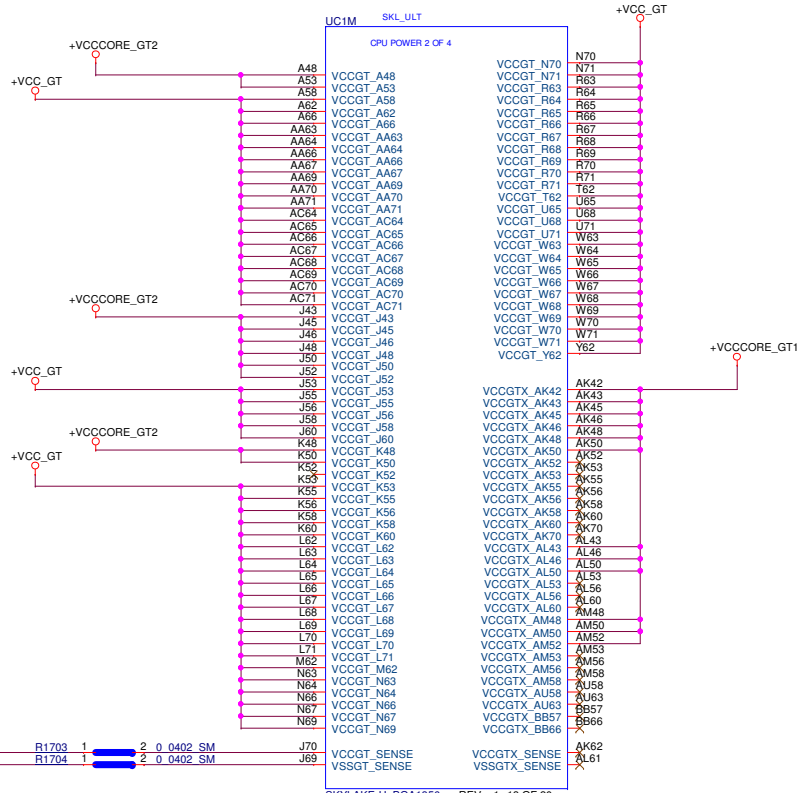
+VCC_GT +VCC_GT <27,89,91>

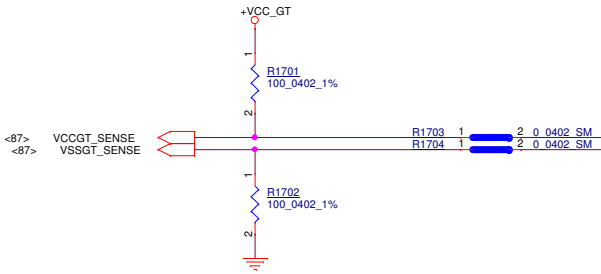
+VCC_CORE +VCC_CORE <16,27,88,91>

For KBL-R U42 and KBL U22 control



Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.





Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(M)_PW-VCCGT

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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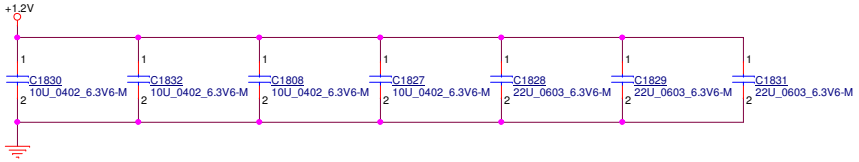
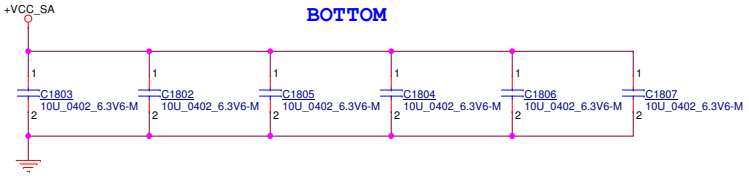
+1.2V +1.2V <6,7,23,24,25,26,86>
+VCC_IO +VCC_IO <5,11,21,71>
+VCC_SA +VCC_SA <90,91>

+VCC_STG +VCC_STG <8,16,71>
+VCC_ST +VCC_ST <8,15,16,21,71,87>

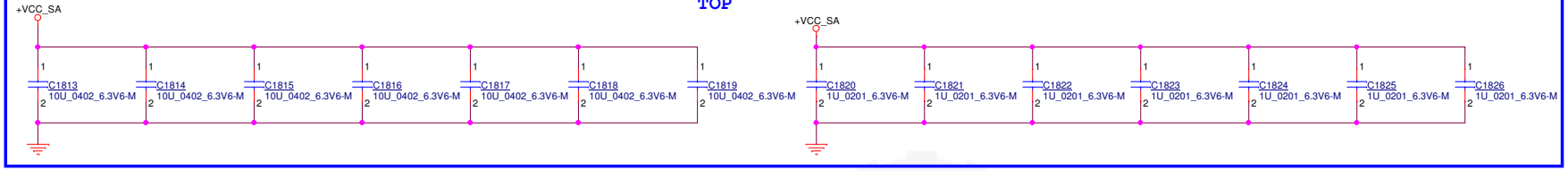
[KBL-R U4+2/KBL U2+2 Processo]VDDQ BOTTOM
[KBL-R U4+2/KBL U2+2 Processo]10uF x4, 22uF x3

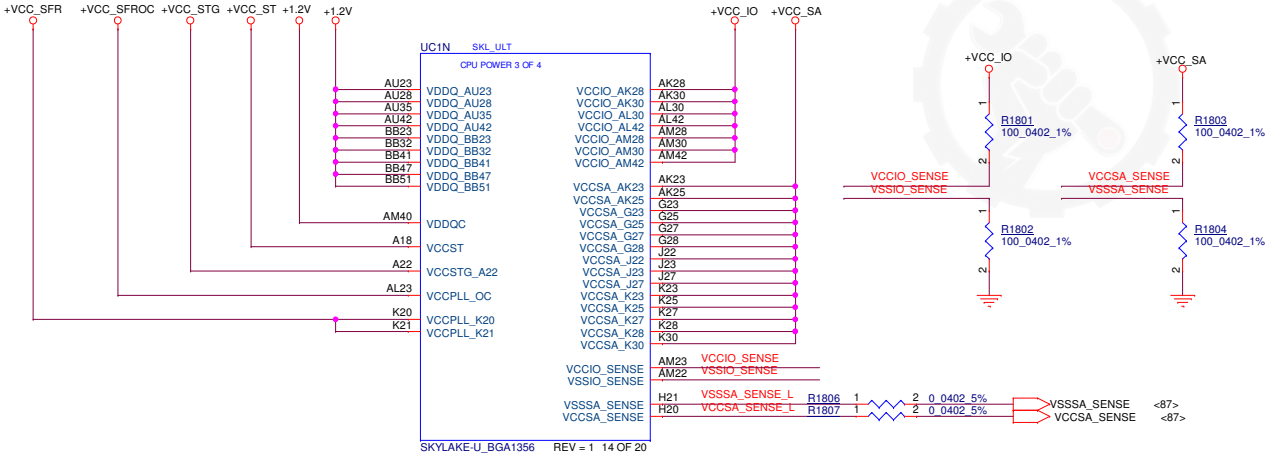


[KBL-R U4+2/KBL U2+2 ProcessoG]VCCSA
[KBL-R U4+2/KBL U2+2 Processo]10uF x6 BOTTOM



[KBL-R U4+2/KBL U2+2 ProcessoG]VCCSA
[KBL-R U4+2/KBL U2+2 Processo]10uF x7, 1uF x7 TOP





Power Rail	Description	Control
VCC	Processor IA Cores Power Rail	SVID
VccGT	Processor Graphics Power Rails	SVID
VccGTX	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VccSA	System Agent Power Rail	SVID
VccIO	IO Power Rail	Fixed
VccST	Sustain Power Rail	Fixed
VccPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed
VccOPC	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccOPC_1P8	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccEOPIO	Processor OPC power rail (available only in SKU' s with OPC)	Fixed

[SKL PDG]VCCSTG
[SKL PDG]1uF x1
+VCC_STG
C1833 1U_0402_10V6K

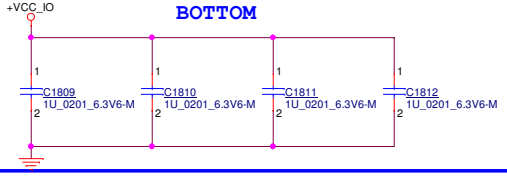
[SKL PDG]VCCST
[SKL PDG]1uF x1
Primary side cap
+VCC_ST
C1834 1U_0402_10V6K

[SKL PDG]VCCPLL
[SKL PDG]1uF x1
Primary side cap
+VCC_ST
+VCC_SFR
R1808 0_0402_SM
C1835 1U_0402_10V6K

[SKL PDG]VDDQC
[SKL PDG]10uF x1
+1.2V
C1836 10U_0402_6.3V6-M

[SKL PDG]VCCPLL
[SKL PDG]1uF x1
Primary side cap
+1.2V
R1809 0_0603_5%
+VCC_SFROC
C1801 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processo]VCCIO
[KBL-R U4+2/KBL U2+2 Processo]1uF x4 BOTTOM



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(N)_PW-VCCIO & VCCSA
Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2
Date: Friday, October 06, 2017 | Sheet 18 of 99

+1.2V +1.2V <6,7,18,23,24,25,26,86>

+1VALW_PCH +1VALW_PCH <21>
+3VALW_PCH +3VALW_PCH <8,9,10,11,12>
+VCC_ST +VCC_ST <8,15,16,18,21,71,87>
+3VALW_PRIM +3VALW_PRIM <15>
+RTCVCC +RTCVCC <14,15>
+3VALW +3VALW <6,9,10,12,15,39,40,43,45,46,49,52,58,60,62,63,64,65,67,72,83,84,85,96>

+1VALW +1VALW <14,39,71,96>
+VCC_STG +VCC_STG <8,16,18,71>
+VCC_HDA +VCC_HDA <11>

+1VALW_PCH +VCC_MPHYGT +1VALW_1P0 +1VALW_PCH +1VALW_SUS +1VALW_SUS

R1901 0_0603_SM
R1902 0_0603_SM

UC1O SKL_ULT
CPU POWER 4 OF 4

AB19 VCCPRIM_1P0_AB19
AB20 VCCPRIM_1P0_AB20
P18 VCCPRIM_1P0_P18
AF18 VCCPRIM_CORE_AF18
AF19 VCCPRIM_CORE_AF19
V20 VCCPRIM_CORE_V20
V21 VCCPRIM_CORE_V21
+DCPDSW AL1 DCPDSW_1P0
+1VALW_PCH K17 VCCMPHYAON_1P0_K17
L17 VCCMPHYAON_1P0_L1
+1VALW_1P0 N15 VCCMPHYGT_1P0_N15
N16 VCCMPHYGT_1P0_N16
P15 VCCMPHYGT_1P0_N17
P16 VCCMPHYGT_1P0_P15
VCCMPHYGT_1P0_P16
+VCC_AMPHYPLL K15 VCCAMPHYPLL_1P0_K15
L15 VCCAMPHYPLL_1P0_L15
+1VALW_PLL V15 VCCAPLL_1P0
+VCC_HDA AB17 VCCPRIM_1P0_AB17
+1VALW_SUS Y18 VCCPRIM_1P0_Y18
+VCC_DSW3P3 AD17 VCCDSW_3P3_AD17
AD18 VCCDSW_3P3_AD18
AJ17 VCCDSW_3P3_AJ17
AJ19 VCCHDA
+3V_SPI AJ16 VCCSPI
+VCC_SRAM AF20 VCCSRAM_1P0_AF20
AF21 VCCSRAM_1P0_AF21
T19 VCCSRAM_1P0_T19
T20 VCCSRAM_1P0_T20
+3VALW_PRIM AJ21 VCCPRIM_3P3_AJ21
+1VALW_SUS AK20 VCCPRIM_1P0_AK20
+VCC_PLLEBB N18 VCCAPLLEBB

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AK15 VCCPGPPA
AG15 VCCPGPPB
Y16 VCCPGPPC
Y15 VCCPGPPD
T16 VCCPGPPE
AF16 VCCPGPPF
AD15 VCCPGPPG
V19 VCCPRIM_3P3_V19
T1 VCCPRIM_1P0_T1
AA1 VCCATS_1P8
AK17 VCCRTCPRIM_3P3
AK19 VCCRTC_AK19
BB14 VCCRTC_BB14
BB10 +DCPRTC DCPRTC
A14 VCCCLK1
K19 +1VALW_CLK2 VCCCLK2
L21 VCCCLK3
N20 +1VALW_CLK4 VCCCLK4
L19 +1VALW_CLK5 VCCCLK5
A10 VCCCLK6
AN11 GPP_B0/CORE_VID0
AN13 GPP_B1/CORE_VID1

+1.8VALW_PCH +3VALW_PRIM +1VALW_SUS +1VALW_PCH +3VALW_PCH +3VALW_RTCPRIM +RTCVCC +1.8VALW_PCH

Near AG15 Near Y16 Near T16
+3VALW_PCH
C1903 1U_0402_10V6K
C1904 1U_0402_10V6K
C1905 1U_0402_10V6K

R8013 1 2 0_0603_5% 0603 Footprint
R8014 1 2 0_0603_5% 0603 Footprint
R8015 1 2 0_0603_5% 0603 Footprint

T58 T59

+1VALW +VCC_MPHYGT
R1903 0_0805_SM

C1901 0.1U_0402_10V6-K RF@
C1902 0.1U_0402_10V6-K RF@

LAYOUT note to CPU side

[SKL PDG]The CORE_VID[0:1] signal is used by external VRs to indicate the final settling voltage for VCCPRIM_CORE rail.

[SKL PDG]VccSRAM
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)
[SKL PDG]luF x1
SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.

+VCC_MPHYGT +VCC_SRAM
R1905 0_0805_SM
C1906 1U_0402_10V6K

[SKL PDG]VccAPLLEBB
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1

+VCC_MPHYGT +VCC_PLLEBB
R1906 0_0402_SM
CC52 1U_0402_10V6K

[SKL PDG]VccMPHYGT
[SKL PDG]luF x1
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)
VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)

+VCC_MPHYGT +1VALW_1P0
R1907 0_0805_SM
C1907 1U_0402_10V6K
C1908 47U_0805_6.3V6-M
close to N15

[SKL PDG]DcpDSW
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1
Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.

+DCPDSW
C1909 1U_0402_10V6K

[SKL PDG]DcpRTC
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)
[SKL PDG]0.1uF x1
RTC de-coupling capacitor only. This rail should NOT be driven.

+DCPRTC
C1910 0.1U_0402_10V6-K

[SKL PDG]VccMPHYAON
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1
Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic

+VCC_AMPHYPLL +1VALW_PCH
C1911 1U_0402_10V6K
C1912 1U_0402_10V6K

[SKL PDG]VccATS
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)
[SKL PDG]luF x1
Thermal Sensor Primary Well 1.8 V

+1.8VALW_PCH
C1913 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)
[SKL PDG]luF x1
Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.

+1VALW_PCH +1VALW_SUS
R1908 0_0402_5%
C1914 1U_0402_10V6K

[SKL PDG]VccRTCPRIM
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1,0.1uF x2
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+3VALW_PCH +3VALW_RTCPRIM
R1909 0_0402_5M
C1915 1U_0402_10V6K
C1916 0.1U_0402_10V6-K
C1917 0.1U_0402_10V6-K

[SKL PDG]VccRTC
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1
RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+RTCVCC
C1918 1U_0402_10V6K

[SKL PDG]VccDSW
Deep Sx Well for GPD GPIOs and USB2

+3VL +VCC_DSW3P3
R1910 0_0402_5%
R1911 0_0402_SM

3.3A
+1VALW +1VALW_SUS
J12 @
JUMP_43X118
Reserve for Sense Resistor
R1912 0_0402_SM
R1913 0_0805_SM
R1914 0_0805_5%

[SKL PDG]VccHDA
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)
[SKL PDG]luF x1
HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.

+3VALW_PCH +1.8VALW_PCH +VCC_HDA
R1915 0_0402_5%
R1916 0_0402_SM
C1919 0.1U_0402_10V6-K

[SKL PDG]VccPRIM_Core
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)
[SKL PDG]luF x1
Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.

+1VALW_PCH +1VALW_SUS
R1917 0_0805_5%
C1920 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)
[SKL PDG]luF x1
Primary Well 3.3 V

+3VALW_PCH +3VALW_PRIM
R1918 0_0402_SM
C1921 1U_0402_10V6K

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(O)_PW-OTHERS

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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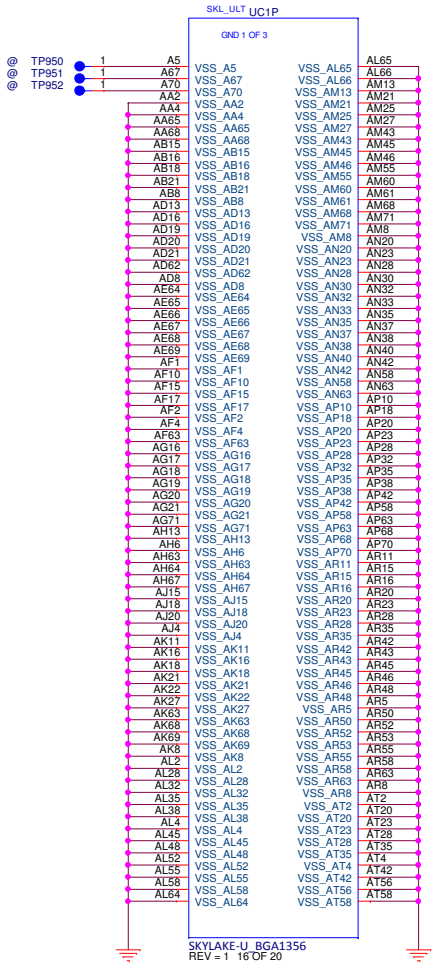

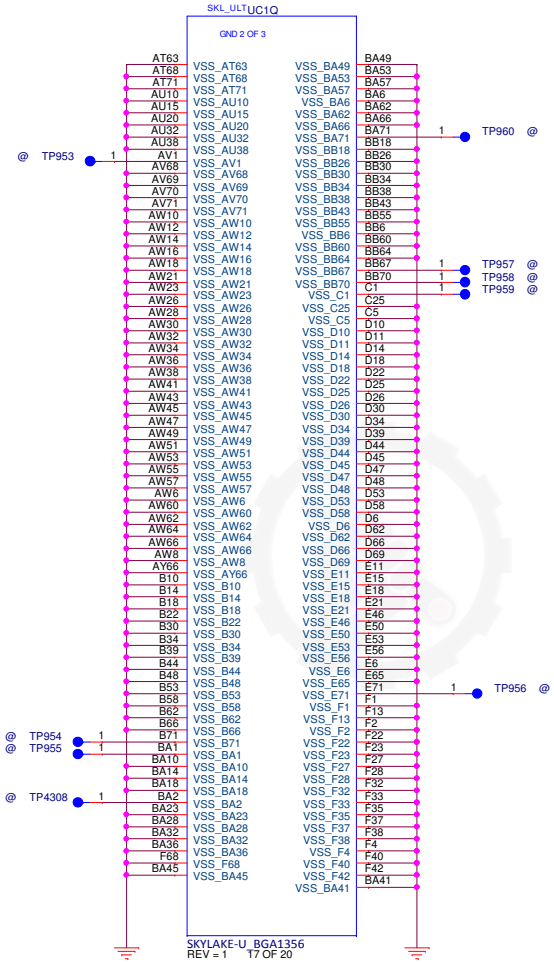

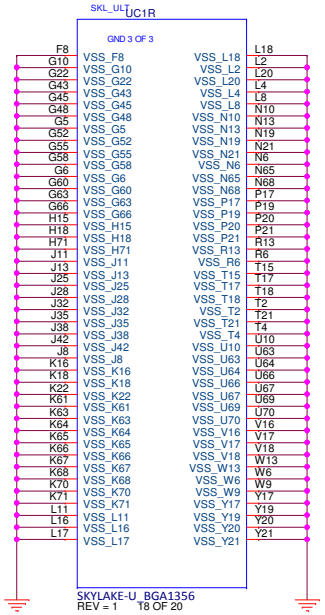

Kaby Lake R Processor Corner NCTF Motherboard Test Point Example (Sheet 1 of 2)

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	

Kaby Lake R Processor Corner NCTF Motherboard Test Point Example (Sheet 2 of 2)

Pin Number	Pin Name	Description	Corner
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	KBL(P/Q/R)_VSS	
Size: Custom	Document Number: EL480 / EL580 NM-B461	Rev: 0.2
Date: Friday, October 06, 2017	Sheet 20 of 99	

+VCC_ST +VCC_ST <8,15,16,18,71,87>

+1VALW_PCH +1VALW_PCH <19>

+VCC_IO +VCC_IO <5,11,18,71>

+VCC_IO

CFG0
[SKL EDS]

R2101 1K_0402_5% @

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG0

R2102 1K_0402_1% @

+VCC_IO

CFG4
*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

R2103 1K_0402_5% @

CFG4

R2104 1K_0402_1%

[SKL CRB]

[SKL PDG]Route HOOK[6] to Skylake ITP_PMODE. Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH_V1.0A Rail.

+1VALW_PCH

R2105 49.9_0402_1% CFG_RCOMP

R2106 1.5K_0402_5% ITP_PMODE

UC1S

SKL_ULT

RESERVED SIGNALS-1

CFG0 CFG4

E68 CFG[0]
B67 CFG[1]
D65 CFG[2]
D67 CFG[3]
E70 CFG[4]
C68 CFG[5]
D68 CFG[6]
C67 CFG[7]
F71 CFG[8]
G69 CFG[9]
F70 CFG[10]
G68 CFG[11]
H70 CFG[12]
G71 CFG[13]
H69 CFG[14]
G70 CFG[15]
E63 CFG[16]
F63 CFG[17]
E66 CFG[18]
F66 CFG[19]
E60 CFG_RCOMP
E8 ITP_PMODE

TP24 TP26 AY2 AY1 RSVD_AY2 RSVD_AY1
TP74 TP30 D1 D3 RSVD_D1 RSVD_D3
K46 K45 RSVD_K46 RSVD_K45
TP88 TP87 AL25 AL27 RSVD_AL25 RSVD_AL27
TP90 TP89 C71 B70 RSVD_C71 RSVD_B70
TP32 F60 RSVD_F60
A52 RSVD_A52
TP92 TP93 BA70 BA68 RSVD_TP_BA70 RSVD_TP_BA68
TP94 TP95 J71 J68 RSVD_J71 RSVD_J68
F65 G65 VSS_F65 VSS_G65
TP96 TP97 F61 E61 RSVD_F61 RSVD_E61

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RSVD_TP_BB68 BB68 TP37
RSVD_TP_BB69 BB69 TP39
RSVD_TP_AK13 AK13 TP43
RSVD_TP_AK12 AK12 TP45
RSVD_BB2 BB2 TP49
RSVD_BA3 BA3 TP51
TP5 AU5 TP59
TP6 AT5 TP60
RSVD_D5 D5 TP22
RSVD_D4 D4 TP23
RSVD_B2 B2 TP25
RSVD_C2 C2 TP27
RSVD_B3 B3 TP64
RSVD_A3 A3 TP66
RSVD_AW1 AW1 TP29
RSVD_E1 E1 TP31
RSVD_E2 E2 TP33
RSVD_BA4 BA4 TP34
RSVD_BB4 BB4 TP35
RSVD_A4 A4 TP67
RSVD_C4 C4 TP68
TP4 BB5 TP54
RSVD_A69 A69 TP927
RSVD_B69 B69 TP928
RSVD_AY3 AY3 R2107 0_0402_SM
RSVD_D71 D71 TP929
RSVD_C70 C70 TP930
RSVD_C54 C54 TP931
RSVD_D54 D54
TP1 AY4 TP933
TP2 BB3 TP934
VSS_AY71 AY71 R2108 0_0402_SM
ZVM# AR56 TP935
RSVD_TP_AW71 AW71 TP936
RSVD_TP_AW70 AW70 TP937
MSM# AP56 TP938
PROC_SELECT# C64

+VCC_ST

R2109 100K_0201_1%

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted **1 : No Stall** **0 : Stall**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM# state	VCCOPC
0V	0V
1V	1V

[SKL EDS]Minimum Speed Mode: VCCEOPIO can be connected to OPC VR in this case VCCEOPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal .
In order to achieve better power/performance it is recommended to use a separate VR for VCCEOPIO in this case VCCEOPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEOPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EOPIO interface as shown below:

ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

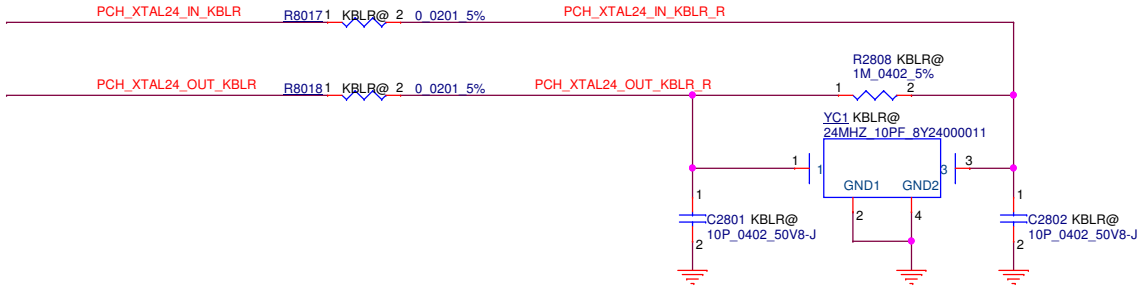
Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

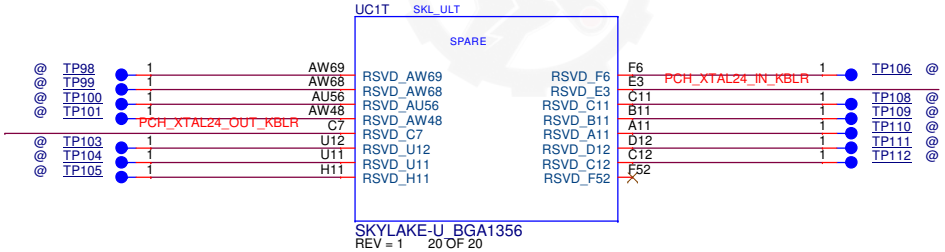
Title: KBL(S)_CFG/ RSVD

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 21 of 99

Need close CPU For KBL-R U42 and KBL U22 control





Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: KBL(T)_RSVD

Size	Document Number	Rev
B	EL480 / EL580 NM-B461	0.2

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+3VS +3VS <5,9,10,11,12,14,15,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>
+2.5V +2.5V <6,24,25,26,95>
+1.2V +1.2V <6,7,18,24,25,26,86>
+0.6VS +0.6VS <24,25,26,86>

<6,7> M_A_DQ[63:0]
<6,7> -M_A_DQS[7:0]
<6,7> M_A_DQS[7:0]
<6> M_A_A[16:0]

JDIMM1A

M_A_DQ1	3	VSS_1	VSS_2	4	M_A_DQ4		
M_A_DQ0	5	DQ5	DQ4	6	M_A_DQ5		
-M_A_DQS0	7	VSS_3	VSS_4	8			
M_A_DQS0	9	DQ1	DQ0	10			
M_A_DQ6	11	VSS_5	VSS_6	12			
M_A_DQ2	13	DQS0_C	DM0_n/DBI0_n	14			
M_A_DQ24	15	DQS0_t	VSS_7	16	M_A_DQ3		
M_A_DQ25	17	VSS_8	DQ6	18	M_A_DQ7		
	19	DQ7	VSS_9	20			
M_A_DQ26	21	VSS_10	DQ2	22	M_A_DQ29		
M_A_DQ31	23	DQ3	VSS_11	24	M_A_DQ28		
M_A_DQ9	25	VSS_12	DQ12	26			
M_A_DQ13	27	DQ13	VSS_13	28	-M_A_DQS3		
-M_A_DQS1	29	VSS_14	DQ8	30	M_A_DQS3		
M_A_DQS1	31	DQ9	VSS_15	32	M_A_DQ27		
M_A_DQ10	33	VSS_16	DQS1_c	34	M_A_DQ30		
M_A_DQ11	35	DM1_n/DBI_n	DQS1_t	36	M_A_DQ8		
M_A_DQ21	37	VSS_17	VSS_18	38	M_A_DQ12		
M_A_DQ20	39	DQ15	DQ14	40			
	41	VSS_19	VSS_20	42	M_A_DQ15		
M_A_DQ18	43	DQ10	DQ11	44	M_A_DQ14		
M_A_DQ22	45	VSS_21	DQ20	46	M_A_DQ17		
	47	DQ21	VSS_22	48	M_A_DQ16		
	49	VSS_23	DQ16	52	-M_A_DQS2		
	51	DQ17	VSS_24	50	M_A_DQS2		
	53	VSS_25	VSS_26	54	M_A_DQ19		
	55	DQS2_c	DM2_n/DBI2_n	56	M_A_DQ23		
	57	DQS2_t	VSS_27	58			
	59	VSS_28	DQ22	60			
	61	DQ23	VSS_29	62			
	63	VSS_30	DQ18	64			
	65	DQ19	VSS_31	66			
	67	VSS_32	DQ28	68			
	69	DQ29	VSS_33	70			
	71	VSS_34	DQ24	72			
	73	DQ25	VSS_35	74			
	75	VSS_36	DQS3_c	76			
	77	DM3_n/DBI3_n	DQS3_t	78			
	79	VSS_37	VSS_38	80			
	81	DQ30	DQ31	82			
	83	VSS_39	VSS_40	84			
	85	DQ26	DQ27	86			
	87	VSS_41	VSS_42	88			
	89	CB5/NC	CB4/NC	90			
	91	VSS_43	VSS_44	92			
	93	CB1/NC	CB0/NC	94			
	95	VSS_45	VSS_46	96			
	97	DQS8_c	DM8_n/DBI_n/NC	98			
	99	DQS8_t	VSS_47	100			
	101	VSS_48	CB6/NC	102			
	103	CB2/NC	VSS_49	104			
	105	VSS_50	CB7/NC	106			
	107	CB3/NC	VSS_51	108			
	109	VSS_52	RESET_n	110	-DRAMRST		
<6> M_A_CKE0	111	CKE0	CKE1	112	M_A_CKE1		
	113	VDD_1	VDD_2	114	-M_A_ACT		
<6> M_A_BG1	115	BG1	ACT_n	116	M_A_ALERT		
<6> M_A_BG0	117	BG0	ALERT_n	118			
M_A_A12	119	VDD_3	VDD_4	120	M_A_A11		
M_A_A9	121	A12	A11	122	M_A_A7		
	123	A9	A7	124			
M_A_A8	125	VDD_5	VDD_6	126	M_A_A5		
M_A_A6	127	A8	A5	128	M_A_A4		
	129	A6	A4	130			
		VDD_7	VDD_8				

ARGOS_D4AR0-26005-1P40
ME@

<6> M_A_CKE0 <7,25> -DRAMRST
<6> M_A_BG1 <6> M_A_ACT
<6> M_A_BG0 <6> M_A_ALERT

C2307 0.1U_0402_16V7-K EMC_NS@

JDIMM1B

M_A_A3	131	A3	A2	132	EVENT_n_I	M_A_A2	
M_A_A1	133	A1	EVENT_n/NF	134			
<6> M_A_DDRCLK0_1066M	135	VDD_9	VDD_10	136	M_A_DDRCLK1_1066M		
<6> -M_A_DDRCLK0_1066M	137	CK0_t	CK1_t/NF	138	-M_A_DDRCLK1_1066M	<6> M_A_DDRCLK1_1066M	
M_A_DDRCLK0_1066M	139	CK0_c	CK1_c/NF	140	M_A_DDRCLK1_1066M	<6> -M_A_DDRCLK1_1066M	
-M_A_DDRCLK0_1066M	141	VDD_11	VDD_12	142			
M_A_PARITY	143	Parity	A0	144	M_A_A0		
<6> M_A_PARITY	145	BA1	A10/AP	146	M_A_A10		
<6> M_A_BS1	147	VDD_13	VDD_14	148	M_A_BS0		
-M_A_CS0	149	CS0_n	BA0	150	M_A_A16	M_A_BS0	<6>
<6> -M_A_CS0	151	A14/WE_n	A16/RAS_n	152			
M_A_A14	153	VDD_15	VDD_16	154	M_A_A15		
M_A_ODT0	155	ODT0	A15/CAS_n	156	M_A_A13		
<6> M_A_ODT0	157	CS1_n	A13	158			
M_A_CS1	159	VDD_17	VDD_18	160			
<6> -M_A_CS1	161	ODT1	C0/CS2_n/NC	162			
M_A_ODT1	163	VDD_19	VREFCA	164	M_VREF_CA_DIMMA		
<6> M_A_ODT1	165	C1/CS3_n/NC	SA2	166	SA2_CHA_P		
	167	VSS_53	VSS_54	168			
M_A_DQ48	169	DQ37	DQ36	170	M_A_DQ51		
M_A_DQ49	171	VSS_55	VSS_56	172	M_A_DQ52		
-M_A_DQS6	173	DQ33	DQ32	174			
M_A_DQS6	175	VSS_57	VSS_58	176			
M_A_DQ54	177	DQS4_c	DM4_n/DBI4_n	178			
M_A_DQ55	179	DQS4_t	VSS_59	180	M_A_DQ50		
	181	VSS_60	DQ39	182	M_A_DQ53		
M_A_DQ32	183	DQ38	VSS_61	184			
M_A_DQ36	185	VSS_62	DQ35	186	M_A_DQ33		
	187	DQ34	VSS_63	188	M_A_DQ37		
	189	VSS_64	DQ45	190			
	191	DQ44	VSS_65	192	-M_A_DQS4		
	193	VSS_66	DQ41	194	M_A_DQS4		
	195	DQ40	VSS_67	196	M_A_DQ39		
	197	VSS_68	DQS5_c	198			
	199	DM5_n/DBI5_n	DQS5_t	200	M_A_DQ34		
M_A_DQ35	201	VSS_69	VSS_70	202			
M_A_DQ38	203	DQ46	DQ47	204	M_A_DQ44		
M_A_DQ40	205	VSS_71	VSS_72	206			
M_A_DQ43	207	DQ42	DQ43	208	M_A_DQ45		
-M_A_DQS5	209	VSS_73	VSS_74	210			
M_A_DQS5	211	DQ52	DQ53	212			
M_A_DQ47	213	VSS_75	VSS_76	214	M_A_DQ41		
M_A_DQ42	215	DQ49	DQ48	216	M_A_DQ46		
M_A_DQ56	217	VSS_77	VSS_78	218			
M_A_DQ57	219	DQS6_c	DM6_n/DBI6_n	220	M_A_DQ61		
	221	DQS6_t	VSS_79	222			
	223	VSS_80	DQ54	224	M_A_DQ60		
M_A_DQ63	225	DQS5	VSS_81	226			
M_A_DQ62	227	VSS_82	DQ50	228	-M_A_DQS7		
	229	DQ51	VSS_83	230	M_A_DQS7		
	231	VSS_84	DQ60	232			
	233	DQ61	VSS_85	234	M_A_DQ58		
	235	VSS_86	DQ57	236			
	237	DQ56	VSS_87	238	M_A_DQ59		
	239	VSS_88	DQS7_c	240			
	241	DM7_n/DBI7_n	DQS7_t	242	PM_SMB_DAT		
	243	VSS_89	VSS_90	244	SA0_CHA_P	PM_SMB_DAT	<9,25,65>
	245	DQ62	DQ63	246			
	247	VSS_91	VSS_92	248	SA1_CHA_P		
	249	DQ58	DQ59	250			
	251	VSS_93	VSS_94	252			
	253	SCL	SDA	254			
	255	VDDSPD	SA0	256			
	257	VPP_1	VTT	258			
	259	VPP_2	SA1	260			
	261	GND_1	GND_2	262			

ARGOS_D4AR0-26005-1P40
ME@

RF

R2301 240_0402_1%
C2301 2.2U_0402_6.3V6-M @
C2302 0.1U_0402_10V7-K

R2302 0_0402_SM
<9,25,65> PM_SMB_CLK

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.
Place decoupling cap close to DIMM
C2303 0.1U_0402_10V7-K
C2304 2.2U_0402_6.3V6-M

R2309 1K_0402_1%
R2310 2_0402_1%
<6> M_A_VREF_CA_CPU
M_VREF_CA_DIMMA
C2305 0.022U_0402_25V7-K
R2311 24.9_0402_1%
R2312 1K_0402_1%
C2306 0.1U_0402_16V7-K @

R2303 10K_0402_5% @ SA0_CHA_P
R2304 0_0402_SM
R2305 10K_0402_5% @ SA1_CHA_P
R2306 0_0402_SM
R2307 10K_0402_5% @ SA2_CHA_P
R2308 0_0402_SM

SPD Address = 0H

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: DDR4 CH-A PRIMARY

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2
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+2.5V +2.5V <6,23,25,26,95>

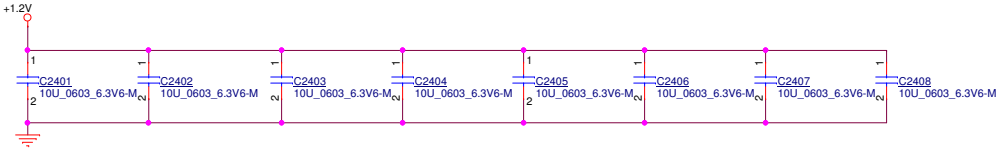
+1.2V +1.2V <6,7,18,23,25,26,86>

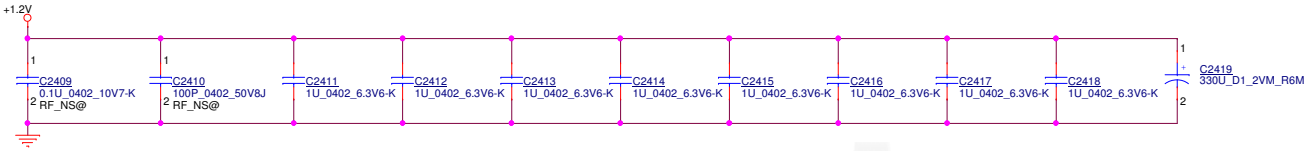
+0.6VS +0.6VS <23,25,26,86>

[KBL PDG]VDDQ

[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

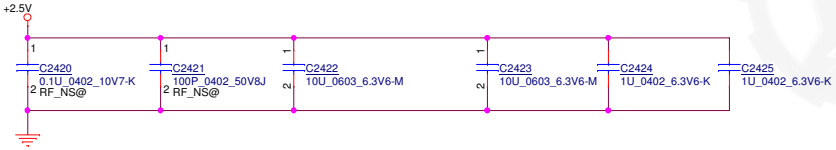




[KBL PDG]VPP

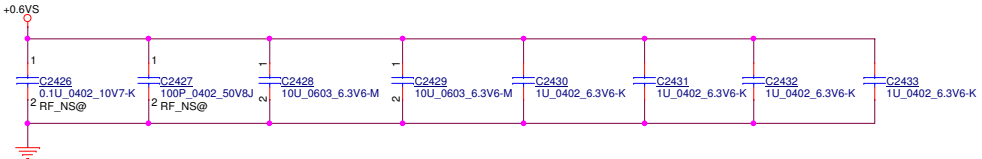
[KBL PDG] EE 10uF x2, 1uF x2.

Place decoupling cap on DRAM side.



[KBL PDG]VTT

[KBL PDG] EE 10uF x2, 1uF x4.



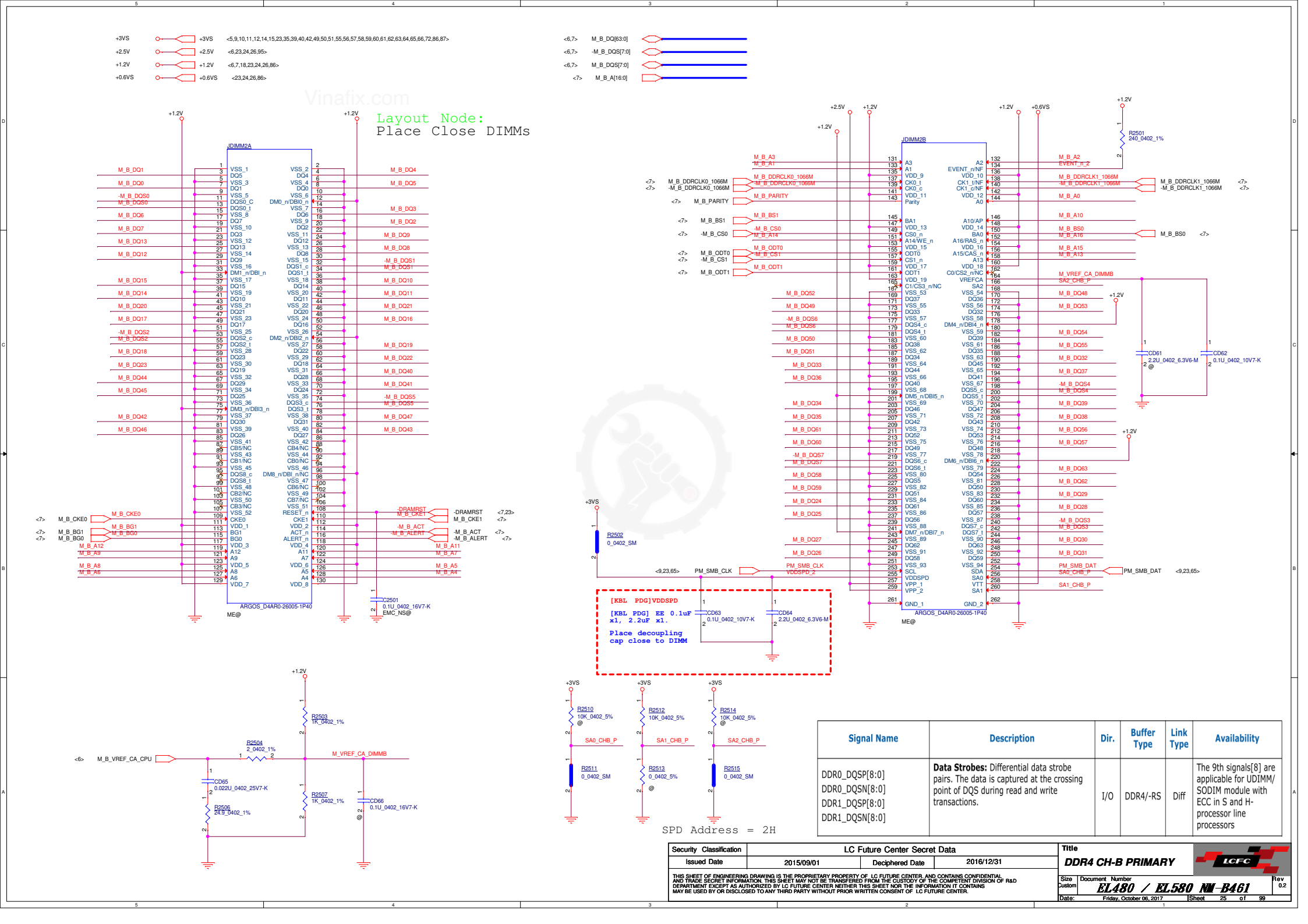
Place decoupling on the VTT plane close to SODIMM

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-A PRIMARY_P

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017 Sheet 24 of 99


+3VS
+2.5V
+1.2V
+0.6VS
<5,9,10,11,12,14,15,23,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,72,86,87>
<6,23,24,26,95>
<6,7,18,23,24,26,86>
<23,24,26,86>
<6,7> M_B_DQ[63:0]
<6,7> -M_B_DQS[7:0]
<6,7> M_B_DQS[7:0]
<7> M_B_A[16:0]
Vinafix.com
Layout Node:
Place Close DIMMs
JDIMM2A
ARGOS_D4AR0-26005-1P40
ME@
JDIMM2B
ARGOS_D4AR0-26005-1P40
ME@
[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.
Place decoupling cap close to DIMM
SPD Address = 2H
Signal Name
Description
Dir.
Buffer Type
Link Type
Availability
DDR0_DQSP[8:0]
DDR0_DQSN[8:0]
DDR1_DQSP[8:0]
DDR1_DQSN[8:0]
Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
I/O
DDR4/-RS
Diff
The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors
Security Classification
LC Future Center Secret Data
Issued Date
2015/09/01
Deciphered Date
2016/12/31
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Title
DDR4 CH-B PRIMARY
Size Custom
Document Number
EL480 / EL580 NM-B461
Rev 0.2
Date: Friday, October 06, 2017
Sheet 25 of 99

+2.5V +2.5V <6,23,24,25,95>

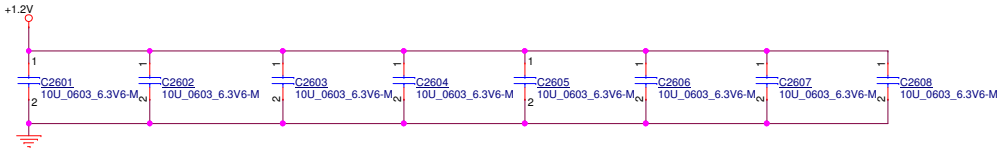
+1.2V +1.2V <6,7,18,23,24,25,86>

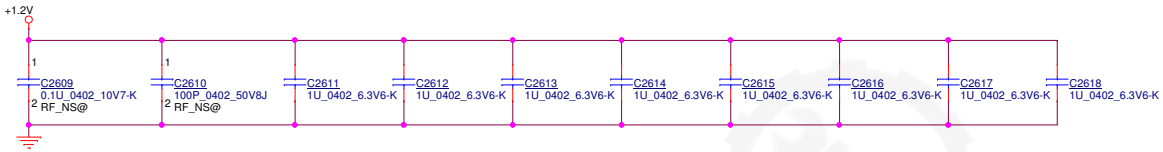
+0.6VS +0.6VS <23,24,25,86>

[KBL PDG]VDDQ

[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins. 330uF placeholder

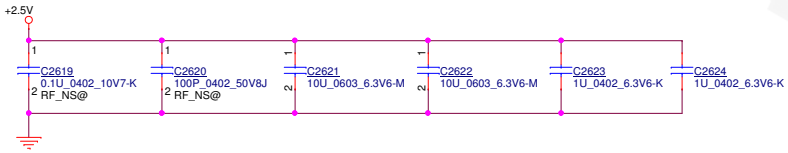




[KBL PDG]VPP

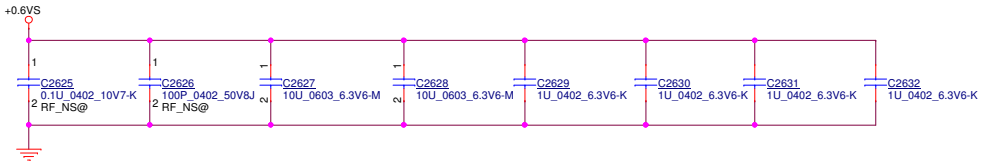
[KBL PDG] EE 10uF x2, 1uF x2.

Place decoupling cap on DRAM side.



[KBL PDG]VTT

[KBL PDG] EE 10uF x2, 1uF x4.



Place decoupling on the VTT plane close to SODIMM

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DDR4 CH-B PRIMARY_P[illegible]

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

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+VCC_CORE +VCC_CORE <16,17,88,91> +VCC_GT +VCC_GT <17,89,91> +VCCCORE_GT2 +VCCCORE_GT2 <17>

[KBL-R U4+2/KBL U2+2 Processor]VCC

[KBL-R U4+2/KBL U2+2 Processor]22uF x9,10uF x8,1uF,47uF x8

+VCC_CORE

BOTTOM

C2719 22U_0603_6.3V6-M C2701 22U_0603_6.3V6-M C2702 22U_0603_6.3V6-M C2703 22U_0603_6.3V6-M C2704 22U_0603_6.3V6-M C2705 22U_0603_6.3V6-M C2706 22U_0603_6.3V6-M C2707 22U_0603_6.3V6-M C2708 22U_0603_6.3V6-M

+VCC_CORE

C2781 10U_0402_6.3V6-M C2775 10U_0402_6.3V6-M C2776 10U_0402_6.3V6-M C2777 10U_0402_6.3V6-M C2778 10U_0402_6.3V6-M C2779 10U_0402_6.3V6-M C2780 10U_0402_6.3V6-M C2782 10U_0402_6.3V6-M

+VCC_CORE

C2783 47U_0603_6.3V6-M C2784 47U_0603_6.3V6-M C2785 47U_0603_6.3V6-M C2786 47U_0603_6.3V6-M C2787 47U_0603_6.3V6-M C2788 47U_0603_6.3V6-M C2789 47U_0603_6.3V6-M C2790 47U_0603_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]10uF x7,1uF x31

TOP

+VCC_CORE

C2720 10U_0402_6.3V6-M C2721 10U_0402_6.3V6-M C2722 10U_0402_6.3V6-M C2723 10U_0402_6.3V6-M C2724 10U_0402_6.3V6-M C2725 10U_0402_6.3V6-M C2726 10U_0402_6.3V6-M

+VCC_CORE

C2747 1U_0201_6.3V6-M

+VCC_CORE

C2709 1U_0201_6.3V6-M C2710 1U_0201_6.3V6-M C2711 1U_0201_6.3V6-M C2712 1U_0201_6.3V6-M C2713 1U_0201_6.3V6-M C2714 1U_0201_6.3V6-M C2715 1U_0201_6.3V6-M C2716 1U_0201_6.3V6-M C2717 1U_0201_6.3V6-M C2718 1U_0201_6.3V6-M

+VCC_CORE

C2727 1U_0201_6.3V6-M C2728 1U_0201_6.3V6-M C2729 1U_0201_6.3V6-M C2730 1U_0201_6.3V6-M C2731 1U_0201_6.3V6-M C2732 1U_0201_6.3V6-M C2733 1U_0201_6.3V6-M C2734 1U_0201_6.3V6-M C2735 1U_0201_6.3V6-M C2736 1U_0201_6.3V6-M

+VCC_CORE

C2737 1U_0201_6.3V6-M C2738 1U_0201_6.3V6-M C2739 1U_0201_6.3V6-M C2740 1U_0201_6.3V6-M C2741 1U_0201_6.3V6-M C2742 1U_0201_6.3V6-M C2743 1U_0201_6.3V6-M C2744 1U_0201_6.3V6-M C2745 1U_0201_6.3V6-M C2746 1U_0201_6.3V6-M

+VCCCORE_GT1

[KBL-R U4+2/KBL U2+2 Processor]1uF X5 BOTTOM

C27113 1U_0201_6.3V6-M C27112 1U_0201_6.3V6-M C27115 1U_0201_6.3V6-M C27114 1U_0201_6.3V6-M C27116 1U_0201_6.3V6-M C27117 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]VCCGT

[KBL-R U4+2/KBL U2+2 Processor]10uF x10,1uF x12

TOP

+VCC_GT

C2752 10U_0402_6.3V6-M C2753 10U_0402_6.3V6-M C2754 10U_0402_6.3V6-M C2755 10U_0402_6.3V6-M C2756 10U_0402_6.3V6-M C2792 10U_0402_6.3V6-M

+VCC_GT

C2757 10U_0402_6.3V6-M C2758 10U_0402_6.3V6-M C2759 10U_0402_6.3V6-M C2760 10U_0402_6.3V6-M C2761 10U_0402_6.3V6-M C2791 10U_0402_6.3V6-M

+VCC_GT

C2762 1U_0201_6.3V6-M C2763 1U_0201_6.3V6-M C2764 1U_0201_6.3V6-M C2765 1U_0201_6.3V6-M C2766 1U_0201_6.3V6-M C2767 1U_0201_6.3V6-M C2793 1U_0201_6.3V6-M

+VCC_GT

C2768 1U_0201_6.3V6-M C2769 1U_0201_6.3V6-M C2770 1U_0201_6.3V6-M C2771 1U_0201_6.3V6-M C2773 1U_0201_6.3V6-M C2774 1U_0201_6.3V6-M C2794 1U_0201_6.3V6-M

[KBL-R U4+2/KBL U2+2 Processor]10uF x7,47uF x3

BOTTOM

+VCC_GT

C27101 22U_0603_6.3V6-M C27100 22U_0603_6.3V6-M C2799 22U_0603_6.3V6-M C2795 22U_0603_6.3V6-M C2798 22U_0603_6.3V6-M C2796 22U_0603_6.3V6-M C2797 22U_0603_6.3V6-M

+VCC_GT

C27102 47U_0603_6.3V6-M C27103 47U_0603_6.3V6-M C27104 47U_0603_6.3V6-M

+VCCCORE_GT2

[KBL-R U4+2/KBL U2+2 Processor]1uF X5

BOTTOM

C27107 1U_0201_6.3V6-M C27105 1U_0201_6.3V6-M C27108 1U_0201_6.3V6-M C27106 1U_0201_6.3V6-M C27109 1U_0201_6.3V6-M

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: VCC_CORE & VCC_GT CAP

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 27 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **BLANK**

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

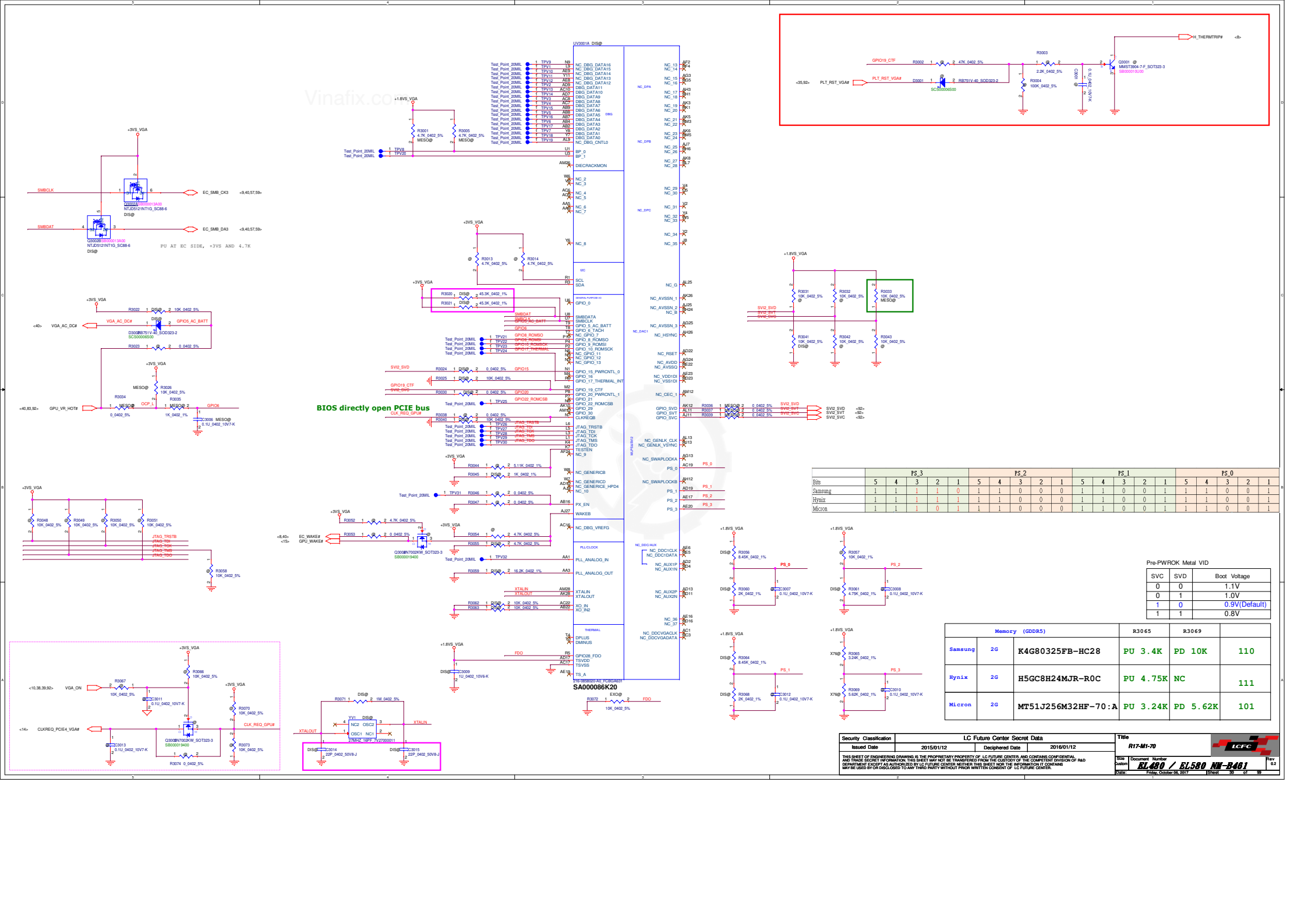
Date: Friday, October 06, 2017 Sheet 28 of 99

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: BLANK

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017 Sheet 29 of 99


BIOS directly open PCIE bus
SA000086K20
PU AT EC SIDE, +3VS AND 4.7K
Pre-PWROK Metal VID
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Memory (GDDR5) R3065 R3069
Samsung 2G K4G80325FB-HC28 PU 3.4K PD 10K 110
Hynix 2G H5GC8H24MJR-R0C PU 4.75K NC 111
Micron 2G MT51J256M32HF-70:A PU 3.24K PD 5.62K 101
PS_3 PS_2 PS_1 PS_0
Bits 5 4 3 2 1 5 4 3 2 1 5 4 3 2 1 5 4 3 2 1
Samsung 1 1 1 1 0 1 1 0 0 0 1 1 0 0 1 1 1 0 0 1
Hynix 1 1 1 1 1 1 1 0 0 0 1 1 0 0 1 1 1 0 0 1
Micron 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 1 1 0 0 1
Security Classification LC Future Center Secret Data
Issued Date 2015/01/12 Deciphered Date 2016/01/12
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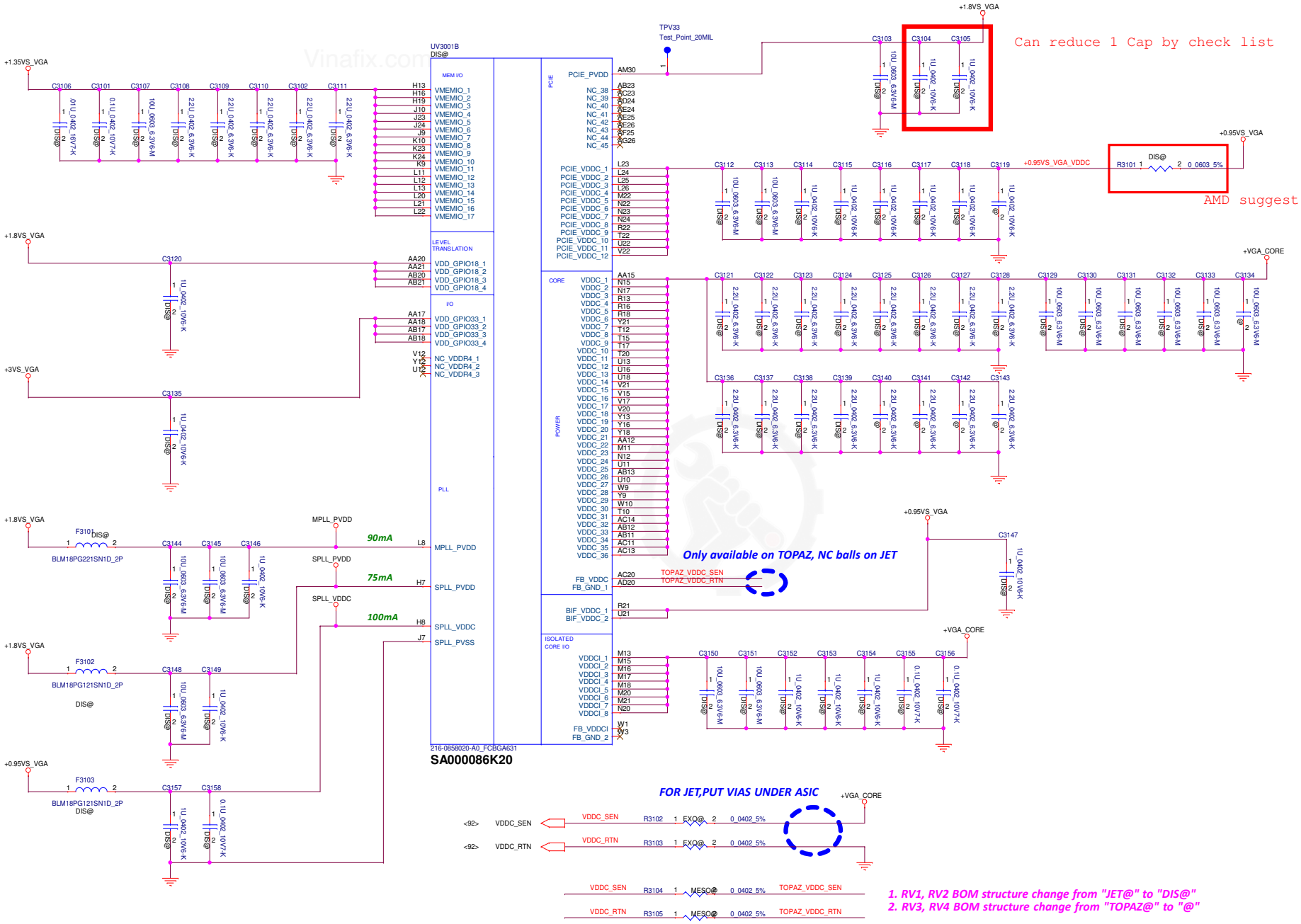
Title R17-M1-70
Size Custom
Document Number EL480 / EL580 MB-B461
Rev 0.2
Date: Friday, October 06, 2017 Sheet 36 of 69



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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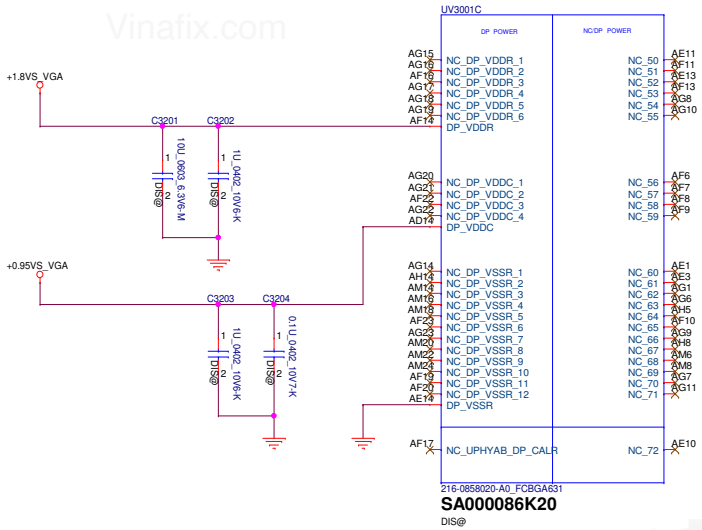
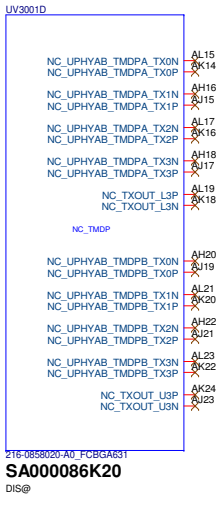
Title	R17M-M1-70_POWER		
Size: Custom	Document Number: EL480 / EL580 NM-B461		Rev: 0.2
Date: Friday, October 06, 2017	Sheet 31 of 99		





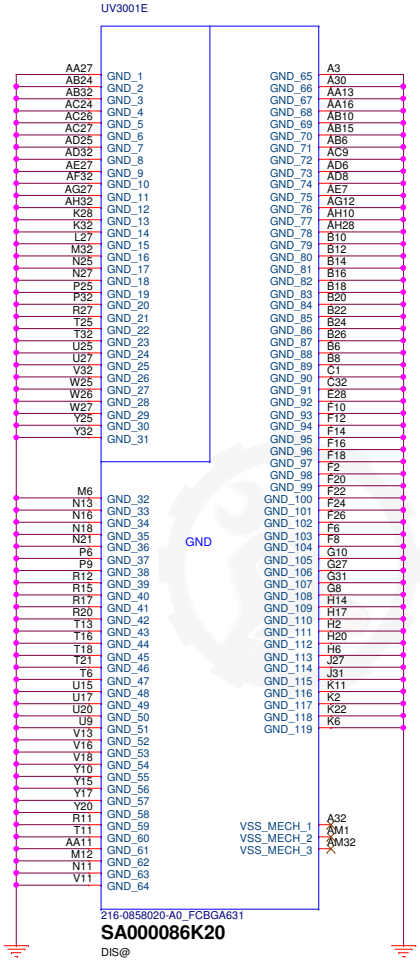
ASIC Ball	Topaz	Jet
U10,T10 AB13,W9 AB11,AB12 AC11,AC13 AC14,Y9,W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13,H16,H19,J10 J23,J24,J9,K10 K23,K24,K9,L11 L12,L13,L20,L21 L22	VMEMIO	VDDR1
AA17,AA18 AB17,AB18	VDD_GPIO33	VDDR3
AA20,AA21 AB20,AB21	VDD_GPIO18	VDD_CT

Title: R17M-M1-70_VDDR/VDDC

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 32 of 99

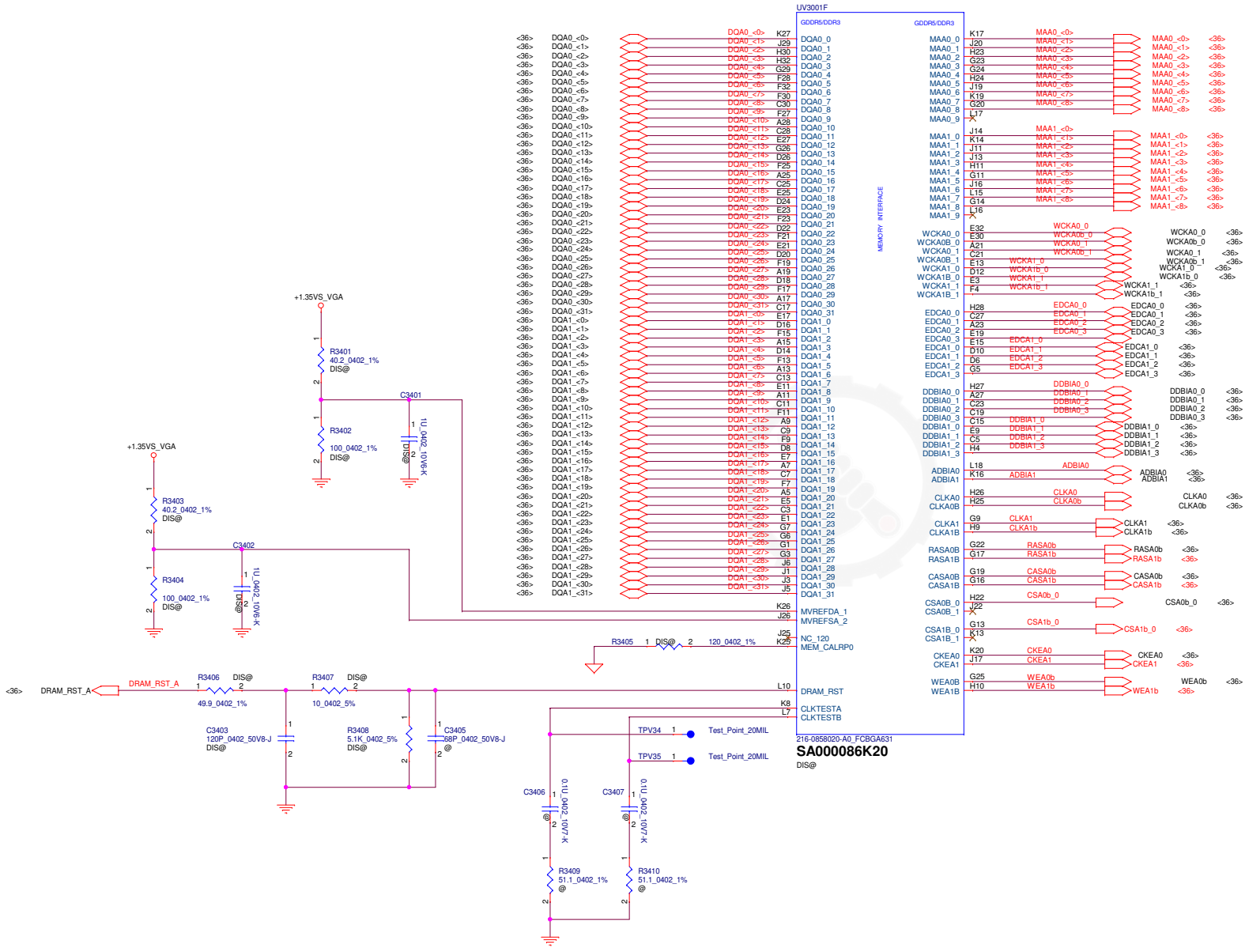


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-M1-70_VSS

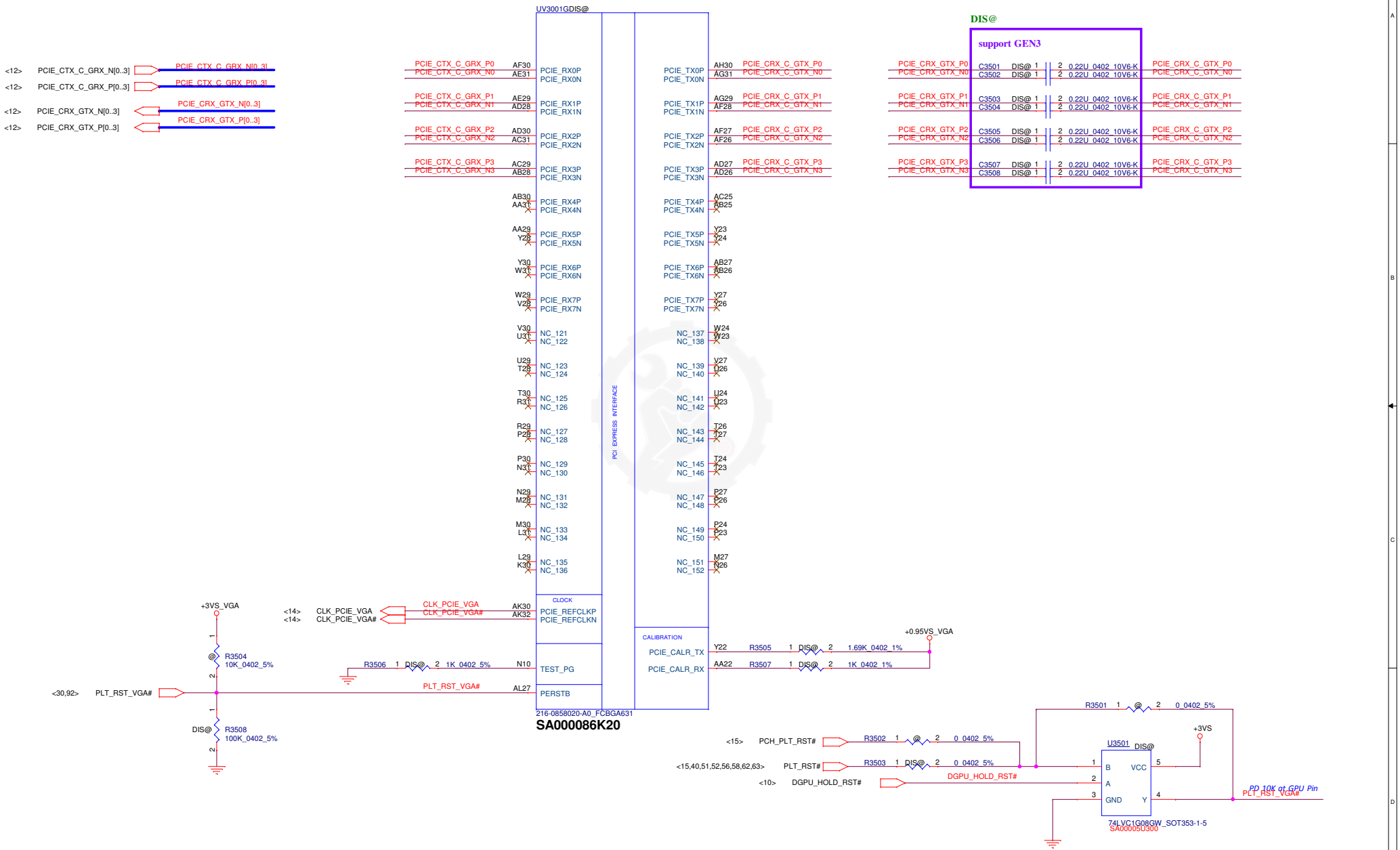
Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017 Sheet 33 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	R17M-M1-70_VRAM		
Size Custom	Document Number EL480 / EL580 MM-B461		Rev 0.2
Date: Friday, October 06, 2017	Sheet 34 of 99		

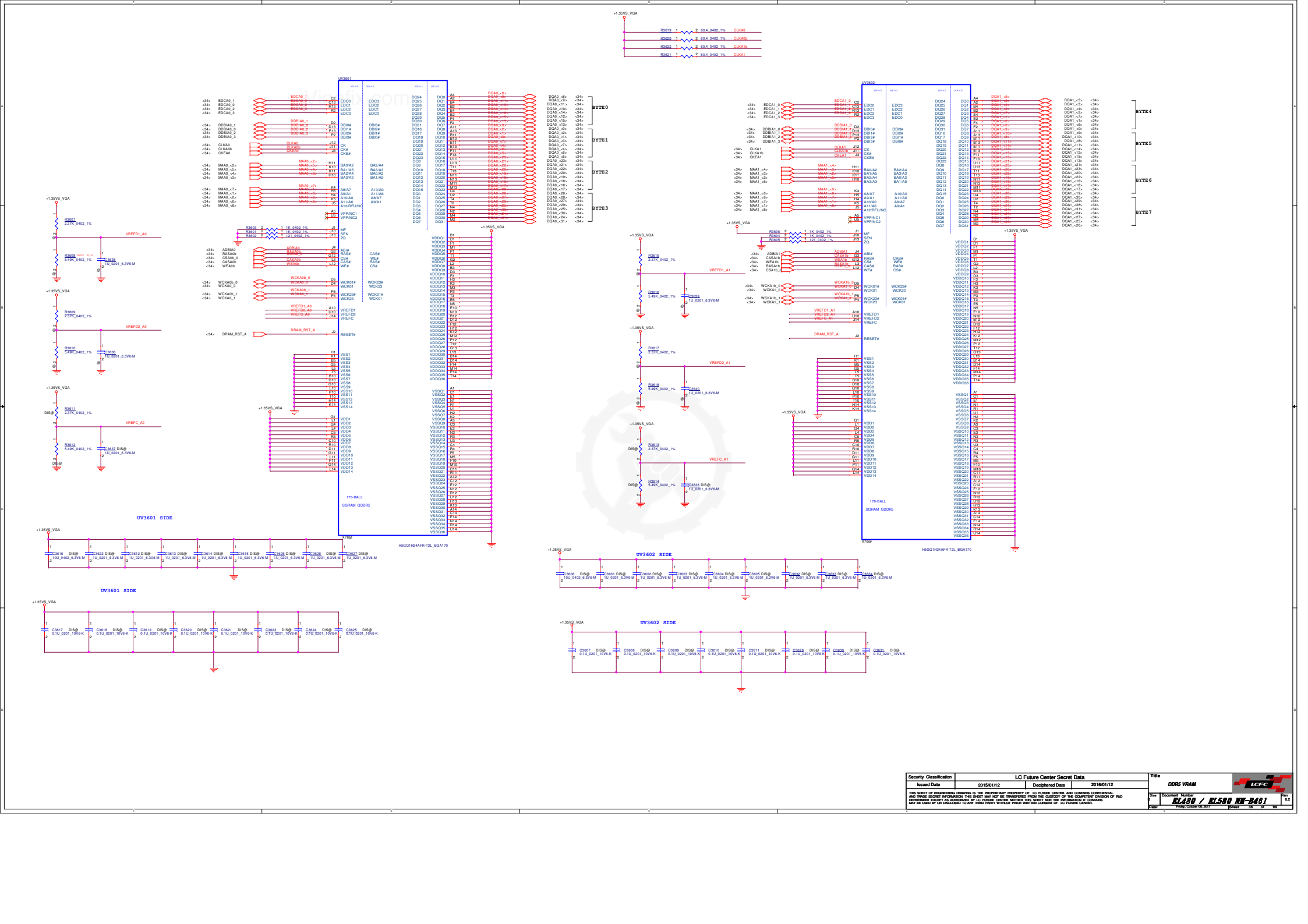


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: R17M-M1-70_PCIE

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 35 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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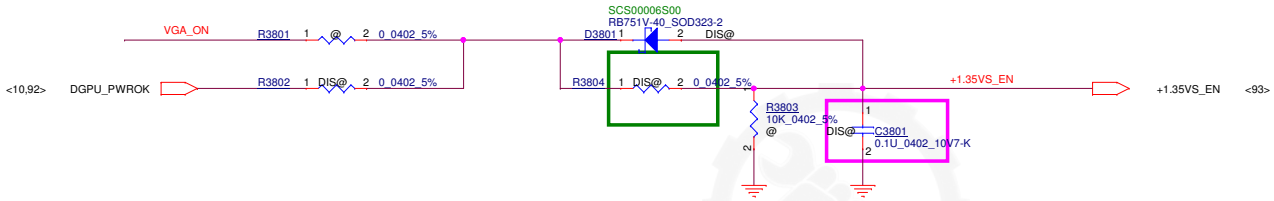
Title: DDR5 VRAM

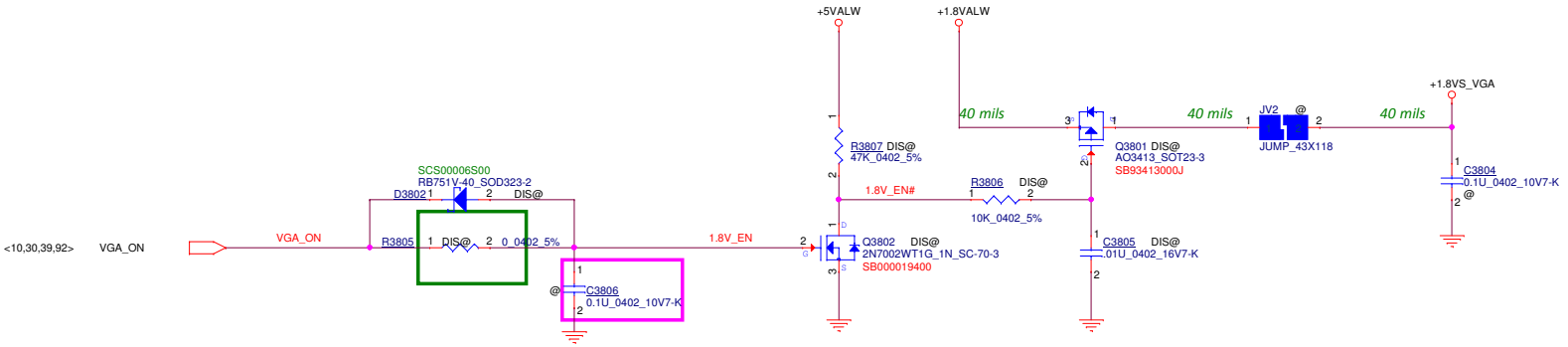
Size: D | Document Number: KL460 / KL580 MB-B461 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 35 of 99

Title	<Title>		
Size A	Document Number EL480 / EL580 NM-B461		Rev <RevCode>
Date: Friday, October 06, 2017		Sheet 37 of 99	



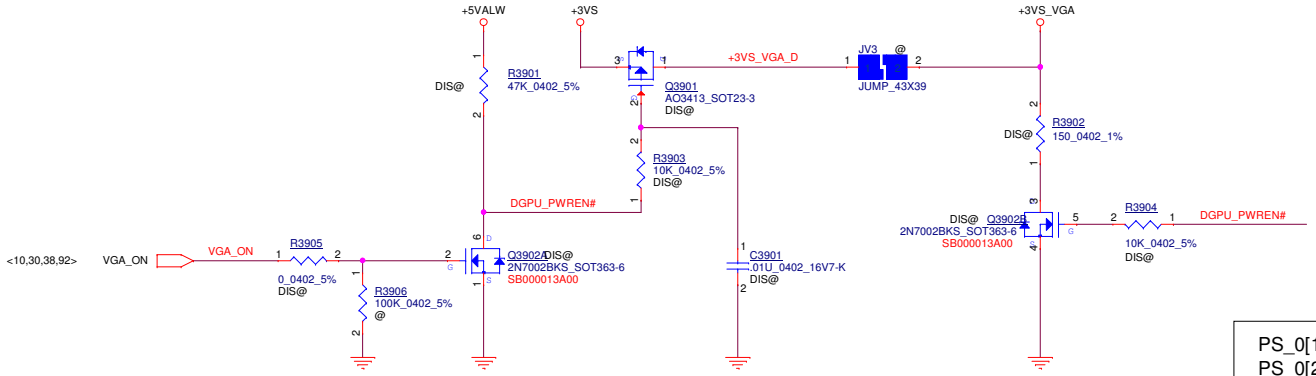
+1.8VALW to +1.8VS_VGA



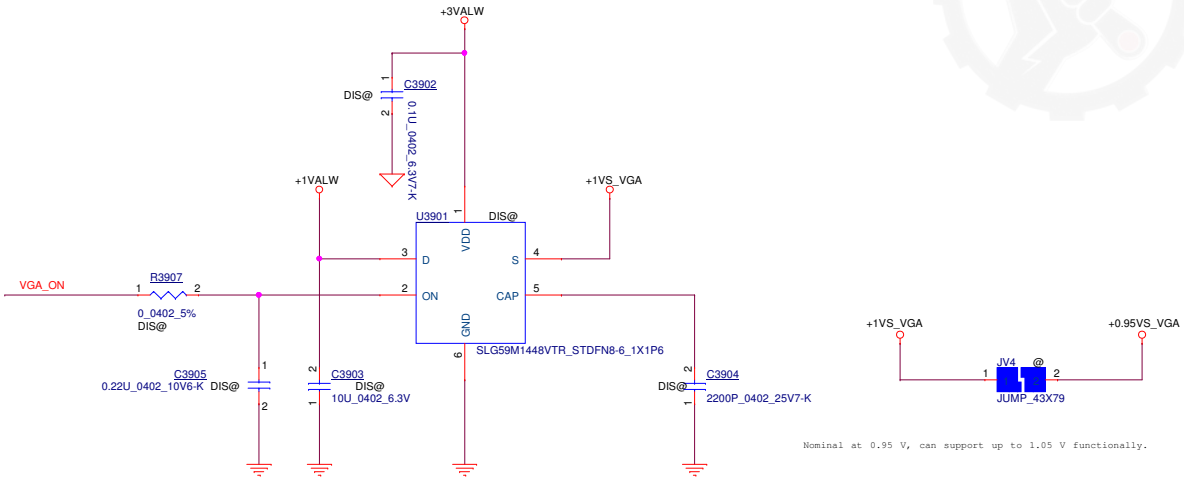
Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	R17M-M1-70_PW SWITCH		
Size: Custom	Document Number: EL480 / EL580 NM-B461		Rev: 0.2
Date: Friday, October 06, 2017	Sheet 38 of 99		

+3VS to +3VS_VGA



+1VALW to +1VS_VGA



MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

Title: R17M-M1-70_PW SWITCH

Size: Custom | Document Number: EL480 / EL580 NM-B461 | Rev: 0.2

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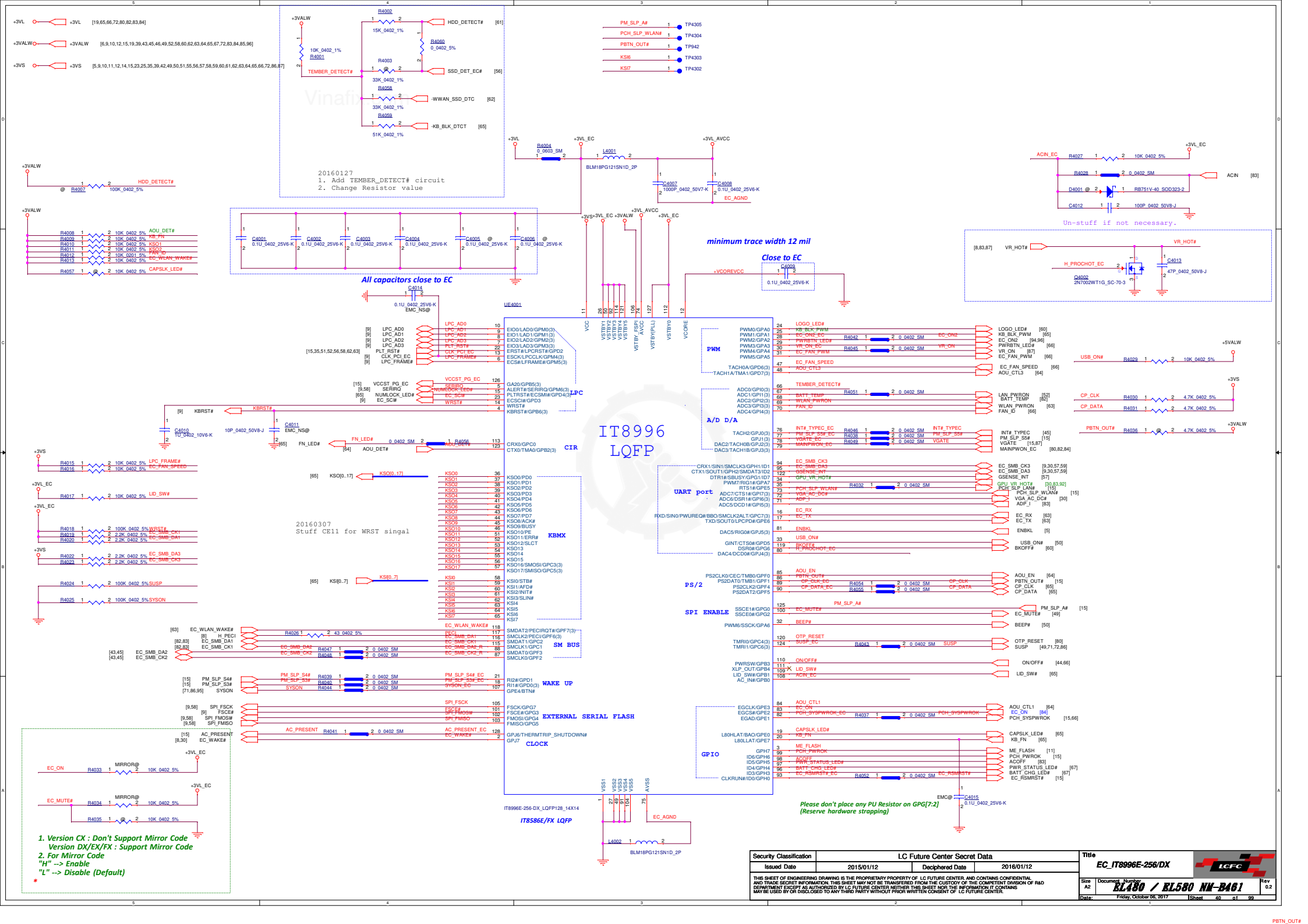
IT8996
LQFP
20160127
1. Add TEMBER_DETECT# circuit
2. Change Resistor value
20160307
Stuff CE11 for WRST singal
All capacitors close to EC
minimum trace width 12 mil
Close to EC
Un-stuff if not necessary.
Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)
1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*
IT8996E-256-DX_LQFP128_14X14
IT8586E/FX LQFP
PWM
LPC
A/D D/A
CIR
UART port
KBMX
PS/2
SM BUS
SPI ENABLE
WAKE UP
EXTERNAL SERIAL FLASH
GPIO
CLOCK
Security Classification
LC Future Center Secret Data
Issued Date
2015/01/12
Deciphered Date
2016/01/12
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Title
EC_IT8996E-256/DX
Size
A2
Document Number
EL480 / EL580 NK-B461
Rev
0.2
Date:
Friday, October 06, 2017
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40
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99

LAYOUT/ROUTING GUIDELINES

1.For the ADC layout notice circuits,
a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.
b) Isolate Analog and Digital ground plane.

2.For all power plane,

a)For the VSTBY circuits,

*Recommended net "VSTBY" minimum trace width 12mils.

b)For the VBAT circuits,

1) Vbat should be routed with a minimum trace width of 12 mils.

2) Please make the trace length short, and the trace width wide enough.

3) Isolate the pin-Vbat of EC and the pin of south bridge VCCRTC to avoid VBAT drops.

4) The capacitor connected to Diode is spare for battery installation glitch.

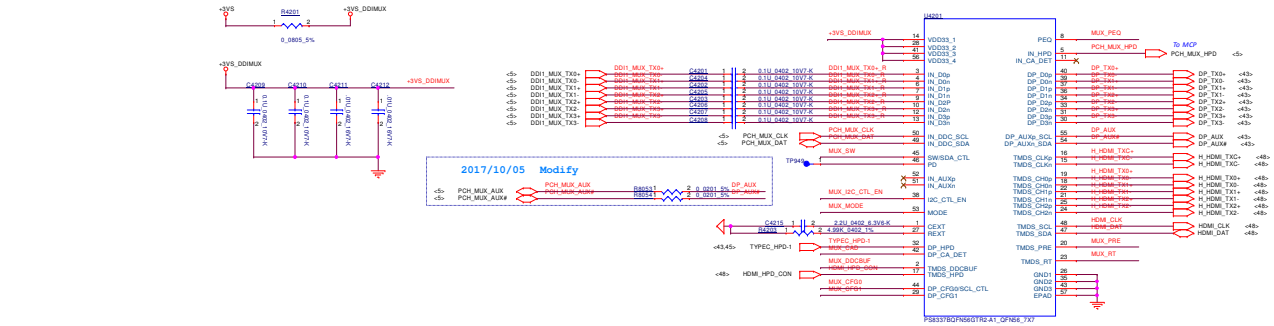
c)For the PLL power circuits,

Internal PLL is supplied by power pin127 of EC only and may have some filter circuit.

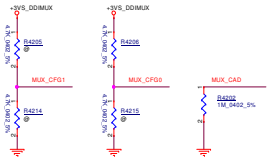
3.For SPI clock lines,
a) If possible, please avoid using any through-hole.
b) Do not use multiple signal layers for clock signals.
c) Please make the trace length short, and the trace width wide enough.
EC should close to PCH for HSPI signals & SPI flash should close to EC for FSPI signals.
d) The spacing to the closest neighbor should be wide enough.
e) The discrete damping resistors and capacitors are recommended.
f) Keep clock traces as straight as possible.Use arc-shaped traces instead of
right-angle bends.

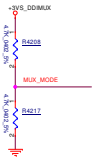
Title		
EC_IT8996E-256/DX		
Size: Custom	Document Number: EL480 / EL580 NM-B461	Rev: 0.2
Date: Friday, October 06, 2017	Sheet 41 of 99	

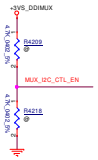
+5VALW <38,39,40,50,52,63,64,66,67,71,72,84,86,87,88,89,90,92,94,95>



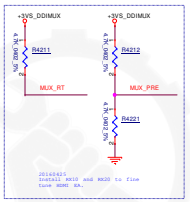
Auto Mode
DP Higher Priolity







Pass Through Mode



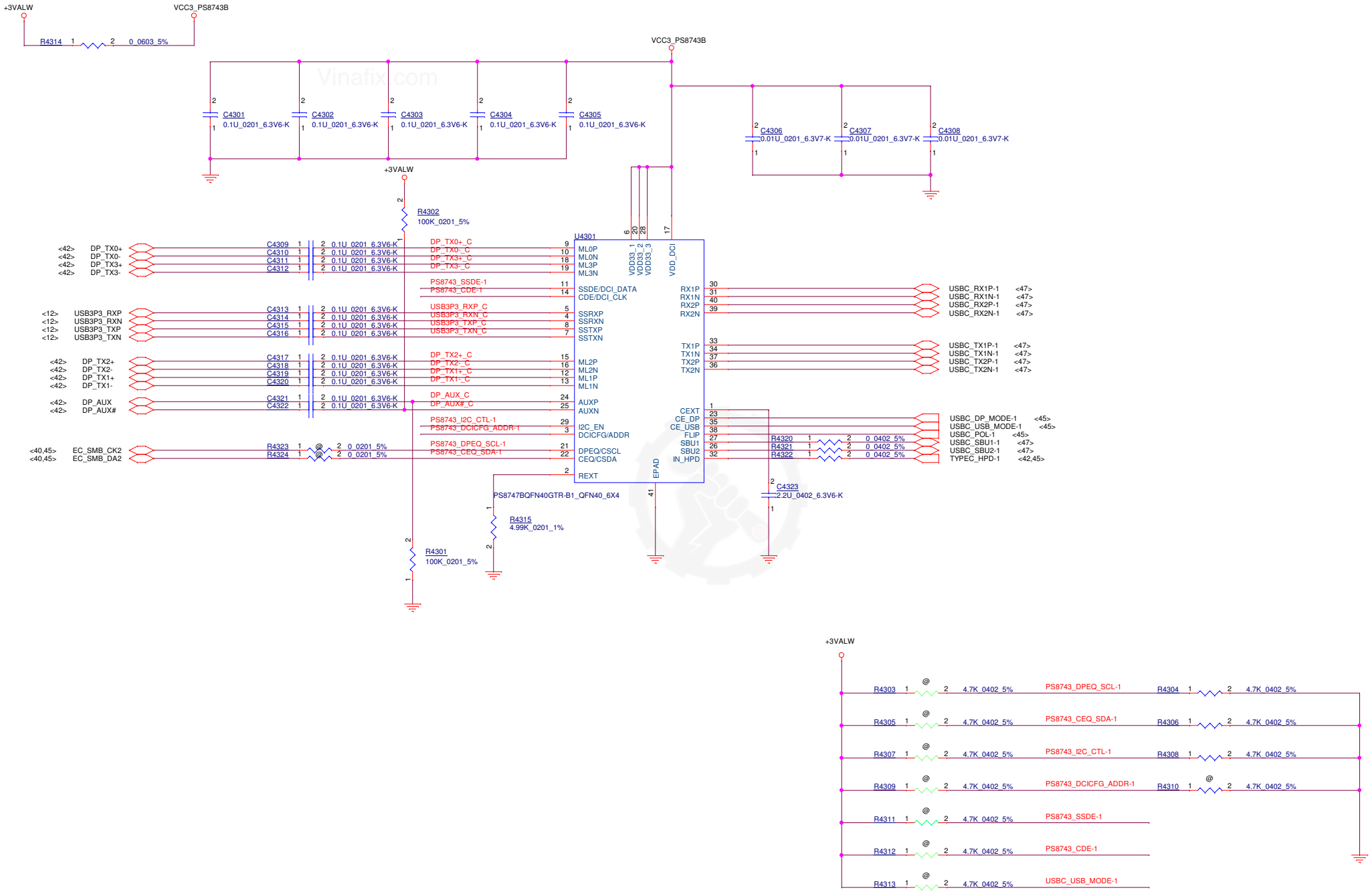
20160419
1. Connect MUX_SW to PCH, display priolity control by BIOS
2. Add R961 0 ohm and unstaff RX15.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: PS8337/HDMI & DP MUX

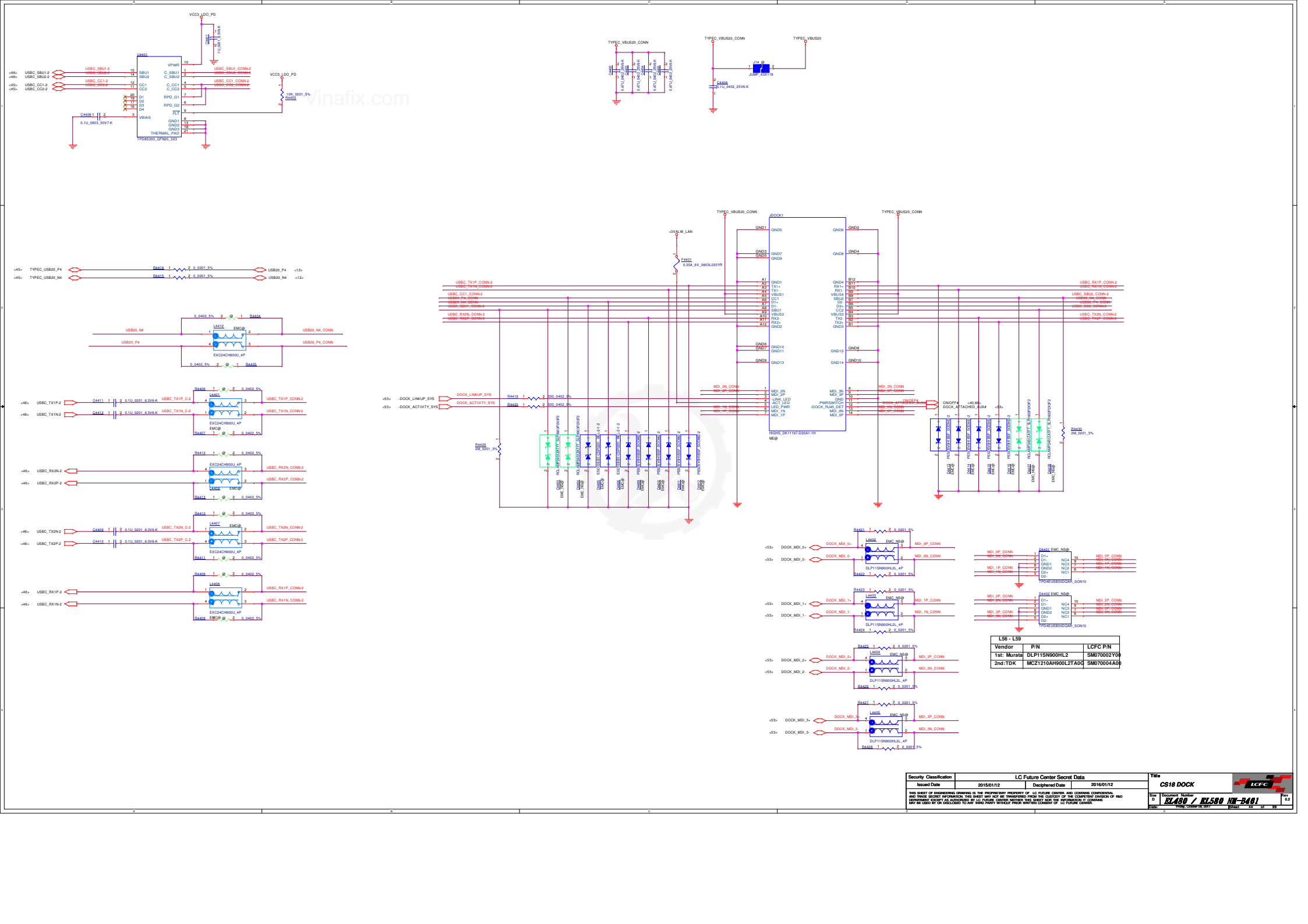
Size	Document Number	Rev
D	KL460 / KL580 NM-B481	0.2

Date: Friday, October 06, 2017 Sheet 42 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	PS8747/USB & TYPEC SWITCH		
Size	Document Number		Rev
Custom	EL480 / EL580 NM-B461		0.2
Date:	Friday, October 06, 2017	Sheet	43 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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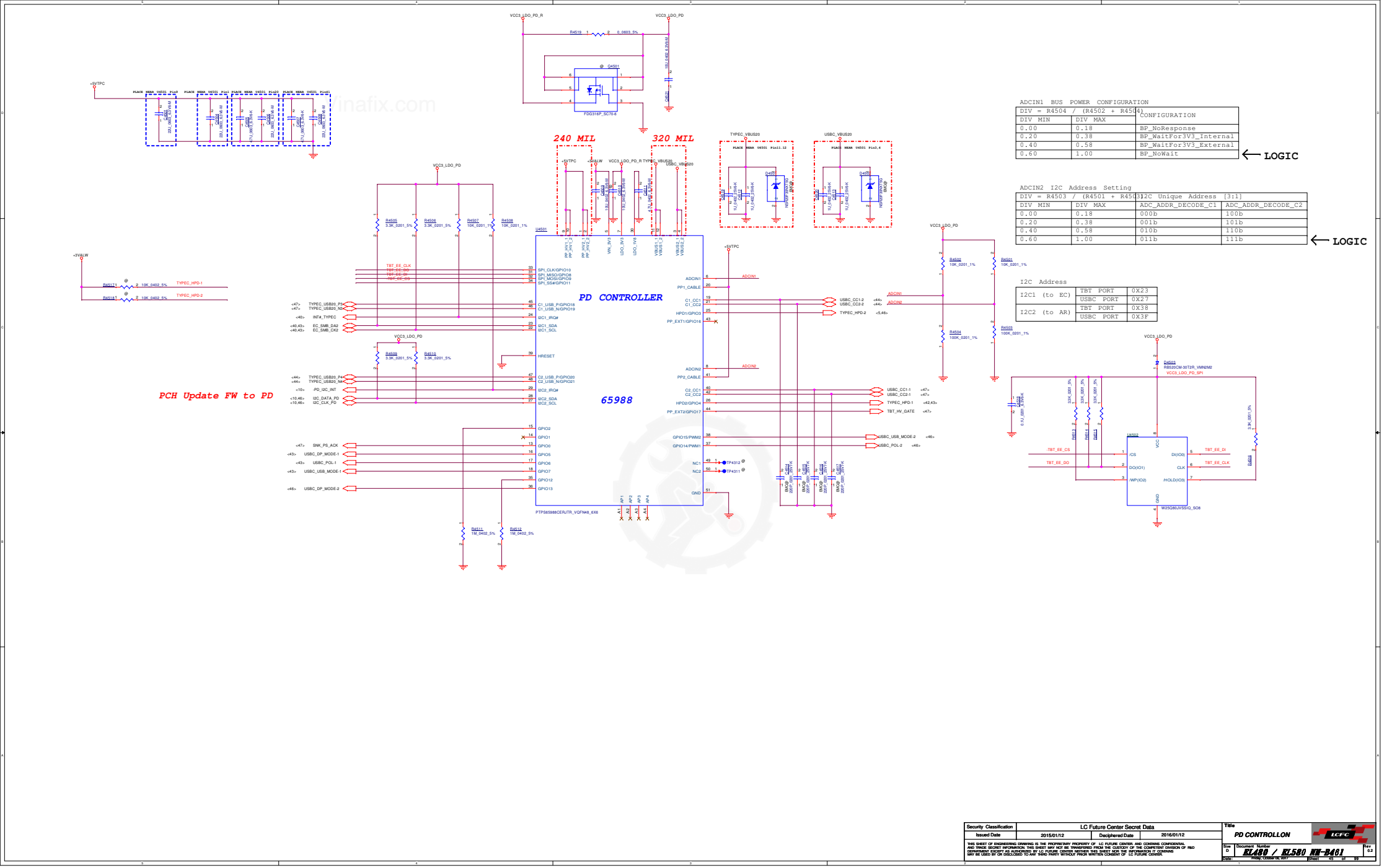
Title: CS18 DOCK

Size: D | Document Number: KL460 / KL580 NM-B481 | Rev: 0.2

Date: Friday, October 06, 2017 | Sheet 44 of 99


240 MIL
320 MIL
PD CONTROLLER
65988
PCH Update FW to PD
PTPS65988CERJTR_VQFN48_6X8
FDG316P_SC70-6
ADCIN1 BUS POWER CONFIGURATION
DIV = R4504 / (R4502 + R4504)
DIV MIN
DIV MAX
CONFIGURATION
0.00
0.18
BP_NoResponse
0.20
0.38
BP_WaitFor3V3_Internal
0.40
0.58
BP_WaitFor3V3_External
0.60
1.00
BP_NoWait
LOGIC
ADCIN2 I2C Address Setting
DIV = R4503 / (R4501 + R4503)
I2C Unique Address [3:1]
ADC_ADDR_DECODE_C1
ADC_ADDR_DECODE_C2
000b
100b
001b
101b
010b
110b
011b
111b
LOGIC
I2C Address
I2C1 (to EC)
I2C2 (to AR)
TBT PORT
USBC PORT
0X23
0X27
0X38
0X3F
Security Classification
LC Future Center Secret Data
Issued Date
2015/01/12
Deciphered Date
2016/01/12
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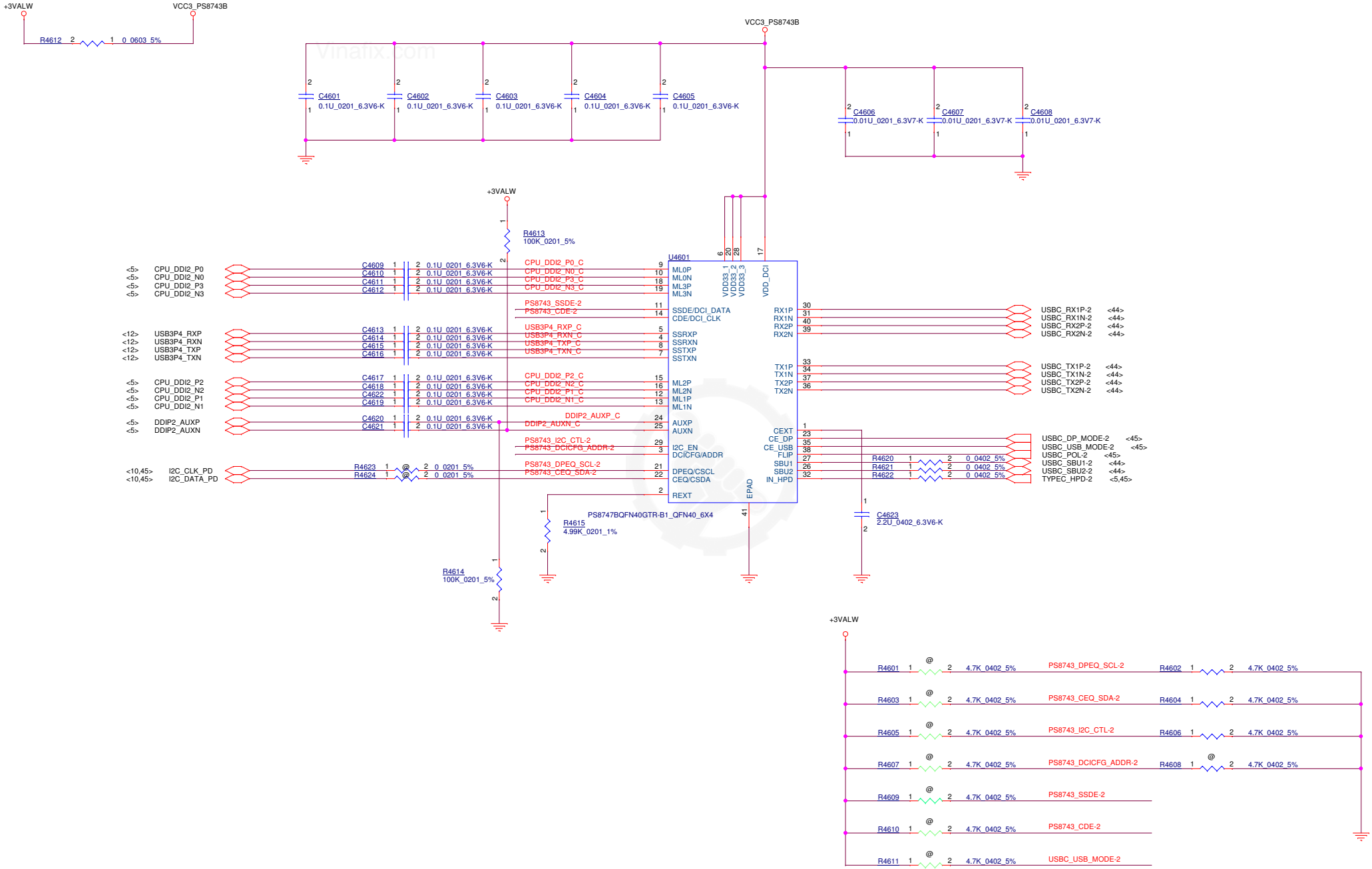
Title
PD CONTROLLON
Size D
Document Number
KL480 / KL580 NB-2461
Rev 0.2
Date: Friday, October 06, 2017
Sheet 45 of 99

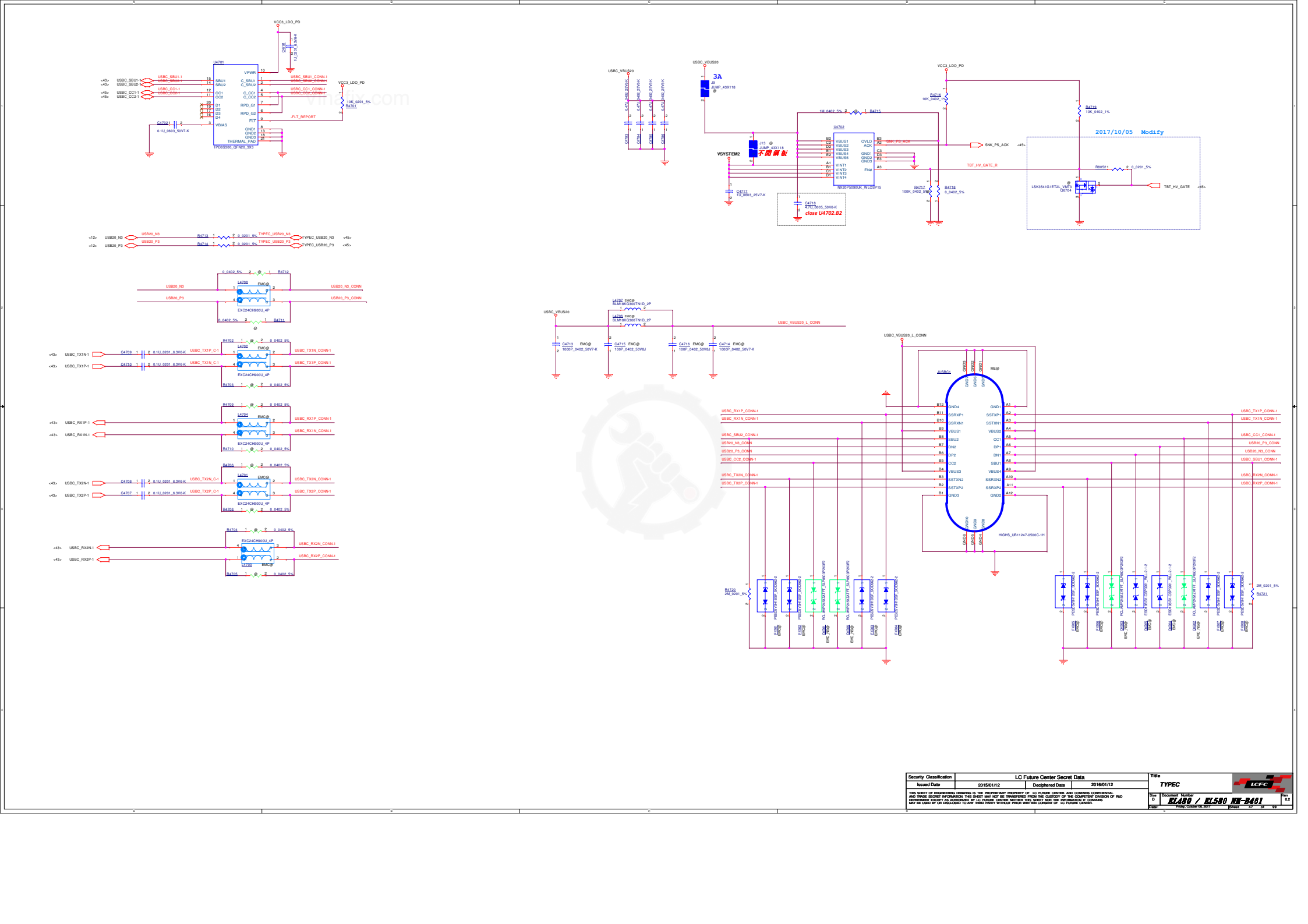


Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: PS8747/USB & TYPEC SWITCH

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017 Sheet 46 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

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Title: TYPEC

Size: D | Document Number: KL480 / KL580 MB-B461 | Rev: 0.2

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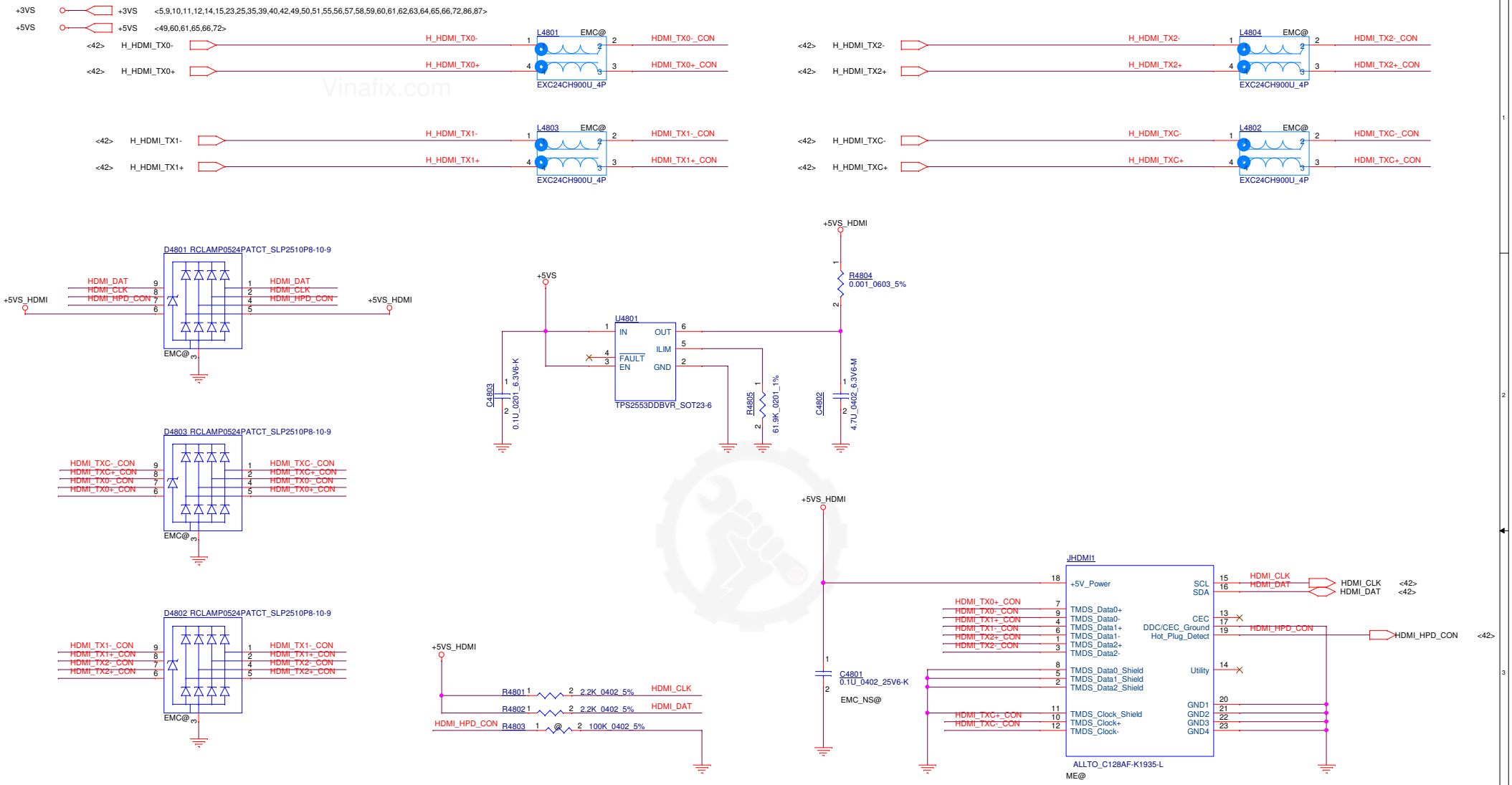


Figure 7-12. HDMI 1.4* HPD Active Level Shifter Design Recommendation

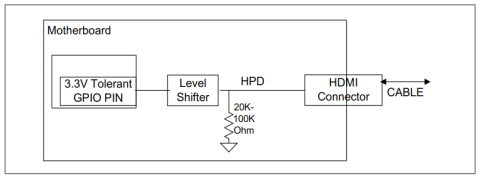
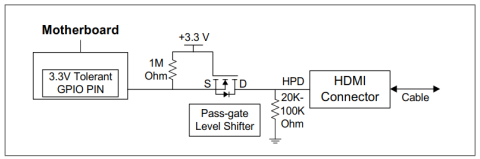


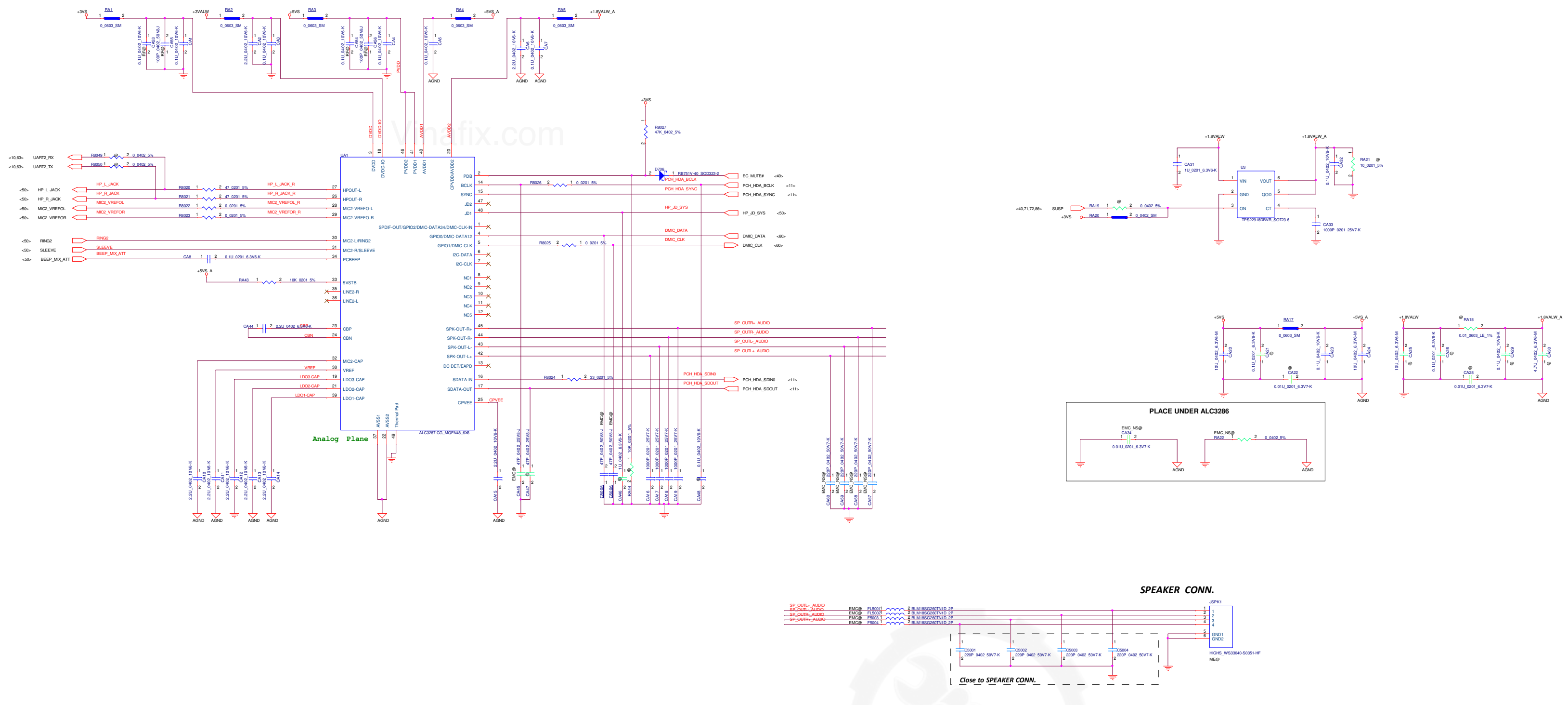
Figure 7-13. HDMI 1.4* HPD Cost Reduced Level Shifter Design Recommendation



Note: 3.3V transistor gate supply must turn off when CPU power is turned off.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	HDMI CONN		
Size	Document Number		Rev
Custom	EL480 / EL580 NM-B461		0.2
Date:	Friday, October 06, 2017	Sheet	48 of 99

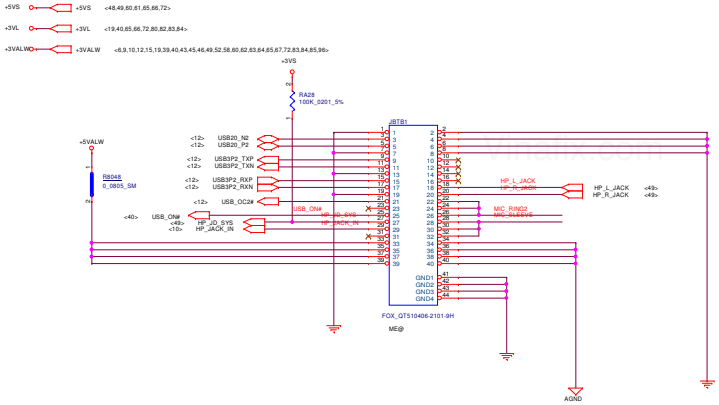


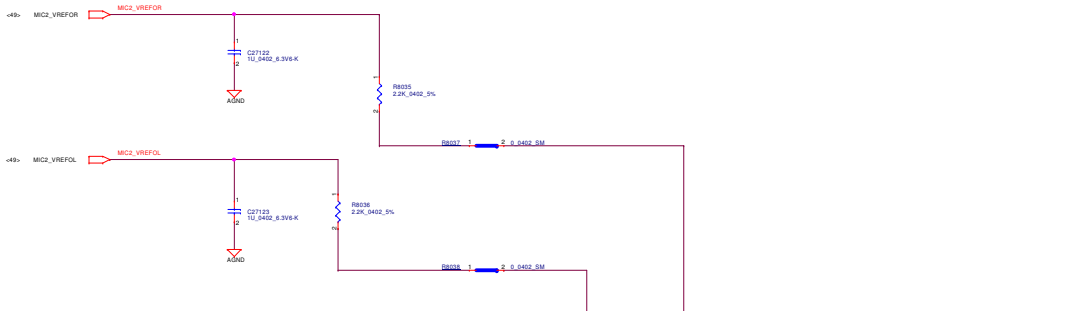
Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

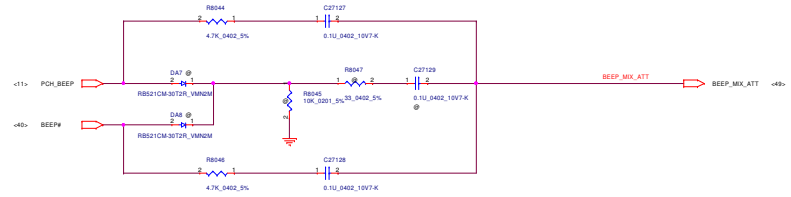
Title: BLANK

Size	Document Number	Rev
E	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017

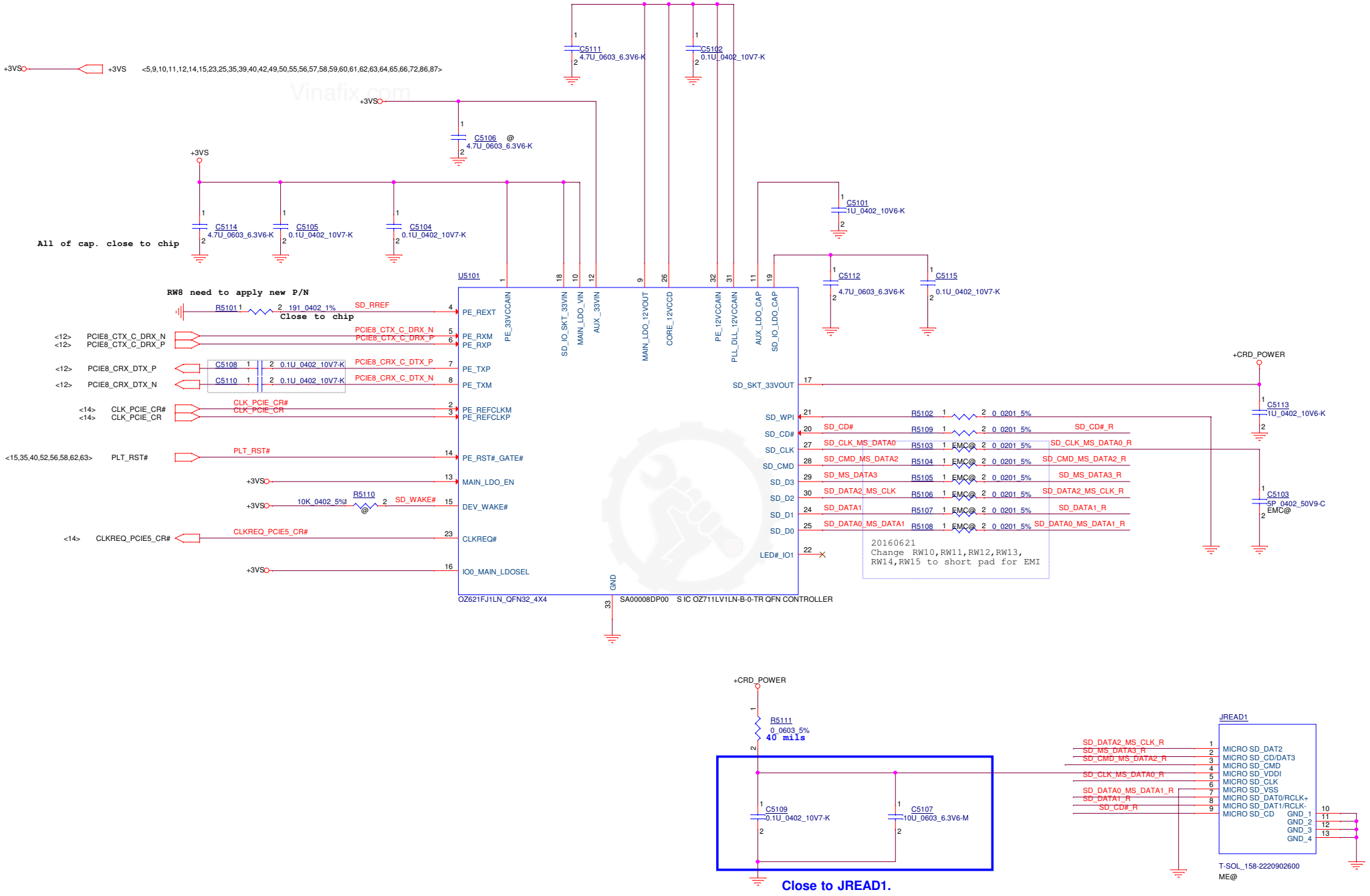






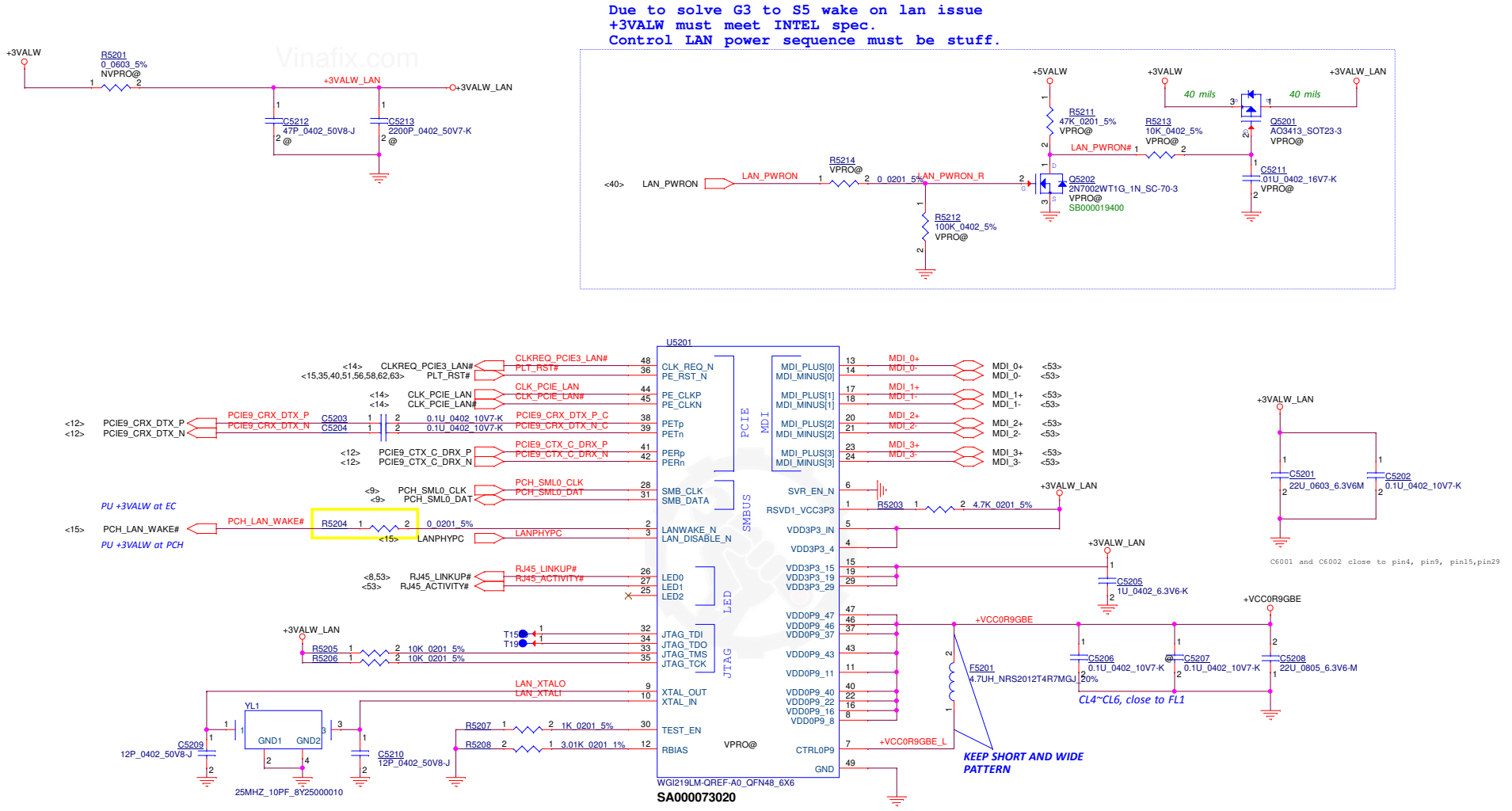
Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	CODEC & USB sub card		
Size	Document Number		Rev
D	KL460 / KL580 MB-B461		0.2
Date: Friday, October 09, 2015	Sheet 50 of 99		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	CARD READER		
Size	Document Number		Rev
Custom	EL480 / EL580 NM-B461		0.2
Date:	Friday, October 06, 2017	Sheet	51 of 99



U5201 GBE PHY

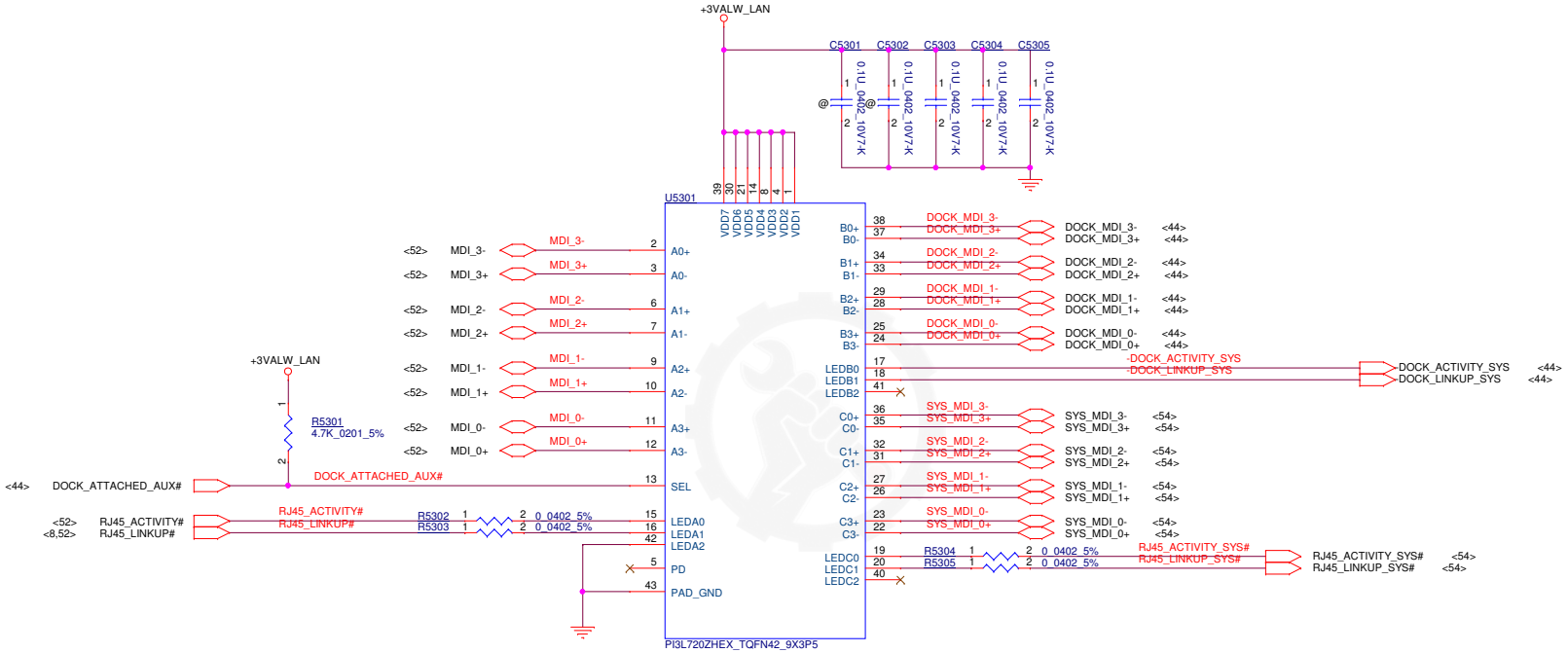
	Model	P/N
vPro	WGI219LM	SA000073020
non-vPro	WGI219V	SA000072Z20

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: GBE LAN PHY

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

Date: Friday, October 06, 2017 Sheet 52 of 99



SA00007E900

Vendor	P/N	NOTE
Pericom	PI3L720ZHE+CX, SA00007E900	Main Source
ONSemi	NCN7201 , SA00005TF00	2nd Source (FVT)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: GBE LAN PHY SWITCH

Size: Custom	Document Number: EL480 / EL580 NM-B461	Rev: 0.2
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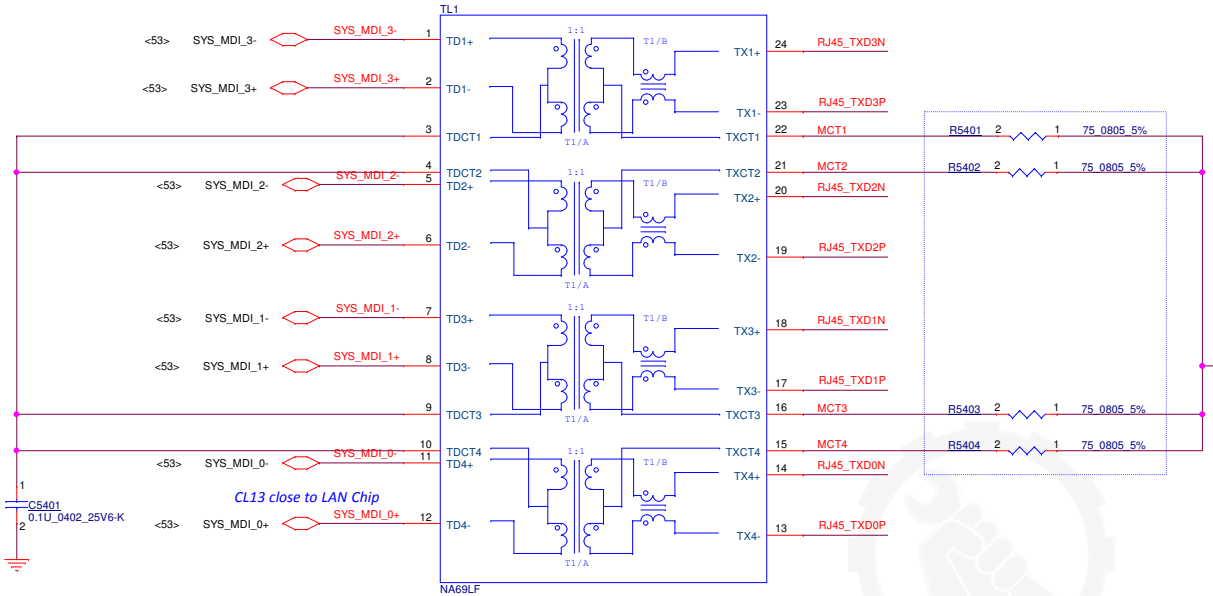
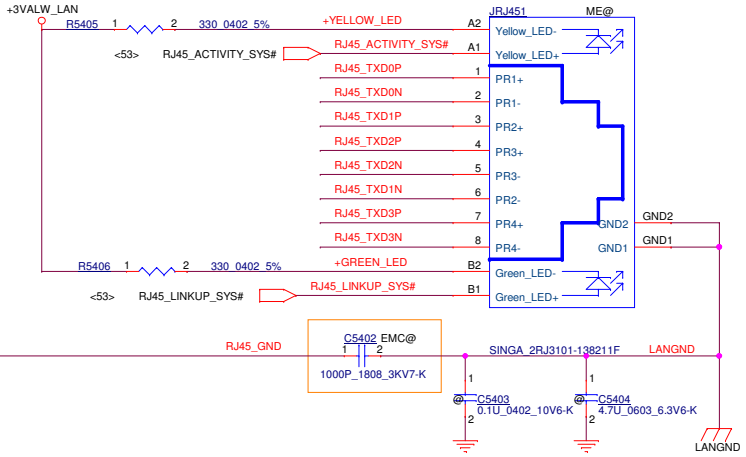
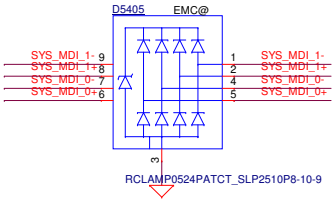
LAN X' FORM

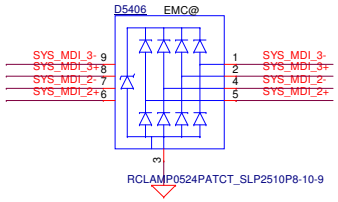


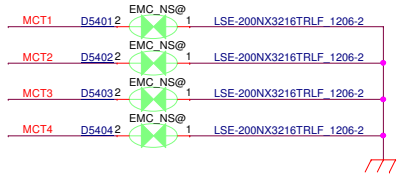
SP050008B00

RJ45 Conn.



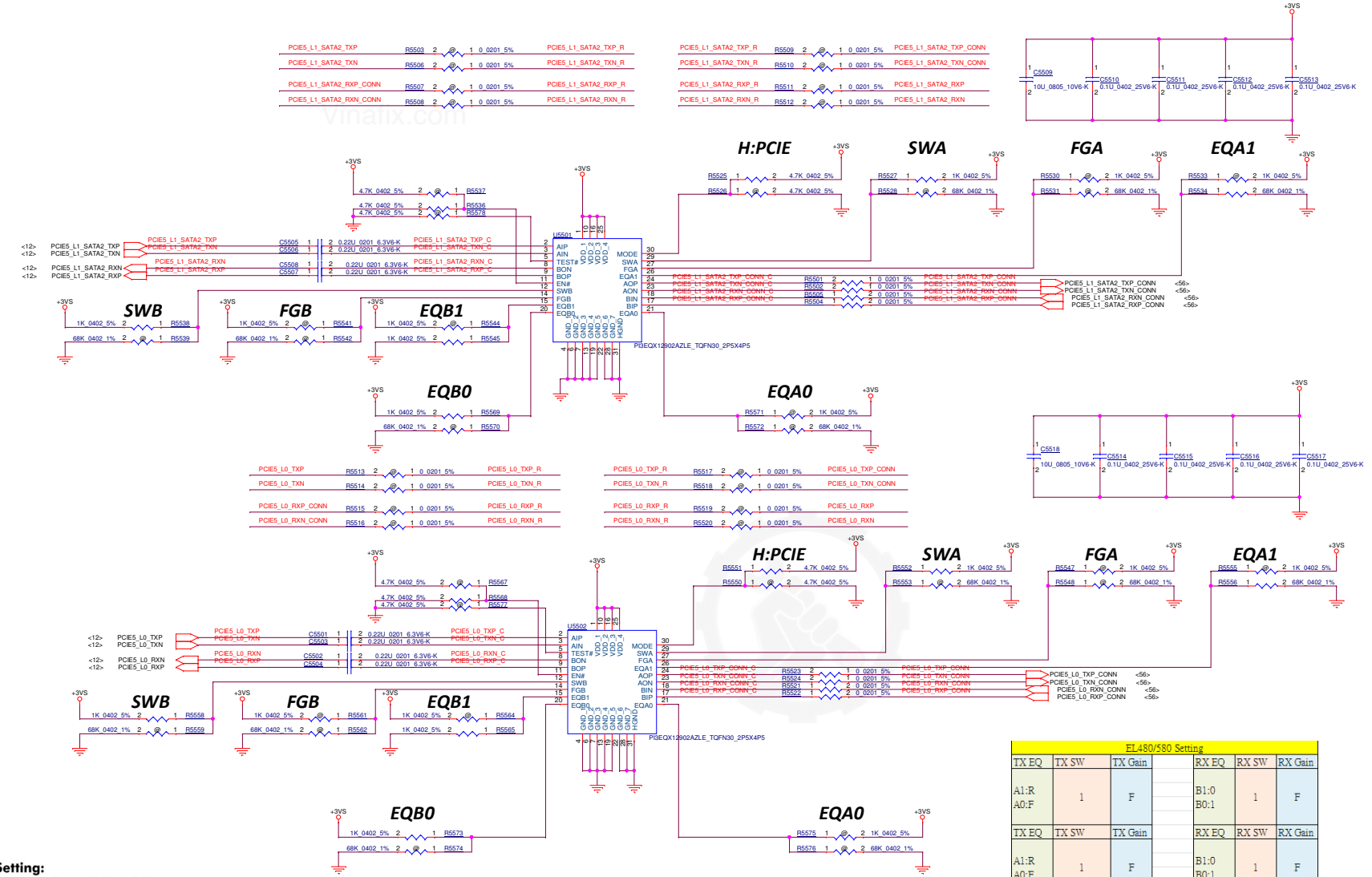






Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	RJ45 CONN		
Size	Document Number		Rev
Custom	EL480 / EL580 NM-B461		0.2
Date:	Friday, October 06, 2017	Sheet	54 of 99



Equalization Setting:

EQA/B are the selection pins for the equalization selection

EQ		Equalizer setting (dB)			
A1/B1	*A0/B0*	*@1.25GHz*	*@2.5GHz*	*@3GHz*	*@4GHz*
0	0	0.4	1.8	2.4	3.9
0	R	0.6	2.3	3.2	4.9
0	F	0.8	2.9	3.9	5.8
0	1	1.0	3.5	4.6	6.6
R	0	2.1	4.4	5.3	7.2
R	R	2.3	4.9	5.9	7.9
R	F	2.5	5.3	6.4	8.5
R	1	2.7	5.8	7.0	9.1
F	0	3.7	6.5	7.7	9.7
F	R	3.9	6.9	8.1	10.2
F	F	4.1	7.3	8.5	10.6
F	1	4.3	7.6	8.9	11.0
1	0	5.4	8.4	9.5	11.4
1	R	5.6	8.7	9.8	11.8
1	F	5.8	9.0	10.2	12.1
1	1	5.9	9.2	10.4	12.5

Flat Gain Setting:

FGA/B are the selection bits for the DC gain

	Flat Gain Settings
FGA/B	*dB*
0	-3.5
R	-1.5
F	0 (Default)
1	+1.5

-1dB compression point output Swing Setting:

SWA/B are the selection bits for the -1dB compression point output swing setting (100Mhz)

	Output Linear Swing Settings
SWA/B	*mVppd*
0	990
R	1050
F	1000 (Default)
1	1120

EL480/580 Setting						
TX EQ	TX SW	TX Gain		RX EQ	RX SW	RX Gain
A1:R A0:F	1	F		B1:0 B0:1	1	F
TX EQ	TX SW	TX Gain		RX EQ	RX SW	RX Gain
A1:R A0:F	1	F		B1:0 B0:1	1	F

For 12902A

0 means , pull down to GND thru 1K ohm
F , Floating
1 , pull up to VDD thru 1K ohm
R , pull down to GND thru 68K ohm.

	Channel Enable Setting
EN#	*Setting*
0	Enabled (Default)
1	Disabled

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Title: REDRIVER for 2280 PCIE SSD

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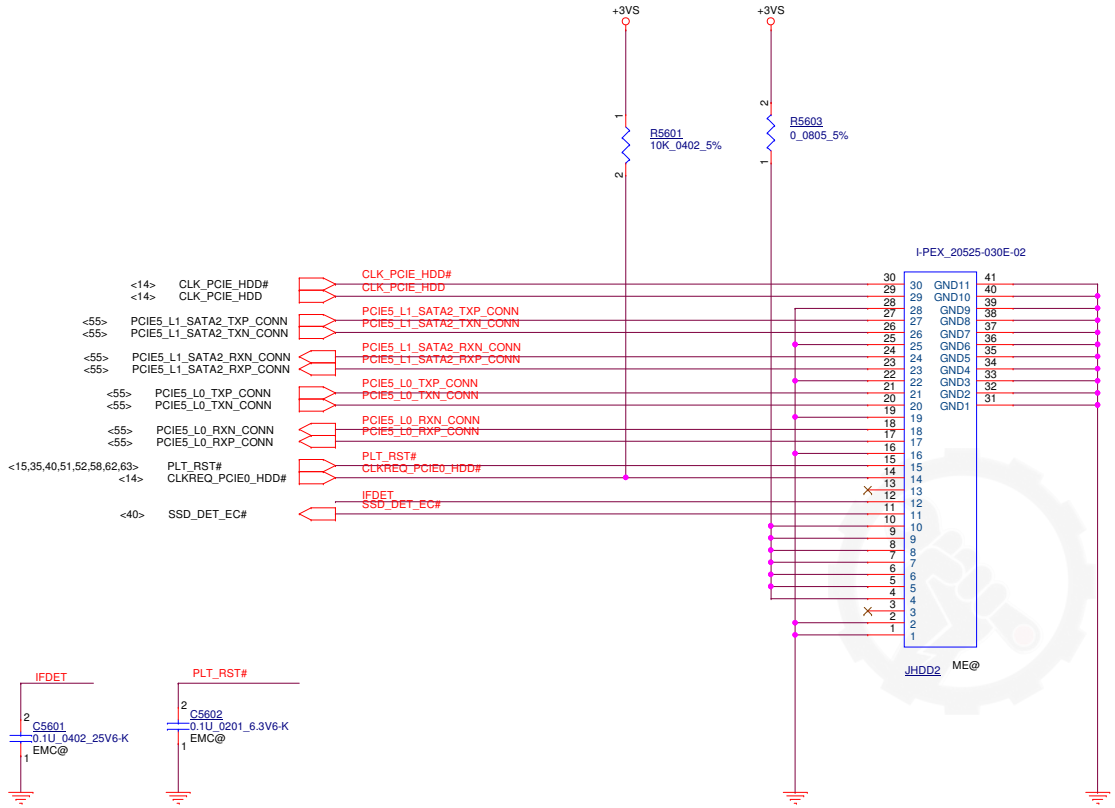

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: **M.2 Sub card CONN**

Size	Document Number	Rev
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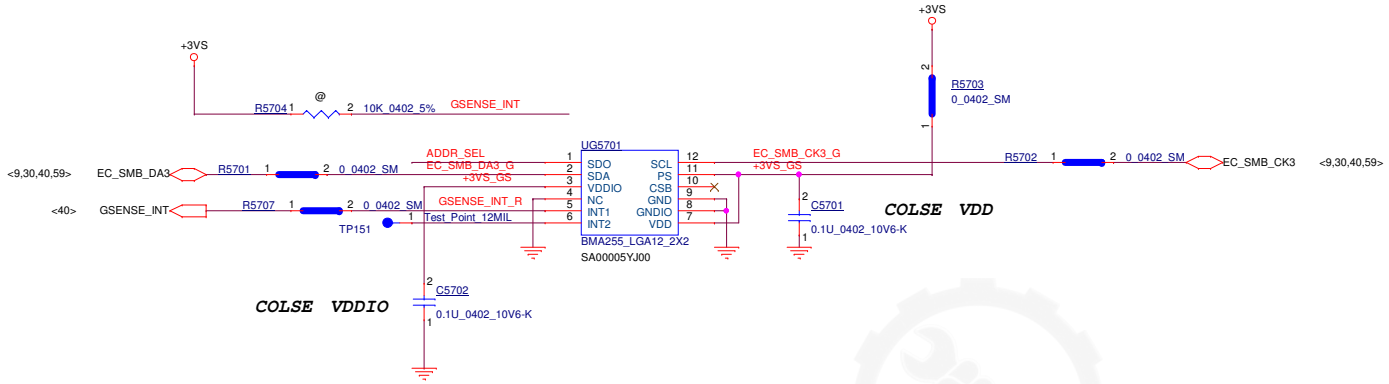
+3VS +3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,58,59,60,61,62,63,64,65,66,72,86,87>



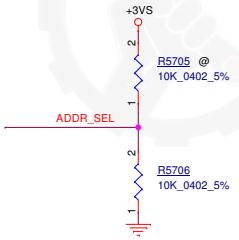


TABLE of G-Sersor (UG5701)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
BMA255	H	30h (W) & 31h (R)
	L	32h (W) & 33h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

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Title: G SENSOR

Size	Document Number	Rev
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+3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,59,60,61,62,63,64,65,66,72,86,87>

+3VALW <6,9,10,12,15,19,39,40,43,45,46,49,52,60,62,63,64,65,67,72,83,84,85,96>

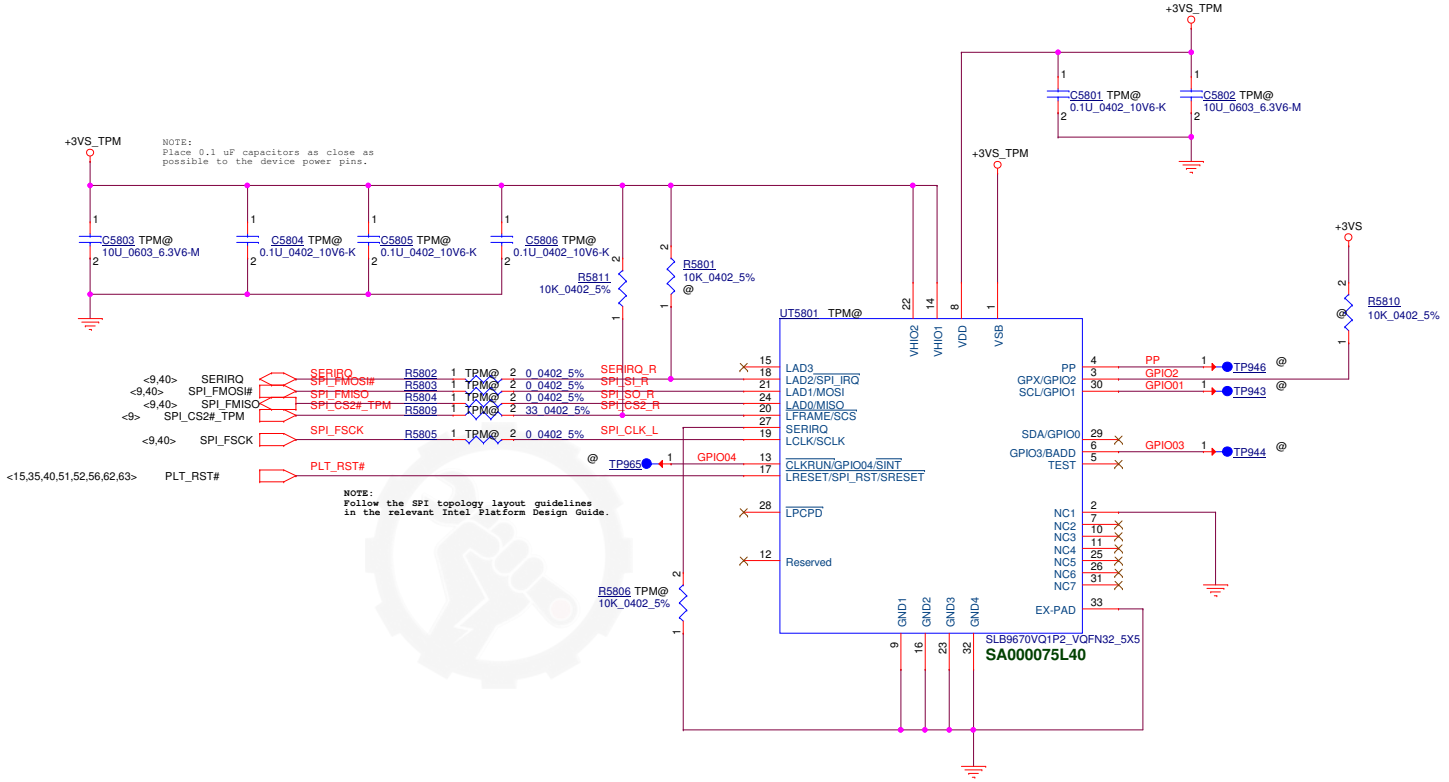
+3VS — R5807 1 @ 2 0_0402_5% — +3VS_TPM

+3VALW — R5808 1 TPM@ 2 0_0402_5% — +3VS_TPM

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	NC	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	NC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table



NOTE:
Check timing sequence in SDV phase.

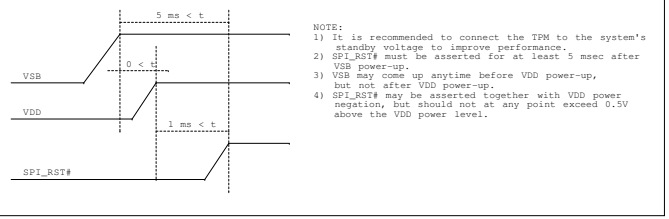


TABLE of TPM (UT5801)		
Vendor	LCFC P/N	Description
Infineon	SA000075L40	S IC SLB9670VQ2.0FW7.61 VQFN 32P TPM
ST	SA000089E10	S IC ST33HTPH2E32AHB4 VQFN 32P TPM

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Title: TPM

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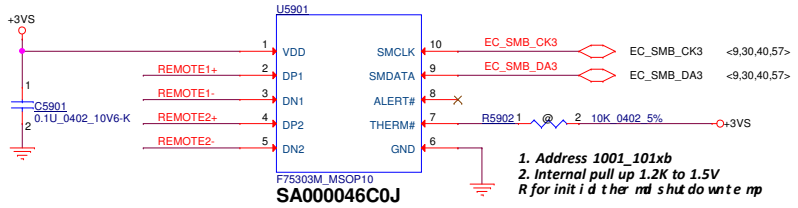
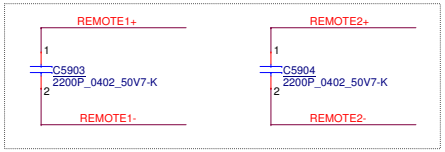
+3VS +3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,60,61,62,63,64,65,66,72,86,87>

Thermal Sensor

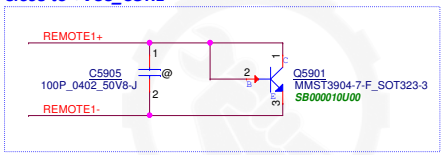


1. Address 1001_101xb
2. Internal pull up 1.2K to 1.5V
R for init i d ther md shut do wn t e mp

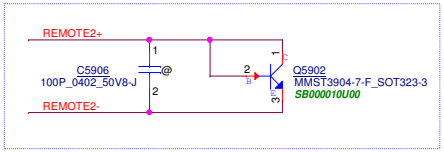
Close to U8



Close to +VCC_CORE



Close JDIMM1&JDIMM2



REMOTE2+/-:
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Trace length:<8"

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: THERMAL SENSOR

Size	Document Number	Rev
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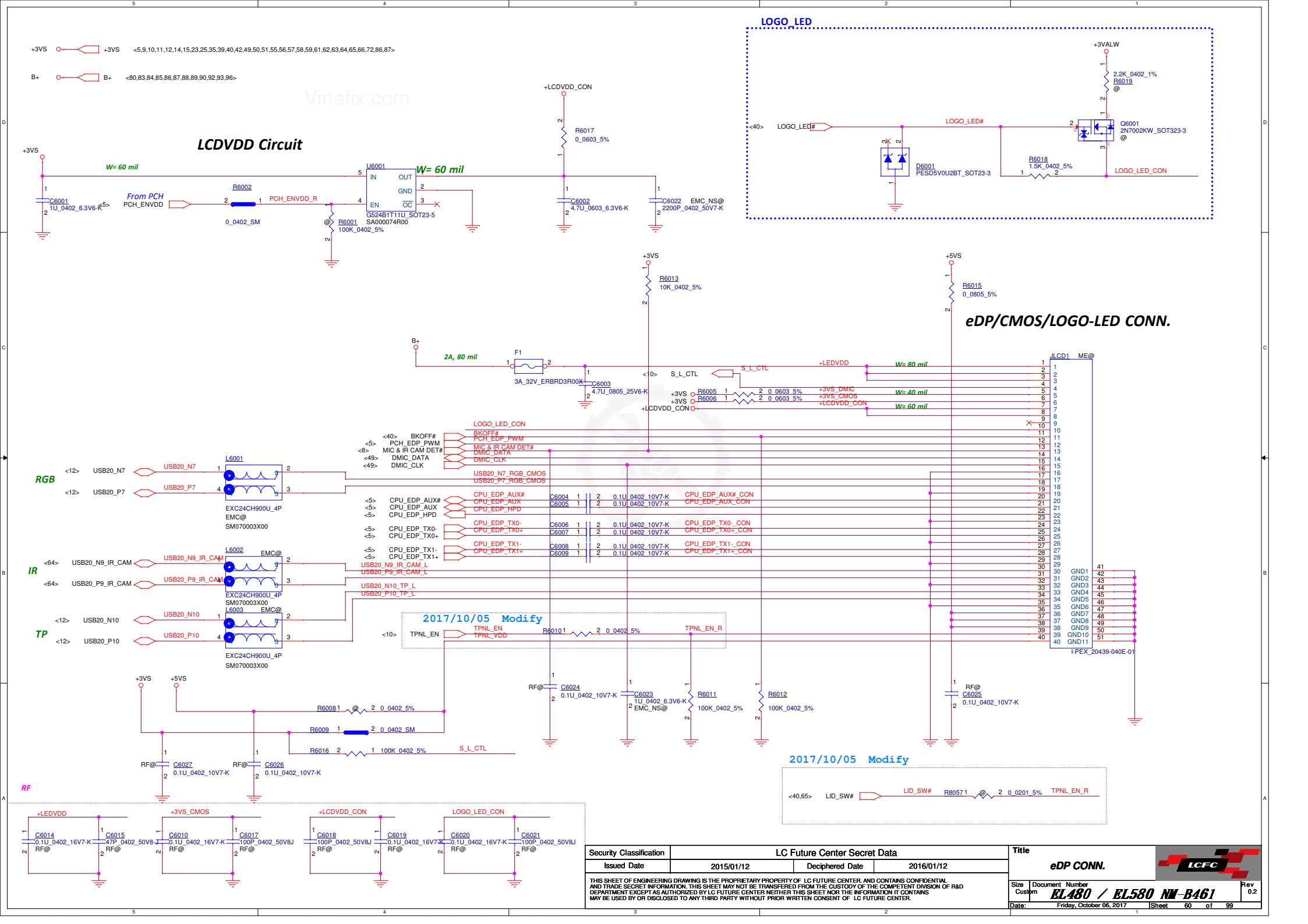

Vinafix.com

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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title	eDP CONN.		
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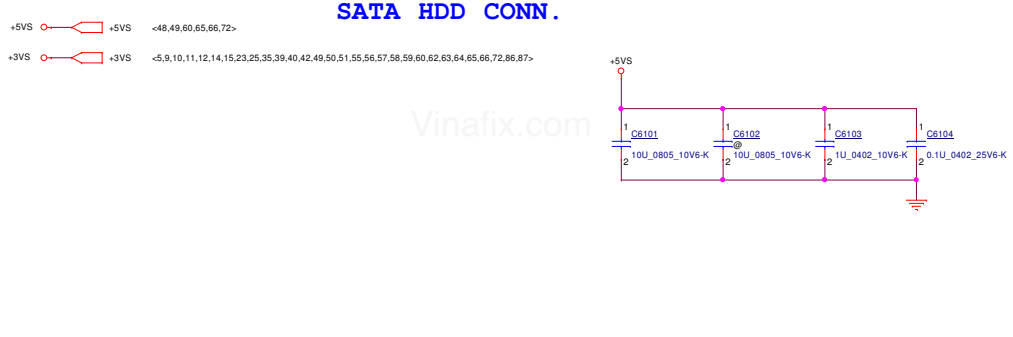
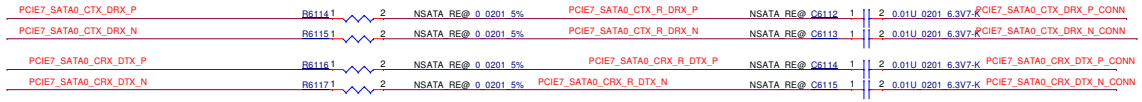
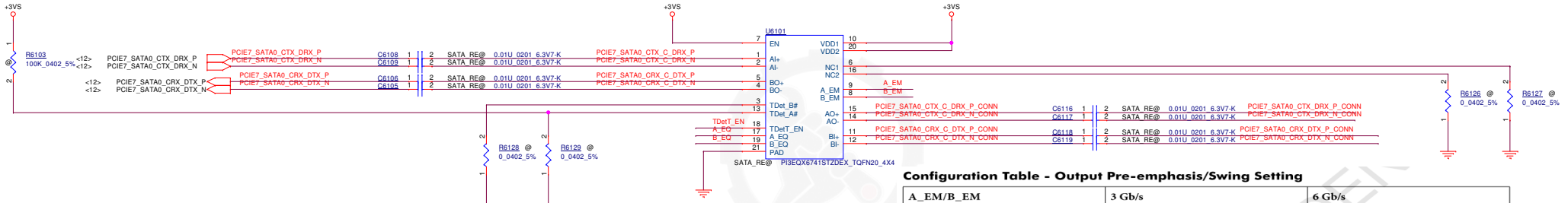
SATA HDD CONN.

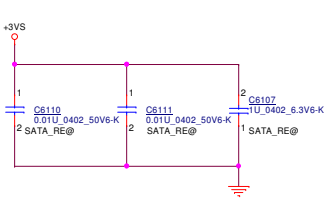


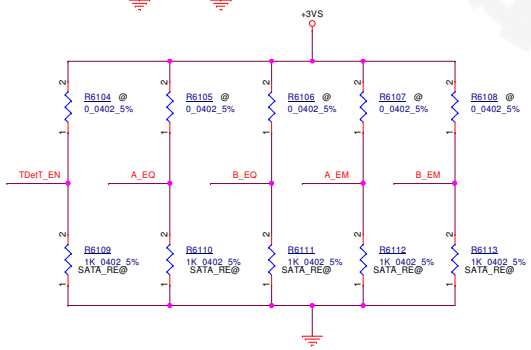


	Diodes	TI	Comment
Pin	PI3EQX6741ST	LVCP601	
3	Tdet_B#	GND	Connect to ground
6	NC	DEW2	Connect to ground and reserve pull-up with 4.7K to 3.3V
13	Tdet_A#	GND	Connect to ground
16	NC	DEW1	Connect to ground and reserve pull-up with 4.7k to 3.3V
18	TDeT_EN	GND	Connect to ground

SATA REDRIVER







Configuration Table - Output Pre-emphasis/Swing Setting

A_EM/B_EM	3 Gb/s	6 Gb/s
0	500mV pp	600mV pp
1	500mV pp + 3dB Pre-emphasis	600mV pp + 1.5dB Pre-emphasis

Configuration Table - Input Equalizer

A_EQ/B_EQ	1.5 Gb/s	3 Gb/s	6Gb/s
0	1 dB	2.5 dB	3 dB
floating	2.5 dB	5 dB	6 dB
1	4 dB	7.5 dB	9 dB

EL480/580 Setting				
TX EQ	TX EM		RX EQ	RX EM
3dB	0dB		3dB	0dB

KENOBI

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Title			
SATA HDD CONN/REDRIVE			
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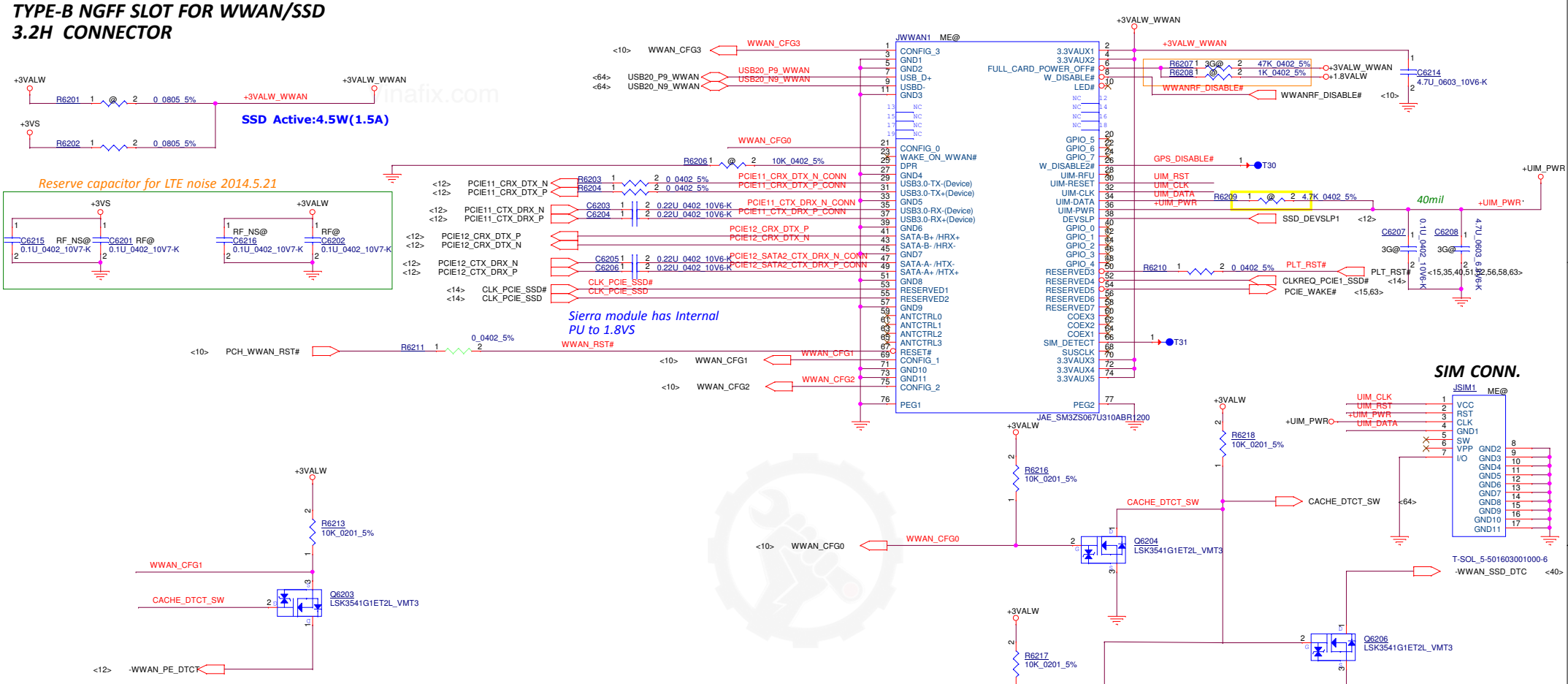
TYPE-B NGFF SLOT FOR WWAN/SSD
3.2H CONNECTOR



		GPP_A21	GPP_A18	GPP_A19	GPP_A20
	Solo/Lando KPL List	PIN 21	PIN 69	PIN 75	PIN 1
		CONFIG_0	**CONFIG_1**	**CONFIG_2**	**CONFIG_3**
WWAN	Sierra (QC) EM7565 LTE-A WWAN (PCIE Interface)	GND	GND	NC	NC
	Fibcom WWAN L831-EAU Product(USB2 Interface)	NC	GND	GND	GND
M.2 2242 SATA SSD	Lite-on 128GB SATA MLC M.2 2242-D3 / CV1-SB128 MLC	GND	GND	GND	GND
M.2 2242 PCIE SSD / Intel Optane	16GB Optane PCIe M.2 2242-S3	GND	NC	GND	GND

WWAN_CFG0	WWAN_CFG3	CACHE_DTCT_SW	-WWAN_SSD_DTCT	
L	L	H	L	SSD
L	H	L	H	PCIE WWAN
H	L	L	H	USB2 WWAN
H	H	L	H	

WWAN_CFG1	CACHE_DTCT_SW	-WWAN_PE_DTCT
L	H(SSD插入)	L(SATA interface) -> SATA SSD
NC	H(SSD插入)	H(PCIE interface) -> PCIE SSD / Optane Memory
L	L(NC or 插入WWAN卡)	H(PCIE interface) -> USB WWAN/ PCIE WWAN
NC	L(NC or 插入WWAN卡)	H(PCIE interface) -> 沒插任何卡

- CACHE_DTCT_SW : H , plug-in SSD or nothing in NGFF Slot. Switch to IR_CAMERA
- CACHE_DTCT_SW : L , plug-in USB/PCIE WWAN in NGFF Slot. Switch to WWAN

This is HW behavior , don't need SW control

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Title		
WWAN NGFF		
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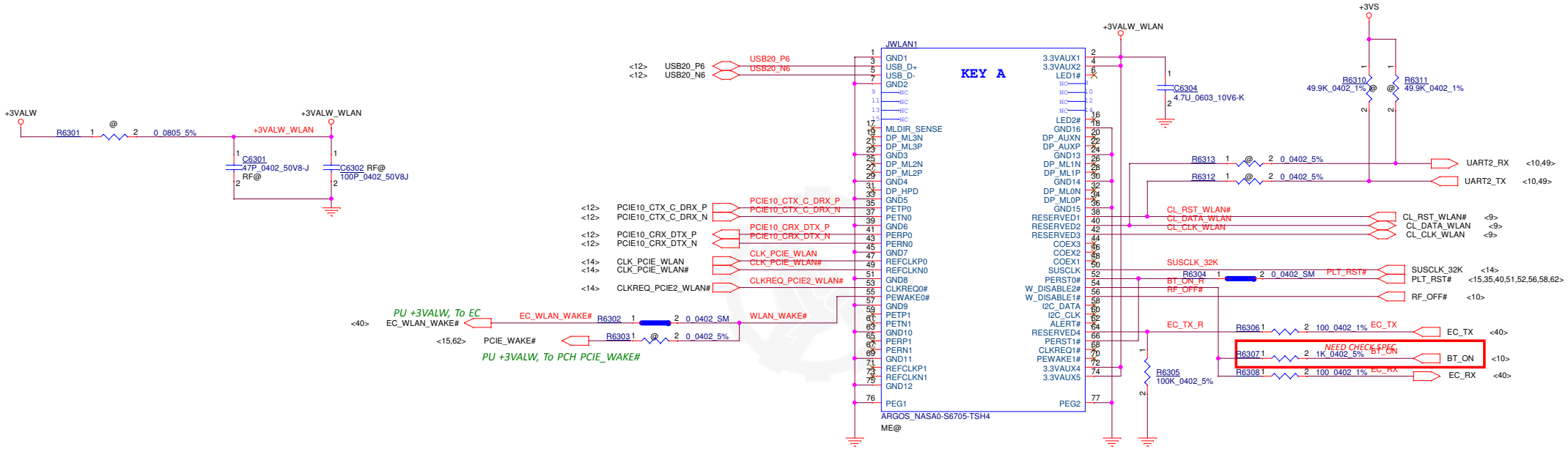
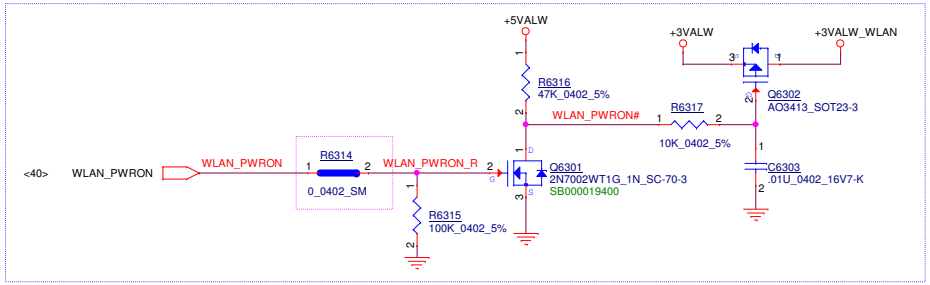
+5VALW +5VALW <38,39,40,50,52,64,66,67,71,72,84,86,87,88,89,90,92,94,95>

+3VALW +3VALW <6,9,10,12,15,19,39,40,43,45,46,49,52,58,60,62,64,65,67,72,83,84,85,96>

TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR





Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: WLAN NGFF CONN.

Size	Document Number	Rev
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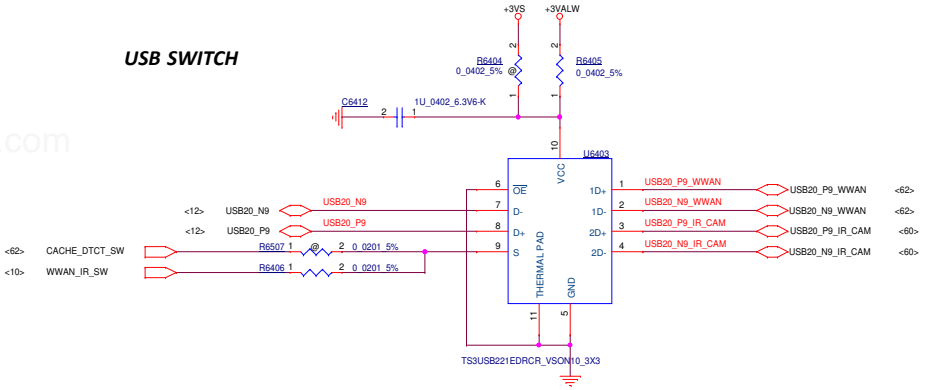
USB HUB

+5VALW +5VALW <38,39,40,50,52,63,66,67,71,72,84,86,87,88,89,90,92,94,95>

+3VS +3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,65,66,72,86,87>

USB SWITCH



- CACHE_DTCT_SW : H , plug-in SSD or nothing in NGFF Slot. Switch to IR_CAMERA
- CACHE_DTCT_SW : L , plug-in USB/PCIE WWAN in NGFF Slot. Switch to WWAN

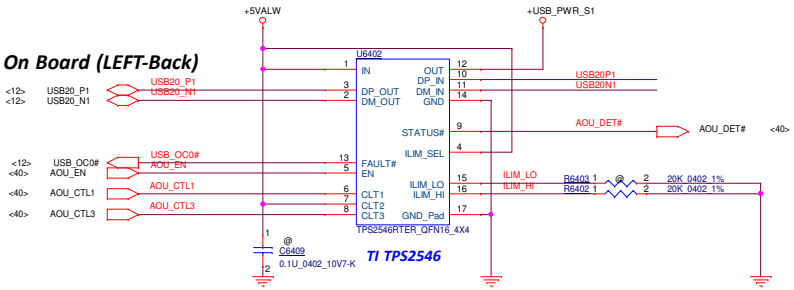
This is HW behavior , don't need SW control

8.4 Device Functional Modes

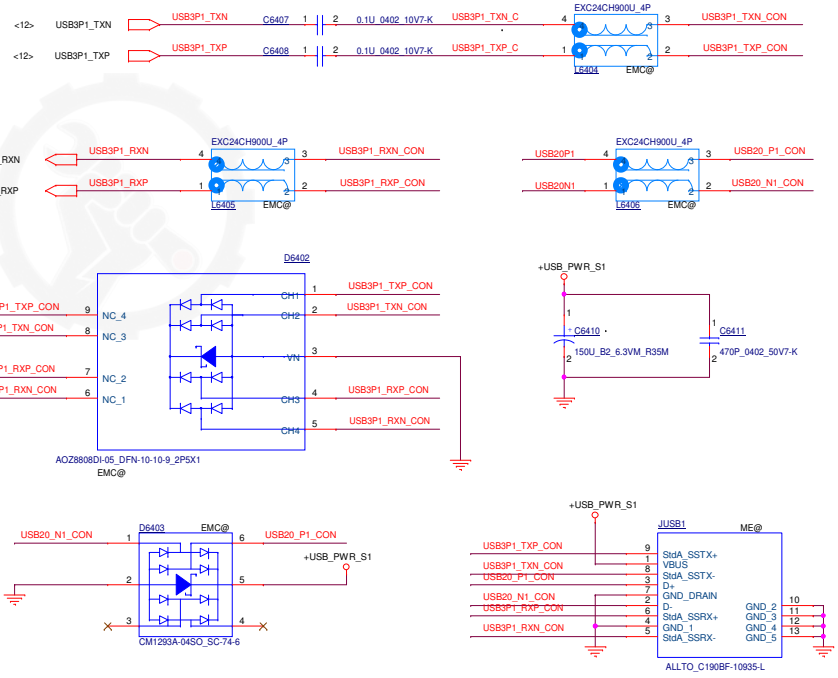
Table 1. Truth Table

S	OE	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

On Board (LEFT-Back)



CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active



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Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: USB AOU/USB SWITCH

Size	Document Number	Rev
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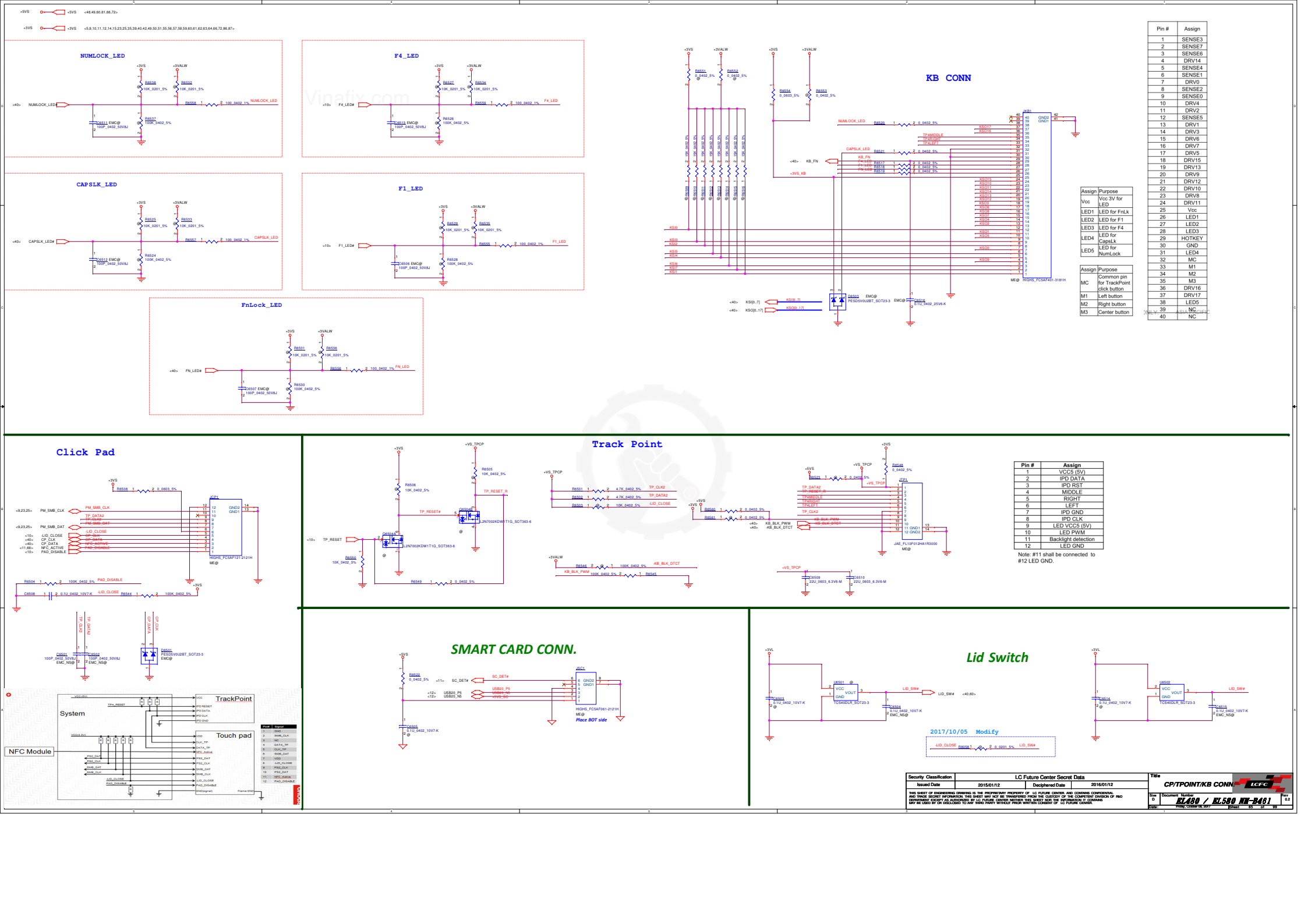

Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLk
LED5	LED for NumLock

Assign	Purpose
MC	Commom pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Pin #	Assign
1	VCC5 (5V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND

Note: #11 shall be connected to #12 LED GND.

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Title	CP/TPOINT/KB CONN
Size D	Document Number KL480 / KL580 MB-B461
Date: Friday, October 06, 2017	Sheet 65 of 99

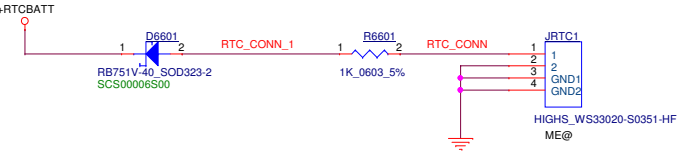
+RTCBATT +RTCBATT <14,80>

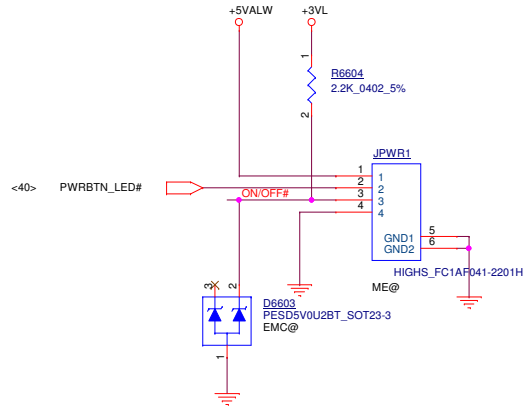
+5VS +5VS <48,49,60,61,65,72>

+3VS +3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,72,86,87>

+3VALW +3VALW <6,9,10,12,15,19,39,40,43,45,46,49,52,58,60,62,63,64,65,67,72,83,84,85,96>

RTC CONN.

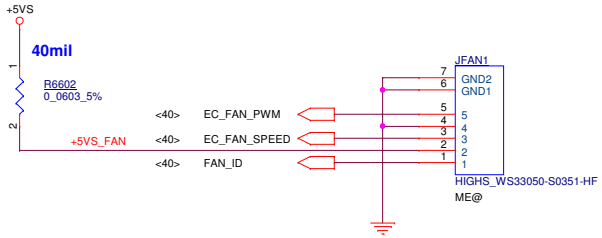




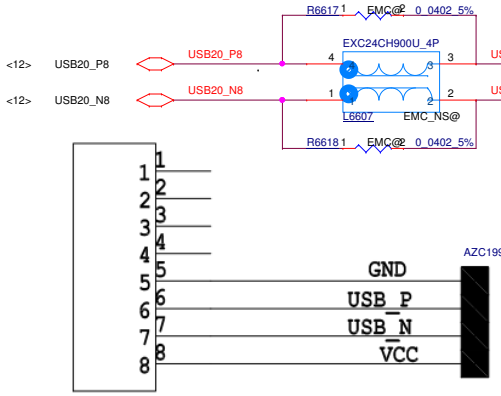
PWRBTN FOR DENUG

Bottom Side

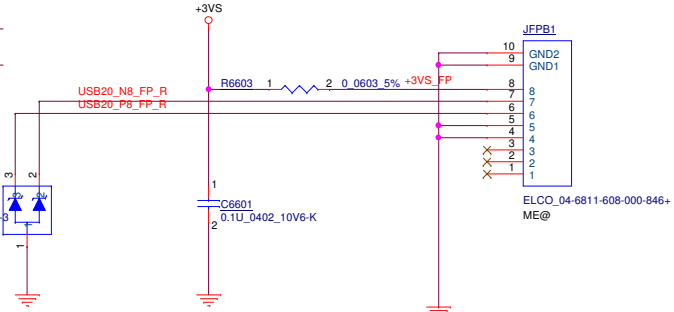
FAN CONN.



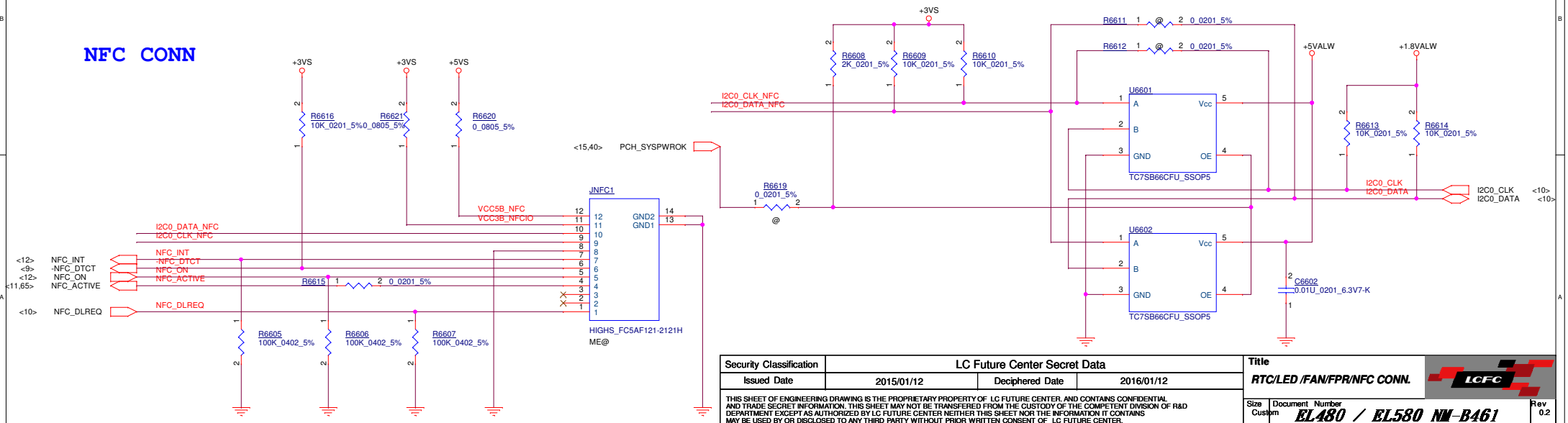
CO-LAY



FingerPrint CONN.



NFC CONN



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: RTC/LED /FAN/FPR/NFC CONN.

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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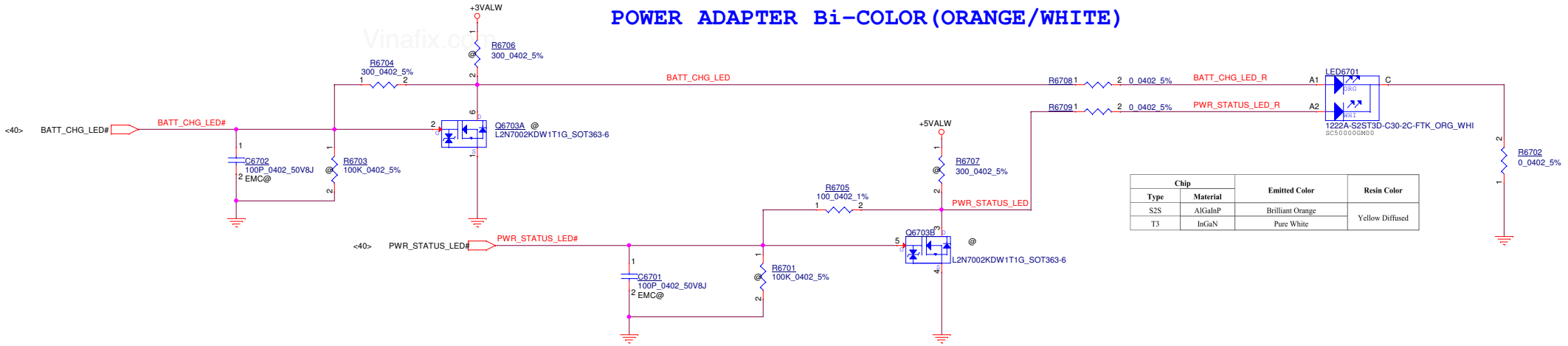
POWER ADAPTER Bi-COLOR(ORANGE/WHITE)



Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: POWER ADAPTER LED

Size	Document Number	Rev
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Title

LCFC

Size	Document Number	Rev
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THP2

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title

LCFC

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Title

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LCFC

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Custom	EL480 / EL580 NM-B461	0.2

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+1VALW +1VALW <14,19,39,96>

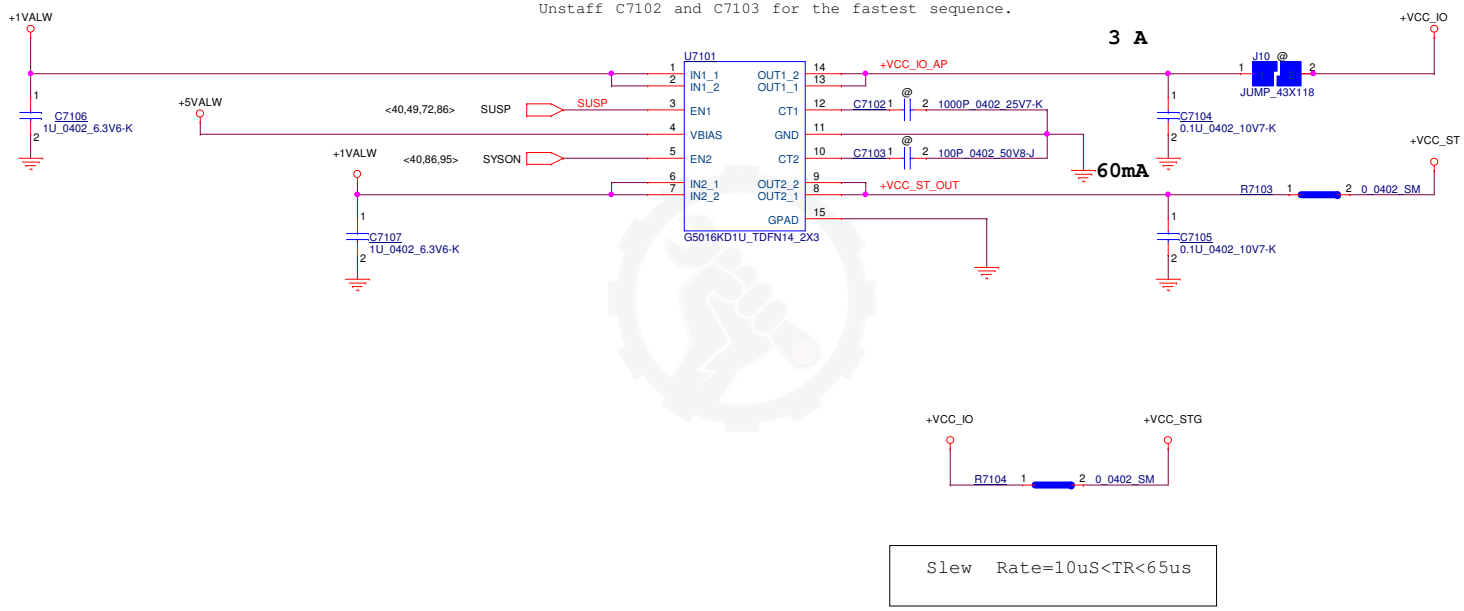
+VCC_STG +VCC_STG <8,16,18>

+VCC_IO +VCC_IO <5,11,18,21>

+5VALW +5VALW <38,39,40,50,52,63,64,66,67,72,84,86,87,88,89,90,92,94,95>

+VCC_ST +VCC_ST <8,15,16,18,21,87>

+1VALW to +VCC_IO_AP & +VCC_ST



Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: VCCIO/VCCSTG/VCCST/+VCC

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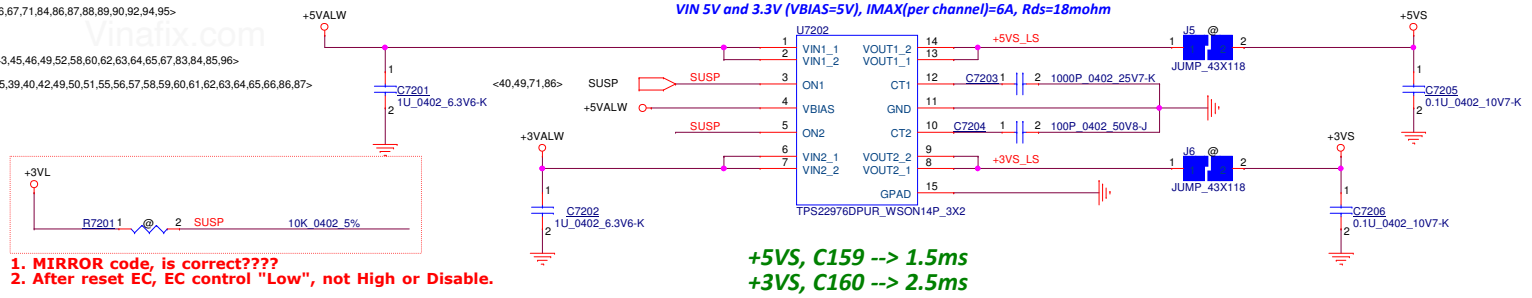
Smart Switch
+5VALW To +5VS
+3VALW To +3VS

+5VALW <38,39,40,50,52,63,64,66,67,71,84,86,87,88,89,90,92,94,95>
+5VS <48,49,60,61,65,66>
+3VALW <6,9,10,12,15,19,39,40,43,45,46,49,52,58,60,62,63,64,65,67,83,84,85,96>
+3VS <5,9,10,11,12,14,15,23,25,35,39,40,42,49,50,51,55,56,57,58,59,60,61,62,63,64,65,66,86,87>
+3VALW_PCH <8,9,10,11,12,19>
+3VL <19,40,65,66,80,82,83,84>
+1VALW_SUS <19>



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: DC V TO VS/ V-PCH

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Title: **BLANK**

Size	Document Number	Rev
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Title: **BLANK**

LCFC

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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Security Classification	LC Future Center Secret Data		
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Title: **BLANK**

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
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Title

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Size	Document Number	Rev
Custom	*EL480 / EL580 NM-B461*	0.2

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Security Classification	LC Future Center Secret Data		
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Title: **BLANK**

Size	Document Number	Rev
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For ME GND hole Screw Hole

H10 PAD_C7P0D3P3
H16 PAD_C8P0D5P5
H17 PAD_C8P0D5P5
H11 PAD_C8P0D2P2
H12 PAD_C8P0D2P3
H13 PAD_C8P0D2P2

For CPU and GPU

H5 PAD_C5P0D2P2
H8 PAD_C6P0D3P2
H9 PAD_C6P0D3P2
H1 PAD_C6P0D3P2
H2 PAD_C6P0D3P2
H3 PAD_C6P0D3P2
H4 PAD_C6P0D3P2
H7 PAD_C6P0D3P2

For KB

H23 PAD_C8P0D2P3
H24 PAD_C8P0D2P3
H25 PAD_C8P0D2P3X2P7

H14 PAD_C8P0D2P3
H15 PAD_C6P0D2P2
H18 PAD_C5P5D2P2
H19 PAD_C6P0D2P2
H20 PAD_C7P0D3P2
H21 PAD_C7P0D3P2
H22 PAD_CT4P8D2P2
H26 PAD_O2P3X2P8D2P3X2P8N
H27 PAD_O2P3X2P6D2P3X2P6N
H28 PAD_C3P0D3P0N
H6 PAD_C5P5D2P2
H29 pad_o2p3x1p6d1p7x1p0
H30 pad_o2p3x1p6d1p7x1p0
H31 pad_r1p3x2p3d0p7x1p7

ZZZ1
NM-B461
PCB@

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: SCREW HOLE

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/12/31

Title

PLM BOM

Size	Document Number	Rev
Custom	EL480 / EL580 NM-B461	0.2

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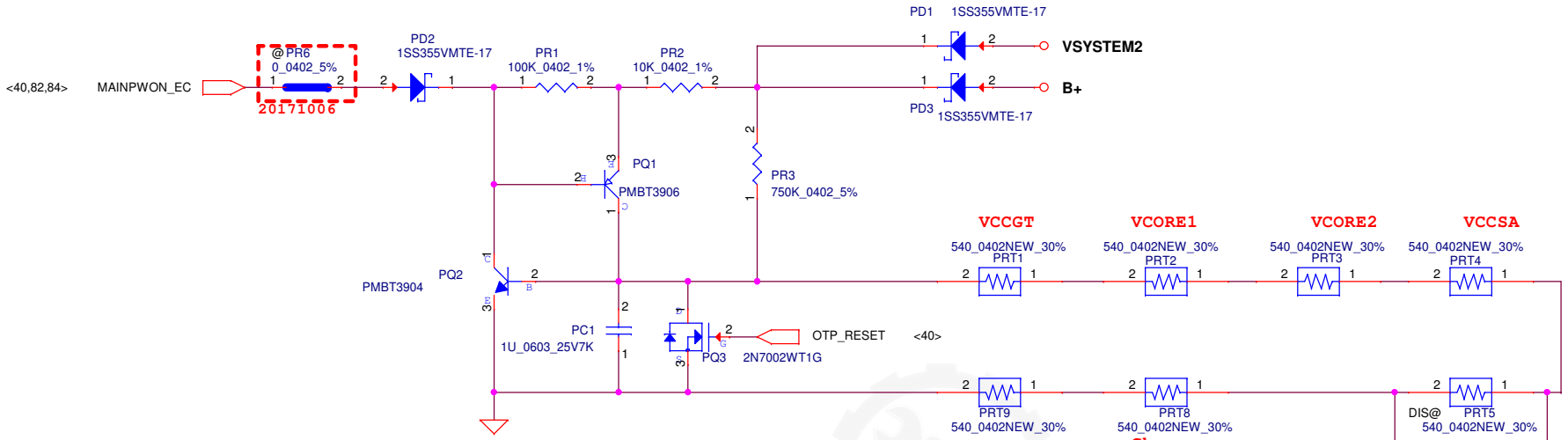
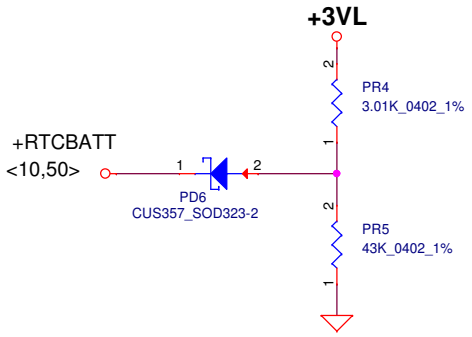


RTC Battery



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	VIN Detector	
Size: Custom	Document Number: KENOBI	Rev: 2.0
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Title: *VIN Detector*		
Size: B	Document Number: KENOBI	Rev: 2.0
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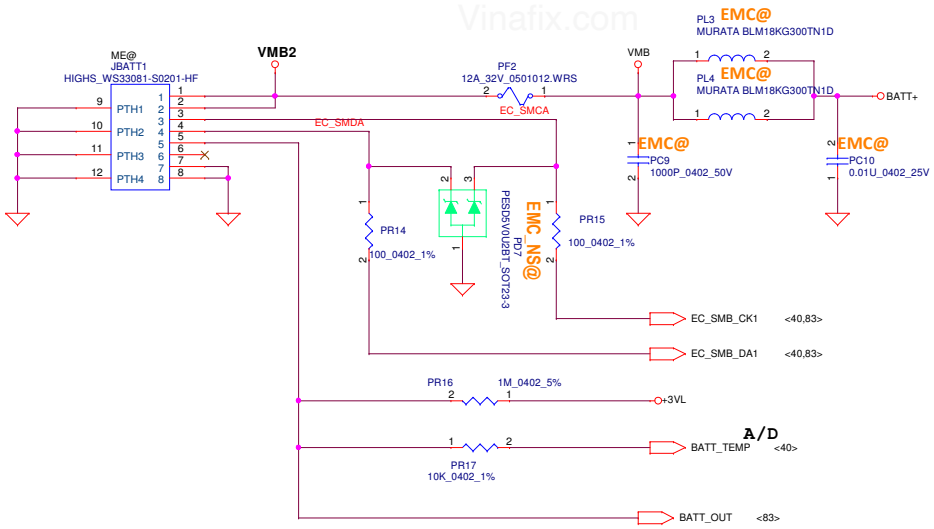
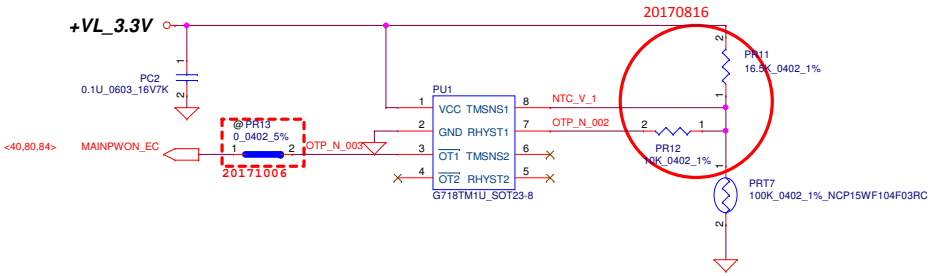


PRT7 under CPU bottom side for CPU thermal protection. This is for thermal team request.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	BATTERY CONN/OTP		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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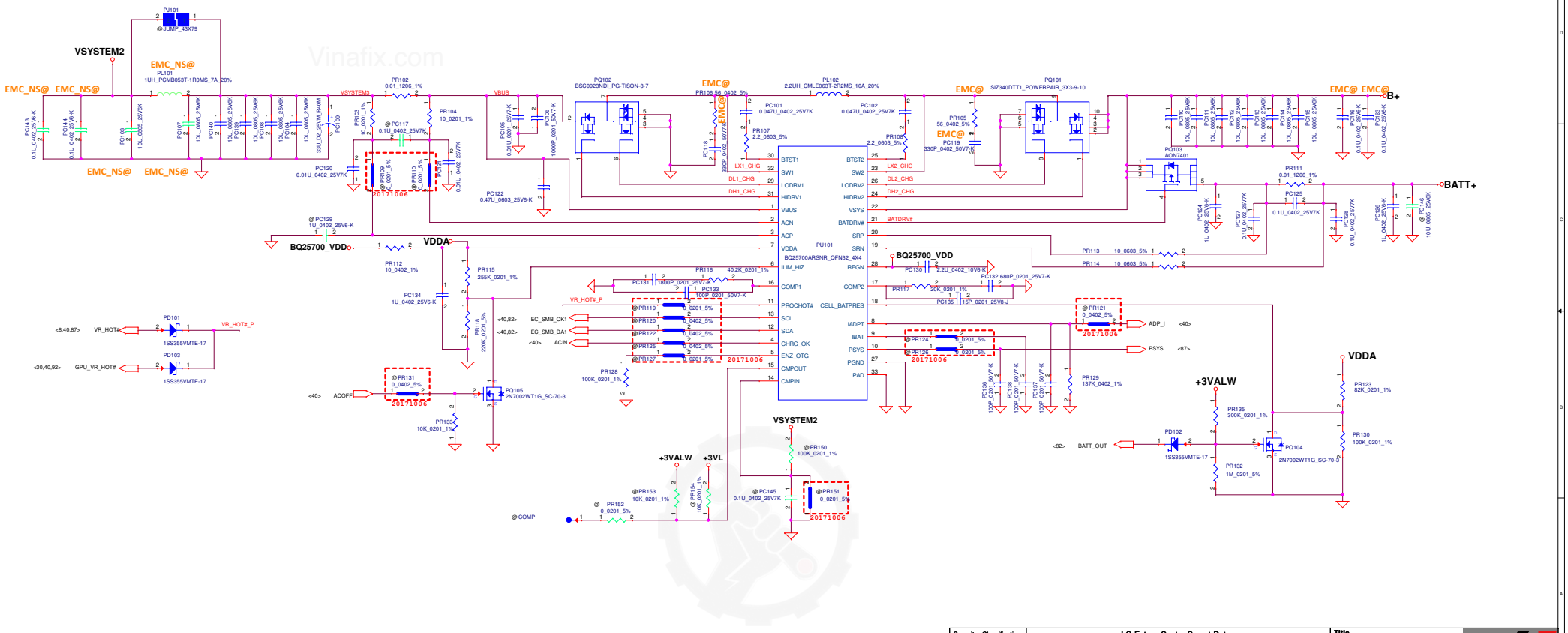

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: CHARGER

Size	Document Number	Rev
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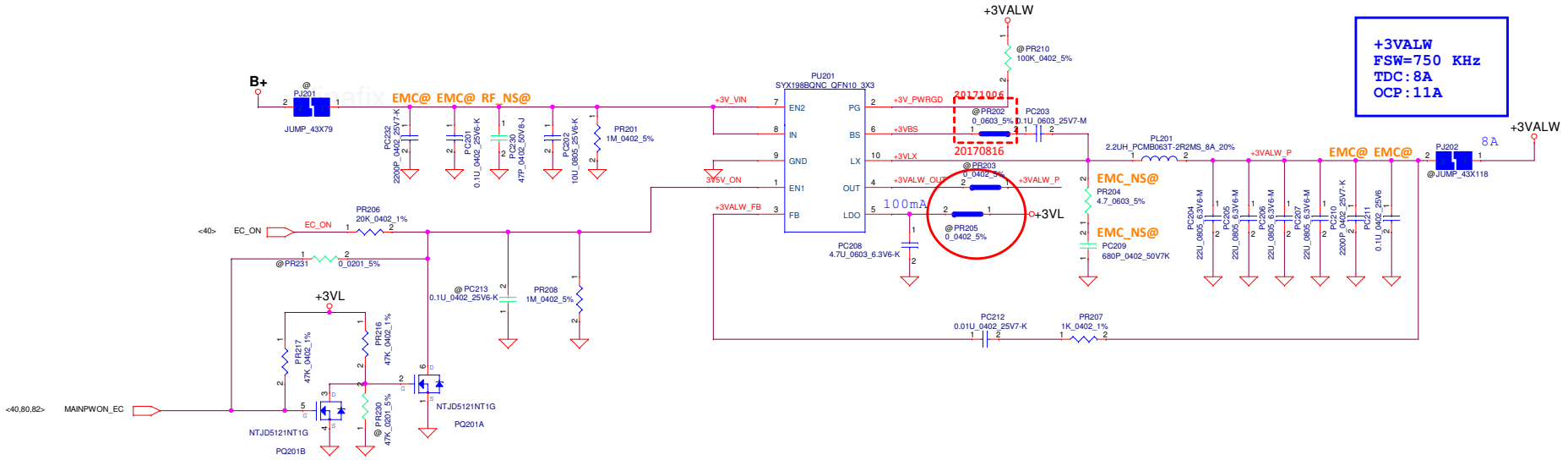

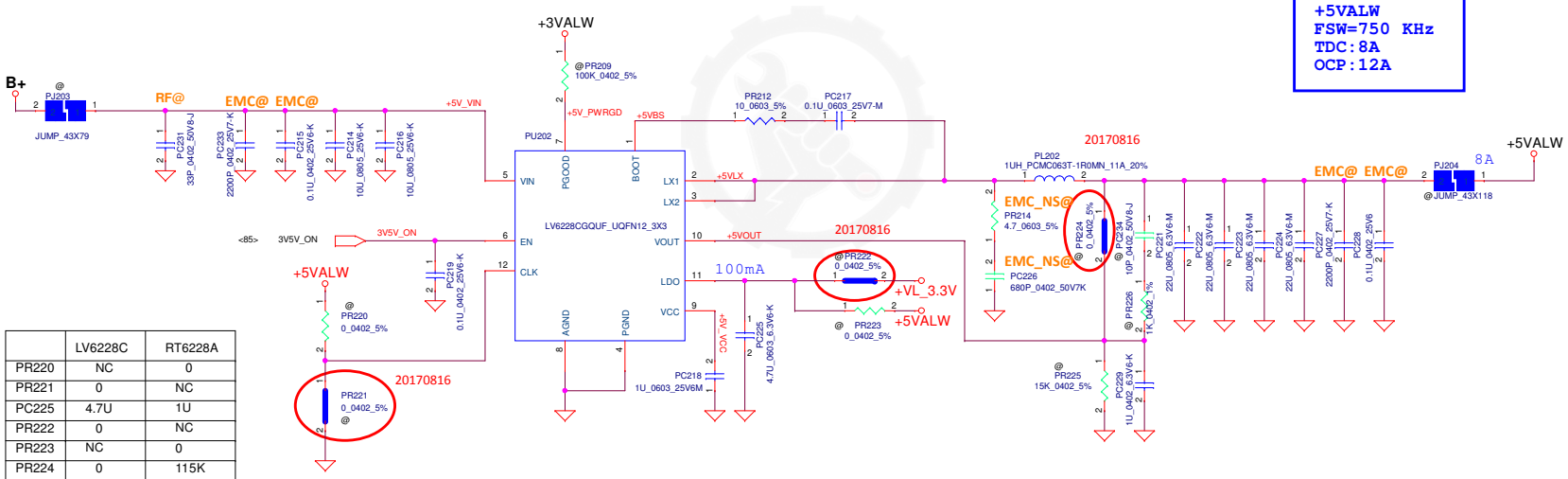

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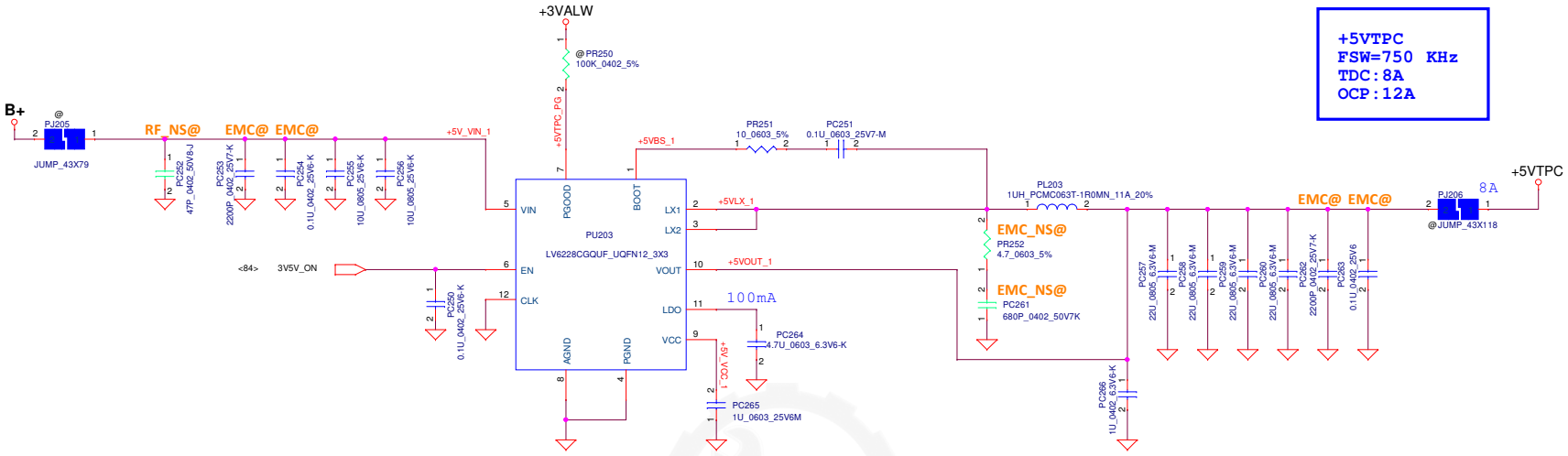
PR220	NC	0
PR221	0	NC
PC225	4.7U	1U
PR222	0	NC
PR223	NC	0
PR224	0	115K
PR225	NC	15K
PC234	NC	10P
PR226	NC	1K

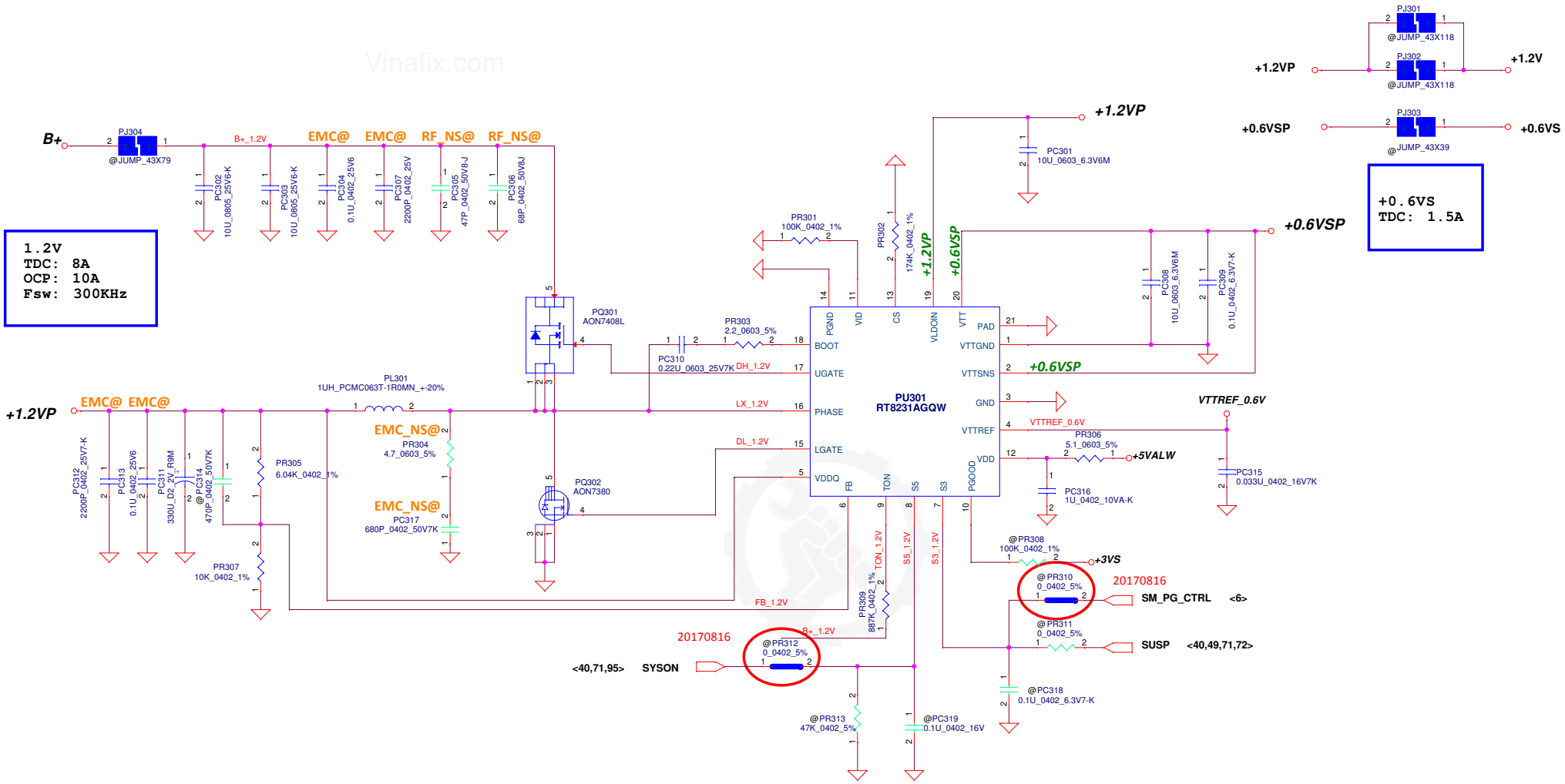
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	3VALWP/5VALWP		
Size	Document Number	KENOBI	Rev 2.0
Custom			
Date:	Friday, October 06, 2017	Sheet	84 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	+5VTPC		
Size: Custom	Document Number: KENOBI		Rev: 2.0
Date: Friday, October 06, 2017	Sheet 85 of 99		



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.2V/+0.6VS

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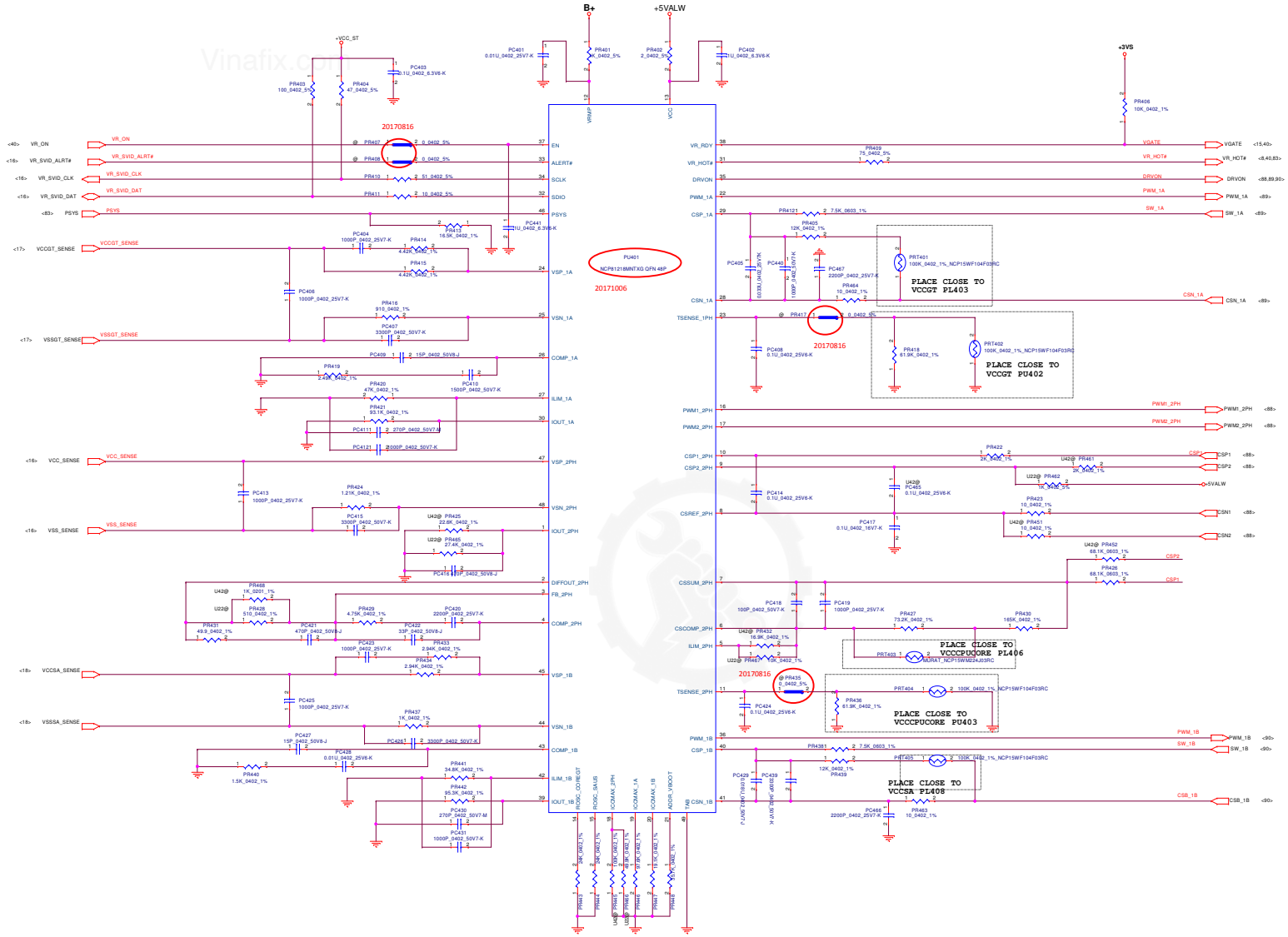

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title: IMVP8

Size: D | Document Number | Rev: 2.0

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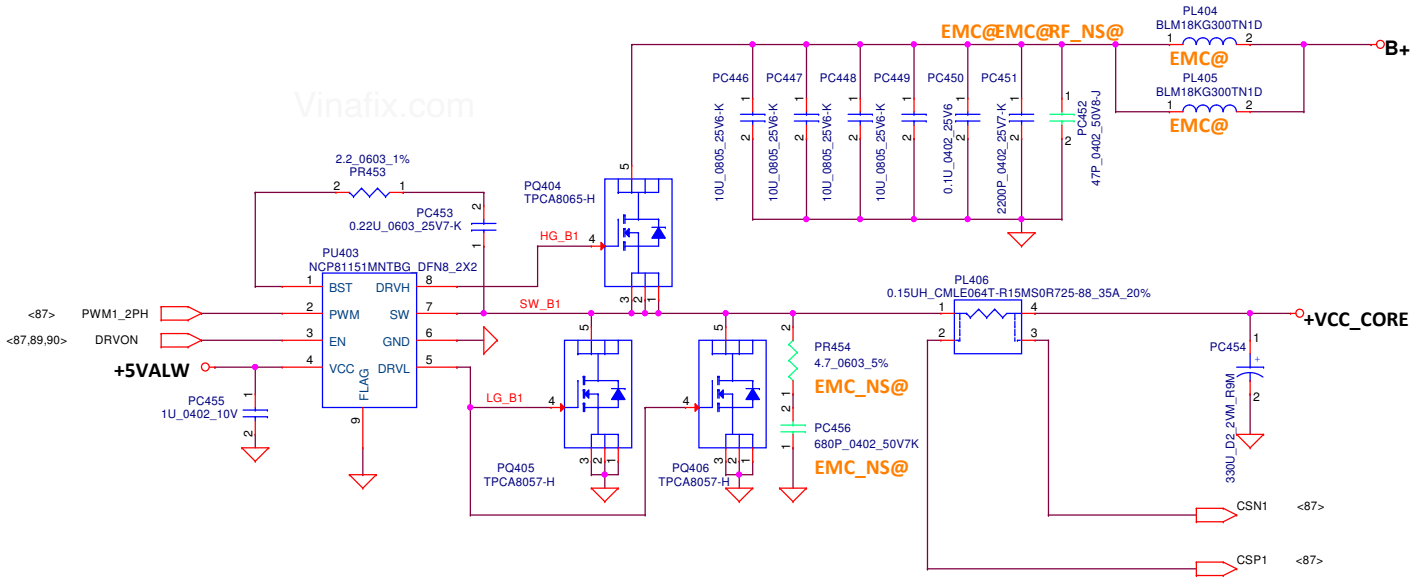


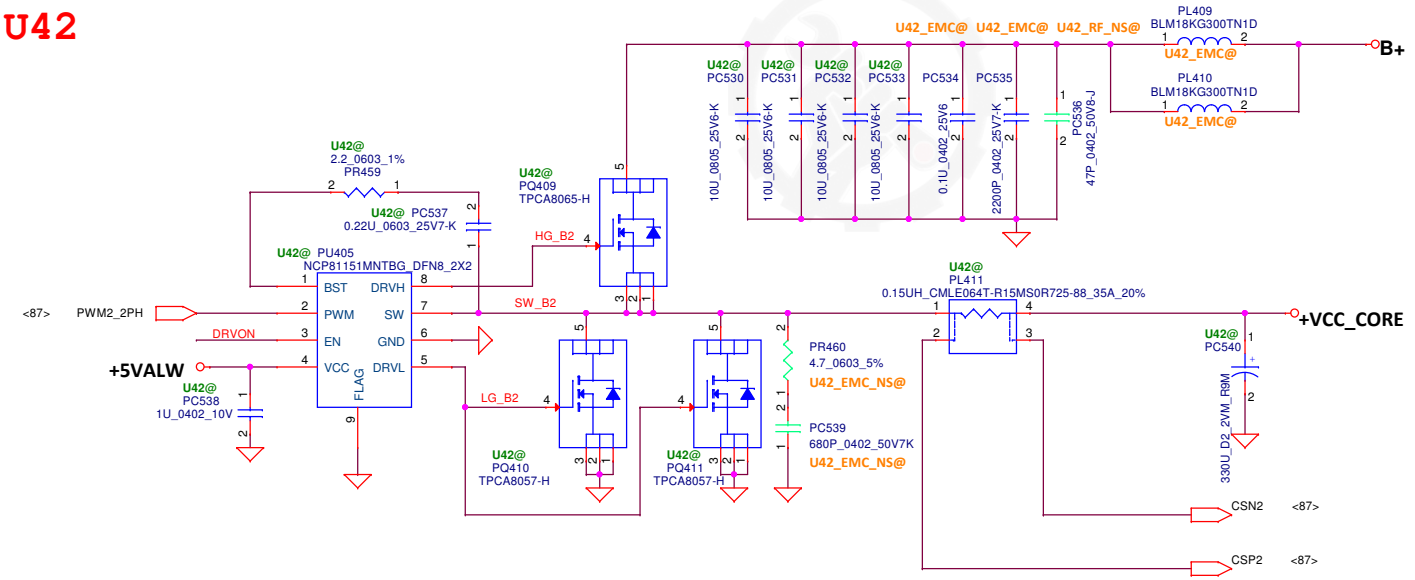
For U42

+VCC_CORE
TDC= 42A
IccMAX=64A
OCP=70A

For U22

+VCC_CORE
TDC= 21A
IccMAX=31A
OCP = 36A

For U42



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

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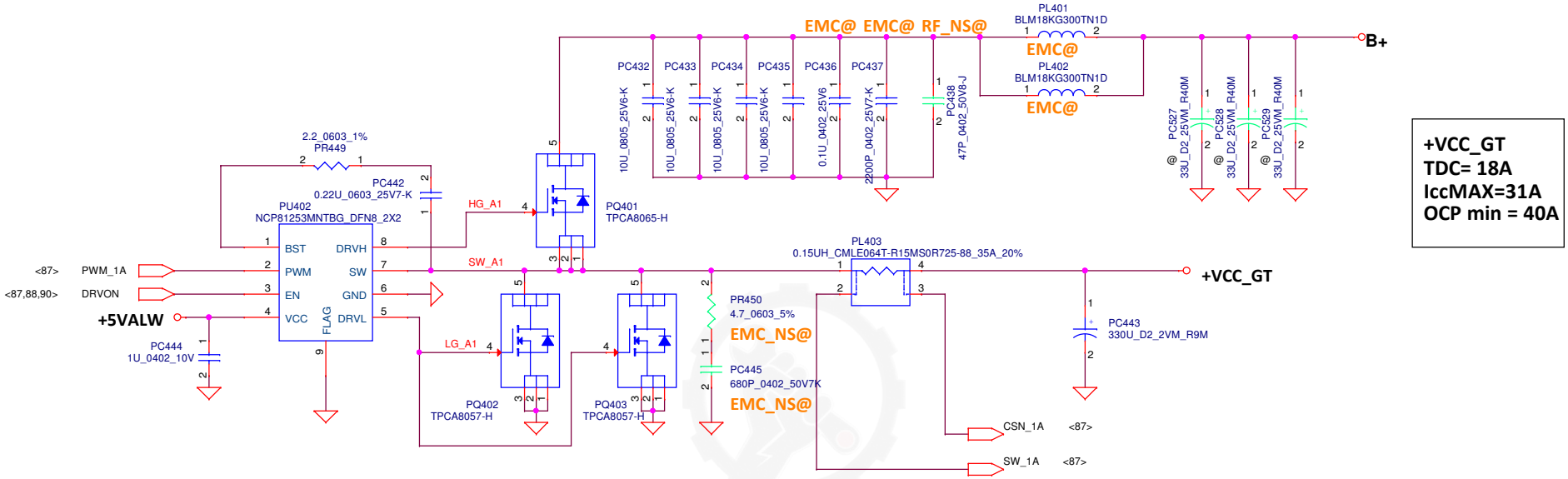

Title	+VCC_GT		
Size: Custom	Document Number: KENOB I		Rev: 2.0
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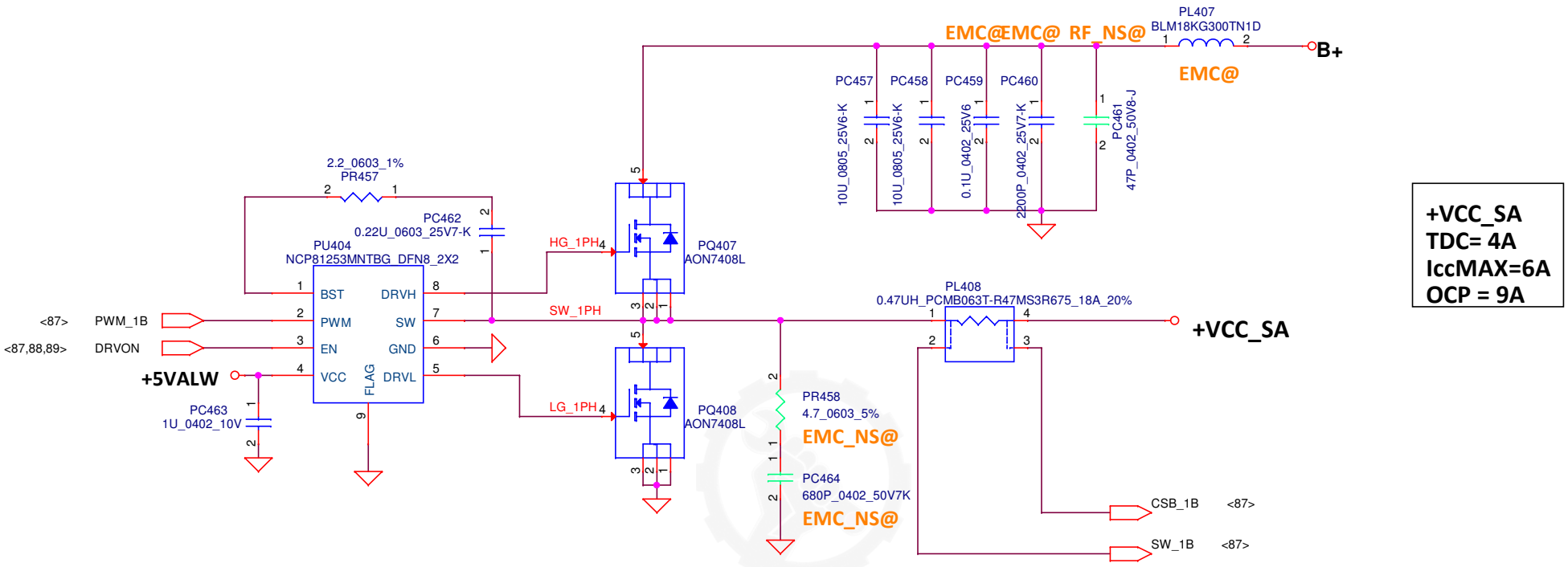

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_SA*

LCFC

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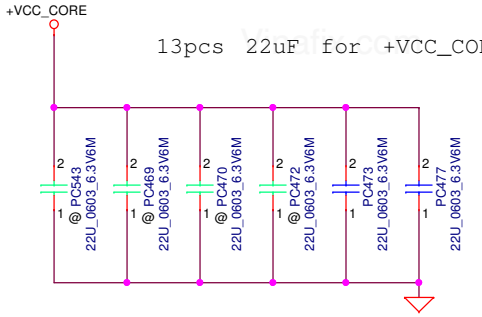
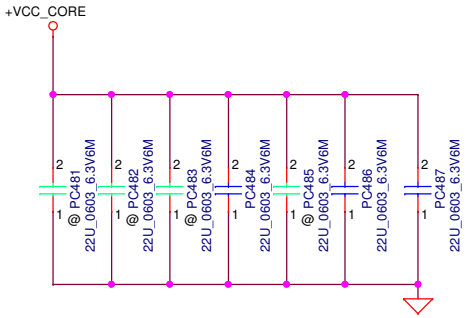
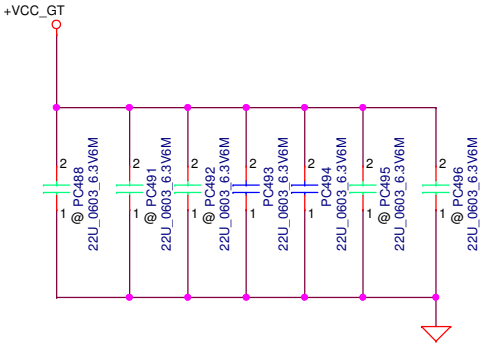
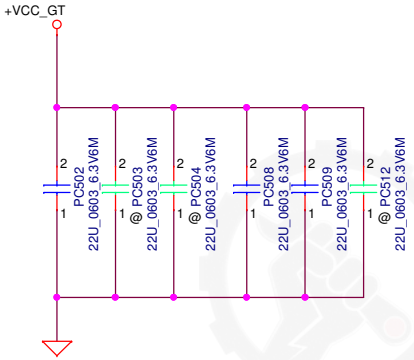
13pcs 22uF for +VCC_CORE



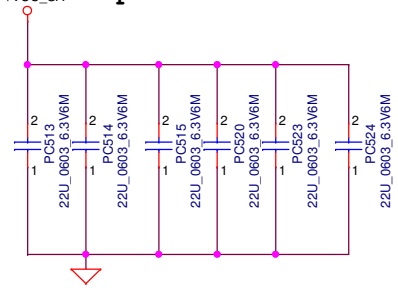


13pcs 22uF for +VCC_GT





6pcs 22uF for +VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

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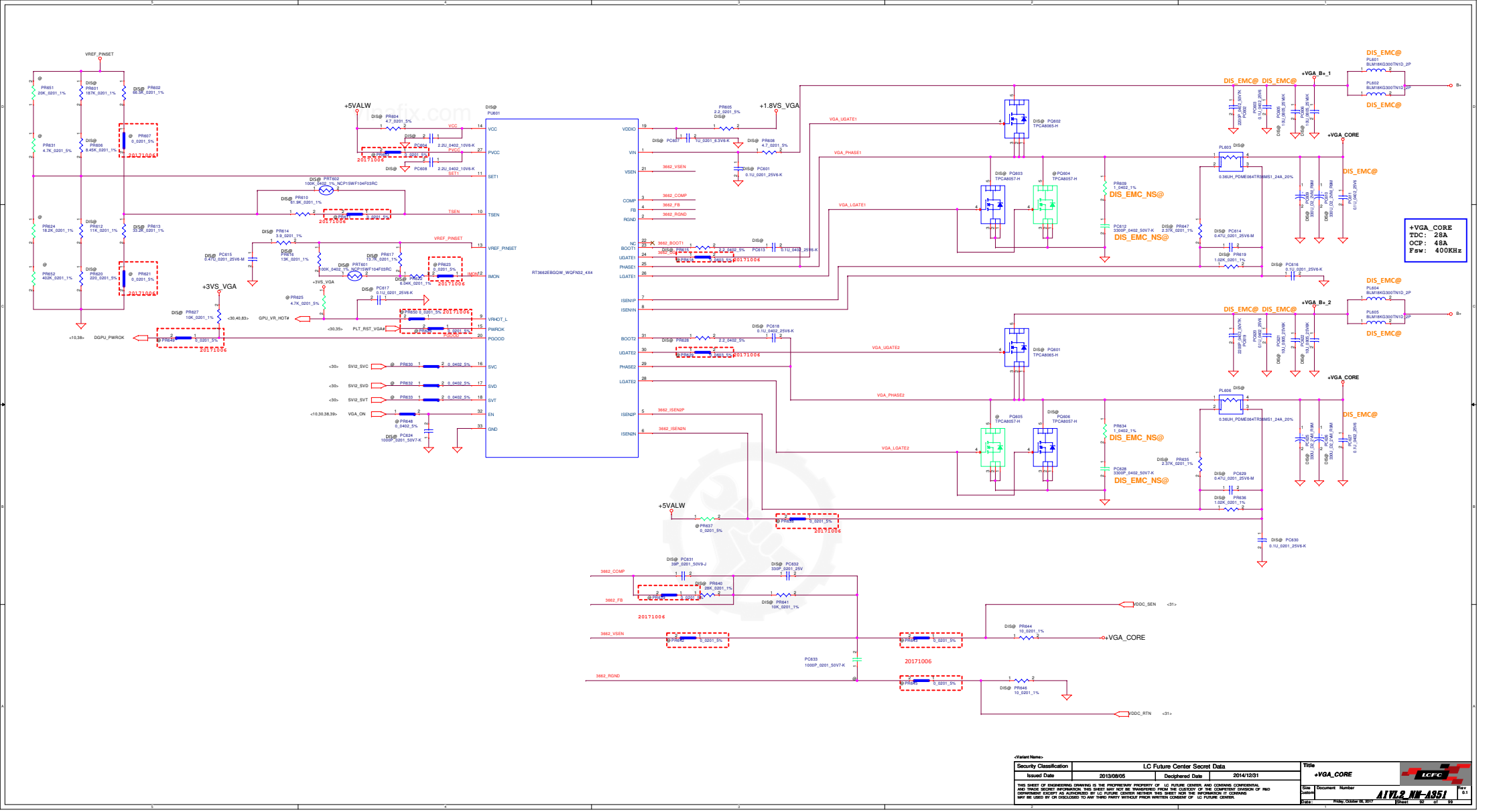

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Title: +VGA_CORE

Size: Custom | Document Number: A1VL2_MB_A351 | Rev: 0.1

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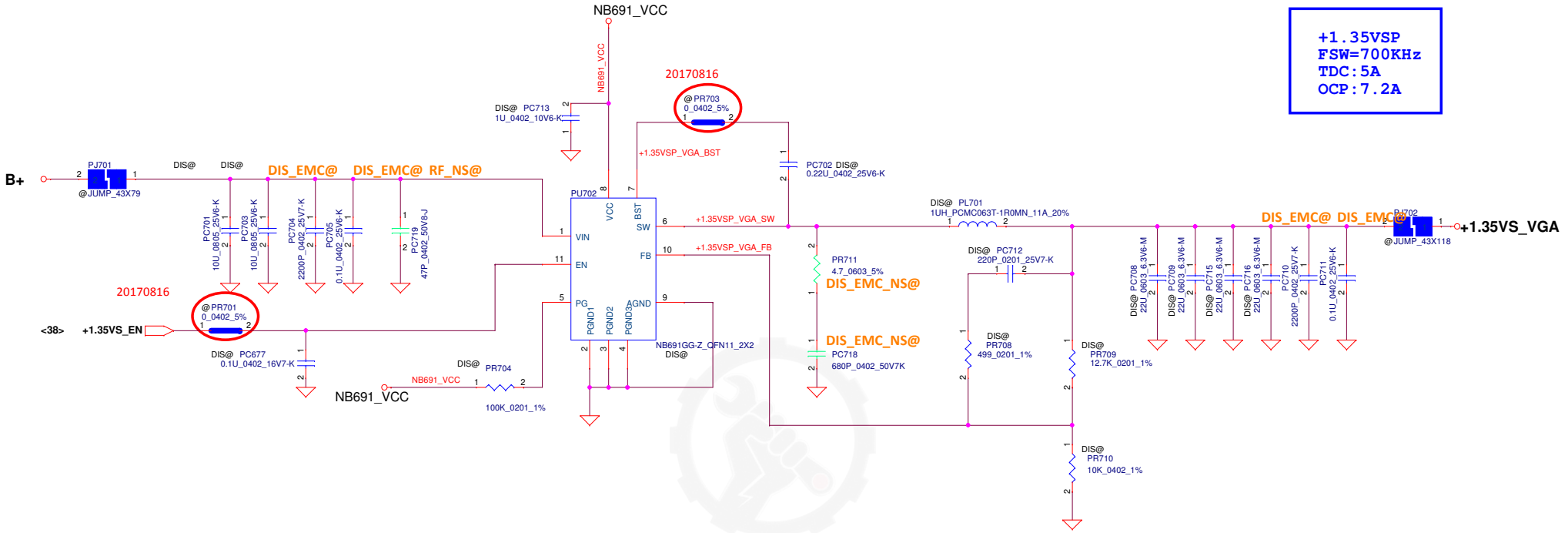

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+1.35VSP*

Size	Document Number	Rev
Custom	*AIVE1_NM-A211*	0.1

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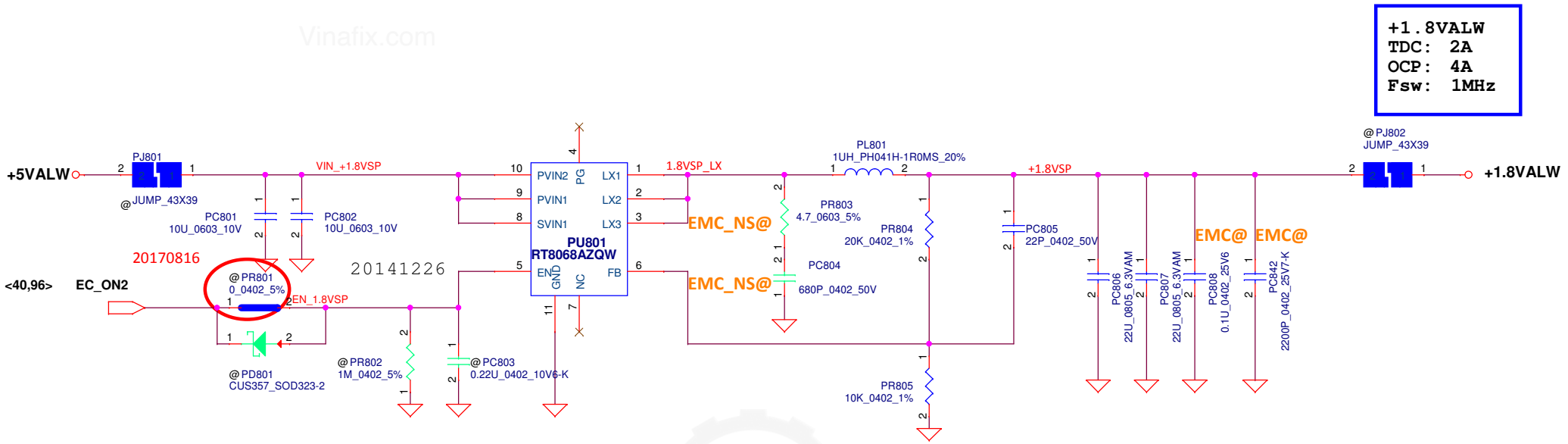

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.8VALW		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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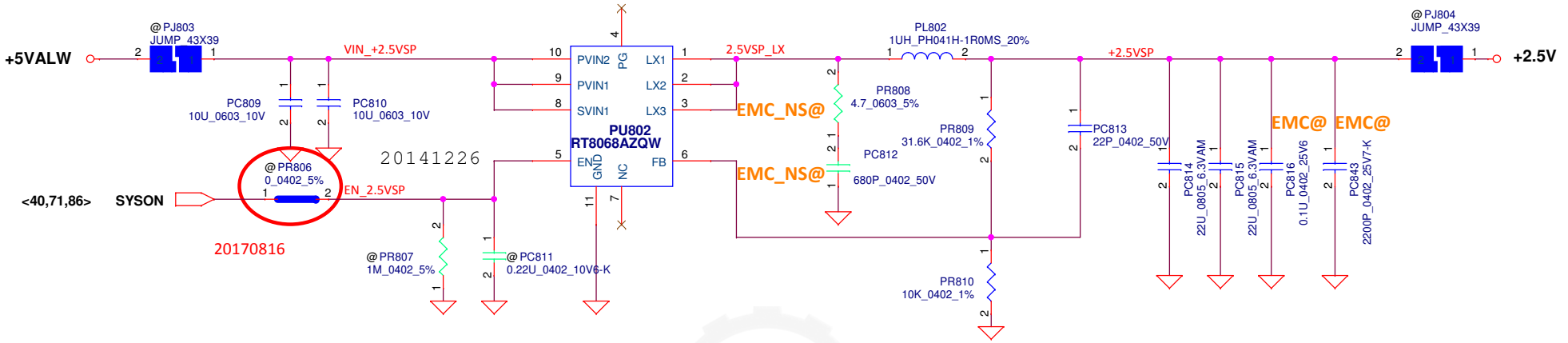

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+2.5V		
Size	Custom	Document Number	KENOBI
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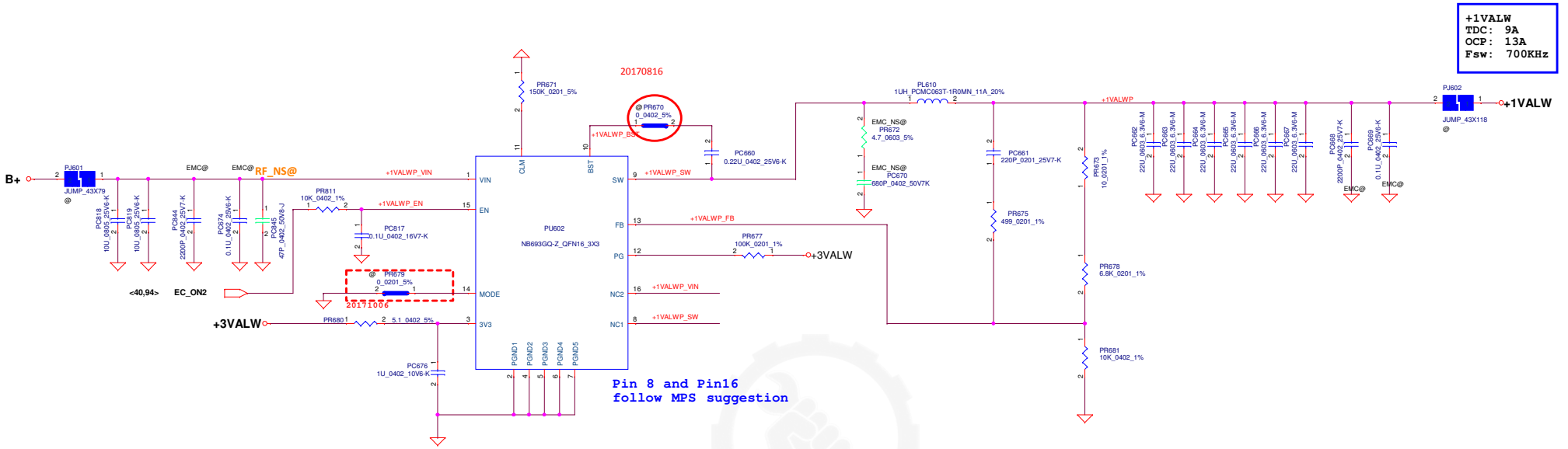

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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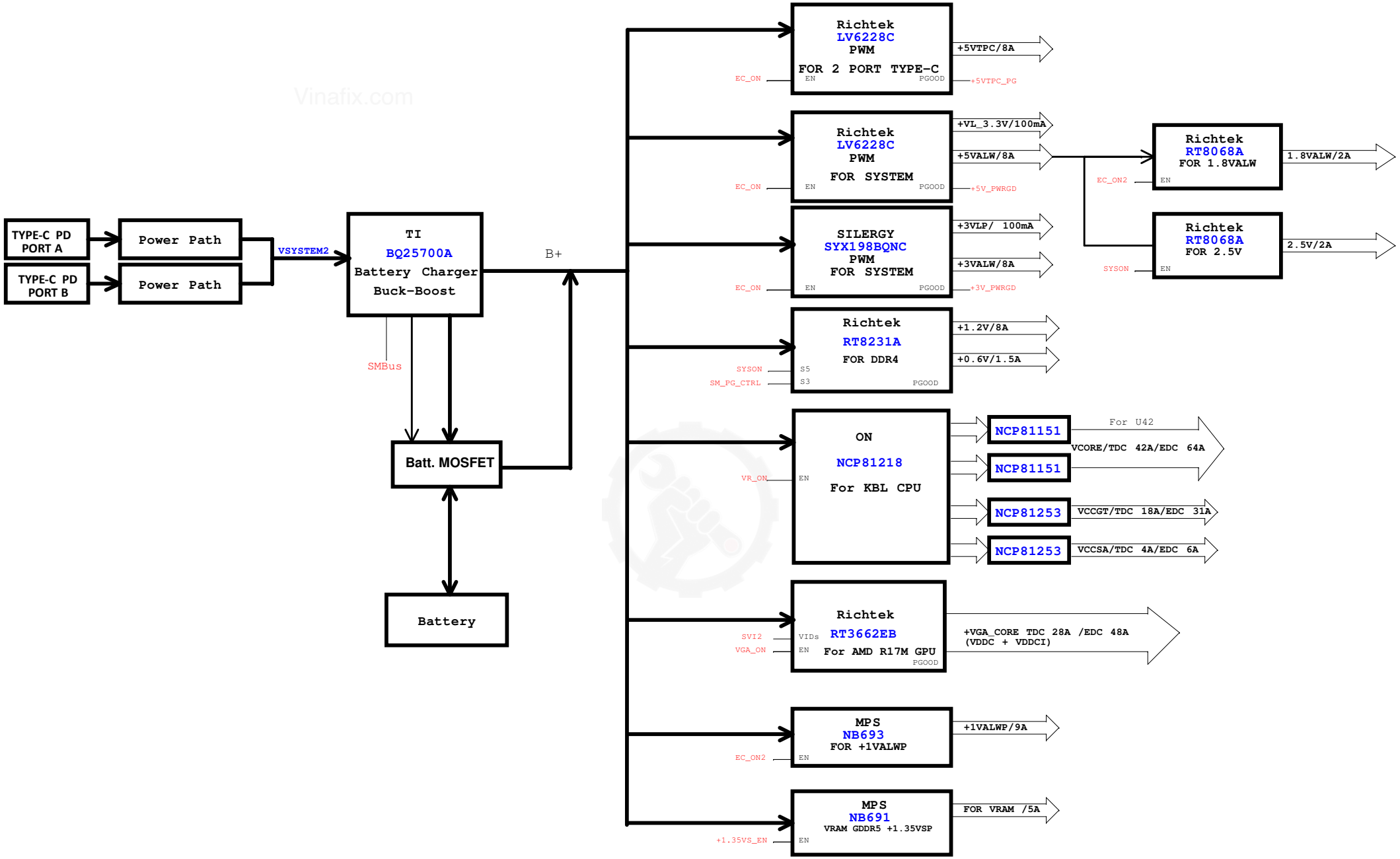
Size: Custom	Document Number: KENOB 1	Rev: 2.0
Date: Friday, October 06, 2017	Sheet 96 of 99	



Security Classification	LC Future Center Secret Data
Issued Date	Deciphered Date

Title: *Power Block Diagram*

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: XXXX

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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Security Classification	LC Future Center Secret Data		
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Title

XXXX

LCFC

Size	Document Number	Rev
Custom	SKYWALKER	2.0

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