

# LCFC Confidential


## NANO G ACL CG521 M/B Schematics Document

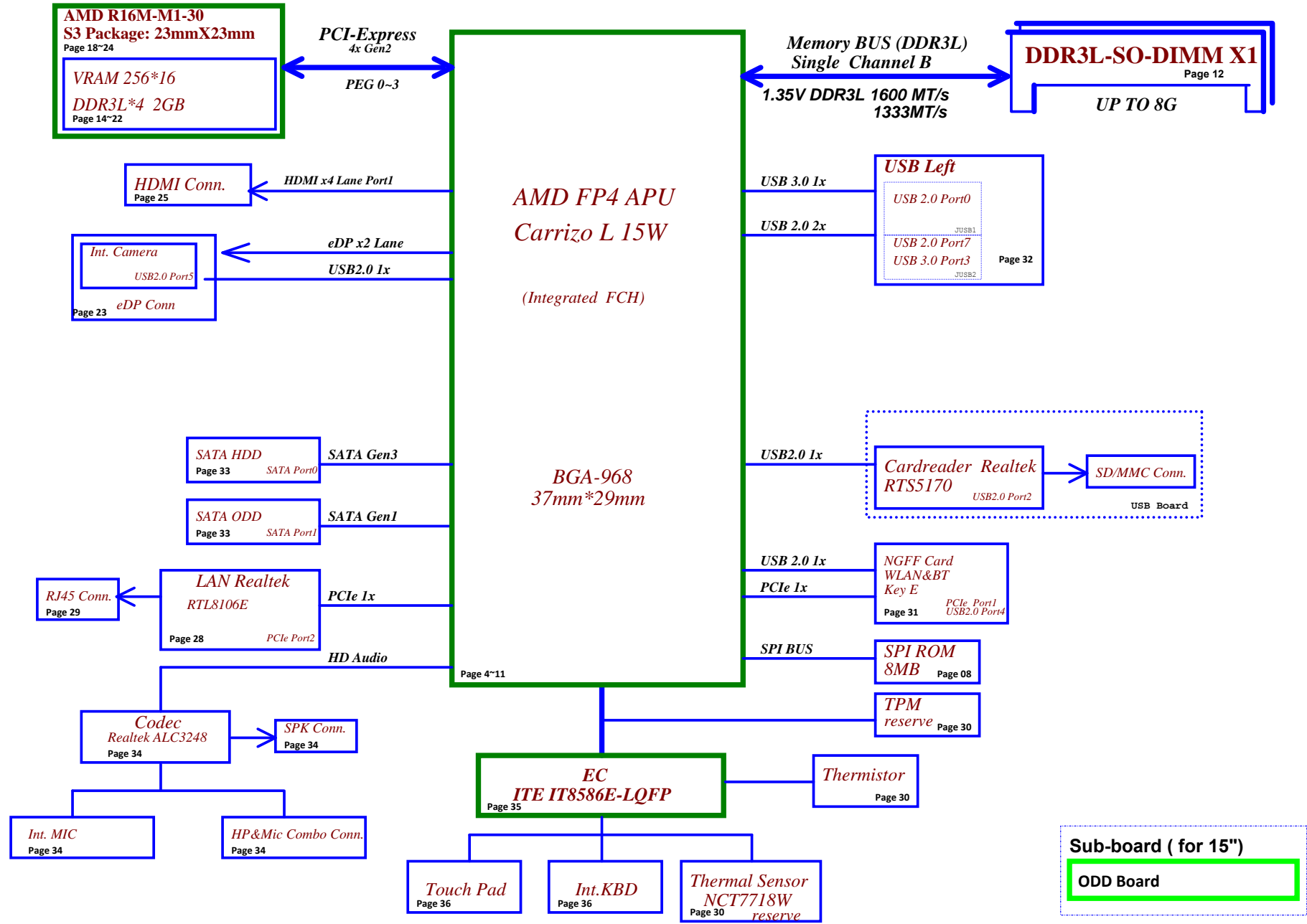
AMD FP4 Carrizo L SOC with DDRIIL

AMD R16M-M1-30

2016-02-24

REV: 1.0

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Issued Date	2013/08/15	Deciphered Date	2013/08/15	<b>Cover Page</b>	Size	Rev
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**Voltage Rails ( O --> Means ON , X --> Means OFF )**

State	power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+1.35V (+VSYSTEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.675VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	X	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID0	BOARD_ID1	BOARD_ID2	Function
	0: 14''	0: Dis		
	1: 15''	1: UMA		

**USB Port Table for CarrizoL**

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	RIGHT USB (2.0)
		1	N/A
		2	Card Reader
		3	Touch screen
EHCI1		4	Blue Tooth
		5	Camera
		6	LEFT USB (3.0)
xHCI		1	LEFT USB (3.0)

**USB Port Table for Carrizo**

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	RIGHT USB (2.0)
		1	N/A
		2	Card Reader
		3	Touch screen
		4	Blue Tooth
xHCI		5	Camera
		2	LEFT USB (3.0)
		3	LEFT USB (3.0)

**BOM Structure Table**

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_CZ@	EMC Carrizo APU part
EMC_15@	EMC 15 part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
CZ@	Carrizo Part
CZL@	CarrizoL part
CZPX@	Carrizo Discrete Part
CZLPX@	CarrizoL Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
CZLUMA@	CarrizoL UMA Part
CZUMA@	Carrizo UMA Part
SIVCD@	SIV COST down material
HDMI@	HDMI Logo

**SMBUS Control Table**

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	HDMI Convert reserve
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V	X		X	X	V	V APU_SIC APU_SID 1.8VS for C2 3VS for C21	X	V
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

**PCIe PORT LIST**

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	CZL GPU CZ GPU
	1	
	2	
	3	
	4	N/A
	5	
	6	
7		

VRAM

**EC SM Bus1 address**

**EC SM Bus2 address**

Device	Address	Device	Address
Battery	0X16	Thermal Sensor	1001_100xb(reserve)
Charger	0001 0010 b	GPU	0x41(default)
		APU SB-TSI	relate to F3x1E4[SbiAddr] or Address Select Pins setting
		HDMI Convert	RSVD

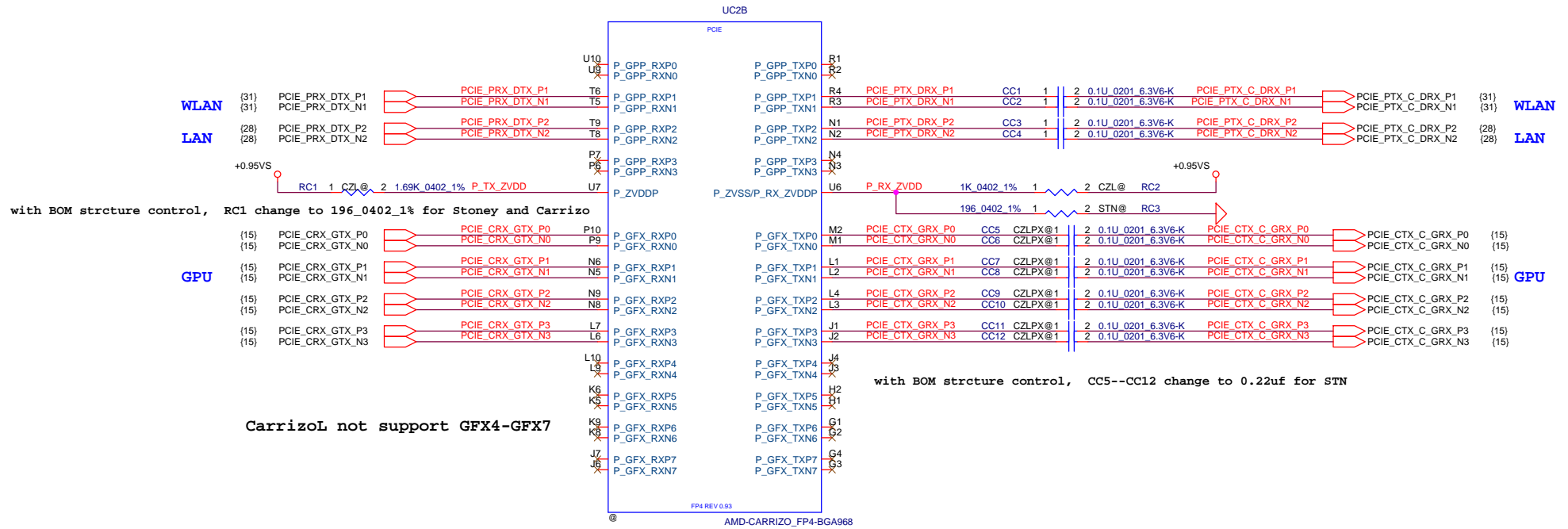
**APU SM Bus address**

Device	Address
DDR DIMMA	0xA0h
DDR DIMMB	0xA2h
WLAN	RSVD


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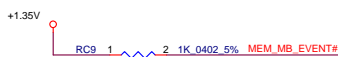
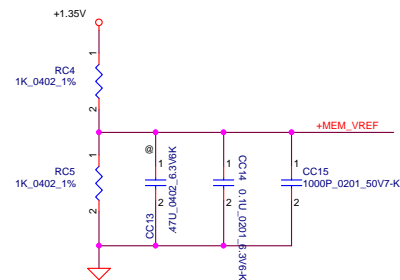
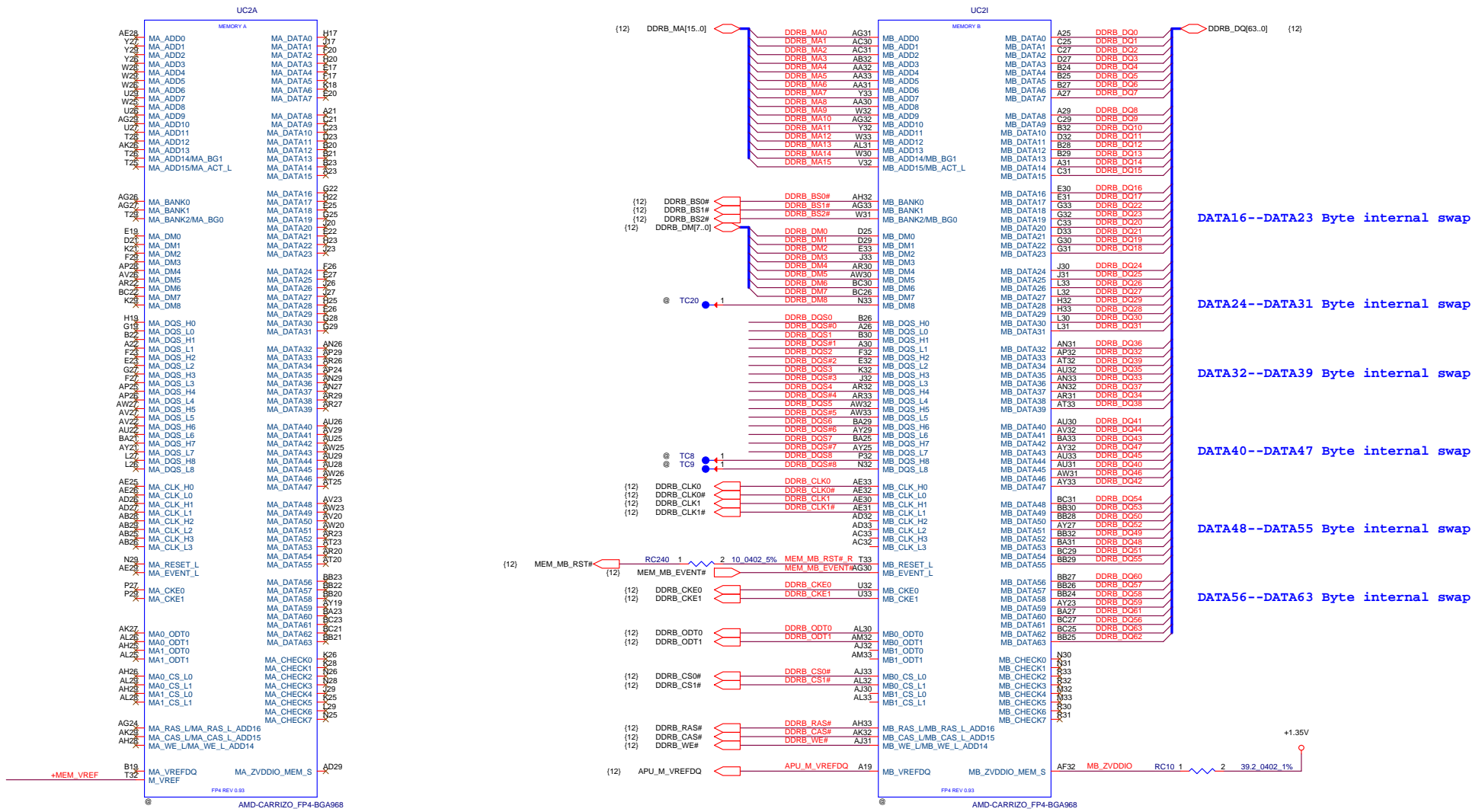


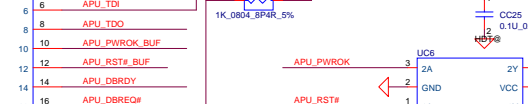
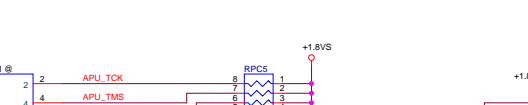
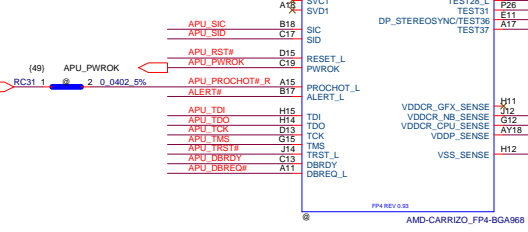
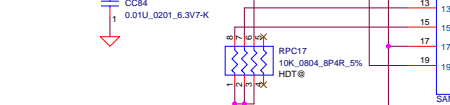
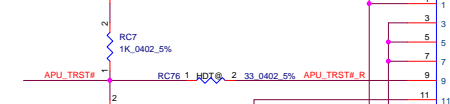
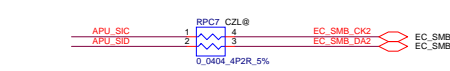
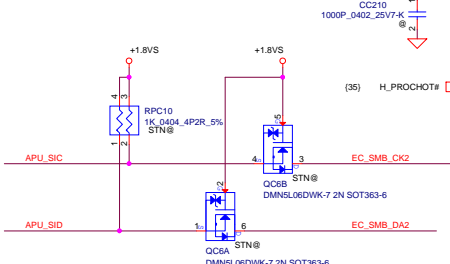
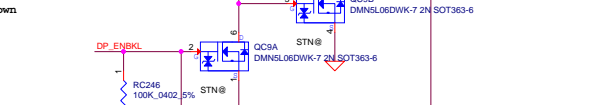
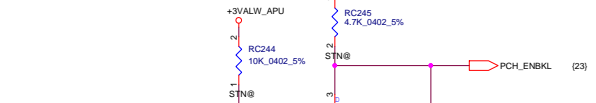
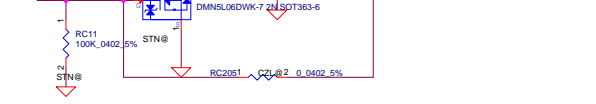
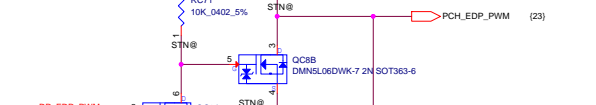
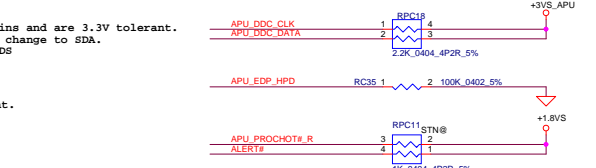
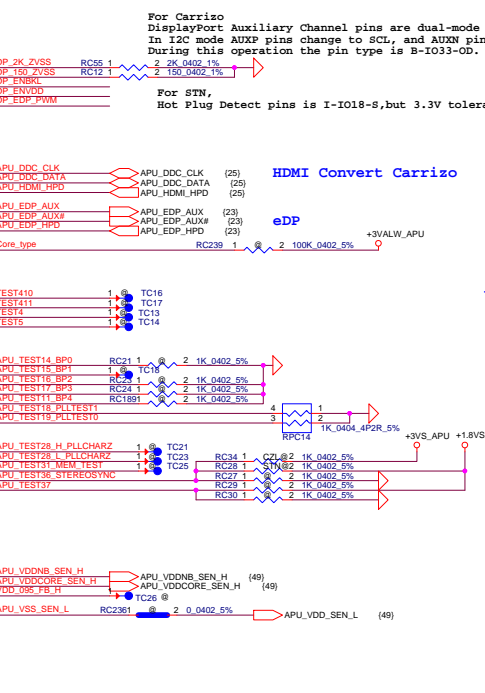
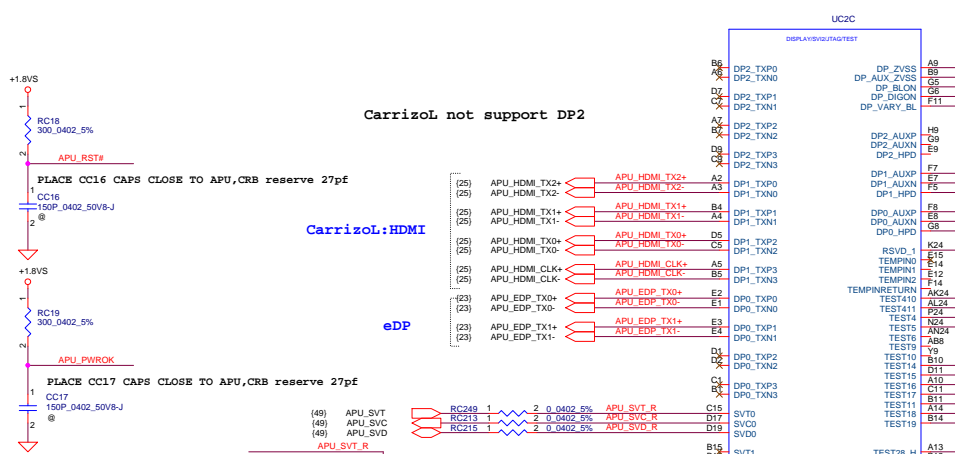


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CarrizoL not support ChannelA

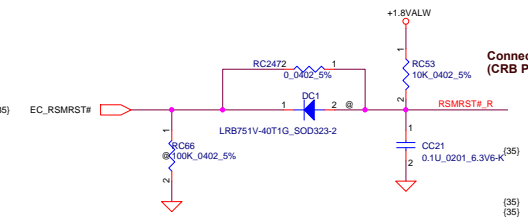
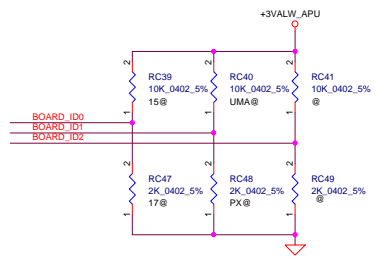
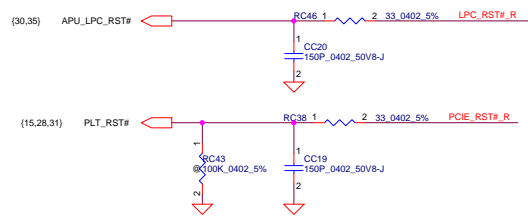




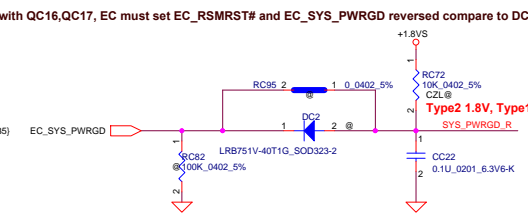
LCD Power IC can change for PCH\_ENVDD for CZ cost down

PCH\_ENBKL can to con EC ADC pin for CZ cost down because 1.8V level

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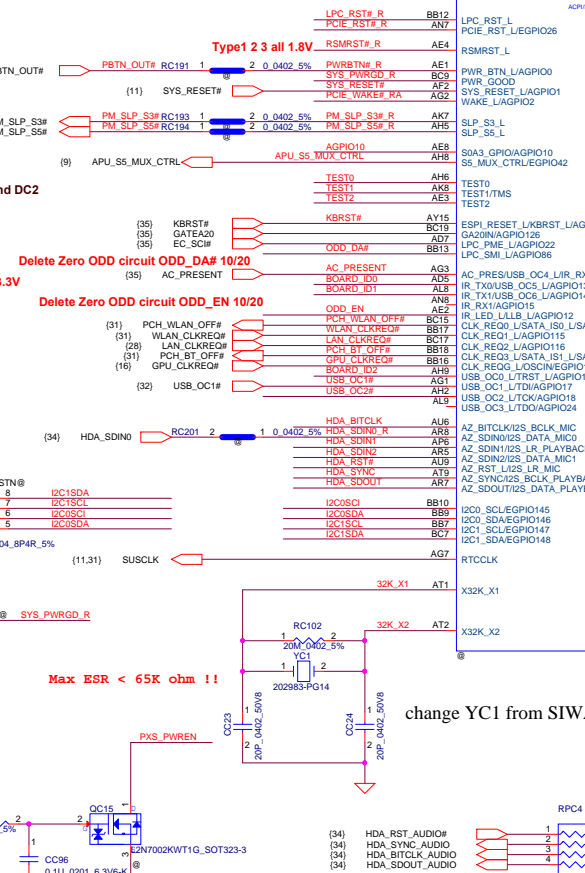
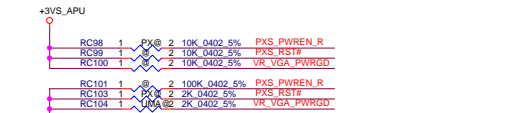
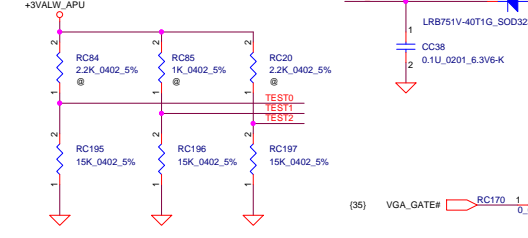
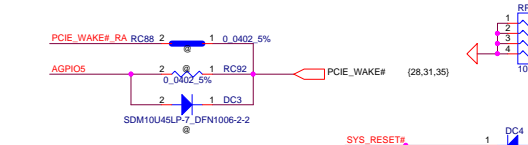
Connected to 10-ms RC-delay circuit on VDD\_18\_S5 power rail. (CRB PWR Dealy: 22K/0.1uF)



With QC16, QC17, EC must set EC\_RSMRST# and EC\_SYS\_PWRGD reversed compare to DC1 and DC2

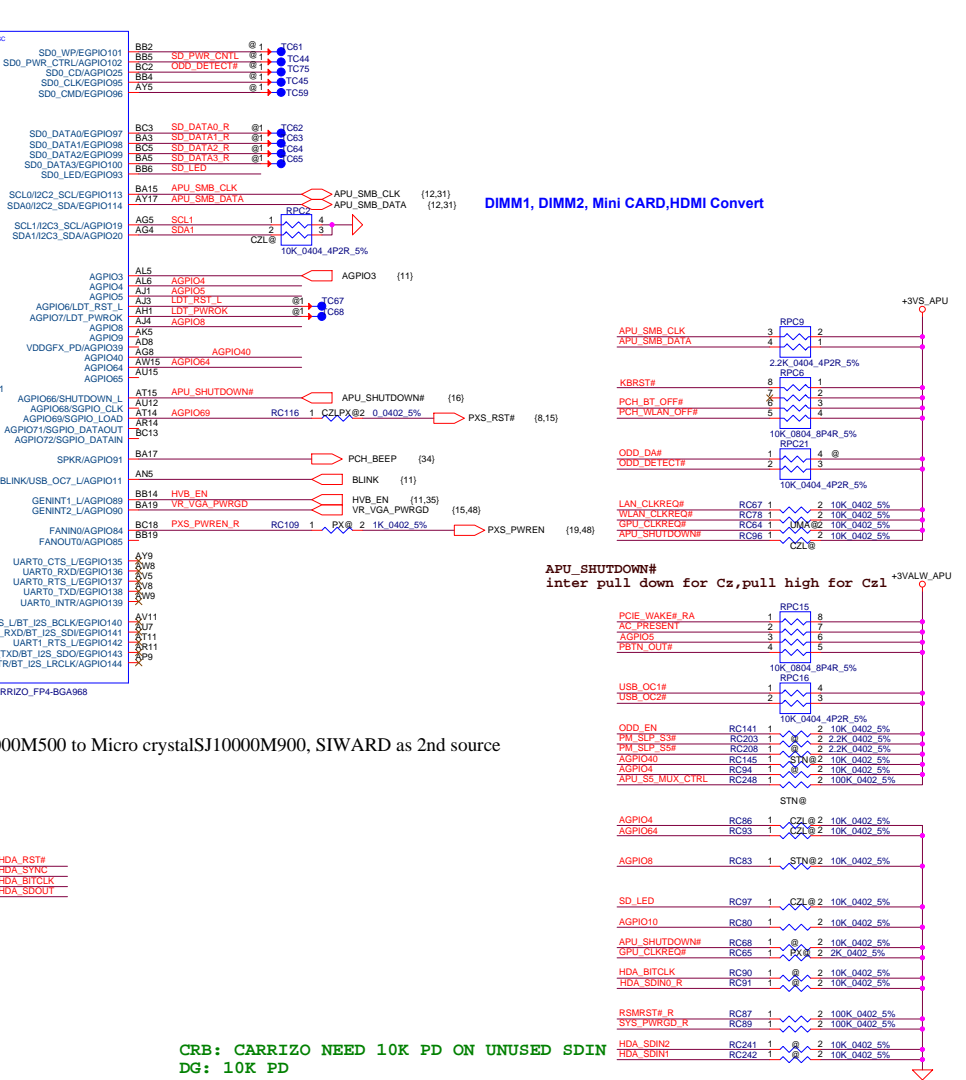
Delete Zero ODD circuit ODD\_DA# 10/20

Delete Zero ODD circuit ODD\_EN 10/20



Max ESR < 65K ohm !!

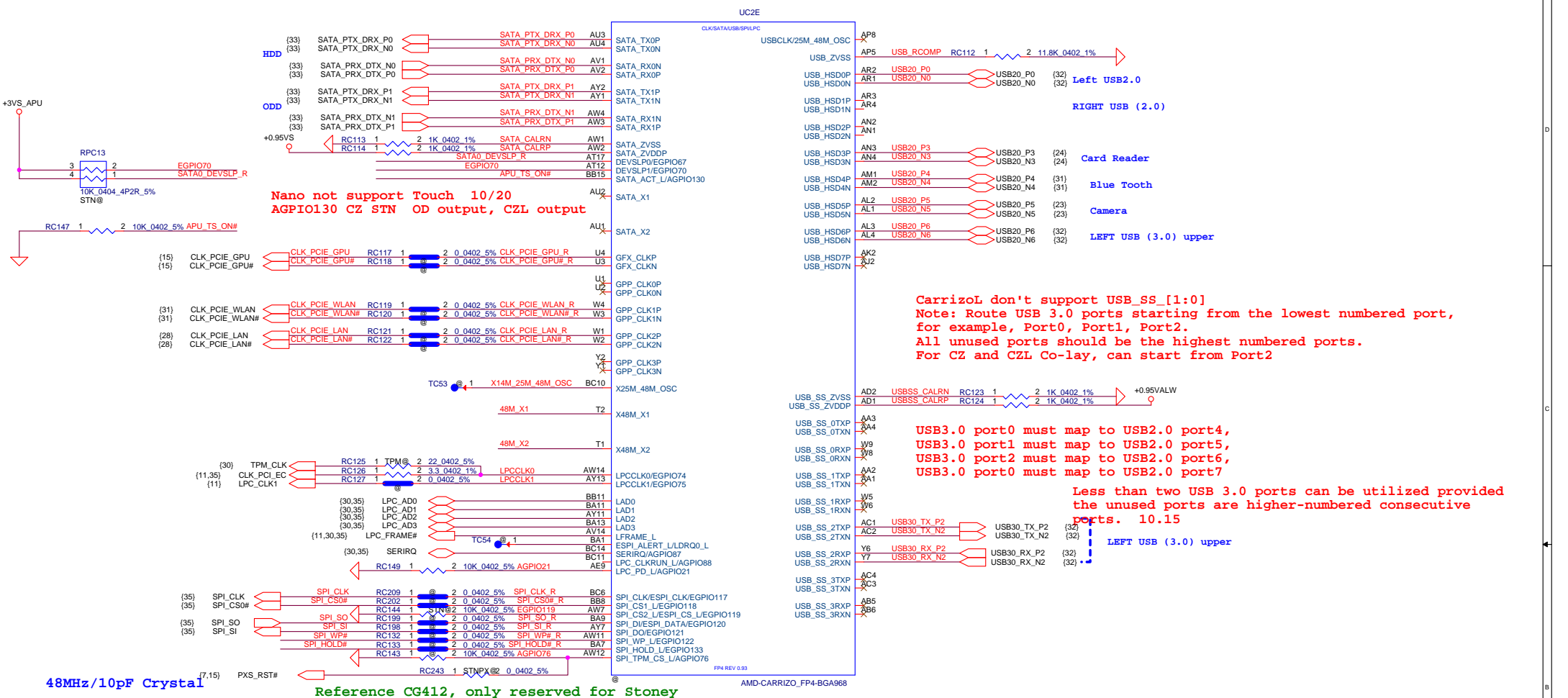
change YC1 from SIWARD SJ10000M500 to Micro crystal SJ10000M900, SIWARD as 2nd source



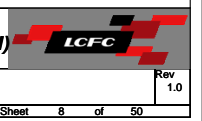
CRB: CARRIZO NEED 10K PD ON UNUSED SDIN DG: 10K PD

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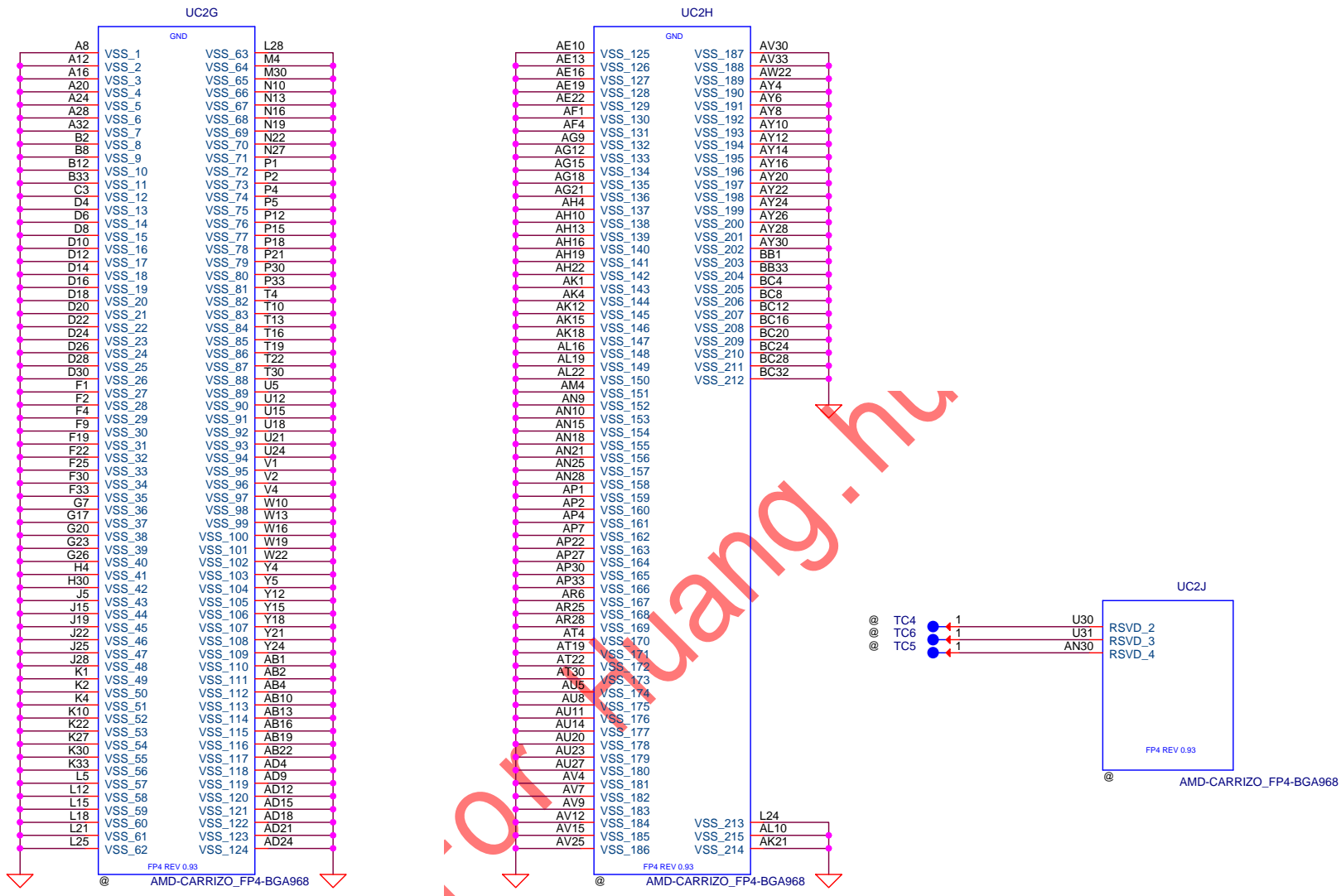


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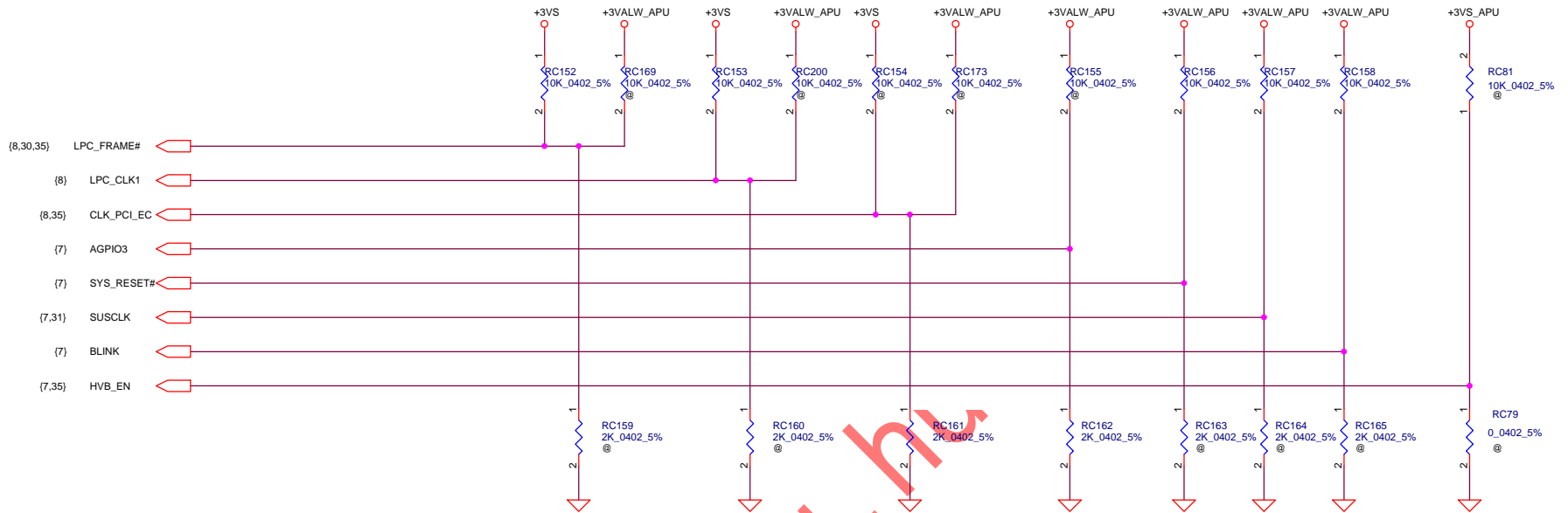






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## STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	GEVENT2_L/AGPIO3		SYS_RESET_L	RTCCLK	BLINK(for CZL strap)	HVB_EN
				Int pull-up					
Type	II	II	II	II	I	I	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	CZL	CZ	Normal Power Up & Reset Timing Default	Coin Battery Default	PWROK and RST pin routed to APU Default	floating
				1.8V SPI	Enhanced reset logic (for quicker S5 resume) Default				
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	3.3VSPI Default	Default to traditional reset logic	Reserved	Direct DC	Reserved	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST\_L, they are captured only once when power is first applied to the processor

Type II straps become valid after PWR\_GOOD is asserted, straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.

Type III straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

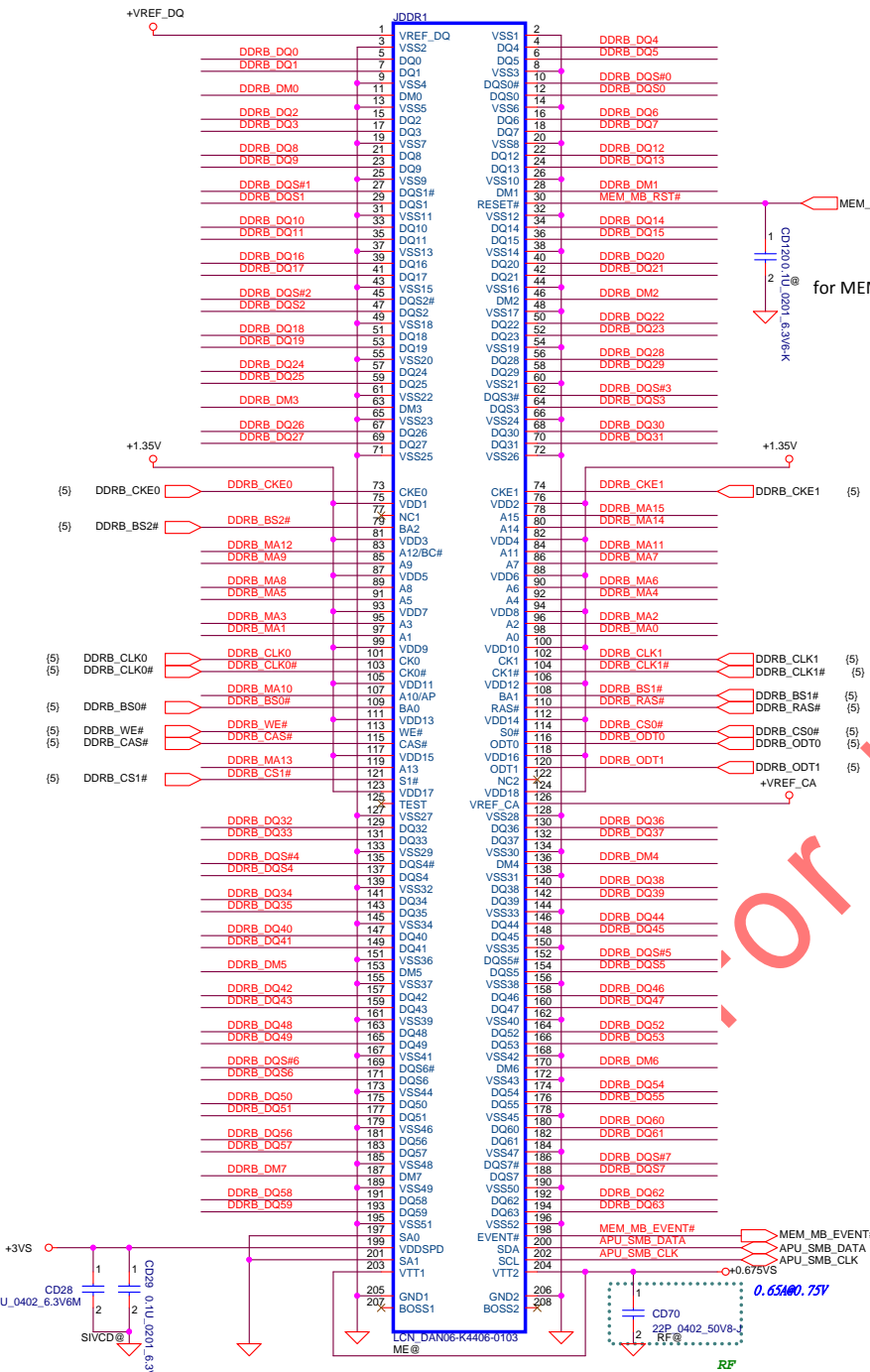
If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD\_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC compliant are recommended to use the Alternate Reset by strapping this pin to '1' for CZ AGPIO3

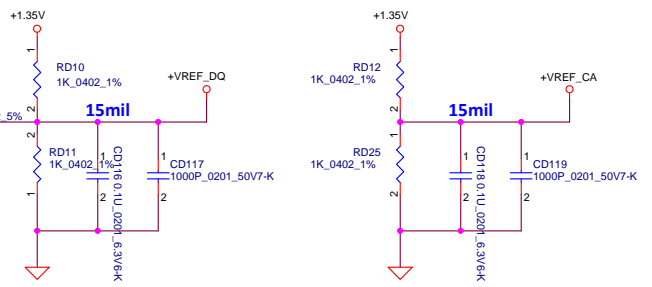
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# DDR3 SO-DIMM A

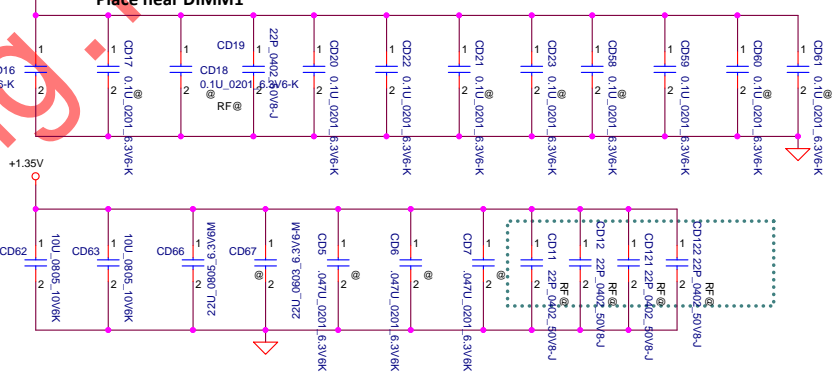


- DDR3\_DQ[0..63] (5)
- DDR3\_DQS[0..7] (5)
- DDR3\_DQS# [0..7] (5)
- DDR3\_MA[0..15] (5)
- DDR3\_DM[0..7] (5)

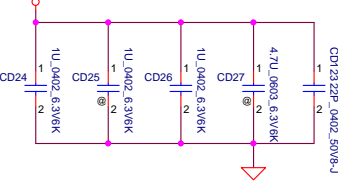
for MEM\_MB\_RST# overshoot issue



Layout Note:  
Place near DIMM1




Layout Note:  
Place near DIMM1



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## Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

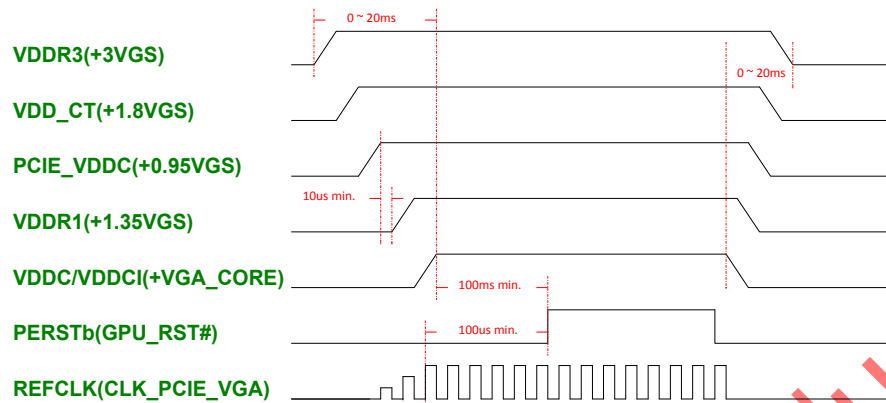
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10  $\mu$ s before VDDC, VDDCI, and VMEMIO start to ramp up.


The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as  $\leq 50$  mV/ $\mu$ s).

For power down, reversing the ramp-up sequence is recommended.



## VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-NOC 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G.N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

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				Rev: 1.0

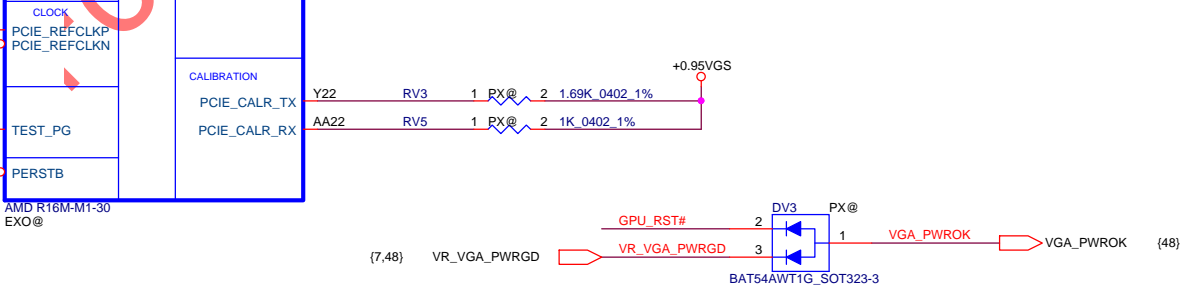
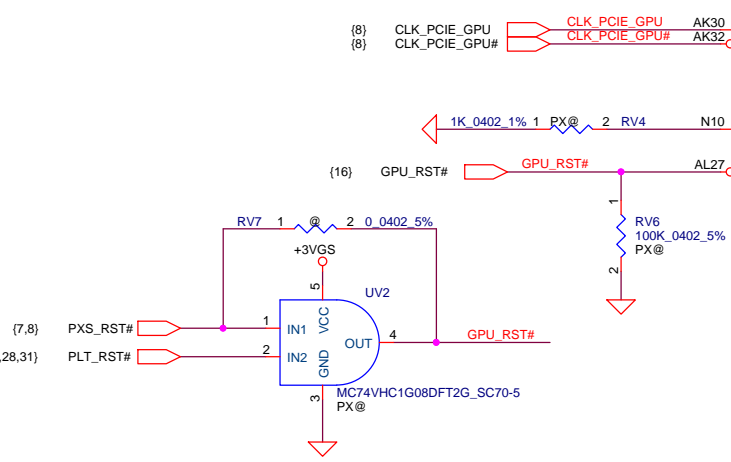
(4) PCIE\_CTX\_C\_GRX\_P[3..0]  $\Rightarrow$  PCIE\_CTX\_C\_GRX\_P[3..0]  
 (4) PCIE\_CTX\_C\_GRX\_N[3..0]  $\Rightarrow$  PCIE\_CTX\_C\_GRX\_N[3..0]

PCIE\_CRX\_GTX\_P[3..0]  $\Rightarrow$  PCIE\_CRX\_GTX\_P[3..0] (4)  
 PCIE\_CRX\_GTX\_N[3..0]  $\Rightarrow$  PCIE\_CRX\_GTX\_N[3..0] (4)



with BOM structure control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok  
 11/4 change to PC sample SA000074V10



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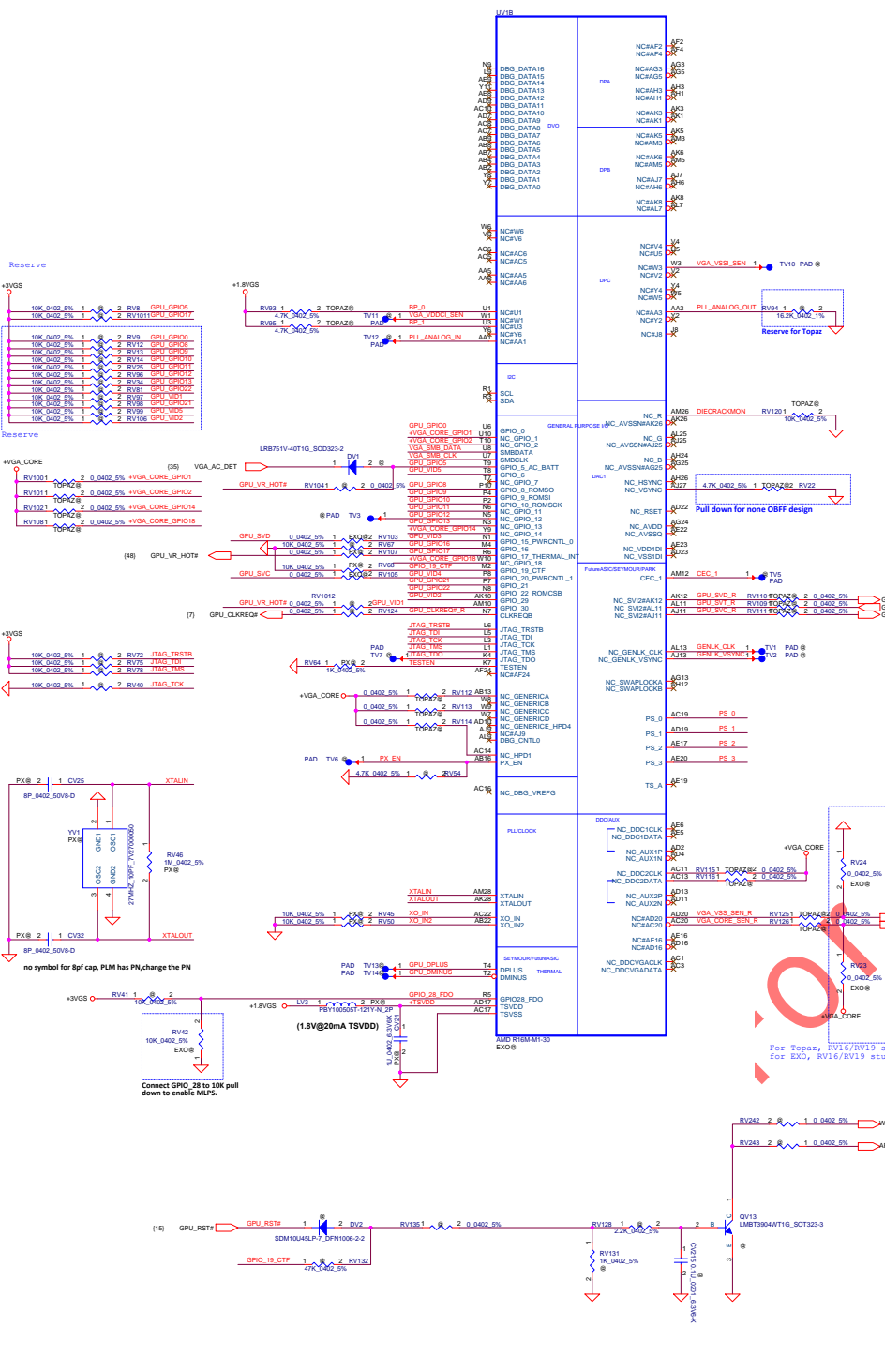
Rev 1.0

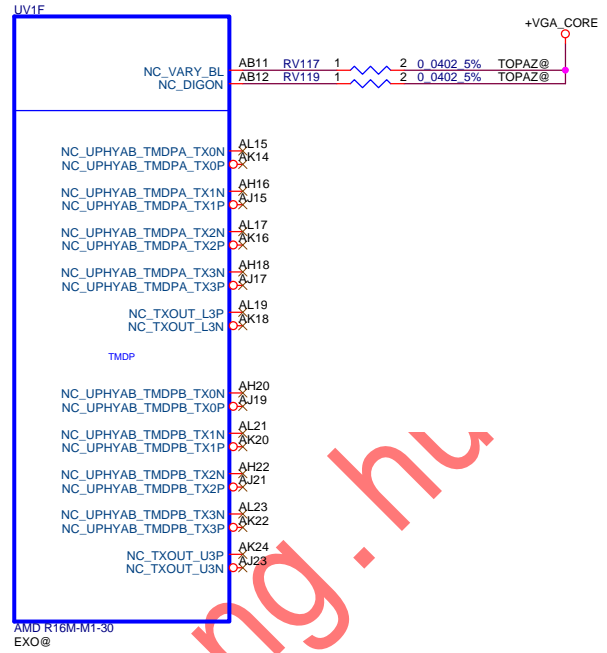


**CONFIGURATION STRAPS**  
**ALLOW FOR PULL UP PADS FOR THESE STRAPS AND IF THESE**  
**GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**


RECOMMENDED SET POINTS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL THE RESISTOR  
 NA= NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[0]	ROM_CONFIG[1]	Define the primary memory footprint size when STRAP_BIOS_ROM_EN = 0.	100 = 256MB
PS_0[4]	NA	Reserved for internal use only. Must be 1 at reset.	1
PS_0[6]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	X
PS_1[11]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	0= Not support
PS_1[12]	STRAP_BIF_CLK_PM_LEN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_1[13]	NA	Reserved for internal use only. Must be 0 at reset.	0
PS_1[14]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter full swing is enabled. 1 = The transmitter full swing is disabled.	1
PS_1[15]	STRAP_TX_DEMPH_LEN	0 = Tx deemphases disabled. 1 = Tx deemphases enabled.	1= Enable
PS_2[1]	NA	Reserved.	NA
PS_2[2]	NA	Reserved.	NA
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0= Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[6]	NA	Reserved.	NA
PS_3[1]	BOARD_CONFIG[0]	Based on configuration related strapping, such as for memory ID	X
PS_3[2]	BOARD_CONFIG[1]	10 = Hynix IG 11 = Micron IG 110 = Samsung IG	X
PS_3[3]	BOARD_CONFIG[2]	00 = Hynix J5 001 = Hynix J5 001 = Samsung J5	X
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be generated for the OS and use (combine with PS_0[6])	X
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	11 = No usable endpoints. 10 = One usable endpoint. 01 = Two usable endpoints. 00 = Three usable endpoints. 001 = Four usable endpoints. 000 = Five usable endpoints. 000 = Six usable endpoints. 000 = All endpoints are usable.	X



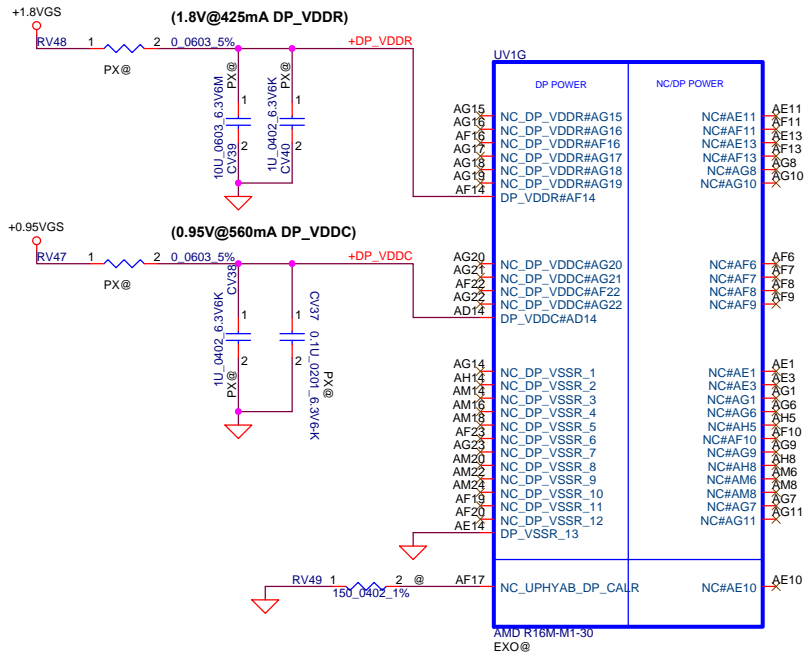


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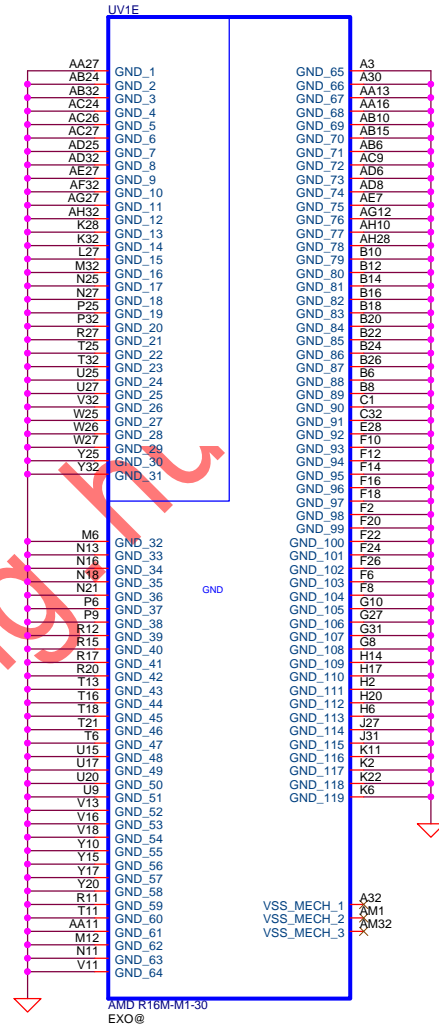
(1.8V@425mA DP\_VDDR)

(0.95V@560mA DP\_VDDC)



UV1G		UV1E	
DP POWER	NC/DP POWER	DP POWER	NC/DP POWER
AG15	NC_DP_VDDR#AG15	NC#AE11	AE11
AG16	NC_DP_VDDR#AG16	NC#AF11	AF11
AF16	NC_DP_VDDR#AF16	NC#AE13	AE13
AG17	NC_DP_VDDR#AG17	NC#AF13	AF13
AG18	NC_DP_VDDR#AG18	NC#AG8	AG8
AG19	NC_DP_VDDR#AG19	NC#AG10	AG10
AF14	NC_DP_VDDR#AF14		
AG20	NC_DP_VDDC#AG20	NC#AF6	AF6
AG21	NC_DP_VDDC#AG21	NC#AF7	AF7
AF22	NC_DP_VDDC#AF22	NC#AF8	AF8
AG22	NC_DP_VDDC#AG22	NC#AF9	AF9
AD14	DP_VDDC#AD14		
AG14	NC_DP_VSSR_1	NC#AE1	AE1
AH14	NC_DP_VSSR_2	NC#AE3	AE3
AM14	NC_DP_VSSR_3	NC#AG1	AG1
AM16	NC_DP_VSSR_4	NC#AG6	AG6
AM18	NC_DP_VSSR_5	NC#AH5	AH5
AF23	NC_DP_VSSR_6	NC#AF10	AF10
AG23	NC_DP_VSSR_7	NC#AG9	AG9
AM20	NC_DP_VSSR_8	NC#AH8	AH8
AM22	NC_DP_VSSR_9	NC#AM6	AM6
AM24	NC_DP_VSSR_10	NC#AM8	AM8
AF19	NC_DP_VSSR_11	NC#AG7	AG7
AF20	NC_DP_VSSR_12	NC#AG11	AG11
AE14	DP_VSSR_13		
	NC_UPHYAB_DP_CALR	NC#AE10	AE10

AMD R18M-M1-30  
EXO@



AMD R18M-M1-30  
EXO@







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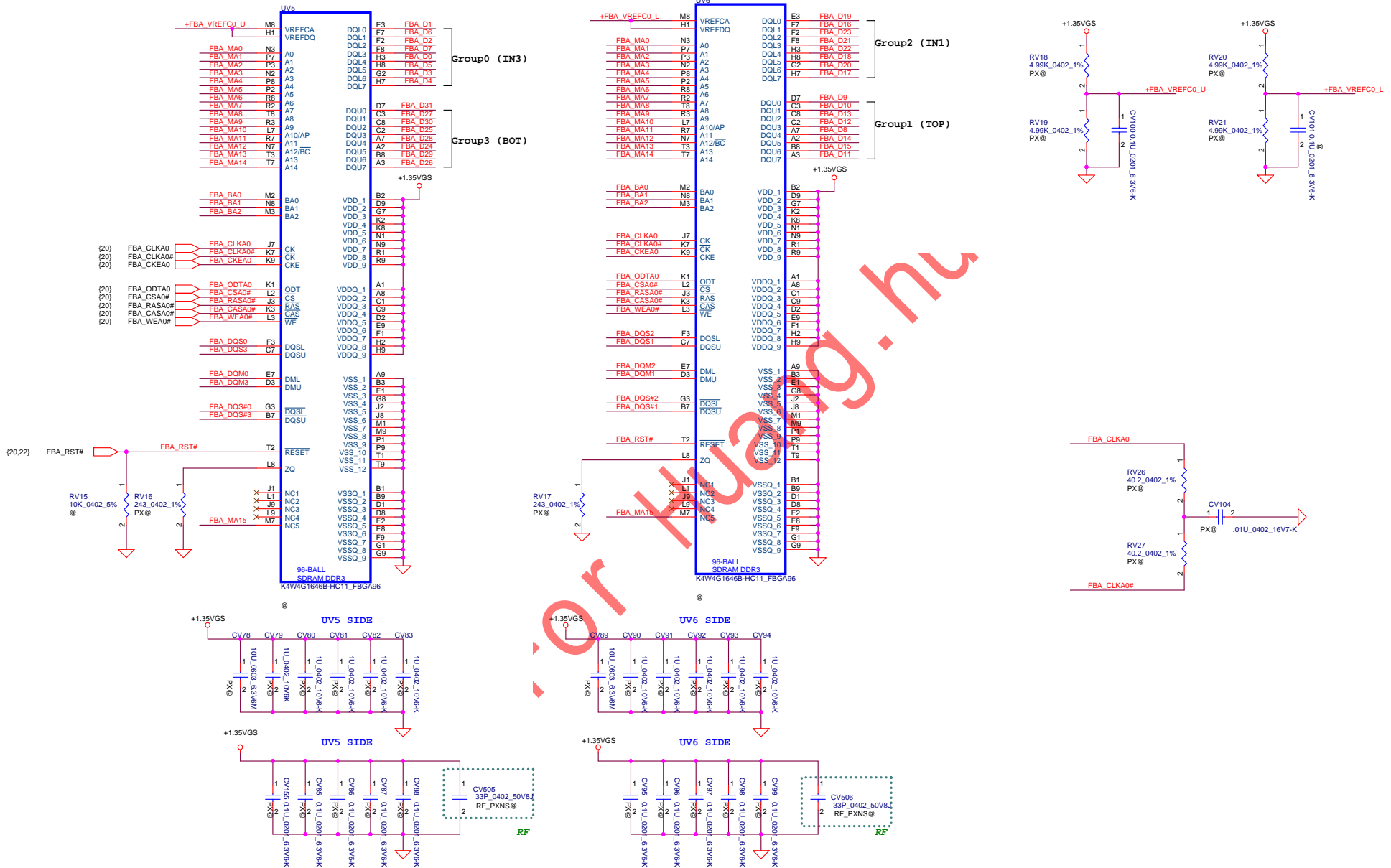
Title			Rev 1.0
ATI_JET-LE_DP Power			
Size	Document Number	CG521	
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# Memory Partition A - Lower 32 bits

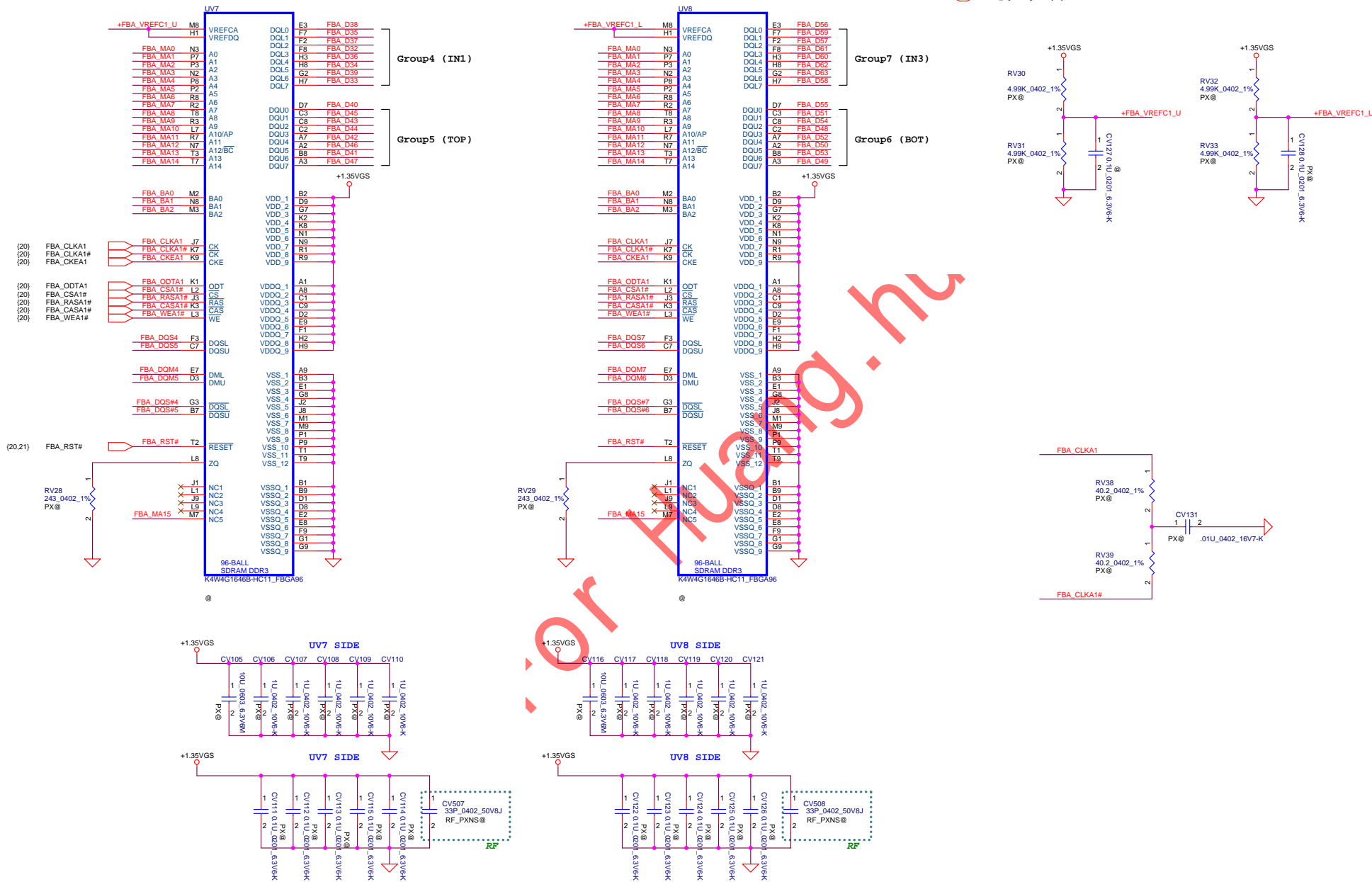
-  FBA\_MA[15..0] (20,22)
-  FBA\_BA[2..0] (20,22)
-  FBA\_DQS[3..0] (20)
-  FBA\_DQM[3..0] (20)
-  FBA\_DQS#[3..0] (20)
-  FBA\_D[31..0] (20)



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Title		
<b>ATI_JET-LE_VRAM_A</b>		
Size	Document Number	Rev
Custom	<b>CG521</b>	1.0
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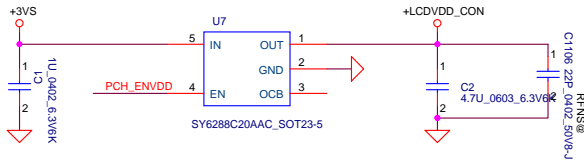
# Memory Partition A - Upper 32 bits



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2013/08/08		2013/08/05		CG521	
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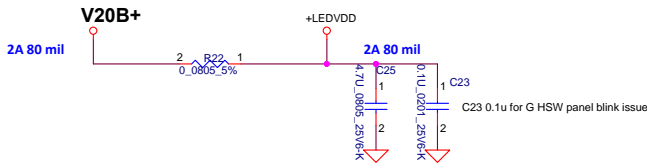
# LCD POWER CIRCUIT



(6) PCH\_ENVDD

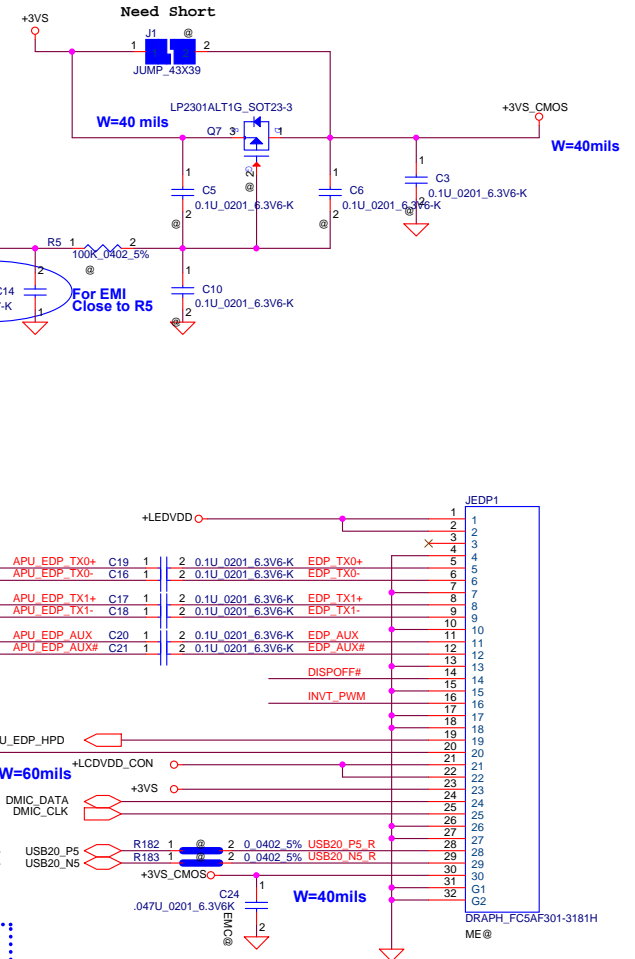
CZL enable is 3.3V, CZ is 1.8V, AP228002AW is 3.3V

# B+ to +LEDVDD POWER

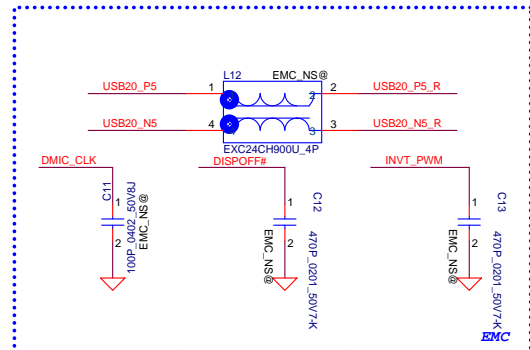


can cost down R20 for CZ

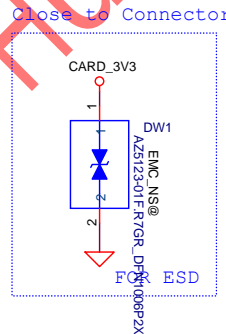
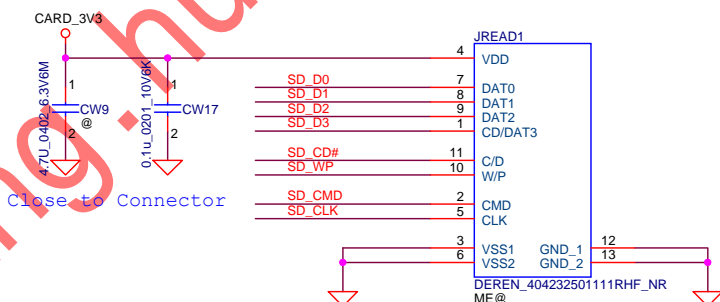
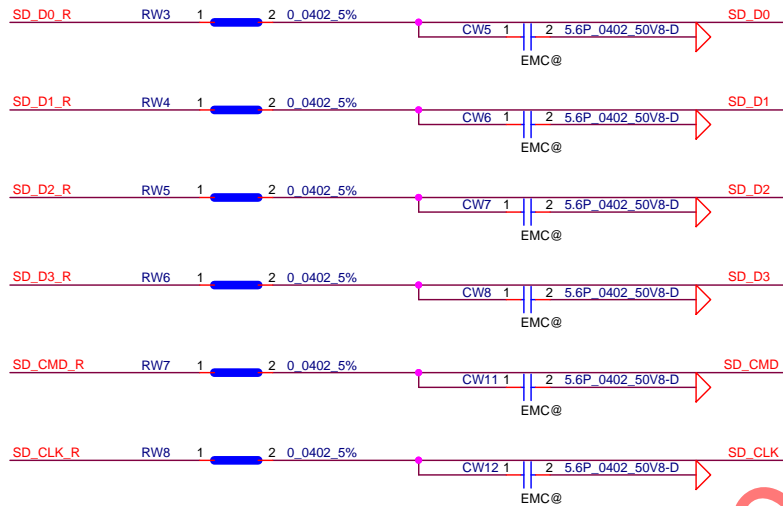
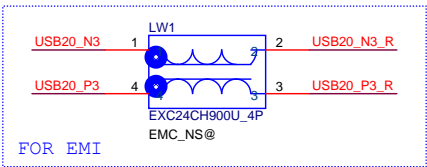
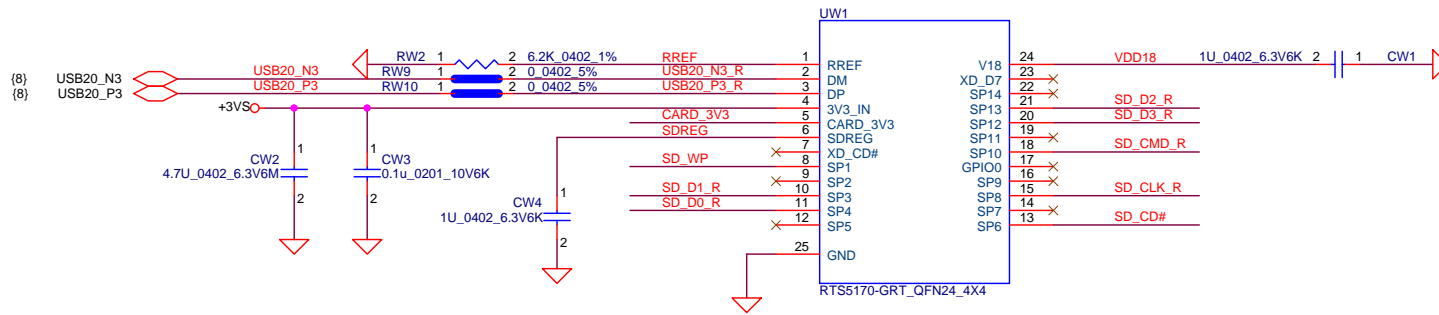
# CMOS Camera



(6)	APU_EDP_TX0+	APU_EDP_TX0+	C19	1	2	0.1U_0201_6.3V6-K	EDP_TX0+	4
(6)	APU_EDP_TX0-	APU_EDP_TX0-	C16	1	2	0.1U_0201_6.3V6-K	EDP_TX0-	5
(6)	APU_EDP_TX1+	APU_EDP_TX1+	C17	1	2	0.1U_0201_6.3V6-K	EDP_TX1+	6
(6)	APU_EDP_TX1-	APU_EDP_TX1-	C18	1	2	0.1U_0201_6.3V6-K	EDP_TX1-	7
(6)	APU_EDP_AUX	APU_EDP_AUX	C20	1	2	0.1U_0201_6.3V6-K	EDP_AUX	8
(6)	APU_EDP_AUX#	APU_EDP_AUX#	C21	1	2	0.1U_0201_6.3V6-K	EDP_AUX#	9
							DISPOFF#	10
							INVT_PWM	11
								12
								13
								14
								15
								16
								17
								18
								19
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								32



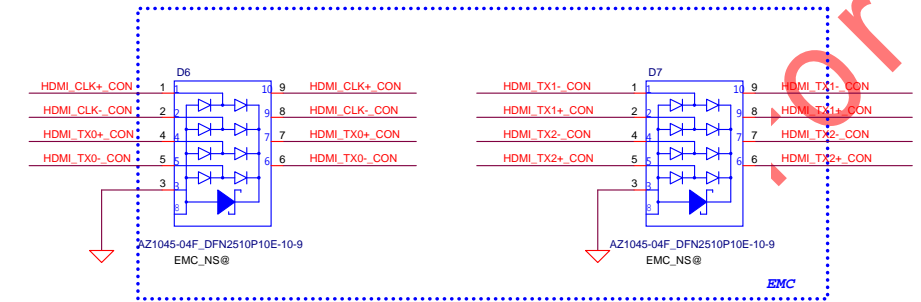
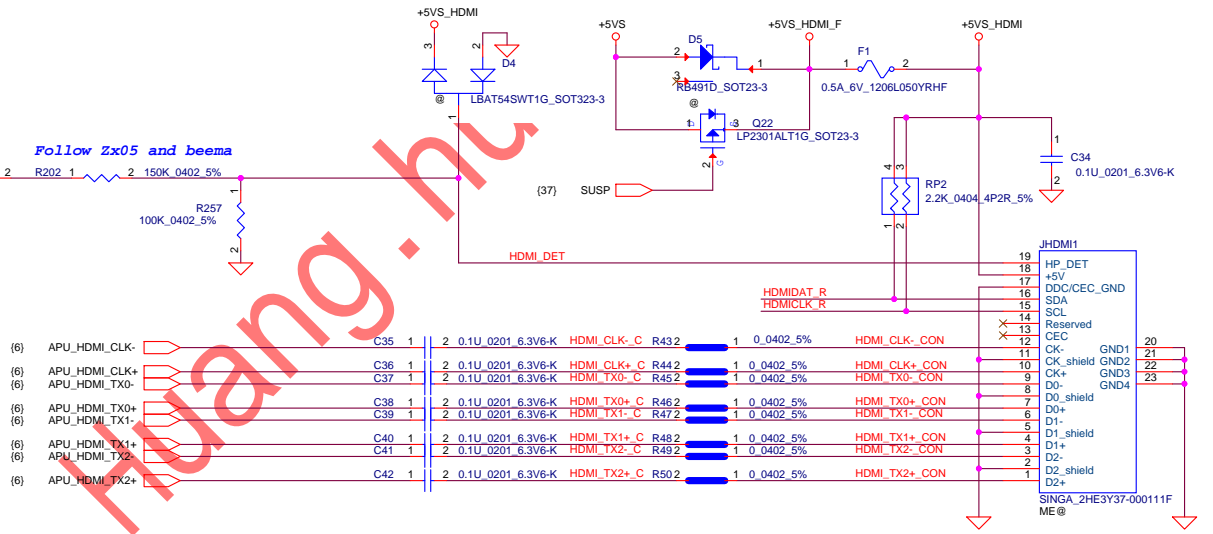
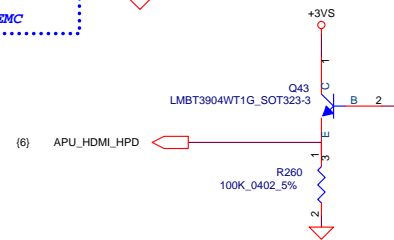
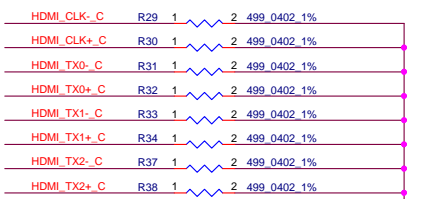
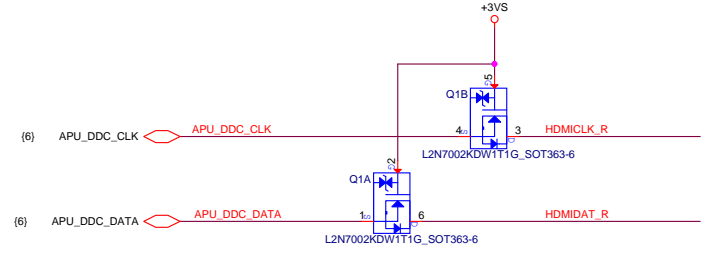
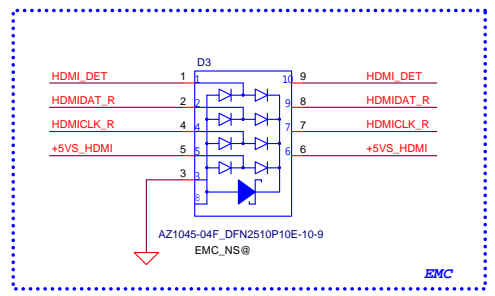
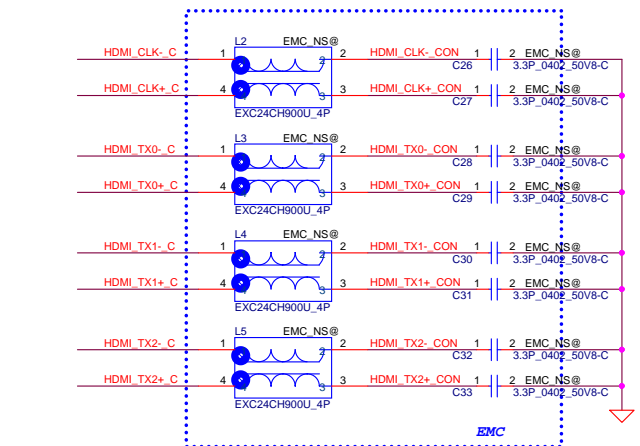
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(6)	APU_HDMI_CLK-	C35	1	2	0.1U 0201 6.3V6-K	HDMI_CLK- C	R432	1	0	0.402 5%	HDMI_CLK- CON	
(6)	APU_HDMI_CLK+	C36	1	2	0.1U 0201 6.3V6-K	HDMI_CLK+ C	R442	1	0	0.402 5%	HDMI_CLK+ CON	
(6)	APU_HDMI_TX0-	C37	1	2	0.1U 0201 6.3V6-K	HDMI_TX0- C	R452	1	0	0.402 5%	HDMI_TX0- CON	
(6)	APU_HDMI_TX0+	C38	1	2	0.1U 0201 6.3V6-K	HDMI_TX0+ C	R462	1	0	0.402 5%	HDMI_TX0+ CON	
(6)	APU_HDMI_TX1-	C39	1	2	0.1U 0201 6.3V6-K	HDMI_TX1- C	R472	1	0	0.402 5%	HDMI_TX1- CON	
(6)	APU_HDMI_TX1+	C40	1	2	0.1U 0201 6.3V6-K	HDMI_TX1+ C	R482	1	0	0.402 5%	HDMI_TX1+ CON	
(6)	APU_HDMI_TX2-	C41	1	2	0.1U 0201 6.3V6-K	HDMI_TX2- C	R492	1	0	0.402 5%	HDMI_TX2- CON	
(6)	APU_HDMI_TX2+	C42	1	2	0.1U 0201 6.3V6-K	HDMI_TX2+ C	R502	1	0	0.402 5%	HDMI_TX2+ CON	

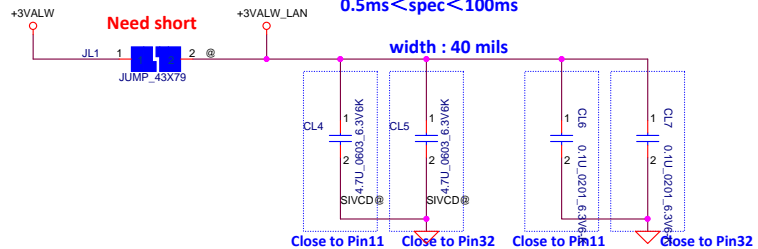
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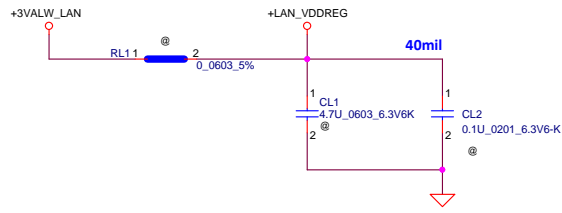
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			Date:	Wednesday, February 24, 2016   Sheet 27 of 50	

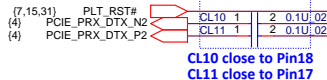
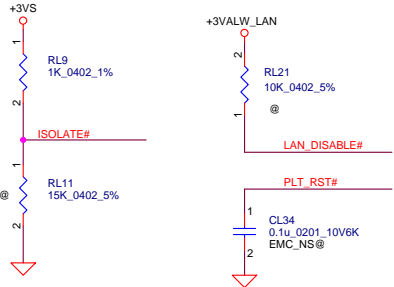
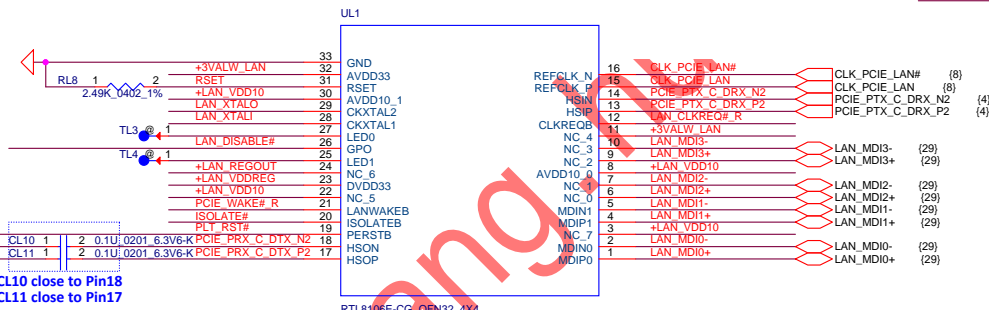
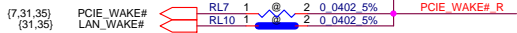
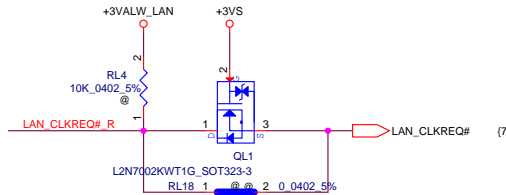
**+3VALW TO +3VALW\_LAN**



**+3VALW\_LAN rising time (10%~90%):**  
0.5ms < spec < 100ms

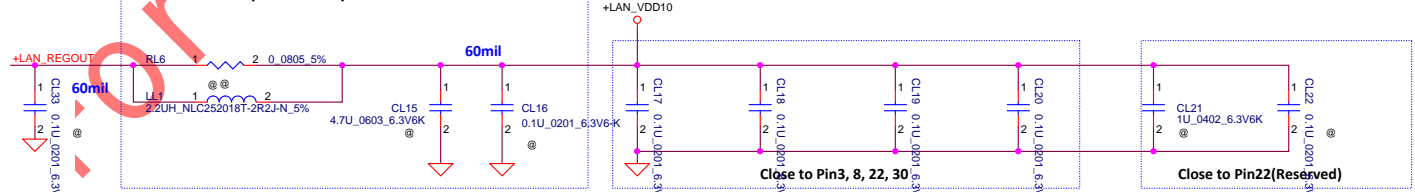


**change the Lan Chip PN to RTL8107ECG**

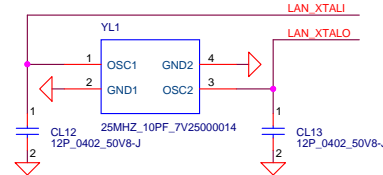


CL10 close to Pin18  
CL11 close to Pin17

**For RTL8111H (LDO mode)**



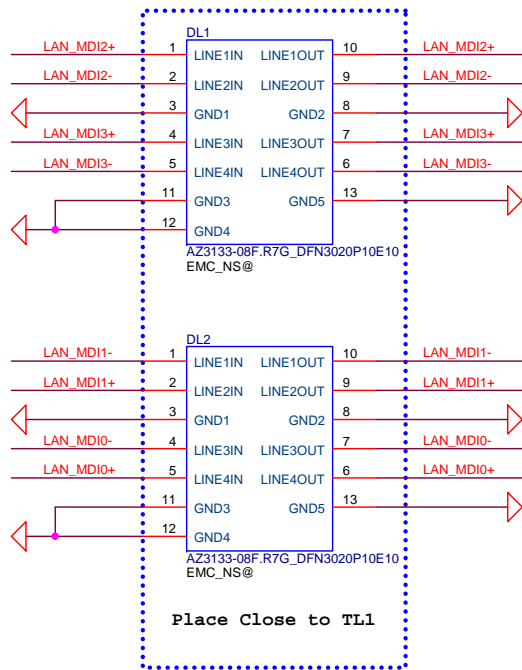
Layout Note: RL6, CL16 must be within 200mil to Pin36, +LAN\_REGOUT: Width = 60mil



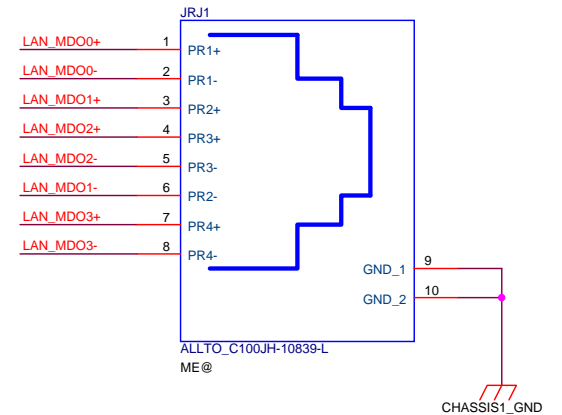
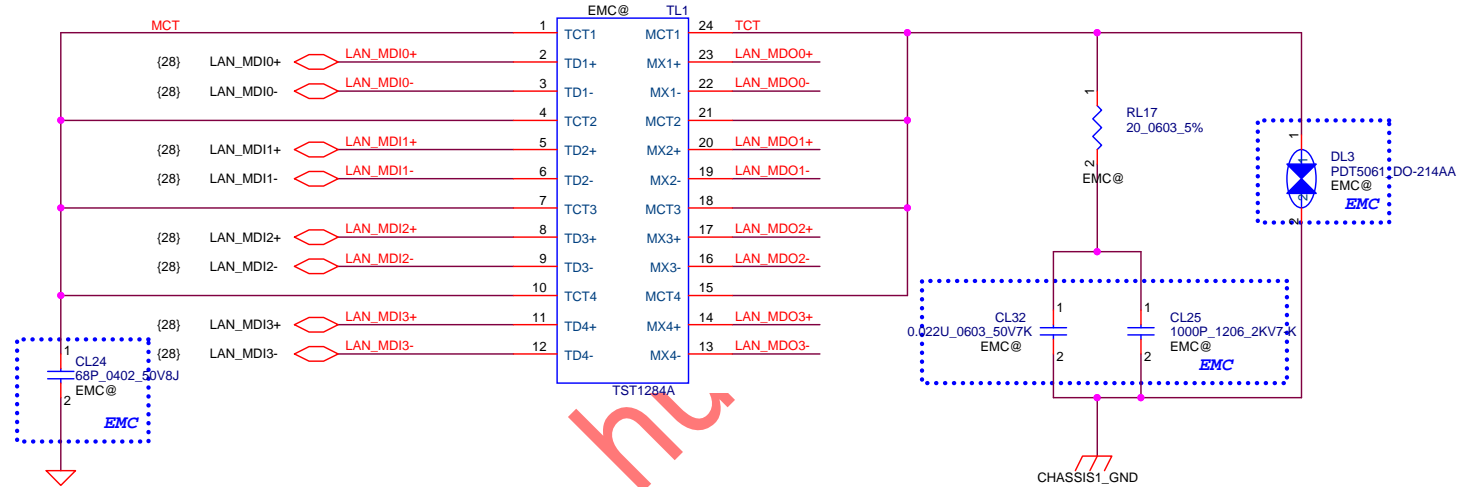
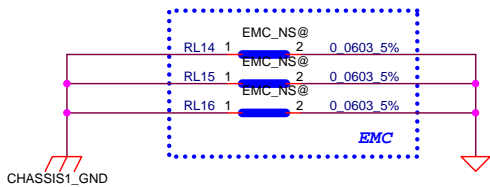
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LAN_RTL8111H_CG		
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DL1/DL2  
1'S PN:SC300003M00



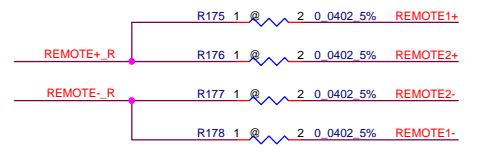
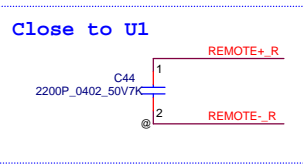
Place Close to TL1



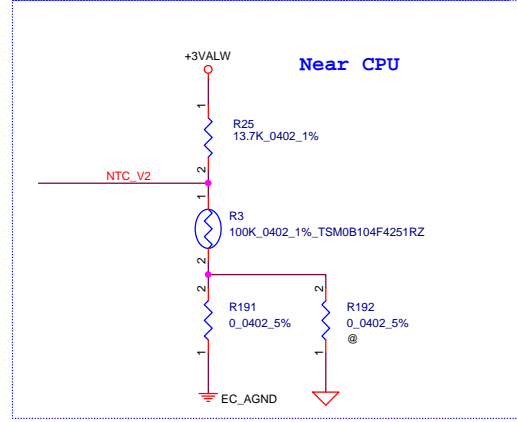
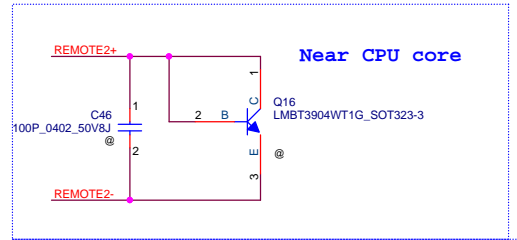
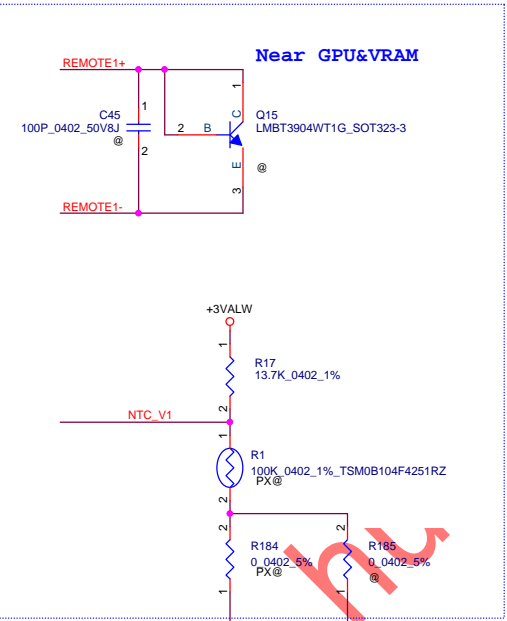
Don't short

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					Date:	Wednesday, February 24, 2016   Sheet 29 of 50

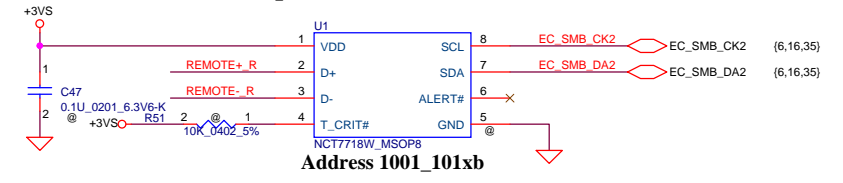




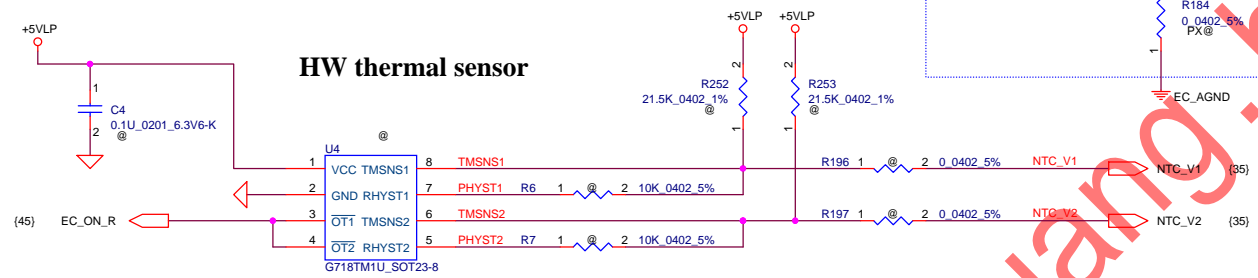
REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:-  
Trace width/space:10/10 mil  
Trace length:<8"



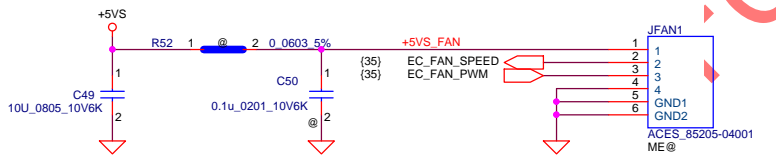
**SMSC thermal sensor placed near DIMM**



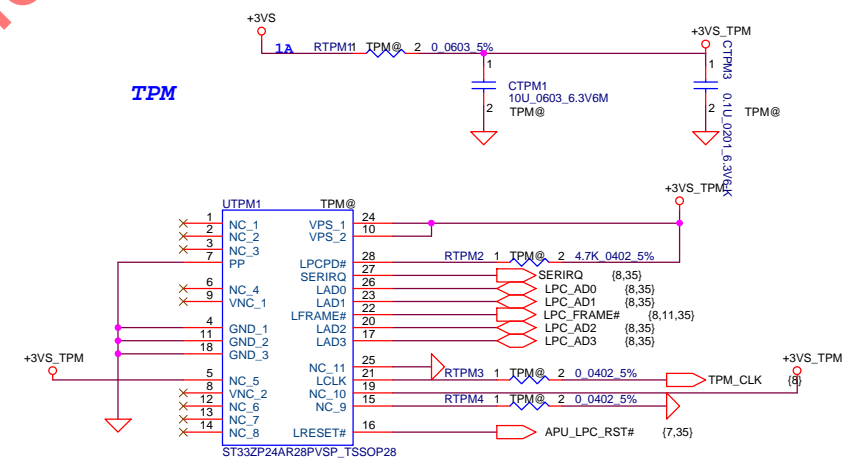
**HW thermal sensor**



over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C



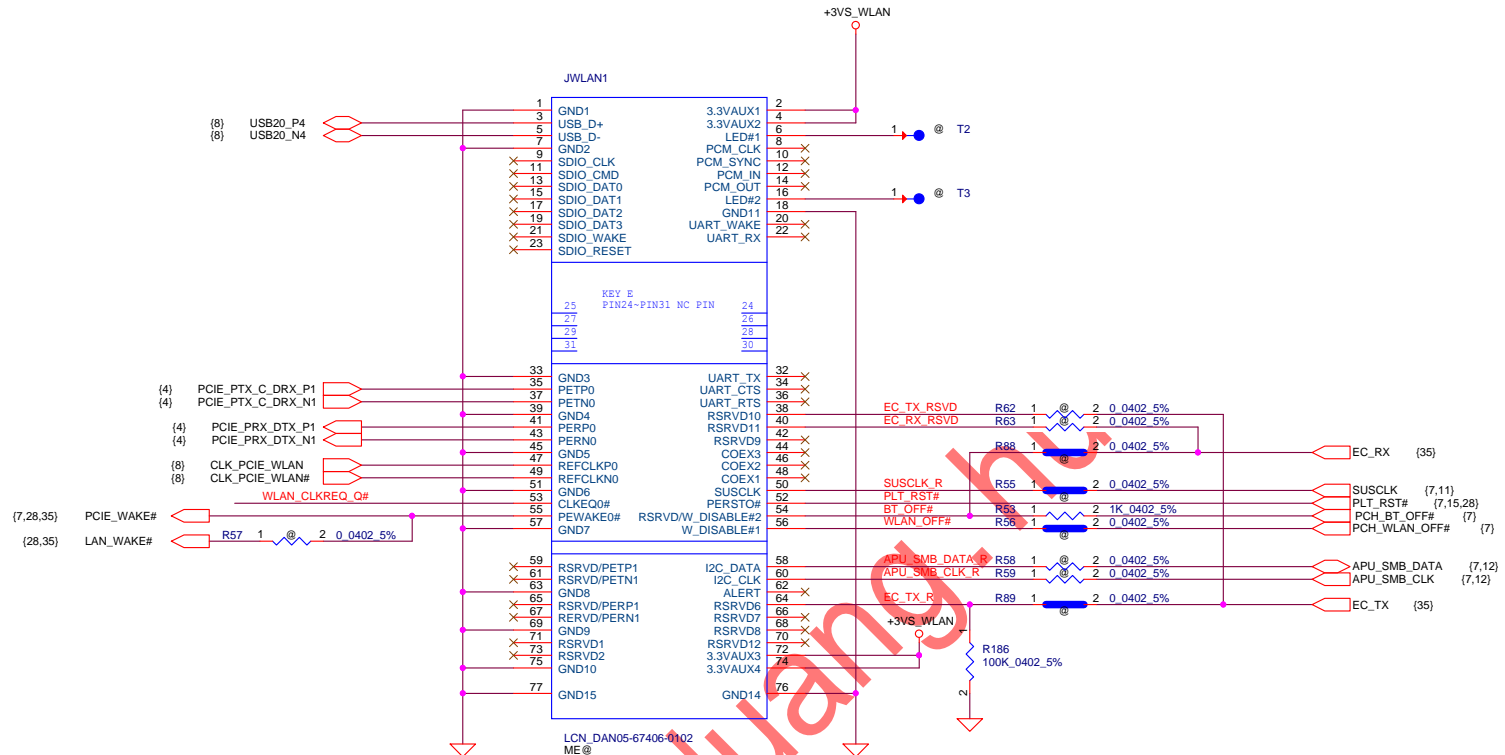
**TPM**



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# Mini-Express Card(WLAN/WiMAX)



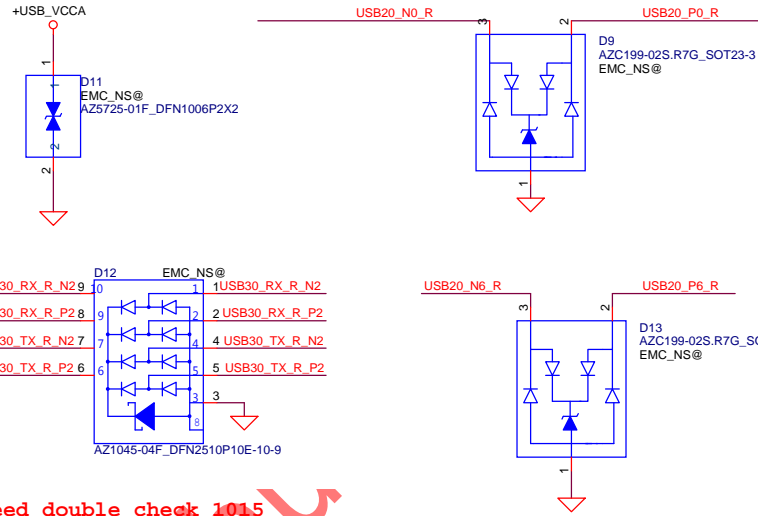
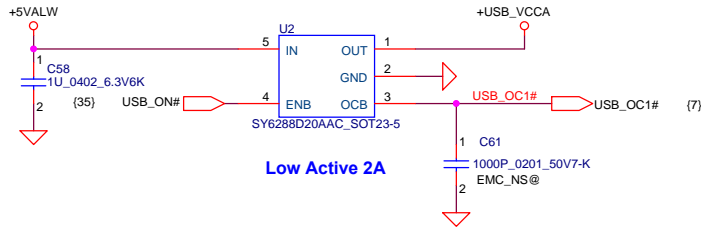
Not support AOAC, delete AOAC power circuit 1015  
 Need short  
 +3VS



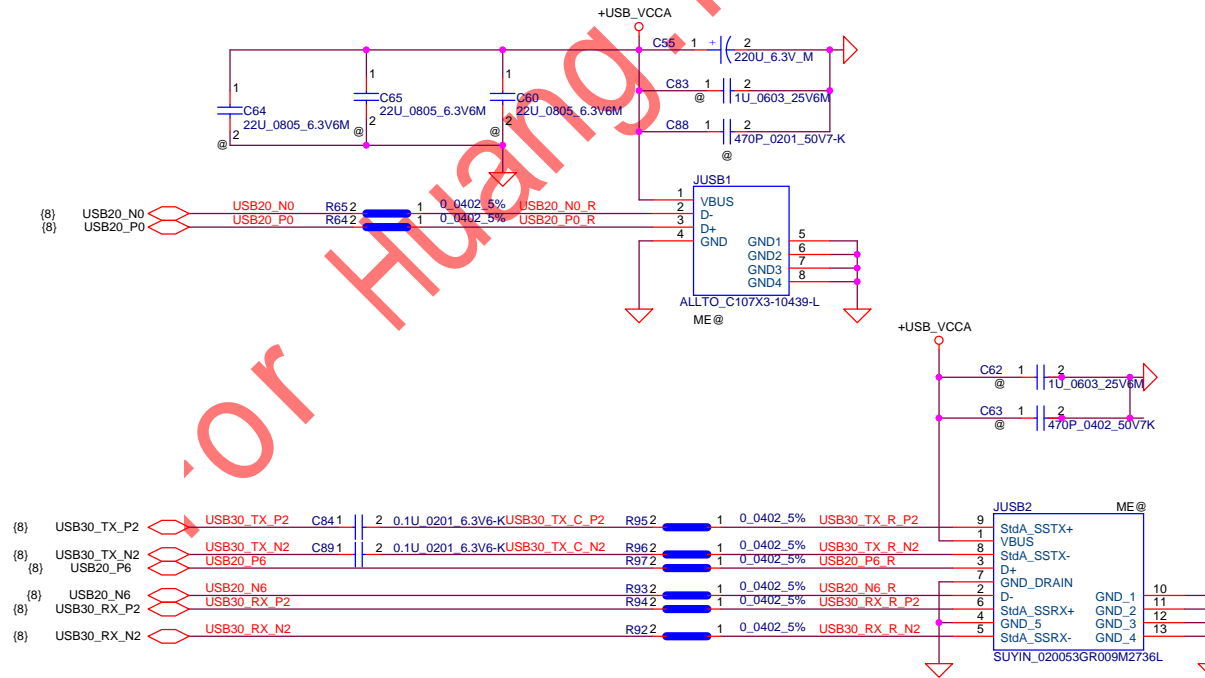
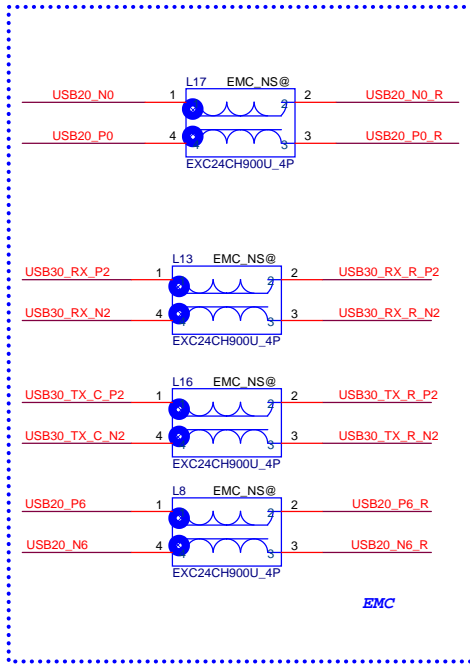
If support AOAC, NC R61;  
 if not support AOAC, stuff R61.

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# LEFT SIDE USB PORT X2

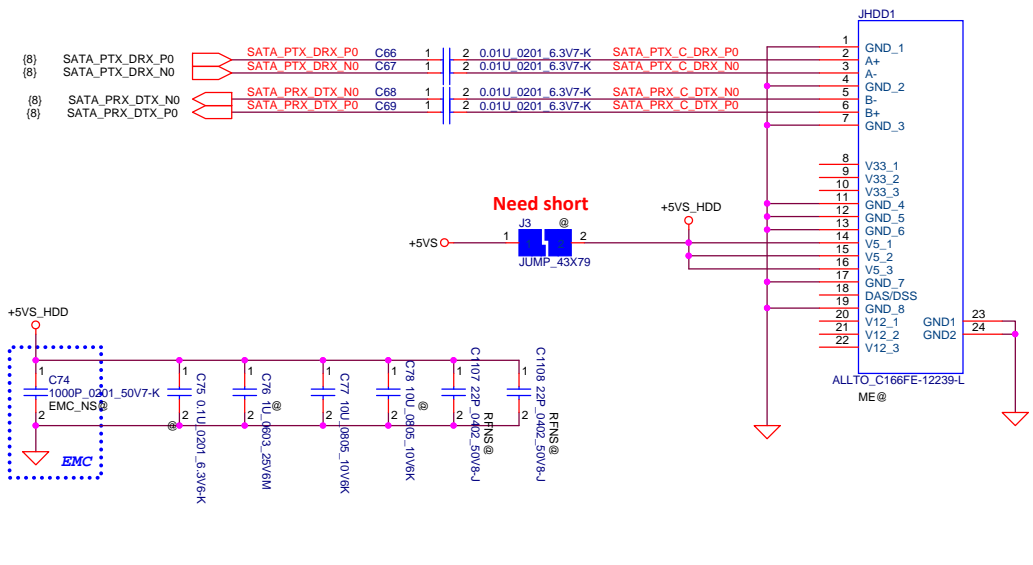


EMC solution need double check 1015

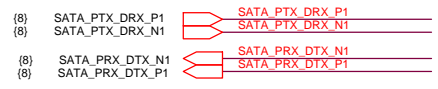


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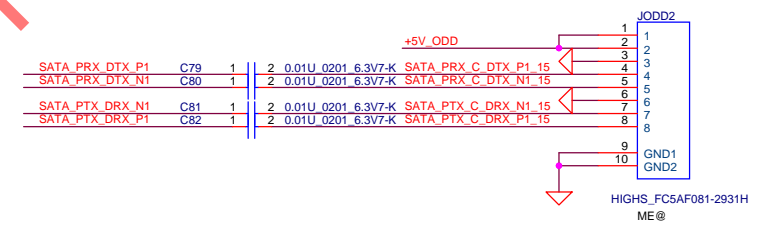
### SATA HDD Conn.



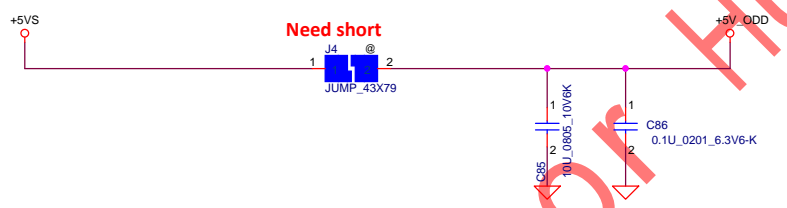
FOR 14"  
SATA ODD Conn.



FOR 15"  
SATA ODD FFC Conn

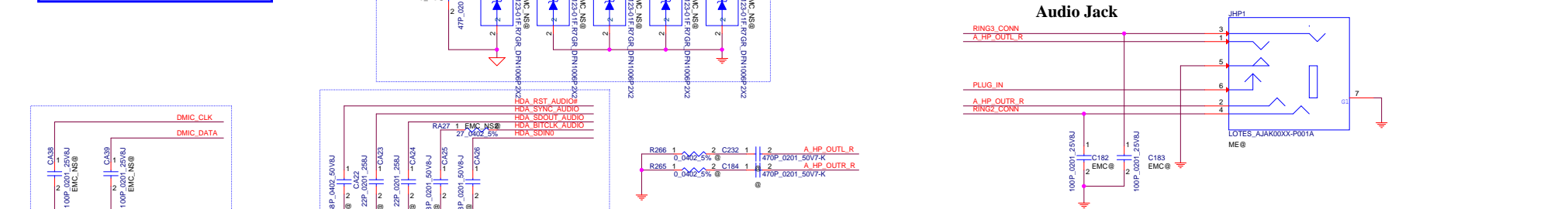
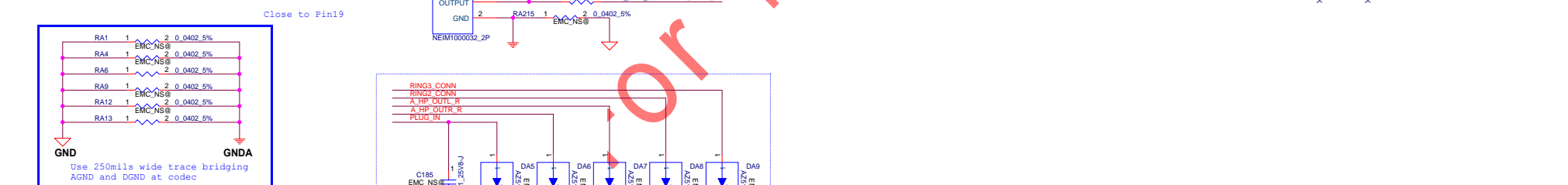
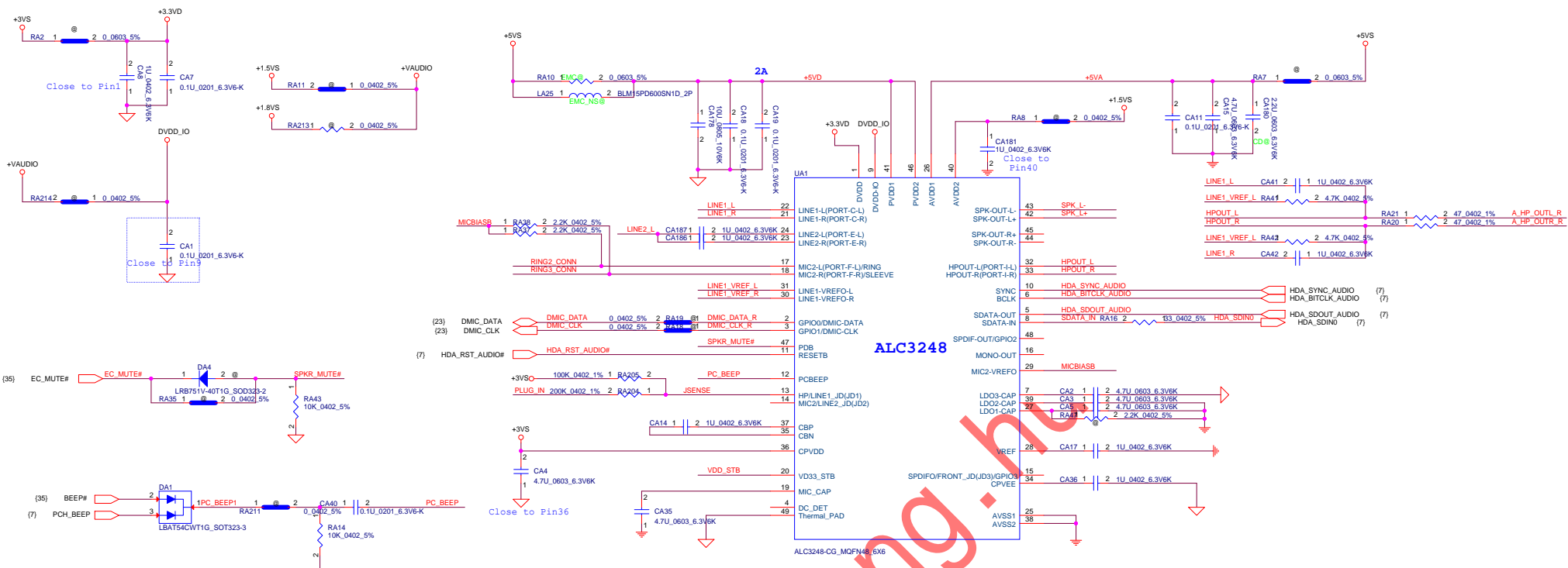



+5VS to +5V\_ODD

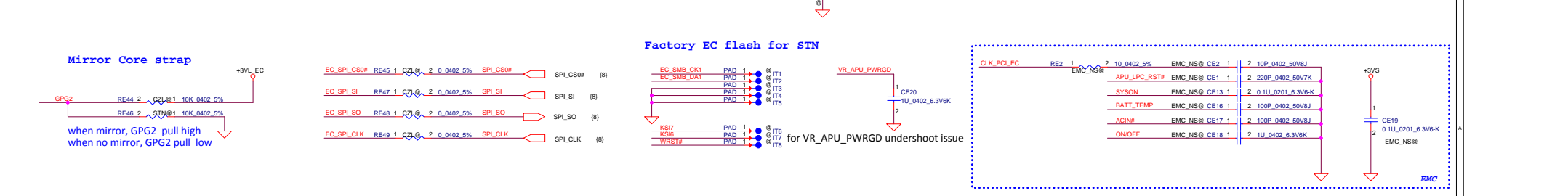
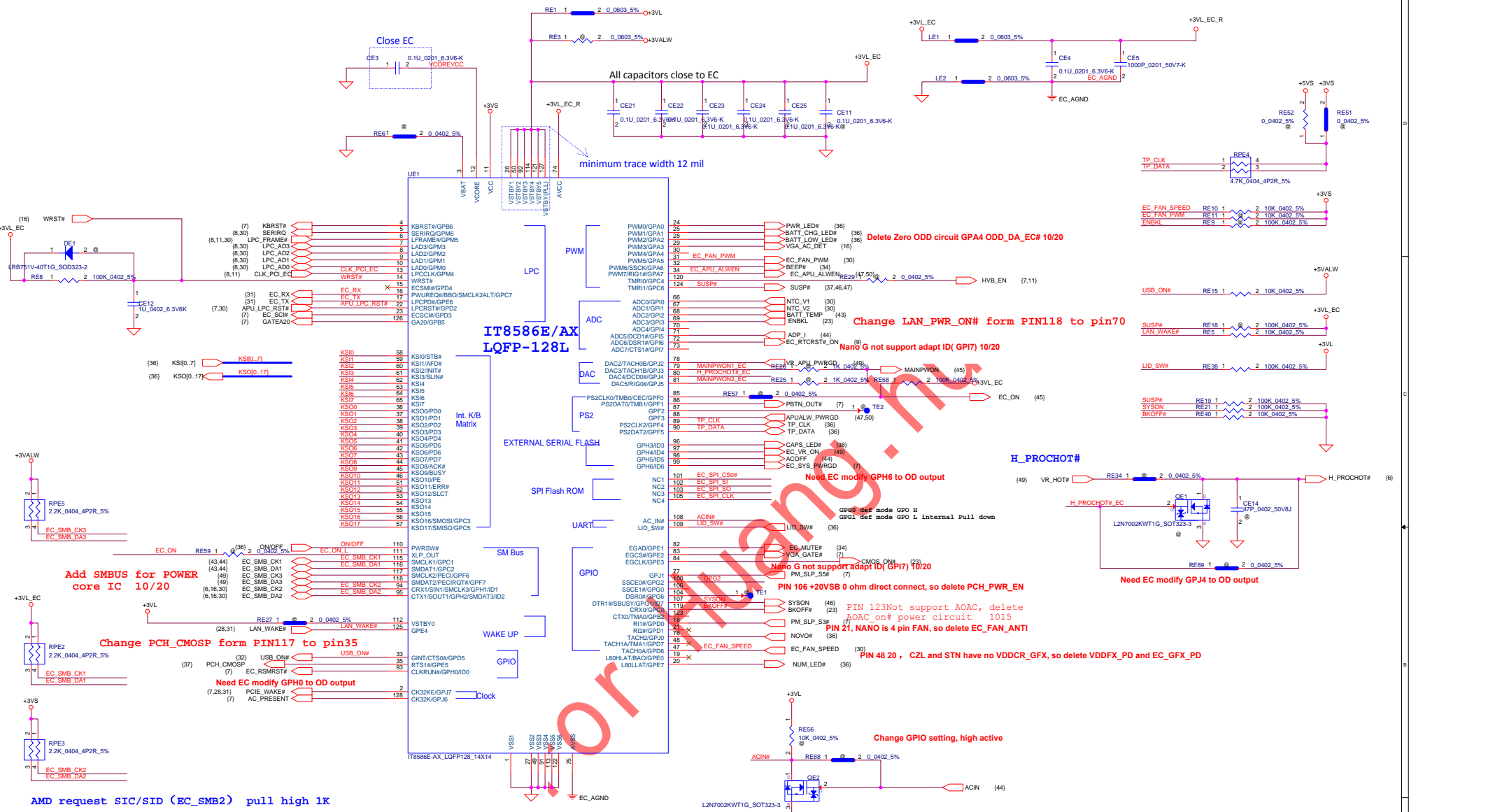


Delete Zero ODD circuit 10/19

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Custom								CG521	
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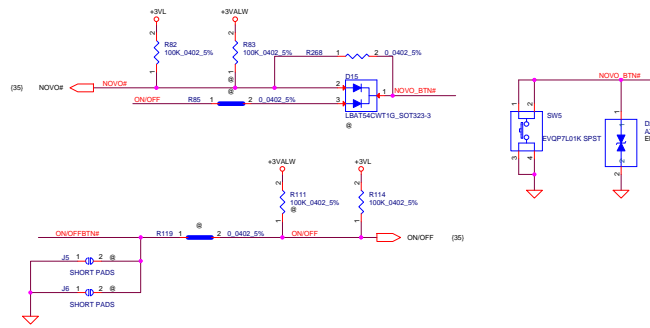


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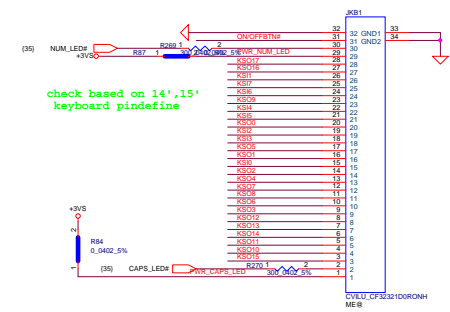
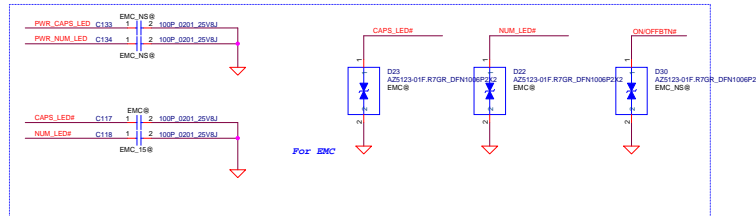
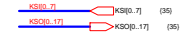


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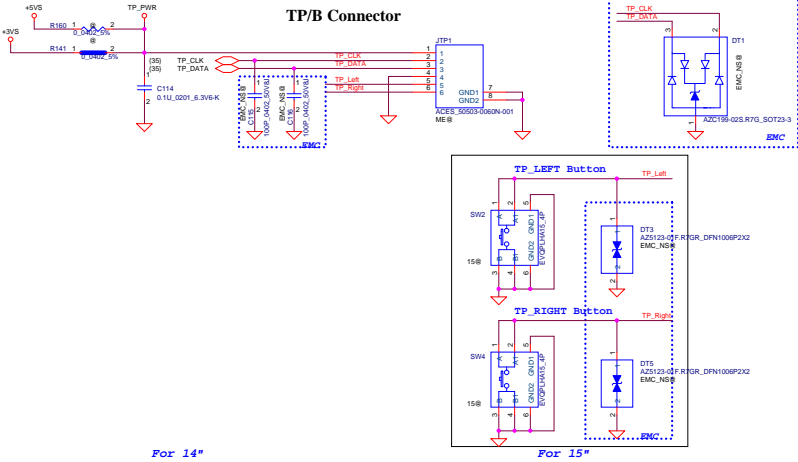
**ON/OFF switch**



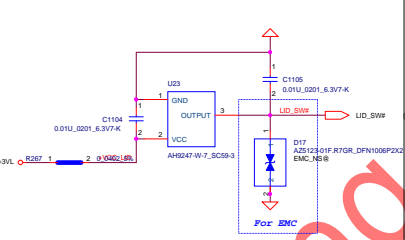
**K/B Connector**



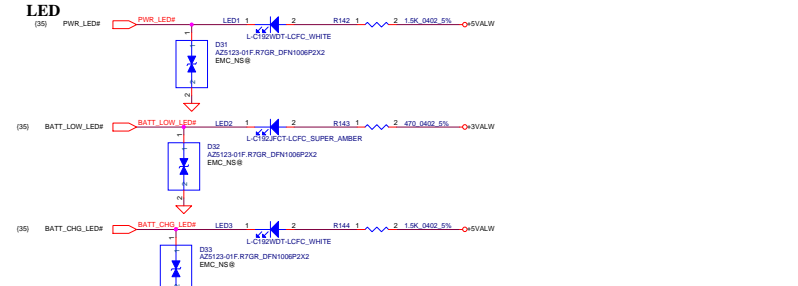
**TP/B Connector**



**PWR/B Connector**



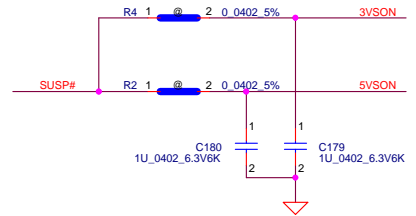
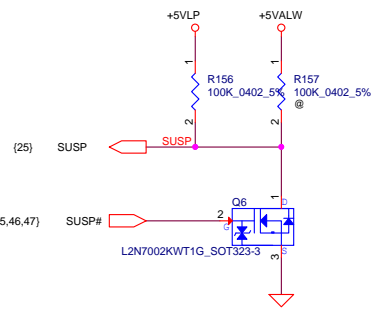
**USB I/O Connector**



For Huang.hu

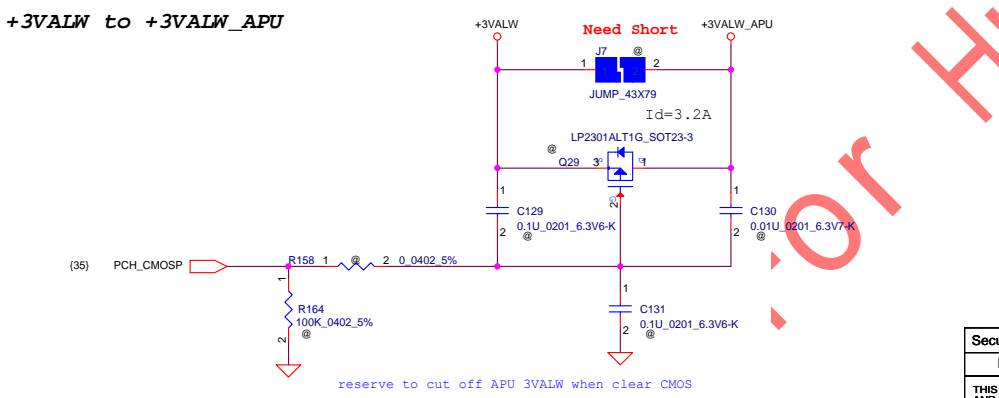
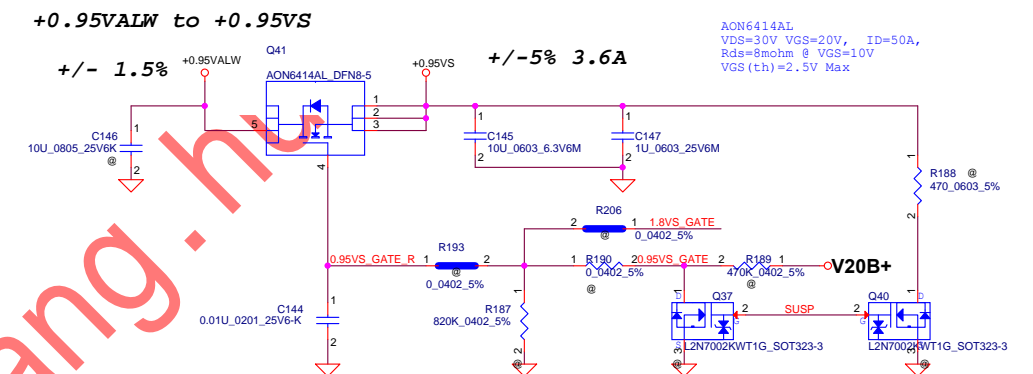
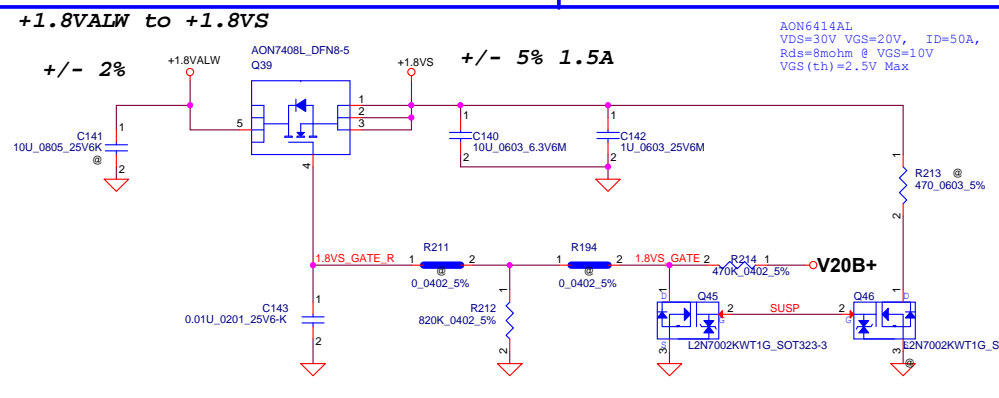
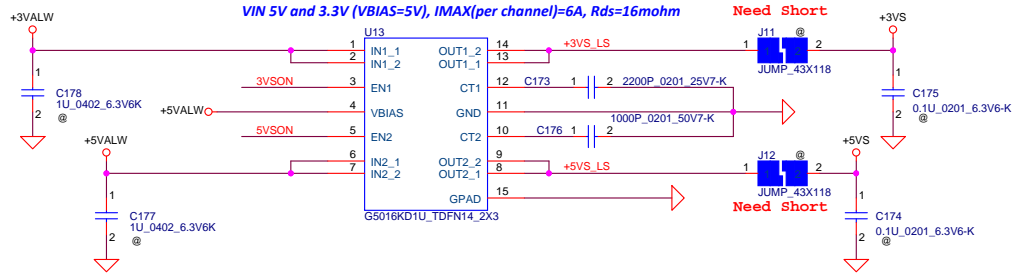
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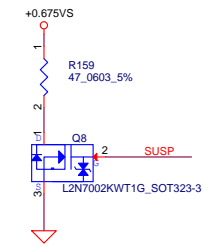



**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**

**+3VS, C173 --> 2.74ms**  
**+5VS, C176 --→ 2.03ms**

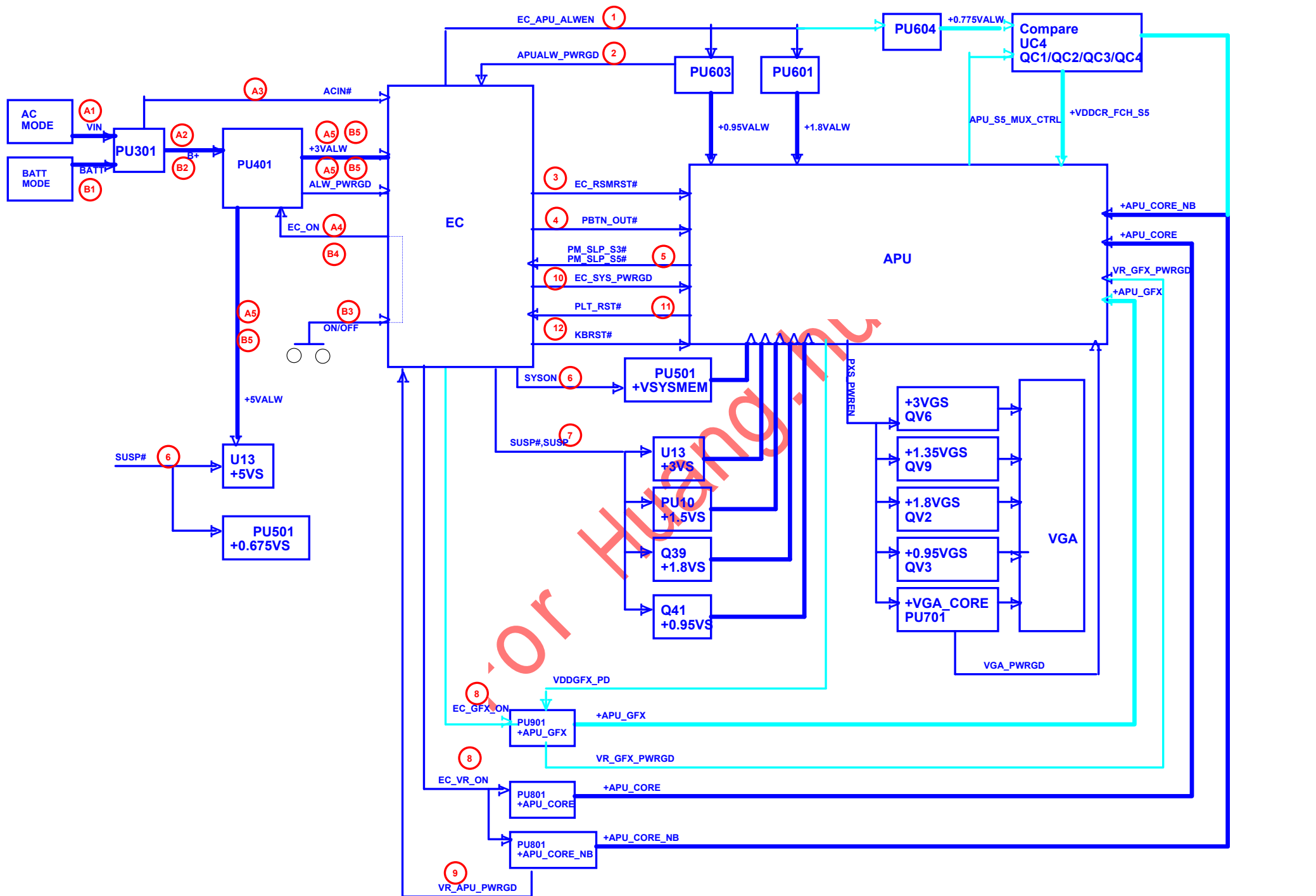



**For DisCharge**



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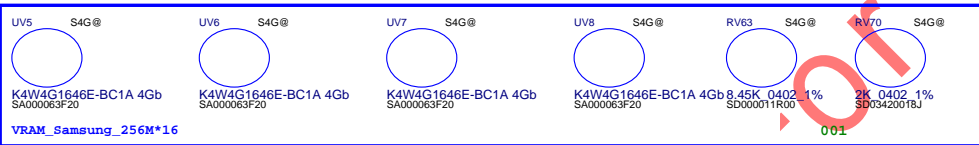
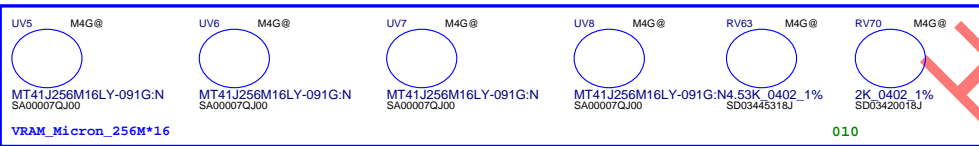
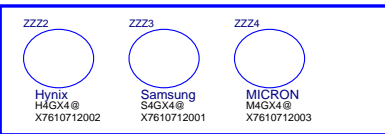
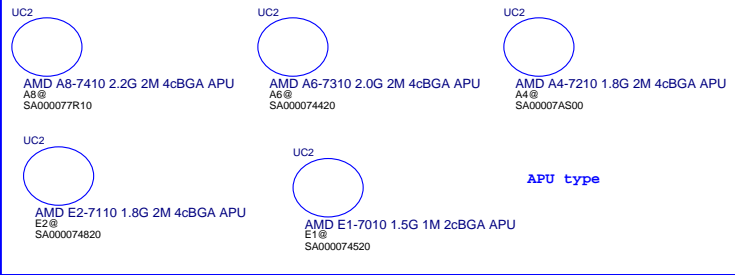
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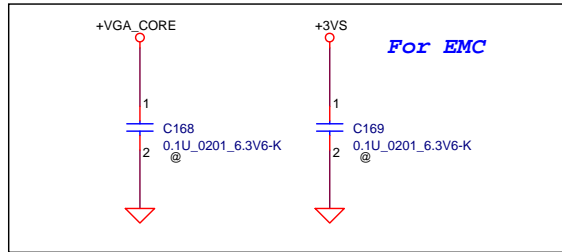
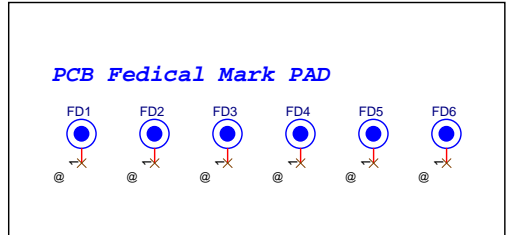
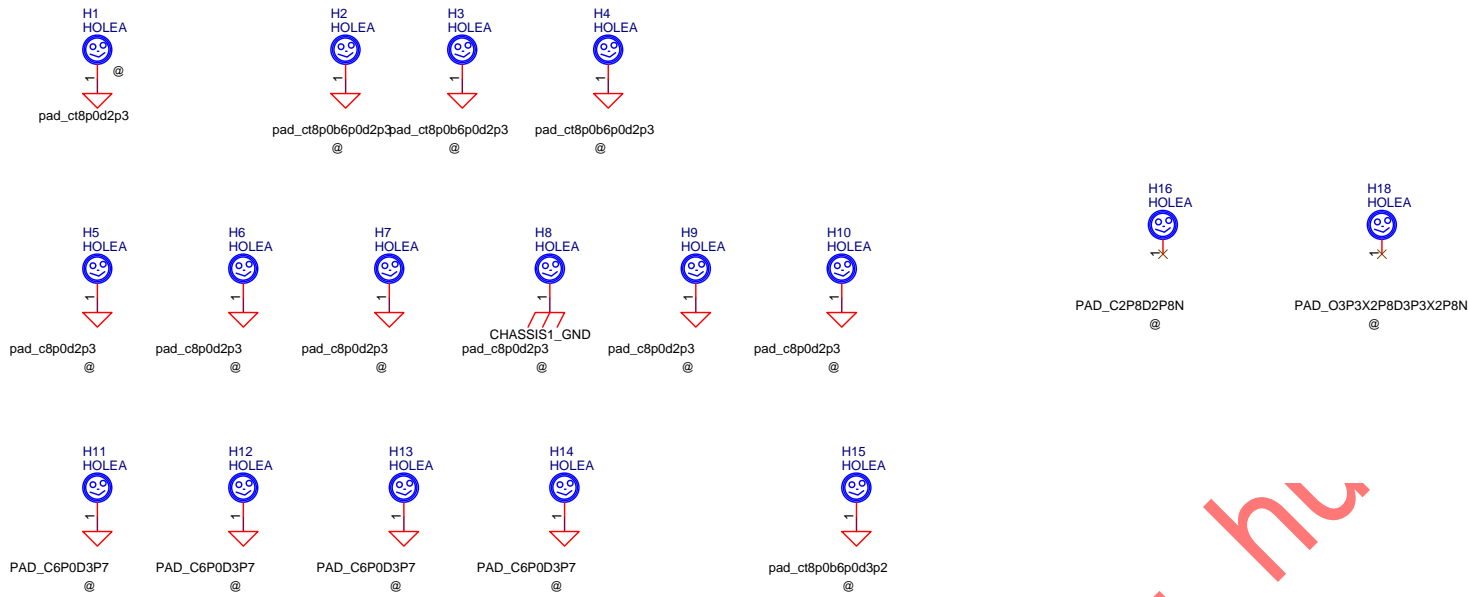
ZZZ1

PCB PN  
DAZ11X00100



VRAM ID config

Memory Type	VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K
	NA	111	4.75K
	NA	110	3.4K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K

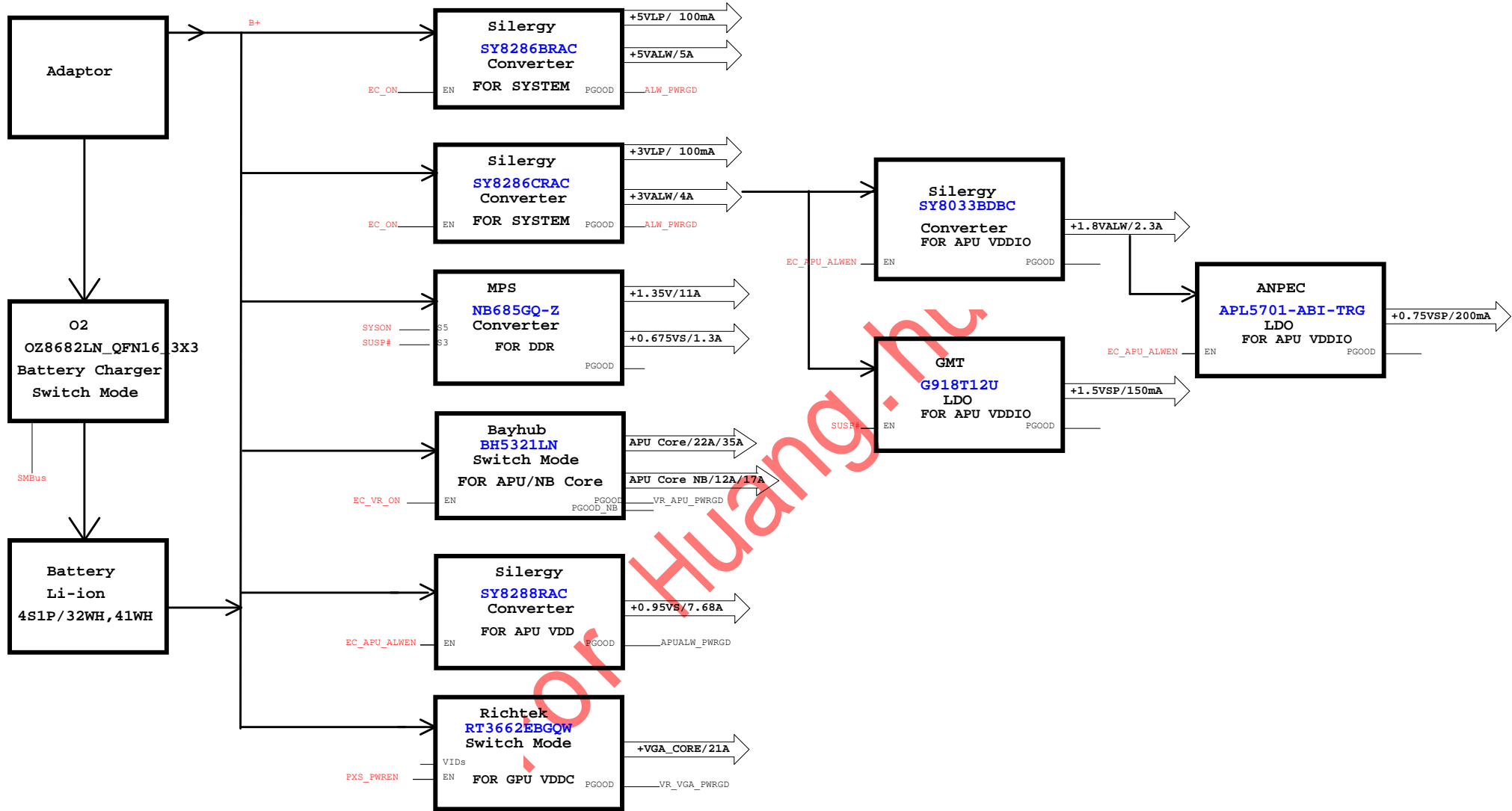


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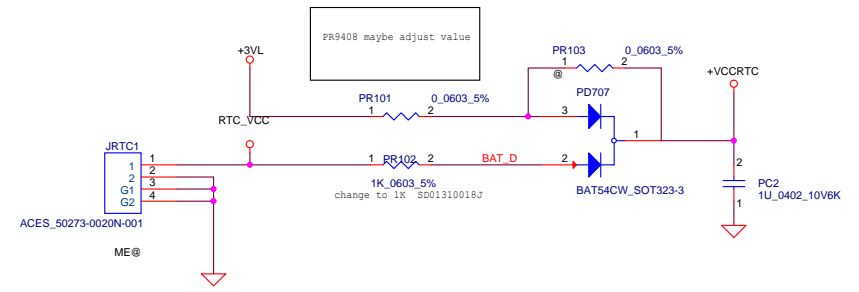
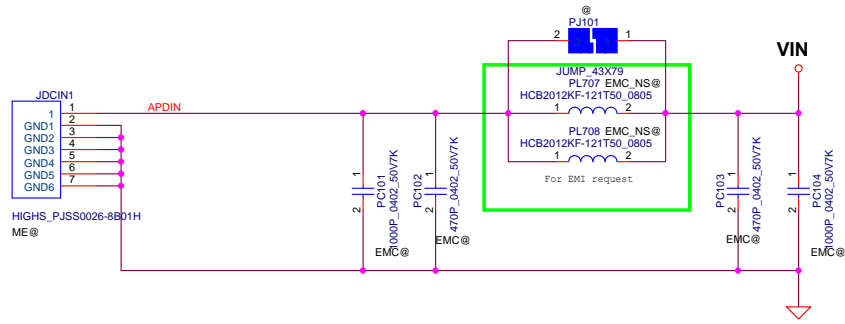
Title	Hole		
Document Number	CG521		
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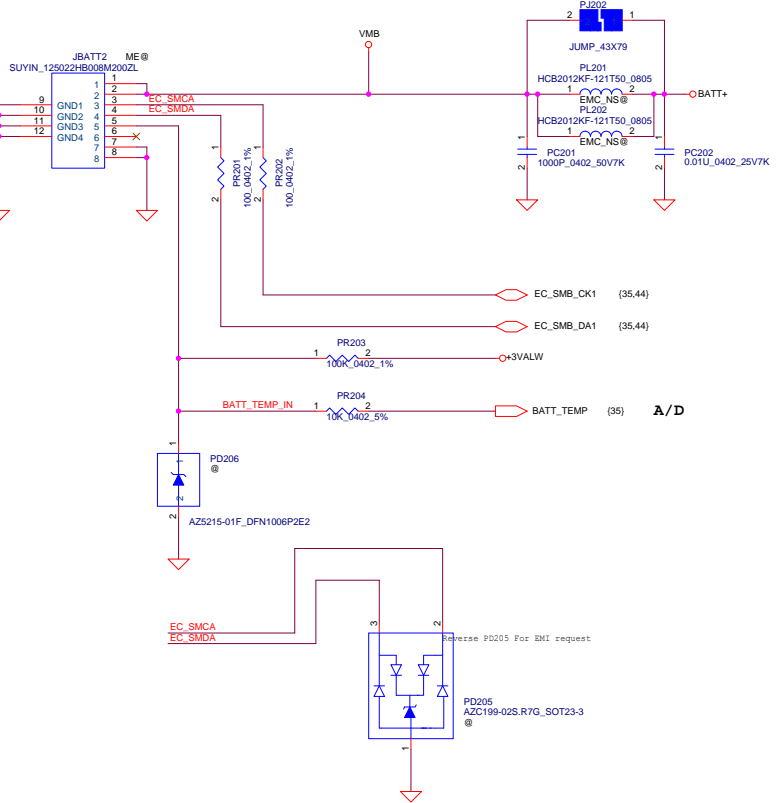


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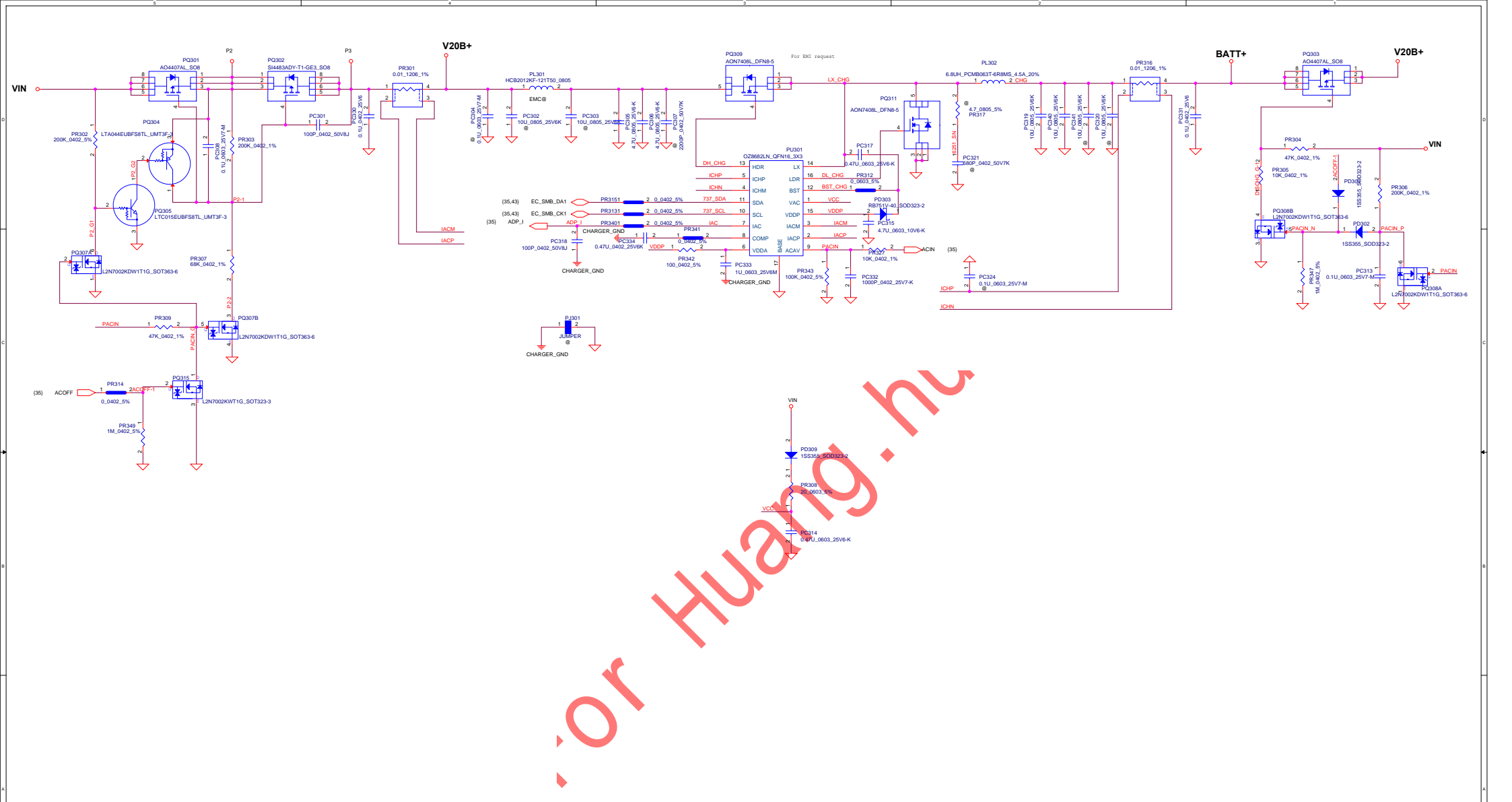
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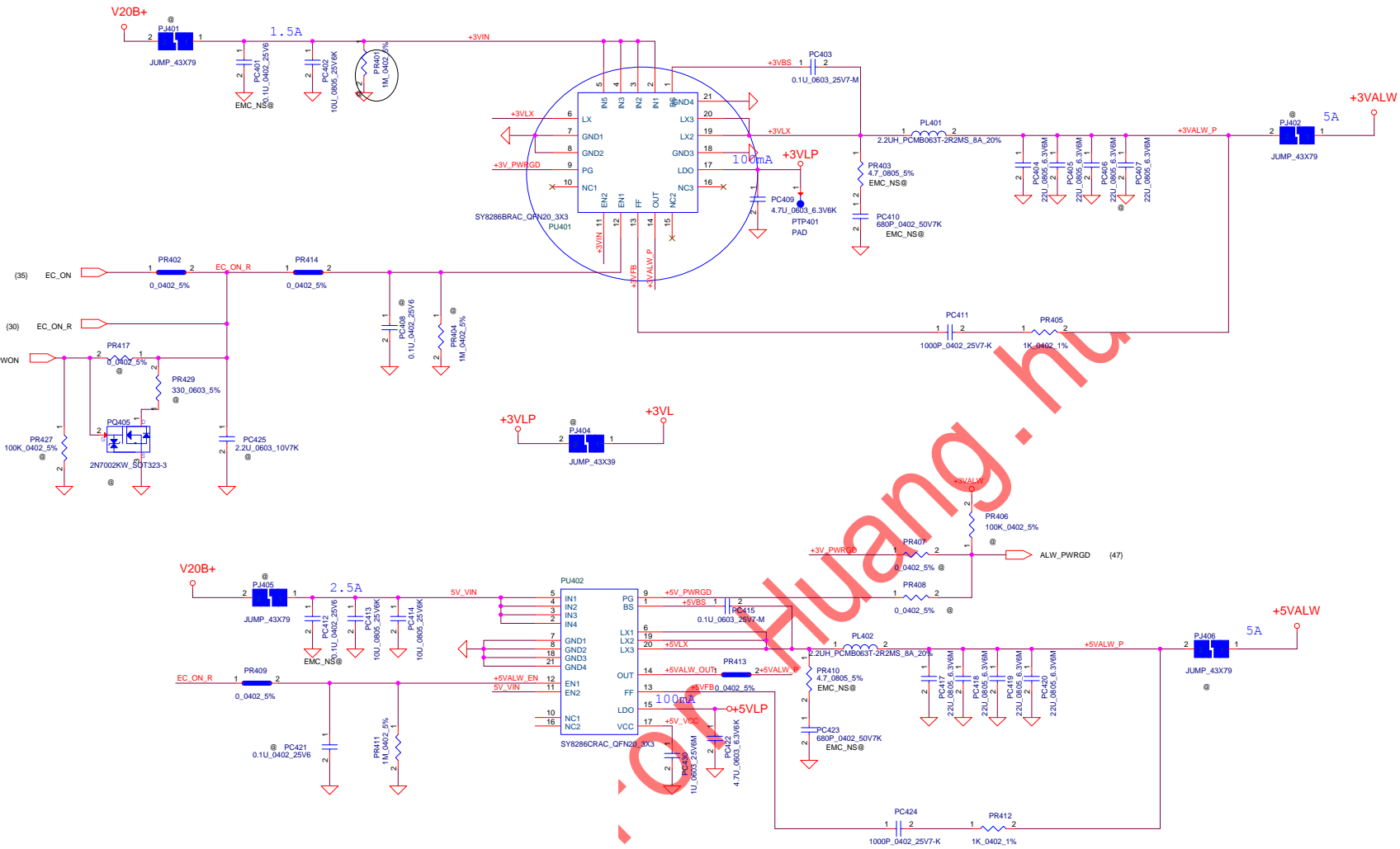
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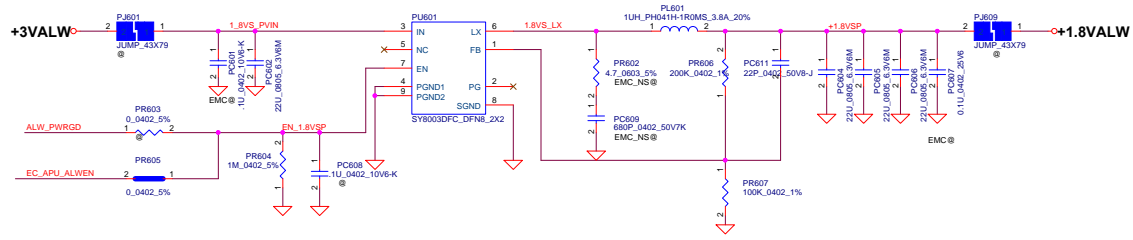
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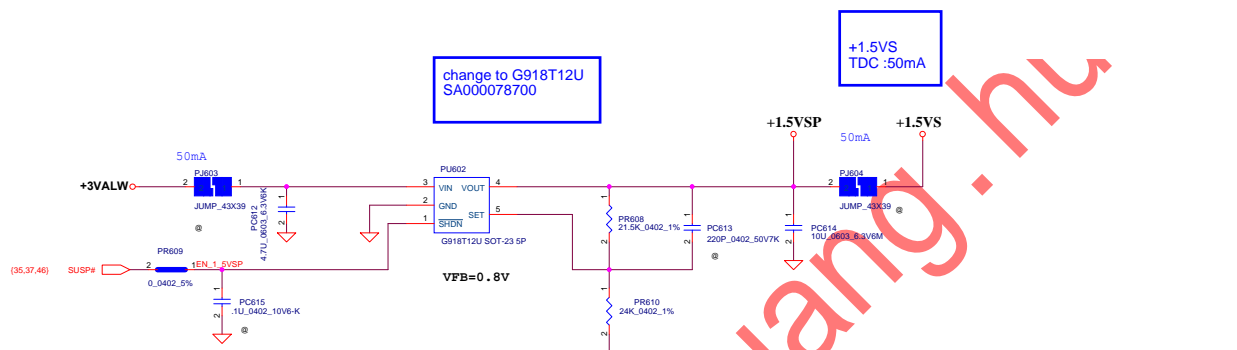


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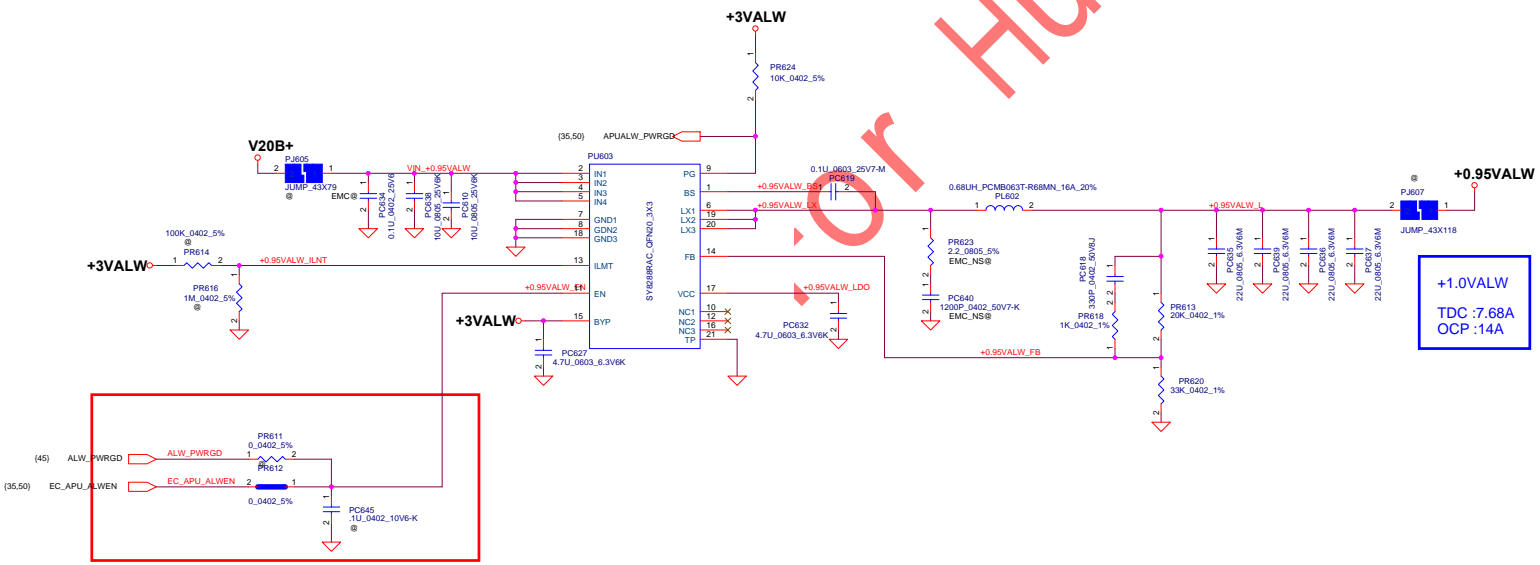


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OCP :3.8A

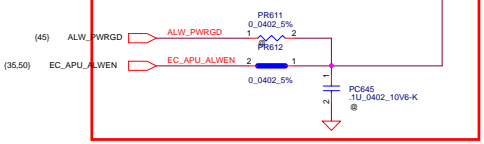


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change to G918T12U  
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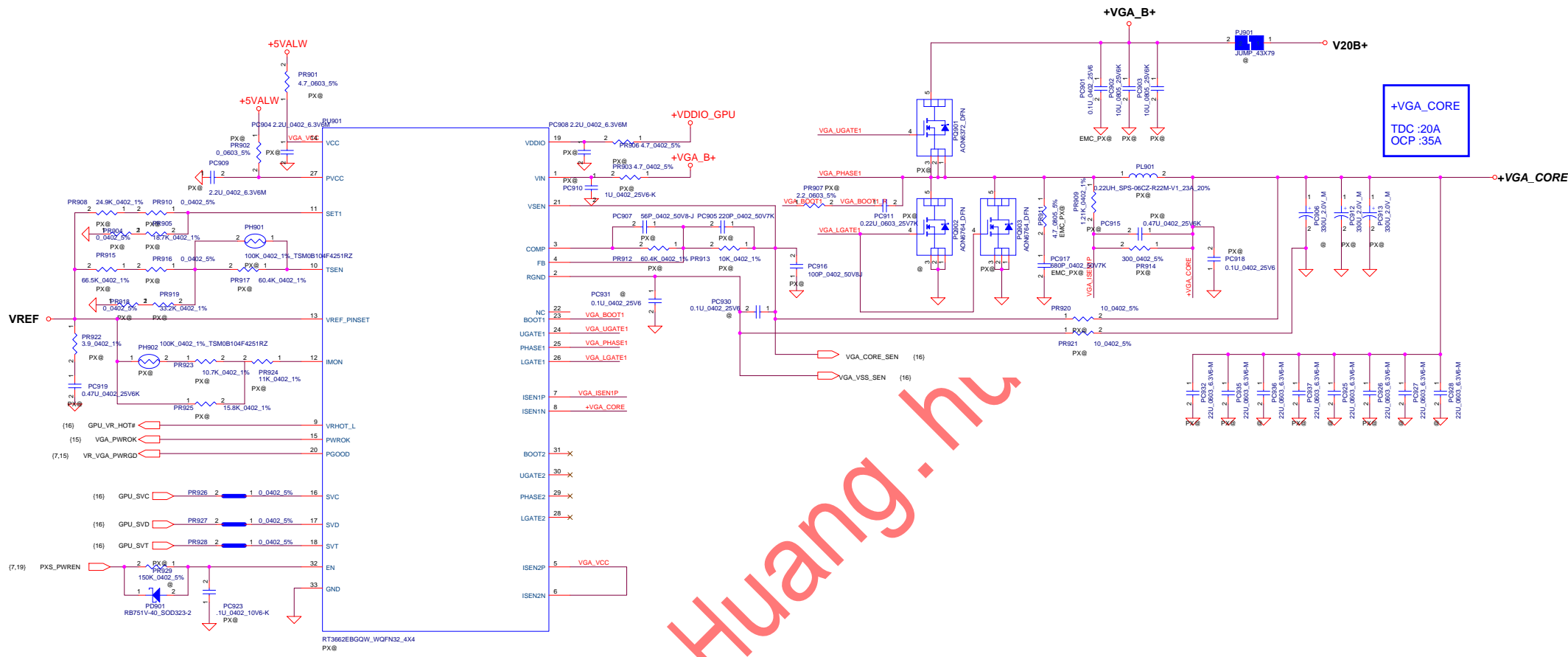


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OCP :14A



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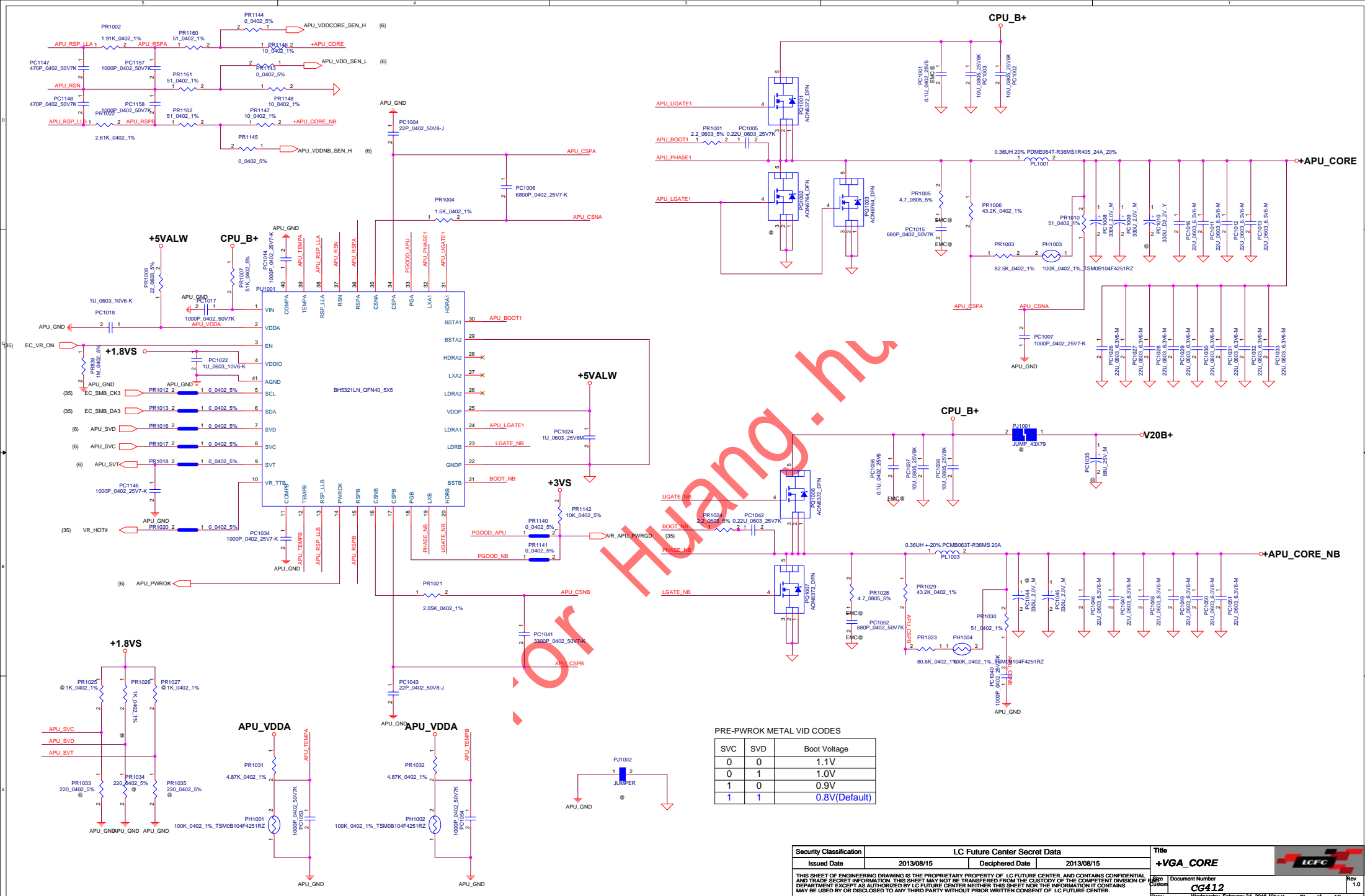


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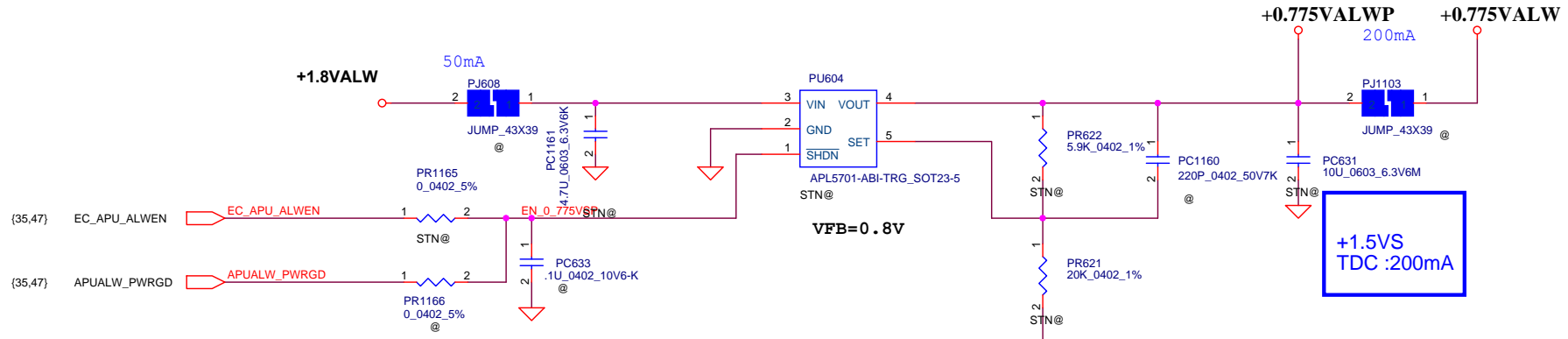
+VGA\_CORE  
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OCP :35A

**+3VGS**

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