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DY510/DY511 M/B Schematics Document

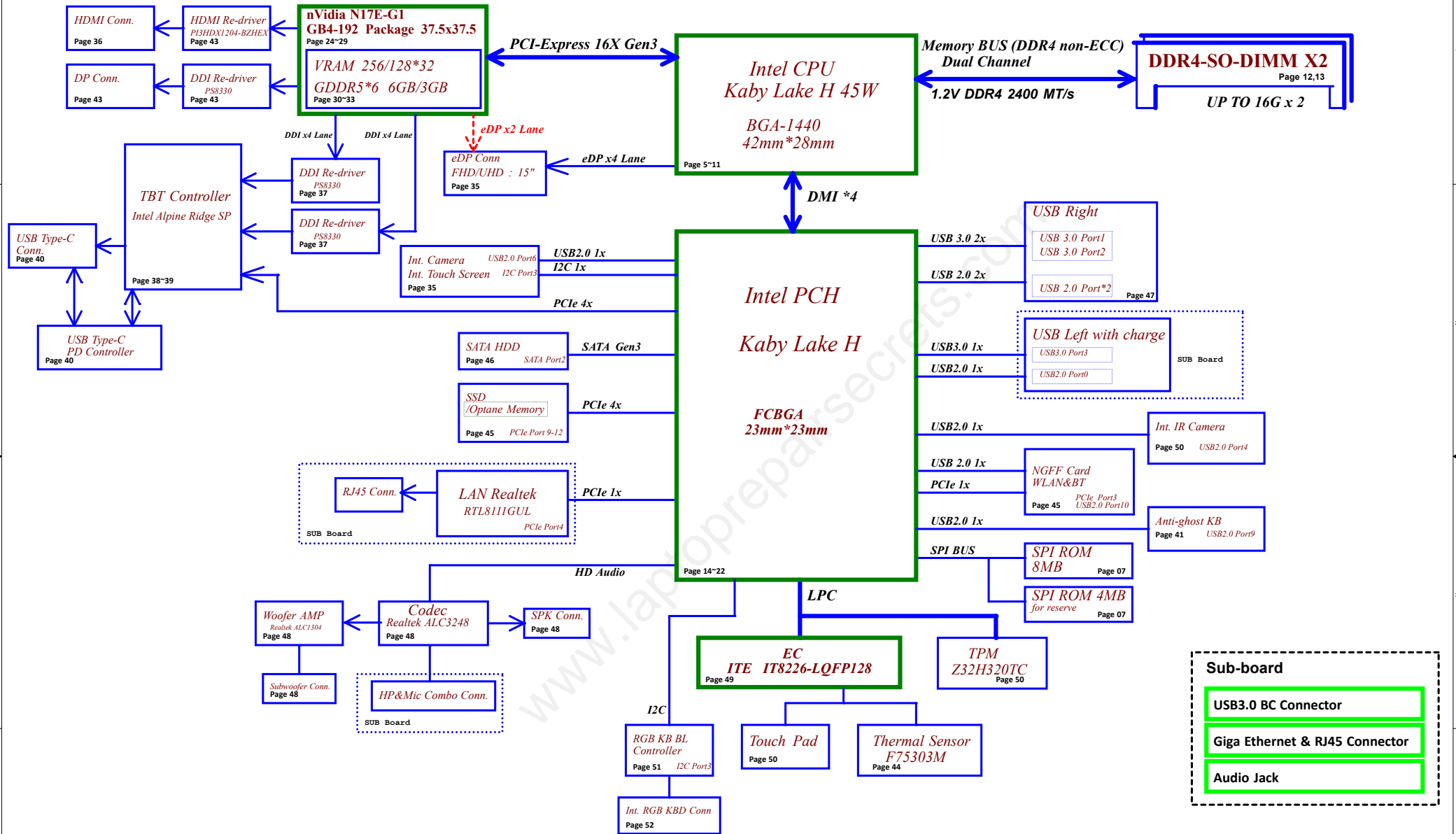
Intel Kabylake H-Processor with DDR4 + NV N17E-G1 GPU

MB NM-B163

2016-12-12

REV: 1.0

| | | | | | | |
|--|------------------------------|-----------------|------------|------------|---|---------------|
| Security Classification | LC Future Center Secret Data | | | Title |  | |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | Cover Page | | |
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| | | | | Custom | DY510/DY511 N17E-G1 | 1.0 |
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Voltage Rails (0 --> Means ON , X --> Means OFF)

| Power Plane | B+ | +3VALW | +3VALW_PCH | +1.2V | +5VS |
|--------------------------------------|----|--------|------------|-------|------------|
| | | | | | +3VS |
| State | | +5VALW | | | VCCIO |
| | | | | | VCCSA |
| | | | | | VCCSTG |
| | | | | | VCCCPUCORE |
| | | | | | VCCGFXCORE |
| | | | | | +1.8VS_AON |
| | | | | | +1.8VGS |
| | | | | | NVDD |
| | | | | | NVDDS |
| | | | | | +1.0VGS |
| | | | | | FBVDDQ |
| S0 | 0 | 0 | 0 | 0 | 0 |
| S3 | 0 | 0 | 0 | 0 | X |
| S3 Battery only | 0 | 0 | 0 | 0 | X |
| S5 S4/AC Only | 0 | 0 | 0 | X | X |
| S5 S4 Battery only | 0 | X | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X | X |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

| Port | Function |
|------|-------------|
| 1 | |
| 2 | Cardreader |
| 3 | WLAN |
| 4 | LAN |
| 5 | Thunderbolt |
| 6 | Thunderbolt |
| 7 | Thunderbolt |
| 8 | Thunderbolt |
| 9 | SSD |
| 10 | SSD |
| 11 | SSD |
| 12 | SSD |
| 13 | |
| 14 | |
| 15 | |
| 16 | |
| 17 | |
| 18 | |
| 19 | |

BOM Structure Table

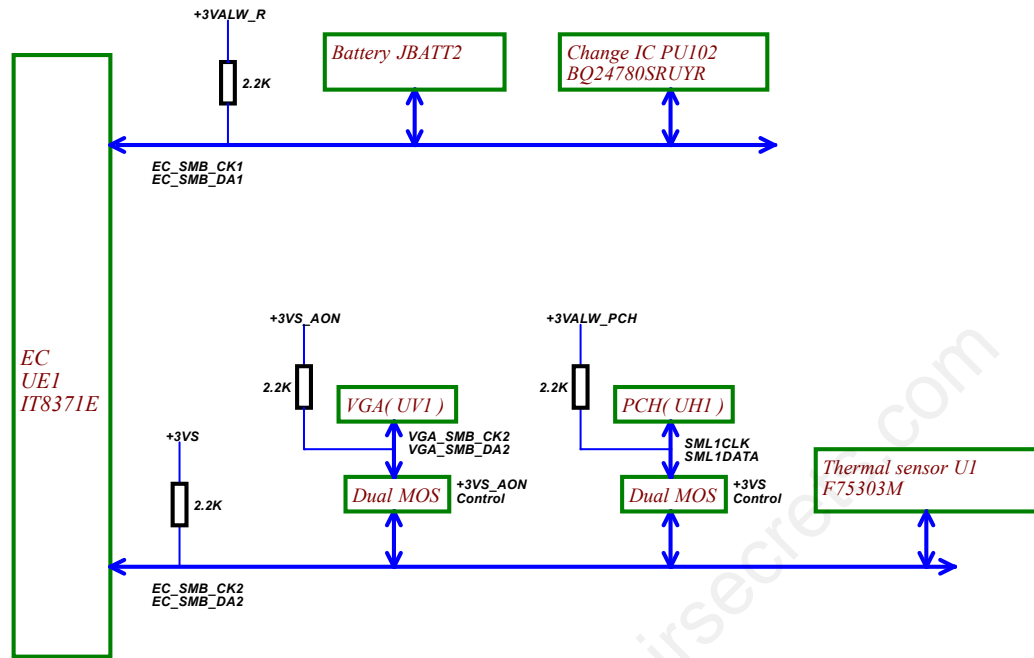
| BOM Structure | BTO Item |
|---------------|---------------------------------------|
| @ | Not stuff |
| AOAC@ | AOAC support part |
| GIGA@ | GIGA LAN Part |
| ME@ | ME part(connector, hole) |
| RANKA@ | For VRAM RankA part |
| RANKB@ | For VRAM RankB part |
| OPT@ | For GPU part |
| TS@ | For support touch panel sku part |
| TPM@ | For support TPM sku part |
| U31@ | For support USB re-driver part |
| IR@ | For support IR camera sku part |
| RGB@ | For support RGB KB Backlight sku part |
| N_KBL@ | For normal KB Backlight sku part |
| AG@ | For support Anti-ghost KB sku part |
| N_KB@ | For normal KB sku part |
| CD@ | Cost down part |
| XBOX@ | For support XBOX Module sku part |

| Port | Function |
|------|--------------------|
| 1 | Right USB2.0 |
| 2 | Left USB3.0 |
| 3 | Left USB3.0 |
| 4 | IR Camera |
| 5 | Touch Screen |
| 6 | Camera |
| 7 | |
| 8 | XBOX Module |
| 9 | Anti-ghost KB |
| 10 | Reserved for debug |
| 11 | Bluetooth |
| 12 | |
| 13 | |
| 14 | |

| Port | Function |
|------|-------------|
| 1 | Left USB3.0 |
| 2 | Left USB3.0 |
| 3 | |
| 4 | |
| 5 | |
| 6 | |

| Port | Function |
|------|-------------------|
| 0 | M.2 SSD SATA Gen3 |
| 1 | HDD SATA Gen3 |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

| | | | |
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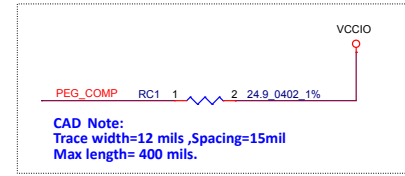
SMBUS Control Table

| | SOURCE | VGA | BATT | IT8226E | SODIMM | WLAN WLMAX | Thermal Sensor | PCH | TP Module | Charger | RGB KB Backlight | USB-C PD | HIFI Audio |
|------------------------------|---------------------|-----|------|---------|--------|------------|----------------|-----|-----------|---------|------------------|----------|------------|
| EC_SMB_CK1 EC_SMB_DA1 | IT8226E +3VALW_R | X | V | V | X | X | X | X | X | V | V | V | X |
| EC_SMB_CK2 EC_SMB_DA2 | IT8226E +3VS | V | X | V | X | X | V | V | X | X | X | X | V |
| PCH_SMBCLK PCH_SMBDATA | PCH +3VALW_PCH | X | X | X | V | V | X | V | V | X | X | X | X |
| PCH_SMBR_SCL PCH_SMBR_SDA | X | X | X | X | X | X | X | X | X | X | V | X | X |

| EC SM Bus1 address | | EC SM Bus2 address | | PCH SM Bus address | | PCH I2C 2 Bus address | |
|--------------------|-------------|------------------------|----------------|--------------------|----------------|-----------------------|----------------|
| Device | Address | Device | Address | Device | Address | Device | Address |
| Smart Battery | 0x16 | Thermal Sensor F75303M | 1001100a b | DSB D1000 | 1010 000x b | RGB Backlight | Need to update |
| Charger | 0001 0010 b | VGA | 0a2E (default) | DSB D1000 | 1010 000x b | | |
| | | PCH | Need to update | TP Module | Need to update | | |
| | | | | Wlan | Reserved | | |

[24] PCIE_CRX_GTX_N[0..15] [24]
 [24] PCIE_CRX_GTX_P[0..15] [24]

PCIE_CTX_C_GRX_N[0..15] [24]
 PCIE_CTX_C_GRX_P[0..15] [24]



| UC1C | | SKYLAKE_HALO | | BGA1440 | | | | | | |
|---------------------|-----|--------------|-------------|---------|------------------|------|------|---|--------------------|---------------------|
| PCIE_CRX_GTX_P15 | E25 | PEG_RXP[0] | PEG_TXP[0] | B25 | PCIE_CTX_GRX_P15 | OPT@ | CC32 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P15 |
| PCIE_CRX_GTX_N15 | D25 | PEG_RXN[0] | PEG_TXN[0] | A25 | PCIE_CTX_GRX_N15 | OPT@ | CC16 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N15 |
| PCIE_CRX_GTX_P14 | E24 | PEG_RXP[1] | PEG_TXP[1] | B24 | PCIE_CTX_GRX_P14 | OPT@ | CC31 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P14 |
| PCIE_CRX_GTX_N14 | F24 | PEG_RXN[1] | PEG_TXN[1] | C24 | PCIE_CTX_GRX_N14 | OPT@ | CC15 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N14 |
| PCIE_CRX_GTX_P13 | E23 | PEG_RXP[2] | PEG_TXP[2] | B23 | PCIE_CTX_GRX_P13 | OPT@ | CC30 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P13 |
| PCIE_CRX_GTX_N13 | D23 | PEG_RXN[2] | PEG_TXN[2] | A23 | PCIE_CTX_GRX_N13 | OPT@ | CC14 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N13 |
| PCIE_CRX_GTX_P12 | E22 | PEG_RXP[3] | PEG_TXP[3] | B22 | PCIE_CTX_GRX_P12 | OPT@ | CC29 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P12 |
| PCIE_CRX_GTX_N12 | F22 | PEG_RXN[3] | PEG_TXN[3] | C22 | PCIE_CTX_GRX_N12 | OPT@ | CC13 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N12 |
| PCIE_CRX_GTX_P11 | E21 | PEG_RXP[4] | PEG_TXP[4] | B21 | PCIE_CTX_GRX_P11 | OPT@ | CC28 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P11 |
| PCIE_CRX_GTX_N11 | D21 | PEG_RXN[4] | PEG_TXN[4] | A21 | PCIE_CTX_GRX_N11 | OPT@ | CC12 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N11 |
| PCIE_CRX_GTX_P10 | E20 | PEG_RXP[5] | PEG_TXP[5] | B20 | PCIE_CTX_GRX_P10 | OPT@ | CC27 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P10 |
| PCIE_CRX_GTX_N10 | F20 | PEG_RXN[5] | PEG_TXN[5] | C20 | PCIE_CTX_GRX_N10 | OPT@ | CC11 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N10 |
| PCIE_CRX_GTX_P9 | E19 | PEG_RXP[6] | PEG_TXP[6] | B19 | PCIE_CTX_GRX_P9 | OPT@ | CC26 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P9 |
| PCIE_CRX_GTX_N9 | D19 | PEG_RXN[6] | PEG_TXN[6] | A19 | PCIE_CTX_GRX_N9 | OPT@ | CC10 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N9 |
| PCIE_CRX_GTX_P8 | E18 | PEG_RXP[7] | PEG_TXP[7] | B18 | PCIE_CTX_GRX_P8 | OPT@ | CC25 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P8 |
| PCIE_CRX_GTX_N8 | F18 | PEG_RXN[7] | PEG_TXN[7] | C18 | PCIE_CTX_GRX_N8 | OPT@ | CC9 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N8 |
| PCIE_CRX_GTX_P7 | D17 | PEG_RXP[8] | PEG_TXP[8] | A17 | PCIE_CTX_GRX_P7 | OPT@ | CC24 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P7 |
| PCIE_CRX_GTX_N7 | E17 | PEG_RXN[8] | PEG_TXN[8] | B17 | PCIE_CTX_GRX_N7 | OPT@ | CC8 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N7 |
| PCIE_CRX_GTX_P6 | F16 | PEG_RXP[9] | PEG_TXP[9] | C16 | PCIE_CTX_GRX_P6 | OPT@ | CC23 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P6 |
| PCIE_CRX_GTX_N6 | E16 | PEG_RXN[9] | PEG_TXN[9] | B16 | PCIE_CTX_GRX_N6 | OPT@ | CC7 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N6 |
| PCIE_CRX_GTX_P5 | D15 | PEG_RXP[10] | PEG_TXP[10] | A15 | PCIE_CTX_GRX_P5 | OPT@ | CC22 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P5 |
| PCIE_CRX_GTX_N5 | E15 | PEG_RXN[10] | PEG_TXN[10] | B15 | PCIE_CTX_GRX_N5 | OPT@ | CC6 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N5 |
| PCIE_CRX_GTX_P4 | F14 | PEG_RXP[11] | PEG_TXP[11] | C14 | PCIE_CTX_GRX_P4 | OPT@ | CC21 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P4 |
| PCIE_CRX_GTX_N4 | E14 | PEG_RXN[11] | PEG_TXN[11] | B14 | PCIE_CTX_GRX_N4 | OPT@ | CC5 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N4 |
| PCIE_CRX_GTX_P3 | D13 | PEG_RXP[12] | PEG_TXP[12] | A13 | PCIE_CTX_GRX_P3 | OPT@ | CC20 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P3 |
| PCIE_CRX_GTX_N3 | E13 | PEG_RXN[12] | PEG_TXN[12] | B13 | PCIE_CTX_GRX_N3 | OPT@ | CC4 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N3 |
| PCIE_CRX_GTX_P2 | F12 | PEG_RXP[13] | PEG_TXP[13] | C12 | PCIE_CTX_GRX_P2 | OPT@ | CC19 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P2 |
| PCIE_CRX_GTX_N2 | E12 | PEG_RXN[13] | PEG_TXN[13] | B12 | PCIE_CTX_GRX_N2 | OPT@ | CC3 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N2 |
| PCIE_CRX_GTX_P1 | D11 | PEG_RXP[14] | PEG_TXP[14] | A11 | PCIE_CTX_GRX_P1 | OPT@ | CC18 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P1 |
| PCIE_CRX_GTX_N1 | E11 | PEG_RXN[14] | PEG_TXN[14] | B11 | PCIE_CTX_GRX_N1 | OPT@ | CC2 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N1 |
| PCIE_CRX_GTX_P0 | F10 | PEG_RXP[15] | PEG_TXP[15] | C10 | PCIE_CTX_GRX_P0 | OPT@ | CC17 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_P0 |
| PCIE_CRX_GTX_N0 | E10 | PEG_RXN[15] | PEG_TXN[15] | B10 | PCIE_CTX_GRX_N0 | OPT@ | CC1 | 1 | 2 0.22U 0402 10V6K | PCIE_CTX_C_GRX_N0 |
| PEG_COMP | G2 | PEG_RCOMP | | | | | | | | |
| [19] DMI_CRX_PTX_P0 | D8 | DMI_RXP[0] | DMI_TXP[0] | B8 | DMI_CTX_PRX_P0 | | | | | DMI_CTX_PRX_P0 [19] |
| [19] DMI_CRX_PTX_N0 | E8 | DMI_RXN[0] | DMI_TXN[0] | A8 | DMI_CTX_PRX_N0 | | | | | DMI_CTX_PRX_N0 [19] |
| [19] DMI_CRX_PTX_P1 | E6 | DMI_RXP[1] | DMI_TXP[1] | C6 | DMI_CTX_PRX_P1 | | | | | DMI_CTX_PRX_P1 [19] |
| [19] DMI_CRX_PTX_N1 | F6 | DMI_RXN[1] | DMI_TXN[1] | B6 | DMI_CTX_PRX_N1 | | | | | DMI_CTX_PRX_N1 [19] |
| [19] DMI_CRX_PTX_P2 | D5 | DMI_RXP[2] | DMI_TXP[2] | B5 | DMI_CTX_PRX_P2 | | | | | DMI_CTX_PRX_P2 [19] |
| [19] DMI_CRX_PTX_N2 | E5 | DMI_RXN[2] | DMI_TXN[2] | A5 | DMI_CTX_PRX_N2 | | | | | DMI_CTX_PRX_N2 [19] |
| [19] DMI_CRX_PTX_P3 | J8 | DMI_RXP[3] | DMI_TXP[3] | D4 | DMI_CTX_PRX_P3 | | | | | DMI_CTX_PRX_P3 [19] |
| [19] DMI_CRX_PTX_N3 | J9 | DMI_RXN[3] | DMI_TXN[3] | B4 | DMI_CTX_PRX_N3 | | | | | DMI_CTX_PRX_N3 [19] |

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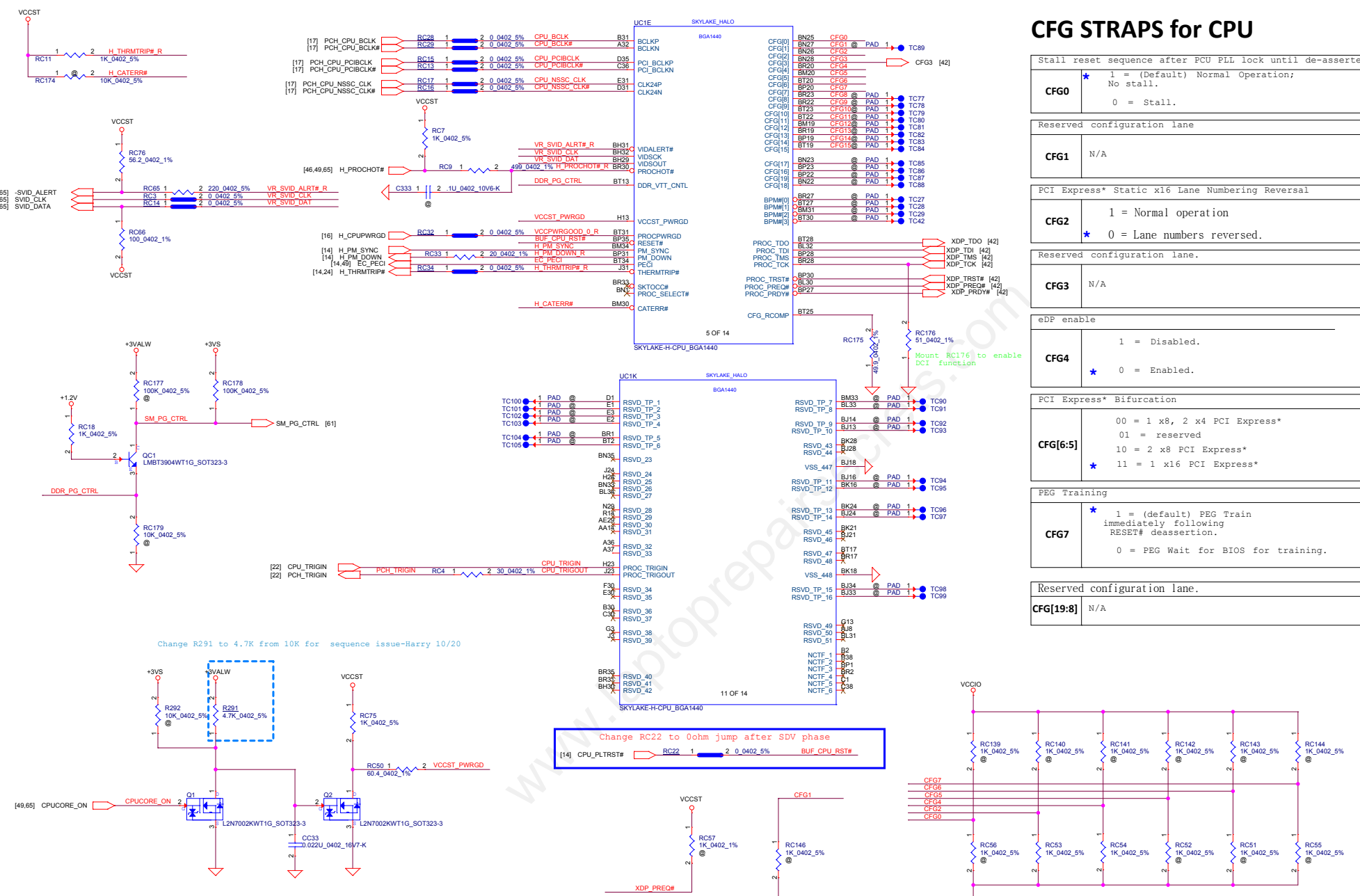
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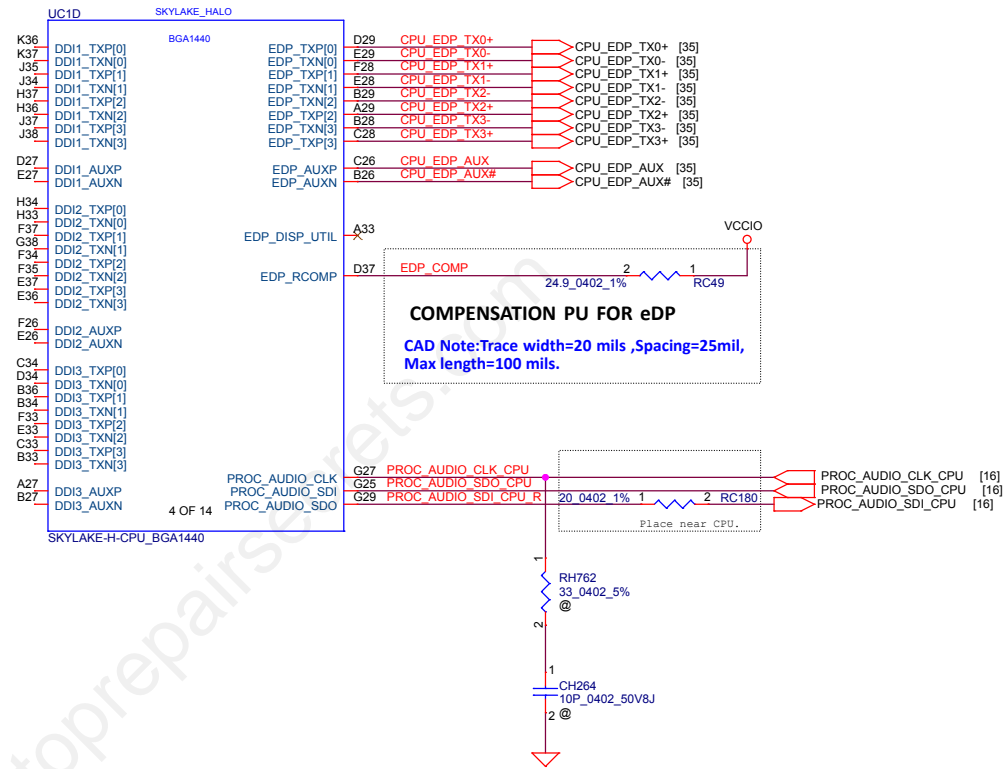
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CFG STRAPS for CPU

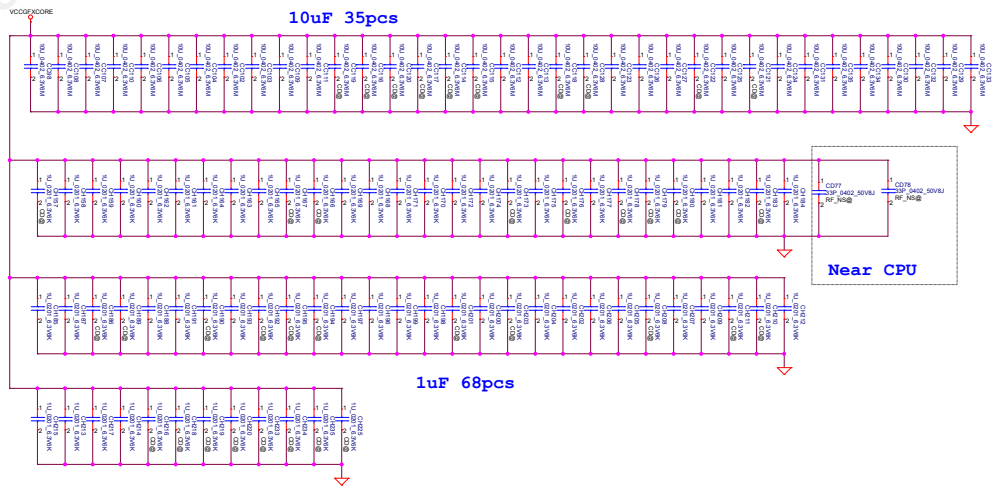
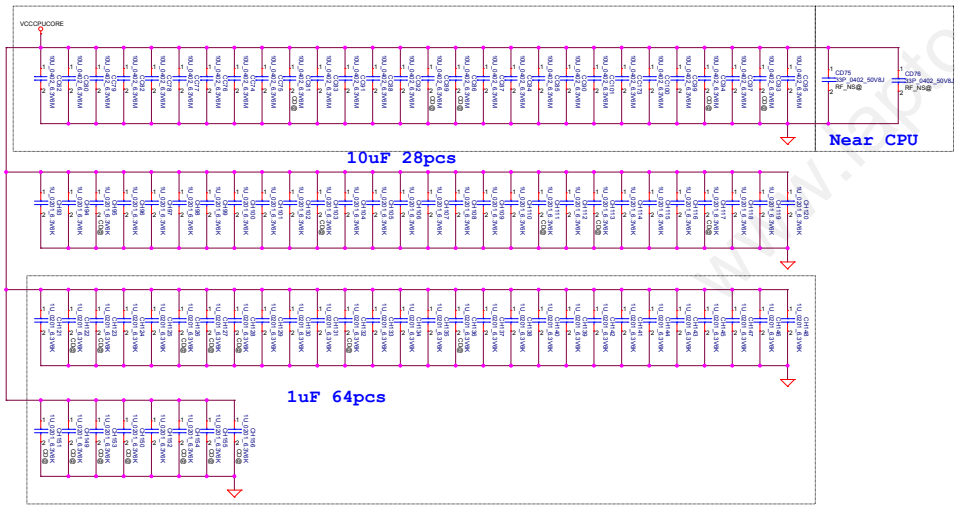
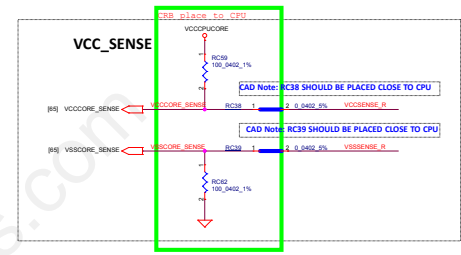
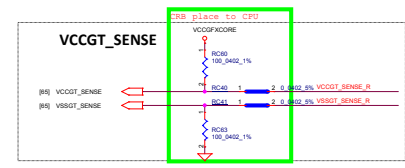
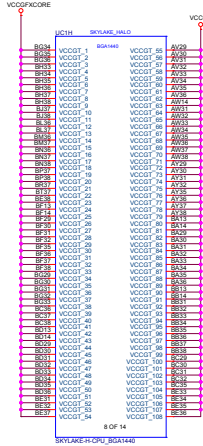
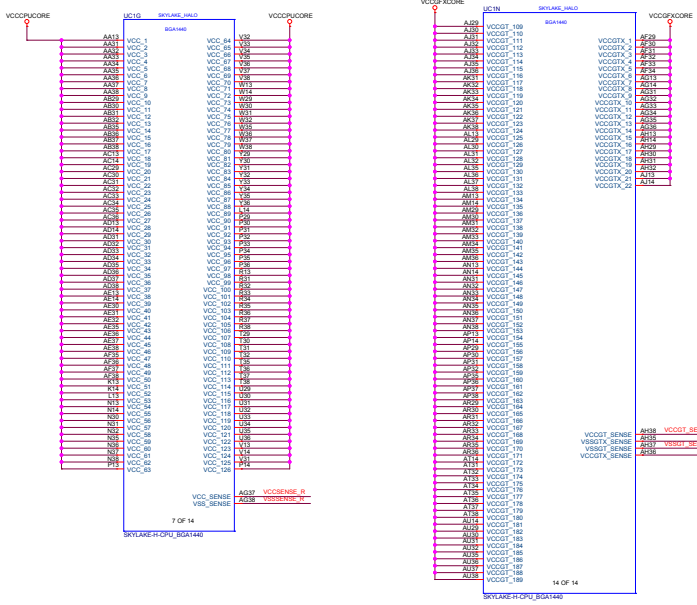
| | |
|---|--|
| Stall reset sequence after FCU PLL lock until de-asserted | |
| CFG0 | <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. |
| Reserved configuration lane | |
| CFG1 | N/A |
| PCI Express* Static x16 Lane Numbering Reversal | |
| CFG2 | <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. |
| Reserved configuration lane. | |
| CFG3 | N/A |
| eDP enable | |
| CFG4 | <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. |
| PCI Express* Bifurcation | |
| CFG[6:5] | <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* |
| PEG Training | |
| CFG7 | <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training. |
| Reserved configuration lane. | |
| CFG[19:8] | N/A |



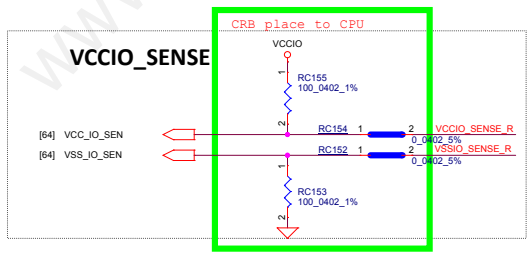
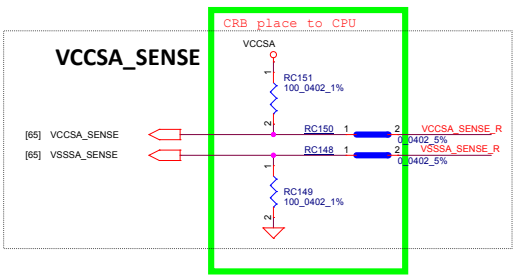
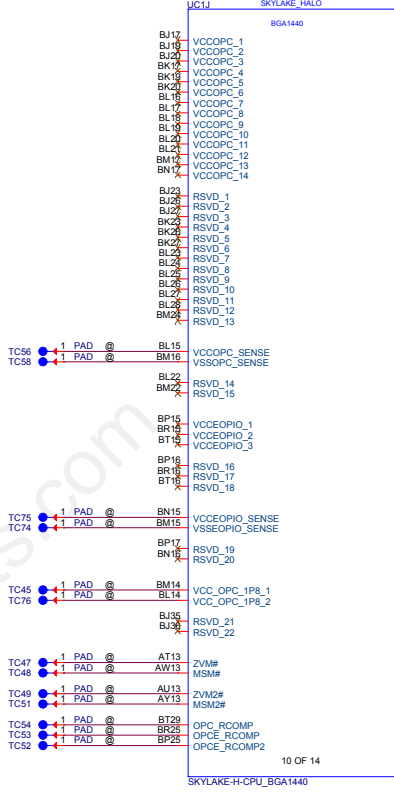
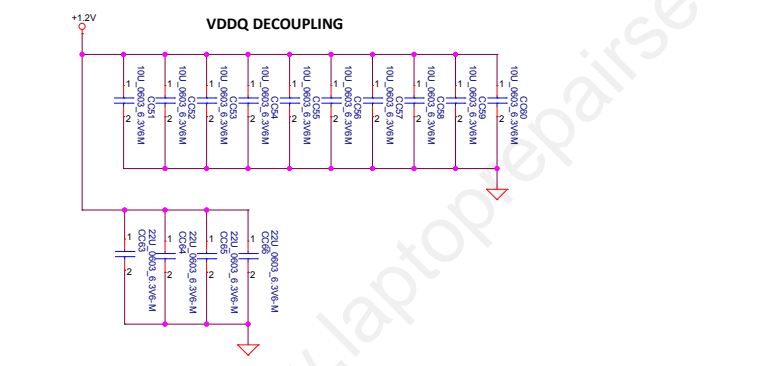
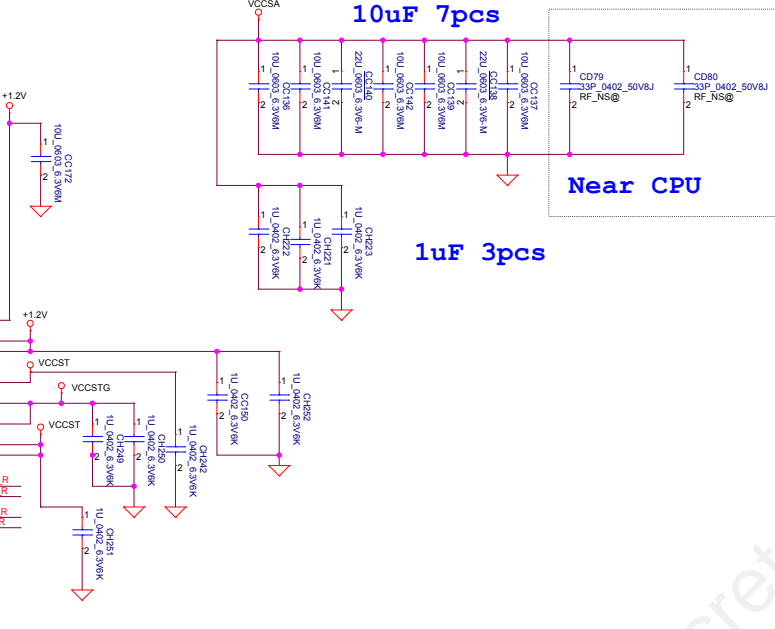
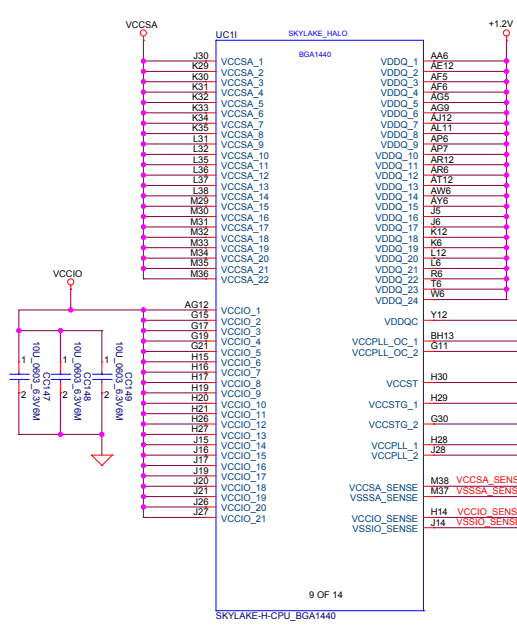


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|--------------------|---------------------------|---------------|
| Title | | |
| CPU (4/7) eDP, DDI | | |
| Size | Document Number | Rev |
| A3 | DY510/DY511 N17E-G1 | 1.0 |
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|--|-------------|------------------------------|------------|----------------------|--|
| Issued Date | 2015/02/26 | Design Date | 2016/02/26 | CPU (57) PWR, BYPASS | |
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| Doc No | DX510/DX511 | Rev | M1E-G1 | 14 | |
| <small>LC Future Center</small> | | | | | |



| UC1F | SKYLAKE_HALO | K1 |
|------|--------------|---------|
| Y38 | VSS_1 | VSS_78 |
| Y37 | VSS_2 | VSS_79 |
| Y14 | VSS_3 | VSS_80 |
| Y13 | VSS_4 | VSS_81 |
| Y11 | VSS_5 | VSS_82 |
| Y10 | VSS_6 | VSS_83 |
| Y9 | VSS_7 | VSS_84 |
| Y8 | VSS_8 | VSS_85 |
| Y7 | VSS_9 | VSS_86 |
| W34 | VSS_10 | VSS_87 |
| W33 | VSS_11 | VSS_88 |
| W12 | VSS_12 | VSS_89 |
| W5 | VSS_13 | VSS_90 |
| W4 | VSS_14 | VSS_91 |
| W3 | VSS_15 | VSS_92 |
| W2 | VSS_16 | VSS_93 |
| W1 | VSS_17 | VSS_94 |
| V29 | VSS_18 | VSS_95 |
| V6 | VSS_19 | VSS_96 |
| V5 | VSS_20 | VSS_97 |
| U36 | VSS_21 | VSS_98 |
| U37 | VSS_22 | VSS_99 |
| U6 | VSS_23 | VSS_100 |
| F34 | VSS_24 | VSS_101 |
| F33 | VSS_25 | VSS_102 |
| F14 | VSS_26 | VSS_103 |
| F13 | VSS_27 | VSS_104 |
| F12 | VSS_28 | VSS_105 |
| F11 | VSS_29 | VSS_106 |
| F10 | VSS_30 | VSS_107 |
| F9 | VSS_31 | VSS_108 |
| F8 | VSS_32 | VSS_109 |
| F7 | VSS_33 | VSS_110 |
| F5 | VSS_34 | VSS_111 |
| F4 | VSS_35 | VSS_112 |
| F3 | VSS_36 | VSS_113 |
| F2 | VSS_37 | VSS_114 |
| F1 | VSS_38 | VSS_115 |
| R30 | VSS_39 | VSS_116 |
| R29 | VSS_40 | VSS_117 |
| R12 | VSS_41 | VSS_118 |
| P38 | VSS_42 | VSS_119 |
| P37 | VSS_43 | VSS_120 |
| P12 | VSS_44 | VSS_121 |
| P6 | VSS_45 | VSS_122 |
| N34 | VSS_46 | VSS_123 |
| N33 | VSS_47 | VSS_124 |
| N12 | VSS_48 | VSS_125 |
| N11 | VSS_49 | VSS_126 |
| N10 | VSS_50 | VSS_127 |
| N9 | VSS_51 | VSS_128 |
| N8 | VSS_52 | VSS_129 |
| N7 | VSS_53 | VSS_130 |
| N6 | VSS_54 | VSS_131 |
| N5 | VSS_55 | VSS_132 |
| N4 | VSS_56 | VSS_133 |
| N3 | VSS_57 | VSS_134 |
| N2 | VSS_58 | VSS_135 |
| N1 | VSS_59 | VSS_136 |
| M14 | VSS_60 | VSS_137 |
| M13 | VSS_61 | VSS_138 |
| M12 | VSS_62 | VSS_139 |
| M6 | VSS_63 | VSS_140 |
| L34 | VSS_64 | VSS_141 |
| L33 | VSS_65 | VSS_142 |
| L29 | VSS_66 | VSS_143 |
| L30 | VSS_67 | VSS_144 |
| K38 | VSS_68 | VSS_145 |
| K11 | VSS_69 | VSS_146 |
| K10 | VSS_70 | VSS_147 |
| K9 | VSS_71 | VSS_148 |
| K8 | VSS_72 | VSS_149 |
| K7 | VSS_73 | VSS_150 |
| K5 | VSS_74 | VSS_151 |
| K4 | VSS_75 | VSS_152 |
| K3 | VSS_76 | VSS_153 |
| K2 | VSS_77 | VSS_154 |

NCTFVSS_1
6 OF 14

SKYLAKE-H-CPU_BGA1440

| UC1L | SKYLAKE_HALO | C25 |
|------|--------------|---------|
| C17 | VSS_154 | VSS_239 |
| C15 | VSS_155 | VSS_240 |
| C9 | VSS_156 | VSS_241 |
| B122 | VSS_157 | VSS_242 |
| B126 | VSS_158 | VSS_243 |
| B124 | VSS_159 | VSS_244 |
| B121 | VSS_160 | VSS_245 |
| B118 | VSS_161 | VSS_246 |
| B114 | VSS_162 | VSS_247 |
| B112 | VSS_163 | VSS_248 |
| B19 | VSS_164 | VSS_249 |
| B15 | VSS_165 | VSS_250 |
| B10 | VSS_166 | VSS_251 |
| BR36 | VSS_167 | VSS_252 |
| BR34 | VSS_168 | VSS_253 |
| BR29 | VSS_169 | VSS_254 |
| BR26 | VSS_170 | VSS_255 |
| BR24 | VSS_171 | VSS_256 |
| BR21 | VSS_172 | VSS_257 |
| BR19 | VSS_173 | VSS_258 |
| BR18 | VSS_174 | VSS_259 |
| BR14 | VSS_175 | VSS_260 |
| BR7 | VSS_176 | VSS_261 |
| BP34 | VSS_177 | VSS_262 |
| BP33 | VSS_178 | VSS_263 |
| BP29 | VSS_179 | VSS_264 |
| BP26 | VSS_180 | VSS_265 |
| BP24 | VSS_181 | VSS_266 |
| BP21 | VSS_182 | VSS_267 |
| BP18 | VSS_183 | VSS_268 |
| BP14 | VSS_184 | VSS_269 |
| BP12 | VSS_185 | VSS_270 |
| BP7 | VSS_186 | VSS_271 |
| BN34 | VSS_187 | VSS_272 |
| BN31 | VSS_188 | VSS_273 |
| BN30 | VSS_189 | VSS_274 |
| BN29 | VSS_190 | VSS_275 |
| BN24 | VSS_191 | VSS_276 |
| BN21 | VSS_192 | VSS_277 |
| BN20 | VSS_193 | VSS_278 |
| BN19 | VSS_194 | VSS_279 |
| BN18 | VSS_195 | VSS_280 |
| BN14 | VSS_196 | VSS_281 |
| BN12 | VSS_197 | VSS_282 |
| BN6 | VSS_198 | VSS_283 |
| BN7 | VSS_199 | VSS_284 |
| BN4 | VSS_200 | VSS_285 |
| BN2 | VSS_201 | VSS_286 |
| BM38 | VSS_202 | VSS_287 |
| BM36 | VSS_203 | VSS_288 |
| BM35 | VSS_204 | VSS_289 |
| BM28 | VSS_205 | VSS_290 |
| BM27 | VSS_206 | VSS_291 |
| BM26 | VSS_207 | VSS_292 |
| BM23 | VSS_208 | VSS_293 |
| BM21 | VSS_209 | VSS_294 |
| BM13 | VSS_210 | VSS_295 |
| BM12 | VSS_211 | VSS_296 |
| BM6 | VSS_212 | VSS_297 |
| BM2 | VSS_213 | VSS_298 |
| BL26 | VSS_214 | VSS_299 |
| BK29 | VSS_215 | |
| BK15 | VSS_216 | |
| BK14 | VSS_217 | |
| BK12 | VSS_218 | |
| BK11 | VSS_219 | |
| BL25 | VSS_220 | |
| BL22 | VSS_221 | |
| BH14 | VSS_222 | |
| BH12 | VSS_223 | |
| BH9 | VSS_224 | |
| BH8 | VSS_225 | |
| BH5 | VSS_226 | |
| BH4 | VSS_227 | |
| BH1 | VSS_228 | |
| BG38 | VSS_229 | |
| BG13 | VSS_230 | |
| BC12 | VSS_231 | |
| BF33 | VSS_232 | |
| BF12 | VSS_233 | |
| BE20 | VSS_234 | |
| BE6 | VSS_235 | |
| BE9 | VSS_236 | |
| BC34 | VSS_237 | |
| BC12 | VSS_238 | |

NCTFVSS_2
NCTFVSS_3
NCTFVSS_4
NCTFVSS_5
NCTFVSS_6
NCTFVSS_7

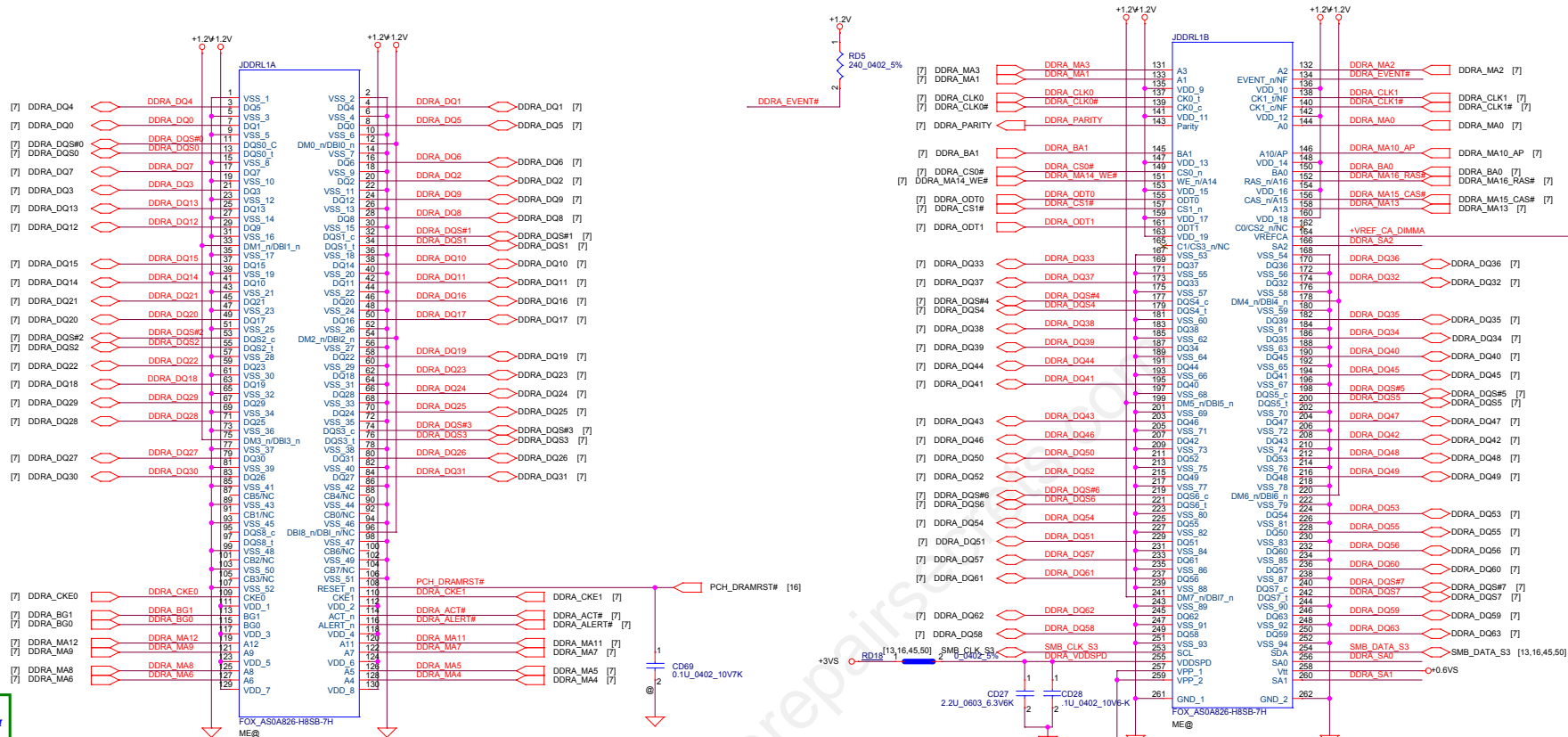
12 OF 14
SKYLAKE-H-CPU_BGA1440

| UC1M | SKYLAKE_HALO | AK30 |
|------|--------------|---------|
| B84 | VSS_300 | VSS_378 |
| B83 | VSS_301 | VSS_379 |
| B82 | VSS_302 | VSS_380 |
| B81 | VSS_303 | VSS_381 |
| B80 | VSS_304 | VSS_382 |
| BA37 | VSS_305 | VSS_383 |
| BA36 | VSS_306 | VSS_384 |
| BA10 | VSS_307 | VSS_385 |
| BA9 | VSS_308 | VSS_386 |
| BA5 | VSS_309 | VSS_387 |
| BA7 | VSS_310 | VSS_388 |
| BA6 | VSS_311 | VSS_389 |
| BA9 | VSS_312 | VSS_390 |
| AV34 | VSS_313 | VSS_391 |
| AV14 | VSS_314 | VSS_392 |
| AV33 | VSS_315 | VSS_393 |
| AV12 | VSS_316 | VSS_394 |
| AV30 | VSS_317 | VSS_395 |
| AW29 | VSS_318 | VSS_396 |
| AW12 | VSS_319 | VSS_397 |
| AW5 | VSS_320 | VSS_398 |
| AW4 | VSS_321 | VSS_399 |
| AW3 | VSS_322 | VSS_400 |
| AW2 | VSS_323 | VSS_401 |
| AW1 | VSS_324 | VSS_402 |
| AV38 | VSS_325 | VSS_403 |
| AV37 | VSS_326 | VSS_404 |
| AV36 | VSS_327 | VSS_405 |
| AU33 | VSS_328 | VSS_406 |
| AU32 | VSS_329 | VSS_407 |
| AU31 | VSS_330 | VSS_408 |
| AU30 | VSS_331 | VSS_409 |
| AU10 | VSS_332 | VSS_410 |
| AU9 | VSS_333 | VSS_411 |
| AU7 | VSS_334 | VSS_412 |
| AU6 | VSS_335 | VSS_413 |
| AT30 | VSS_336 | VSS_414 |
| AT29 | VSS_337 | VSS_415 |
| AT8 | VSS_338 | VSS_416 |
| AR38 | VSS_339 | VSS_417 |
| AR37 | VSS_340 | VSS_418 |
| AR36 | VSS_341 | VSS_419 |
| AR13 | VSS_342 | VSS_420 |
| AR5 | VSS_343 | VSS_421 |
| AR4 | VSS_344 | VSS_422 |
| AR3 | VSS_345 | VSS_423 |
| AR2 | VSS_346 | VSS_424 |
| AR1 | VSS_347 | VSS_425 |
| AP34 | VSS_348 | VSS_426 |
| AP33 | VSS_349 | VSS_427 |
| AP12 | VSS_350 | VSS_428 |
| AP11 | VSS_351 | VSS_429 |
| AP10 | VSS_352 | VSS_430 |
| AP9 | VSS_353 | VSS_431 |
| AP8 | VSS_354 | VSS_432 |
| AN30 | VSS_355 | VSS_433 |
| AN29 | VSS_356 | VSS_434 |
| AN12 | VSS_357 | VSS_435 |
| AN6 | VSS_358 | VSS_436 |
| AN5 | VSS_359 | VSS_437 |
| AN3 | VSS_360 | VSS_438 |
| AM38 | VSS_361 | VSS_439 |
| AM12 | VSS_362 | VSS_440 |
| AM5 | VSS_363 | VSS_441 |
| AM4 | VSS_364 | VSS_442 |
| AM3 | VSS_365 | VSS_443 |
| AM2 | VSS_366 | VSS_444 |
| AM1 | VSS_367 | VSS_445 |
| AL34 | VSS_368 | VSS_446 |
| AL33 | VSS_369 | |
| AL14 | VSS_370 | |
| AL12 | VSS_371 | |
| AL10 | VSS_372 | |
| AL9 | VSS_373 | |
| AL8 | VSS_374 | |
| AL7 | VSS_375 | |
| AL4 | VSS_376 | |
| AL3 | VSS_377 | |

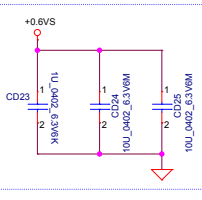
13 OF 14

SKYLAKE-H-CPU_BGA1440

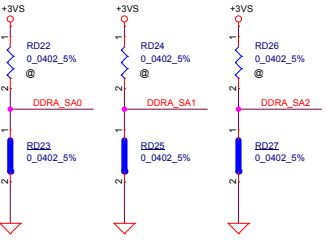
DDR4 SO-DIMM A



Layout Note: Place near DIMM

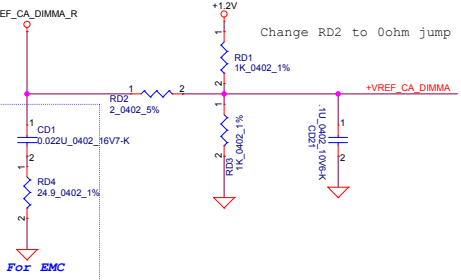


Note: VREF trace width:20 mils at least Spacing:20mils to other signal/planes Place near DIMM socket

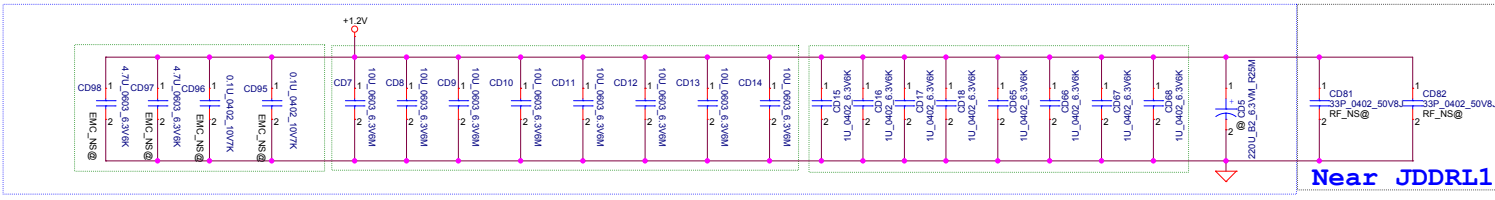


SPD Address = 0H


Layout Note: Place near DIMM



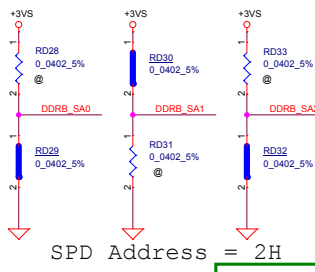
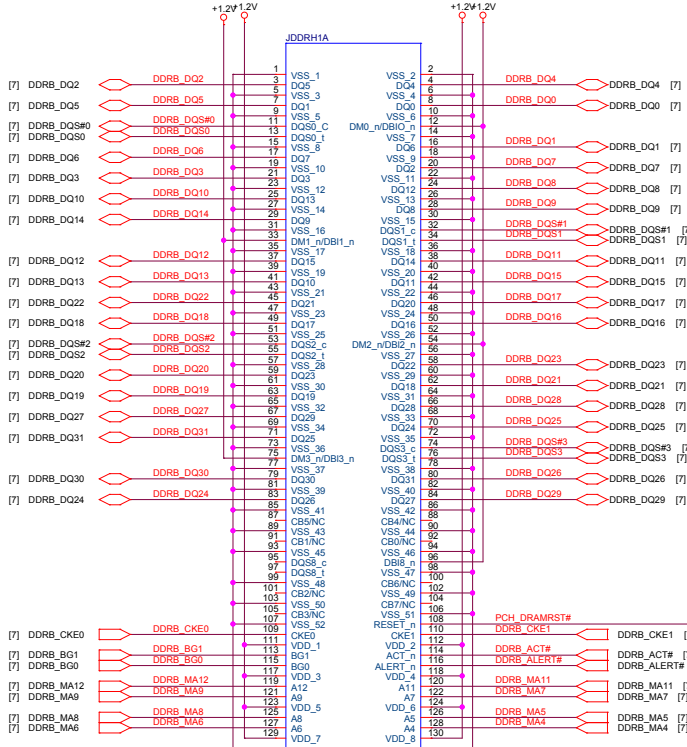
For EMC



Near JDDR11

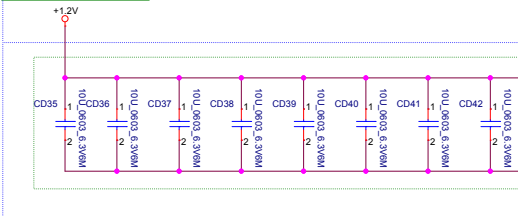
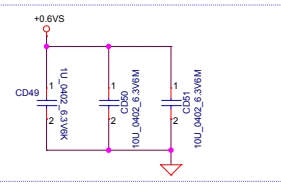
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DDR4 SO-DIMM B

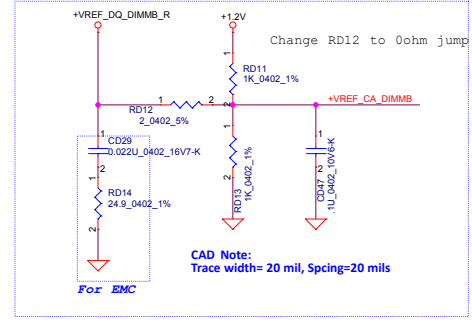


Layout Note: Place near DIMM

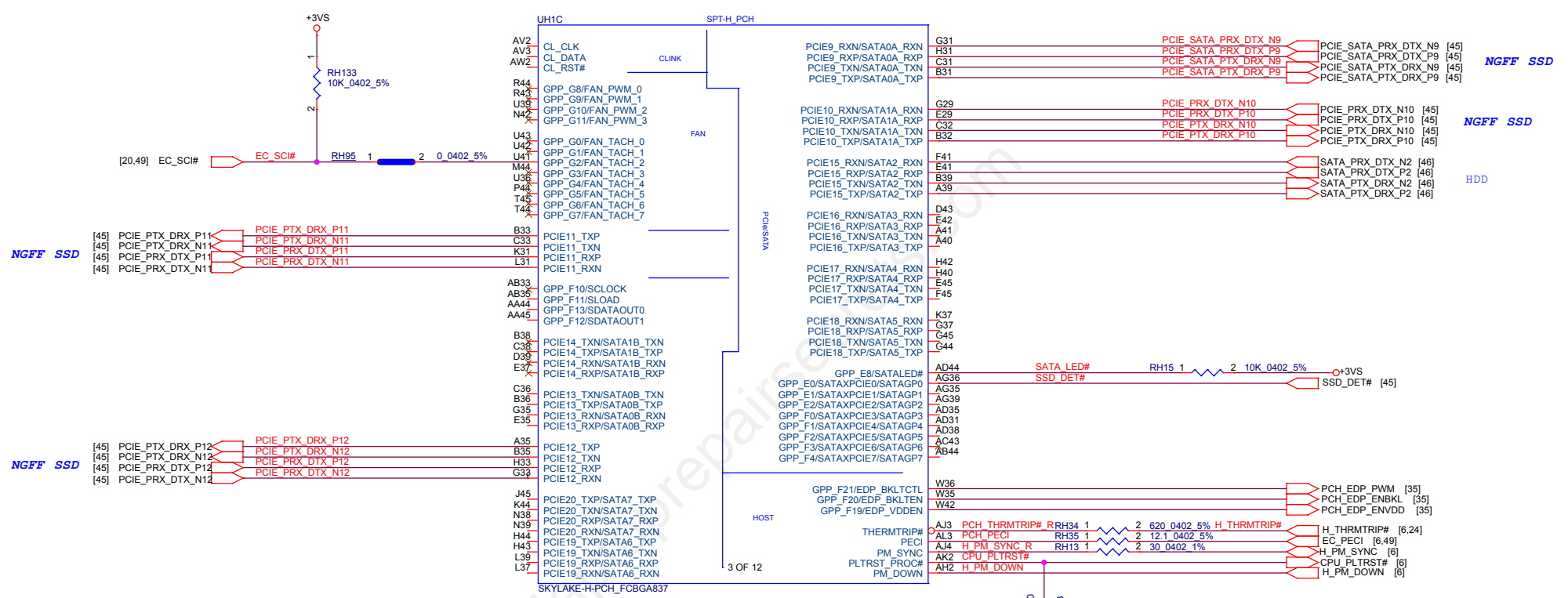
Layout Note: Place near DIMM



Near JDDRH1



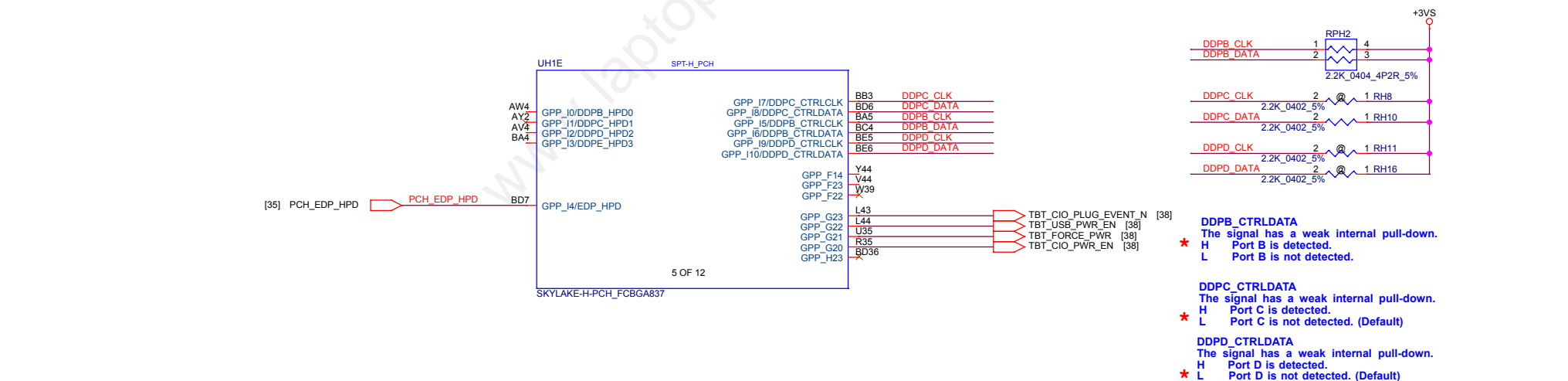
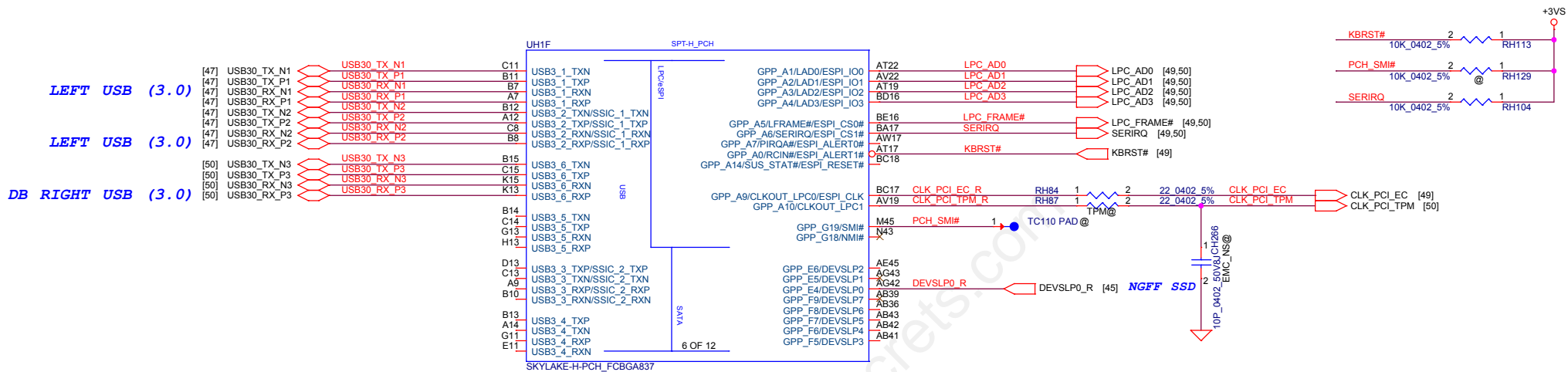
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| Size | Document Number | Title | |
| C | DY510/DY511 N17E-G1 | DDRVI SO-DIMM B | |
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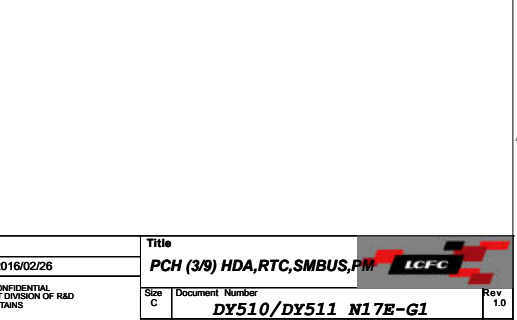
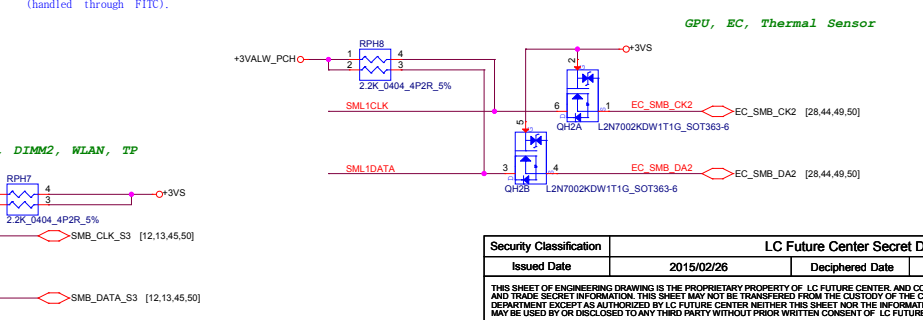
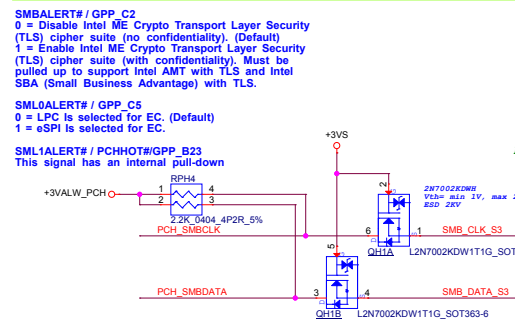
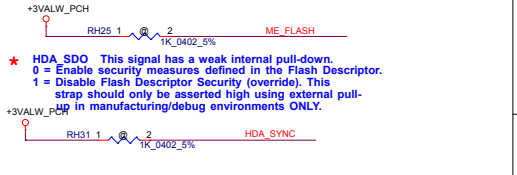
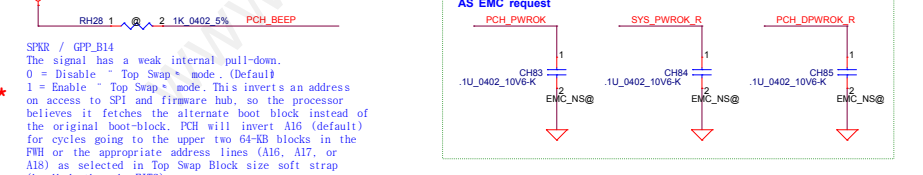
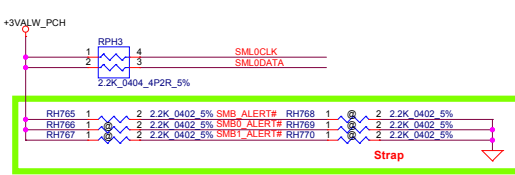
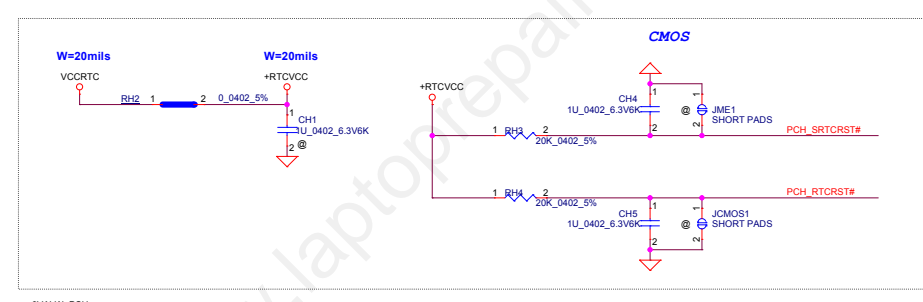
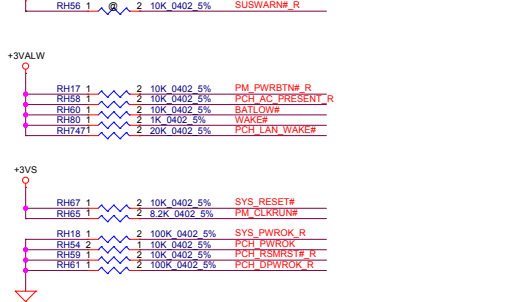
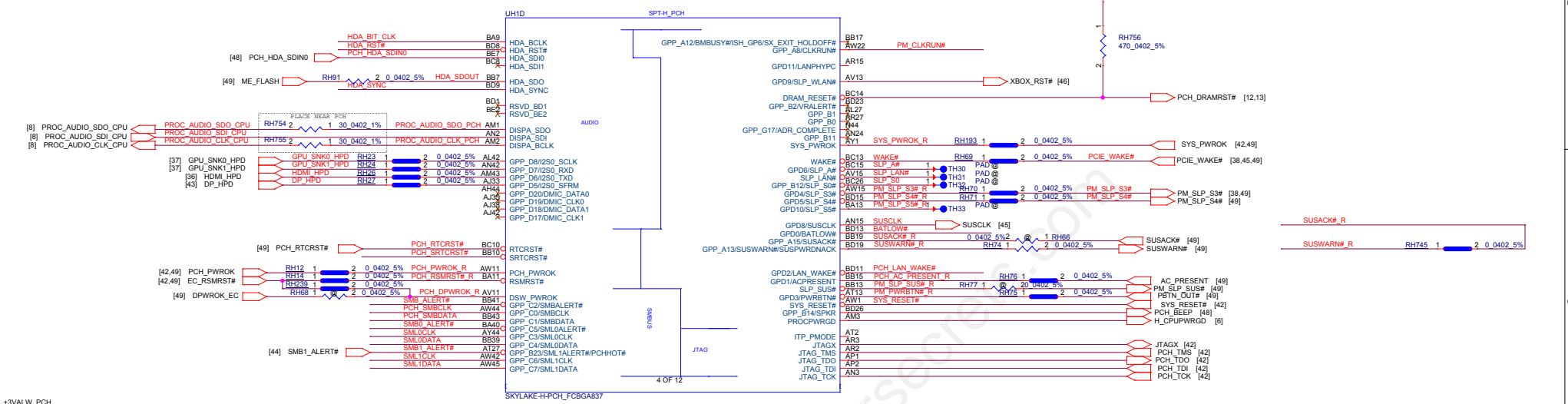
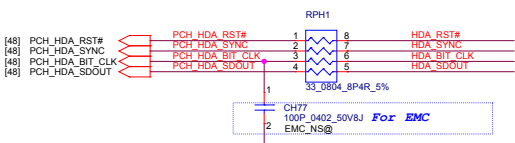
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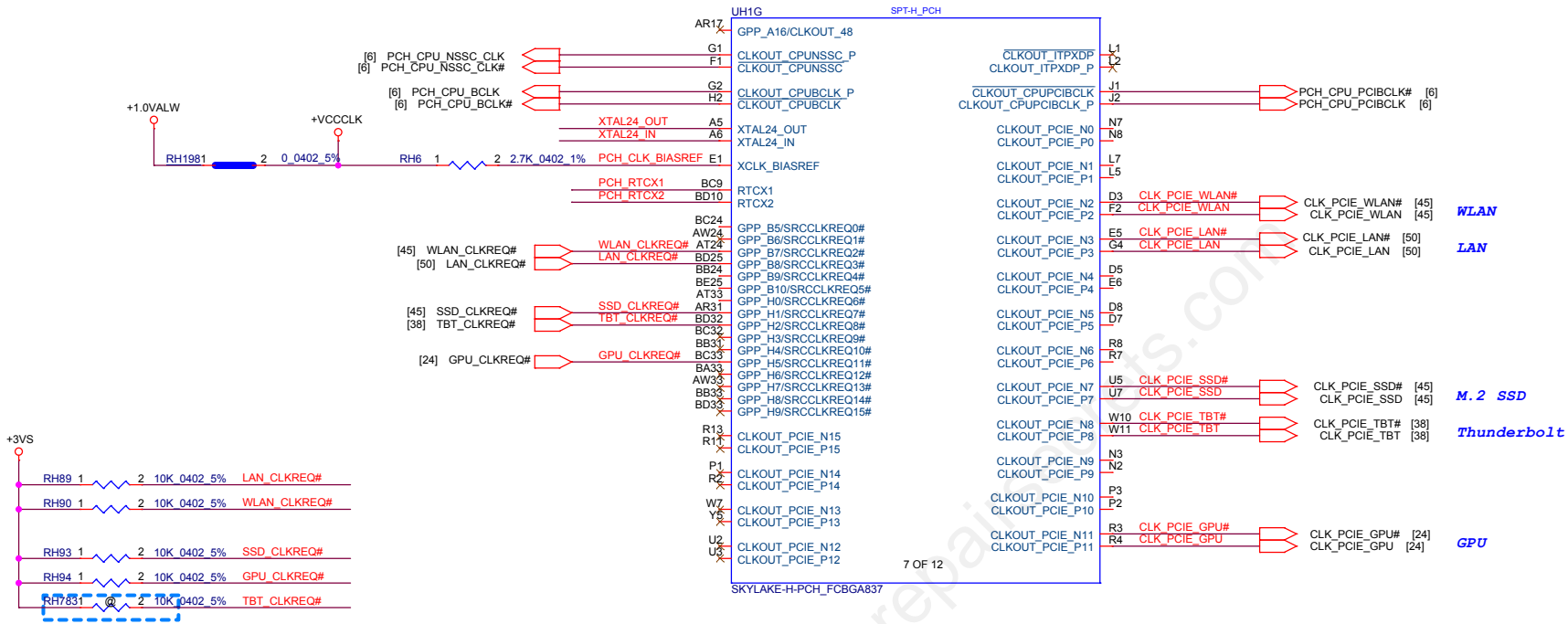
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| Size A3 | Document Number | DY510/DY511 N17E-G1 | | | |
| Date: | | Monday, December 19, 2016 | | Sheet 14 | of 75 |



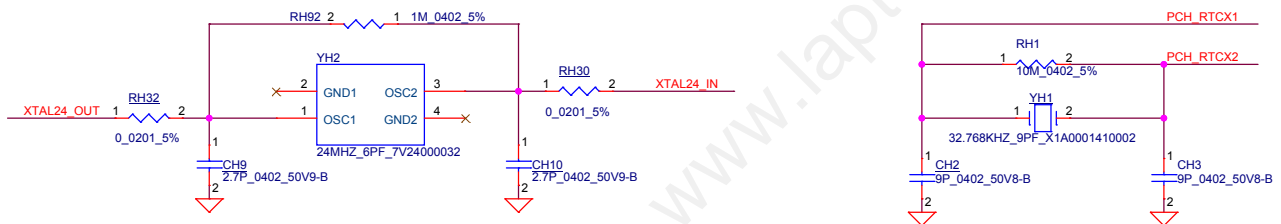
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| Size | Document Number | | Rev |
| C | DY510/DY511 N17E-G1 | | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet | 16 of 75 |

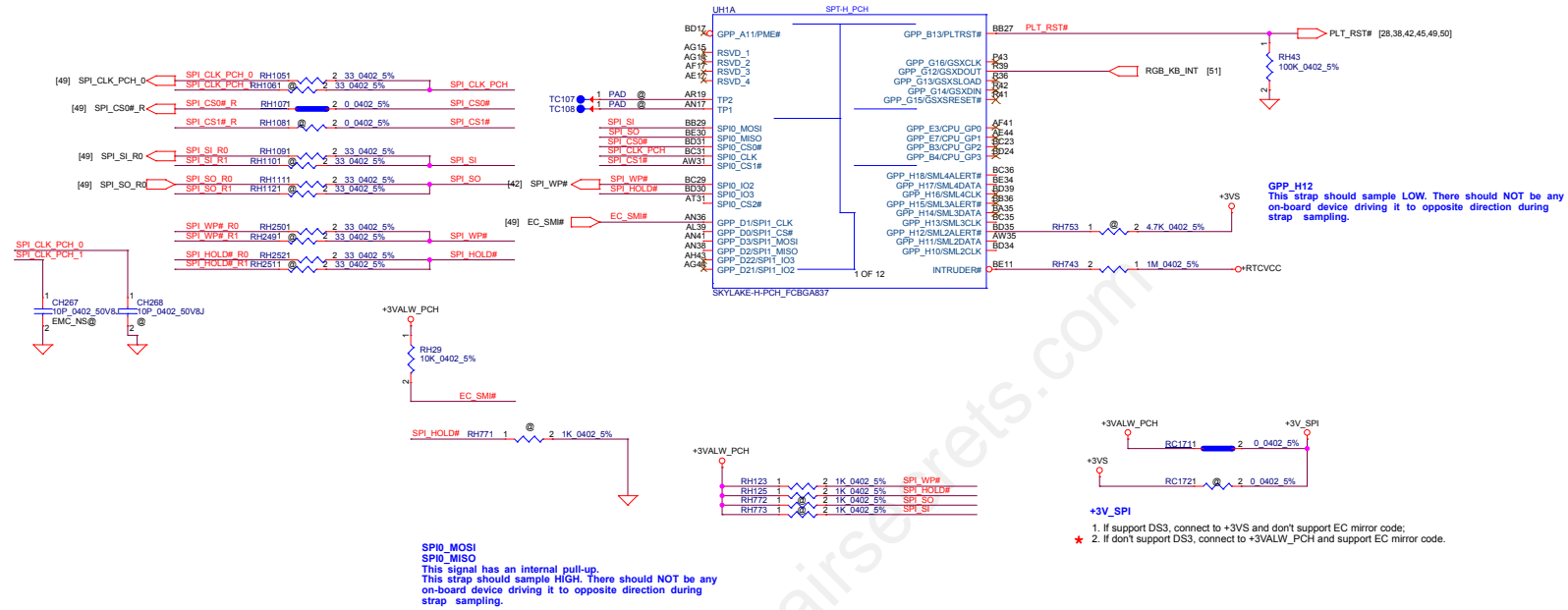


RH783 change to un-stuff-Harry 11/01

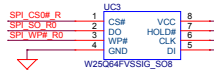


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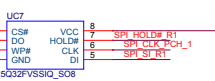
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| | DY510/DY511 N17E-G1 | 1.0 | |
| Date: | Monday, December 19, 2016 | Sheet | 17 of 75 |



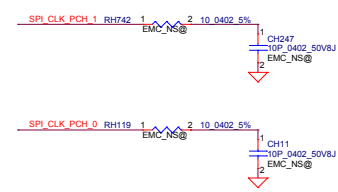
64Mb Flash ROM

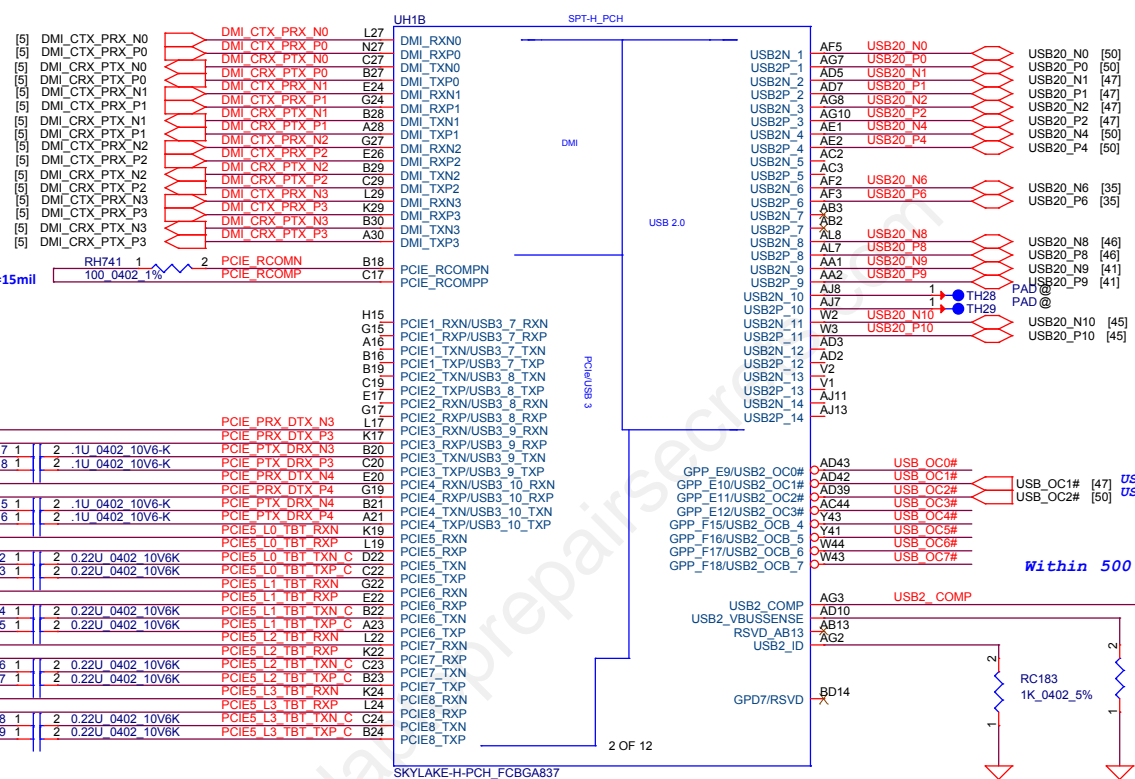


32Mb Flash ROM



For EMI



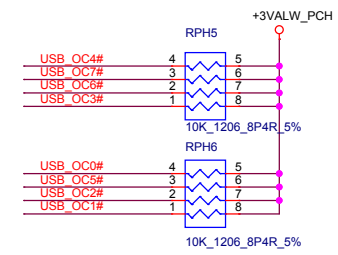


CAD Note:
Trace width=15 mils, Spacing=15mil
Max length= N/A mils.

- RIGHT USB (2.0)
- LEFT USB (3.0)
- LEFT USB (3.0)
- IR Camera
- Camera
- XBOX
- Anti-ghost KB
- Debug port, reserved test point
- Bluetooth

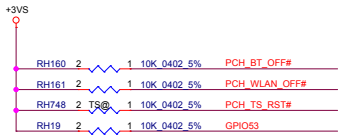
- WLAN
- LAN
- Thunderbolt x 4

SKYLAKE-H-PCH_FCBGA837



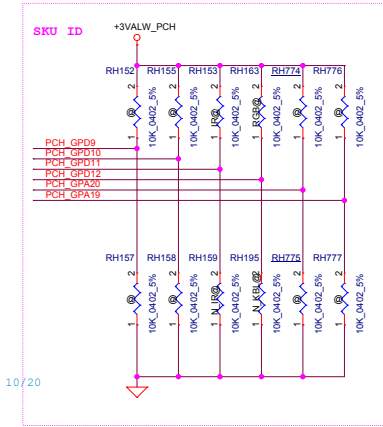
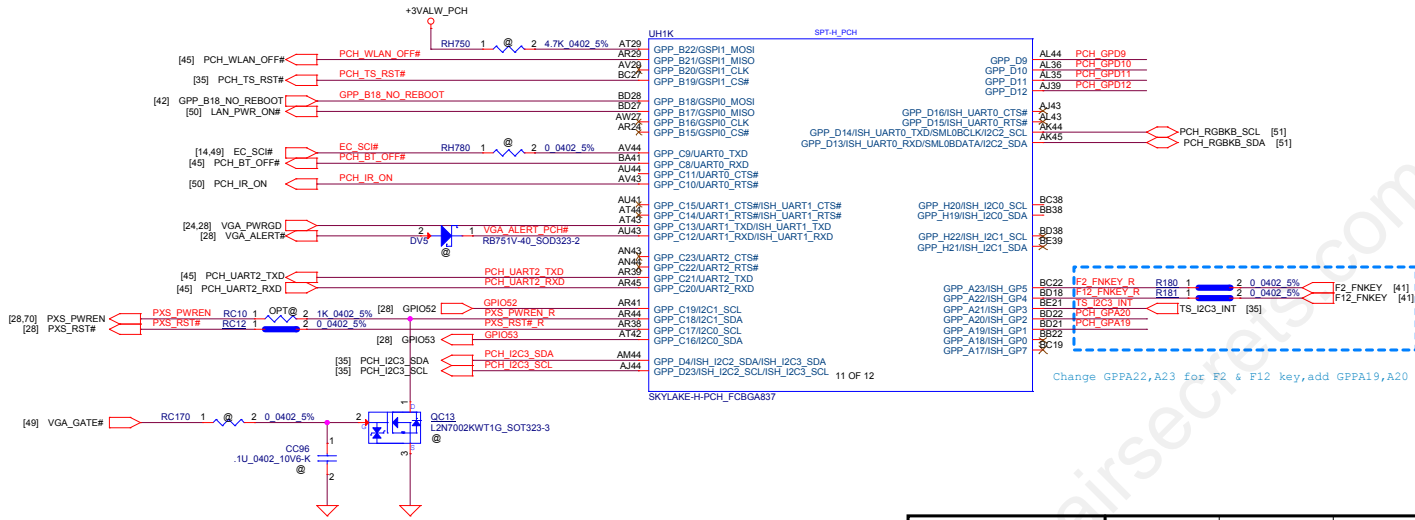
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| Issued Date | 2015/02/26 | Deciphered Date | 2016/02/26 |
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| | | |
|------------------------------|---------------------------|----------------|
| Title | | |
| PCH (5/9) DMI, PCIe, USB2, G | | |
| Size A3 | Document Number | Rev 1.0 |
| Date: | DY510/DY511 | N17E-G1 |
| | Monday, December 19, 2016 | Sheet 19 of 75 |

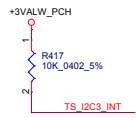
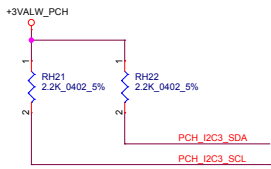


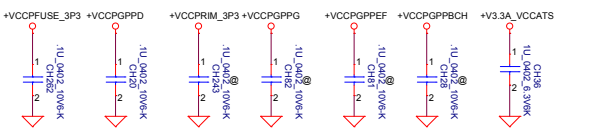
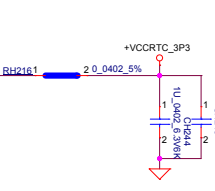
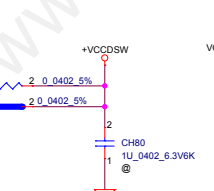
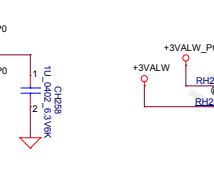
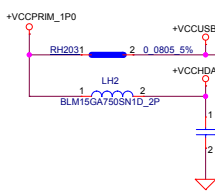
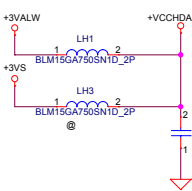
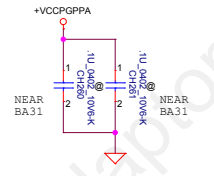
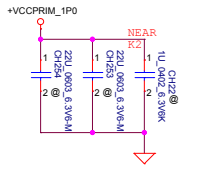
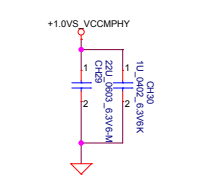
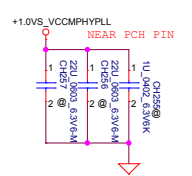
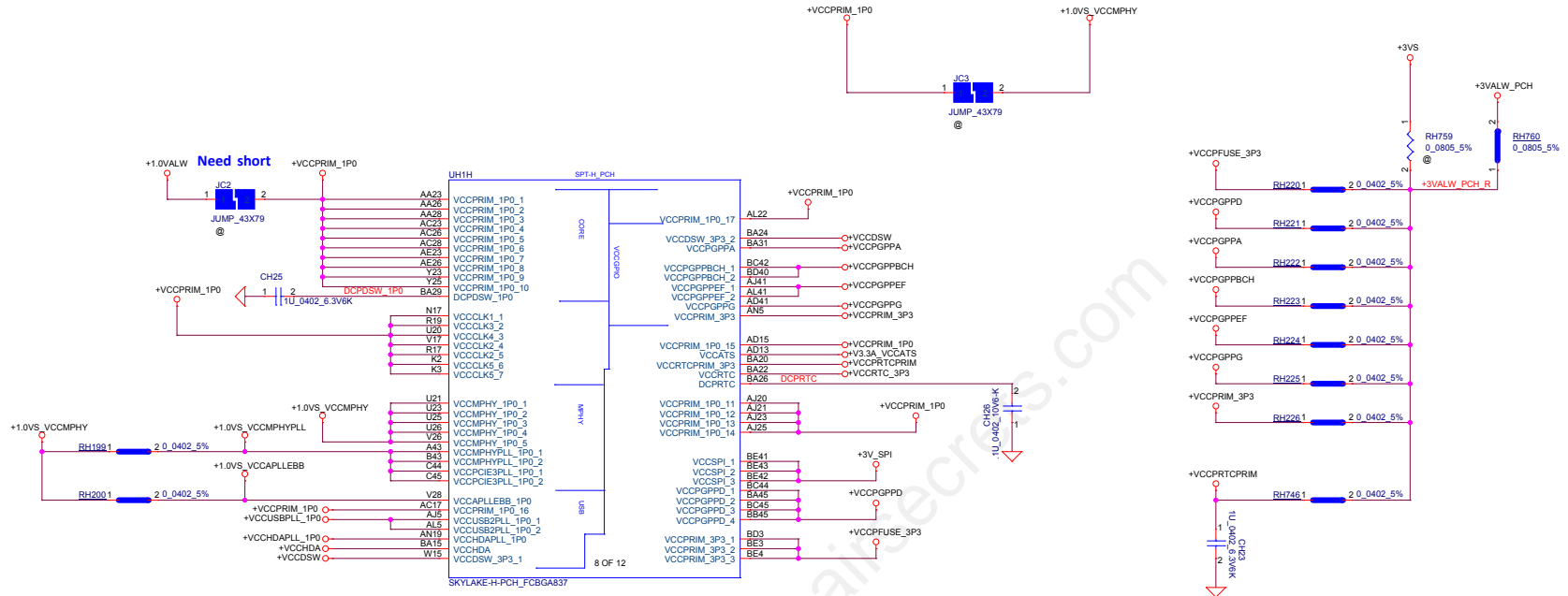
GPIO1_MOSI / GPP_B22
 This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).

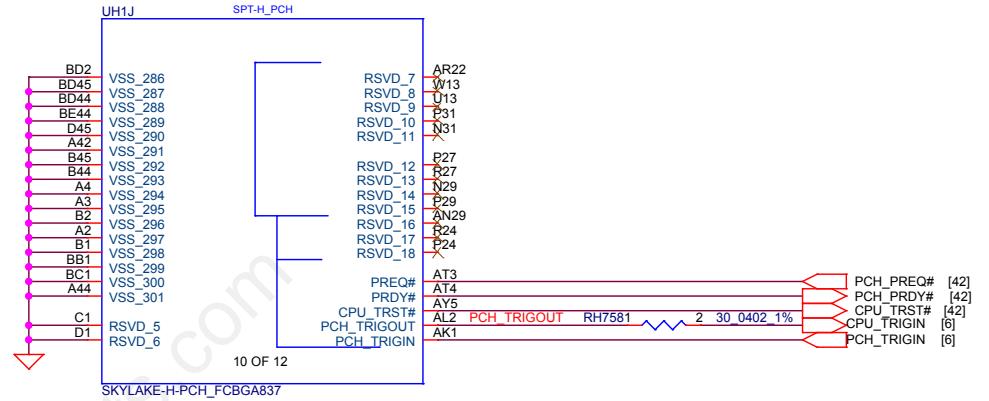
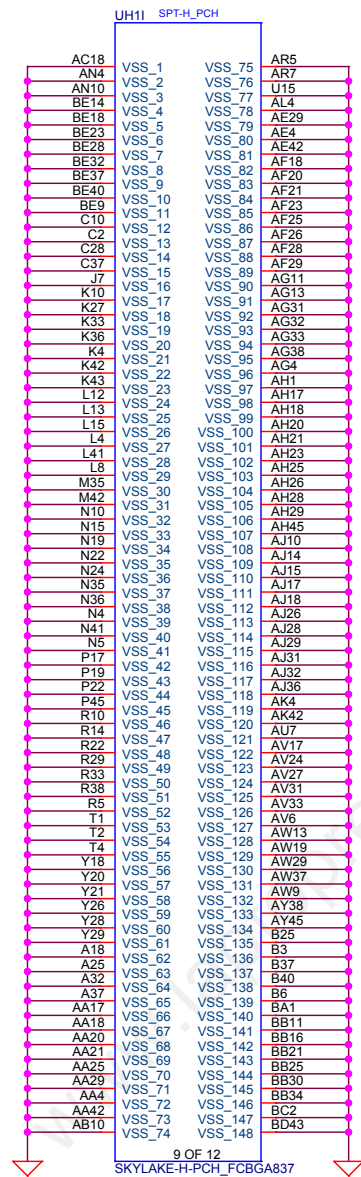
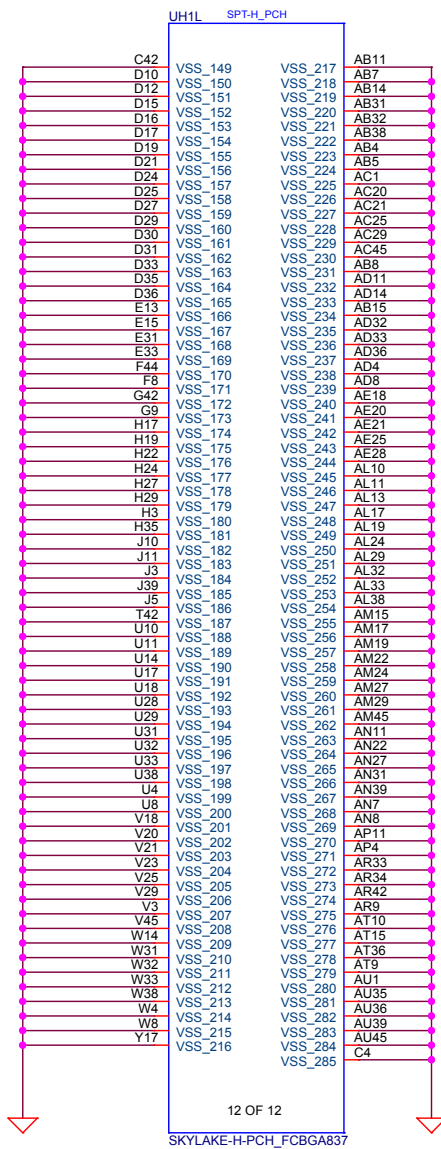
| | |
|-------|-----------------------|
| Bit 6 | Boot BIOS Destination |
| 0 | SPI (Default) |
| 1 | LPC |




| Function | PCH_GPD9 | PCH_GPD10 | PCH_GPD11 | PCH_GPD12 | PCH_GPA19 | PCH_GPA20 |
|---------------|----------|-----------|-----------|-----------|-----------|-----------|
| Optane Memory | 0 | X | X | X | X | X |
| non-touch | X | 1 | X | X | X | X |
| touch | X | 0 | X | X | X | X |
| IR Camera | X | X | 1 | X | X | X |
| Normal Camera | X | X | 0 | X | X | X |
| RGB BL KB | X | X | X | 1 | X | X |
| Red BL KB | X | X | X | 0 | X | X |







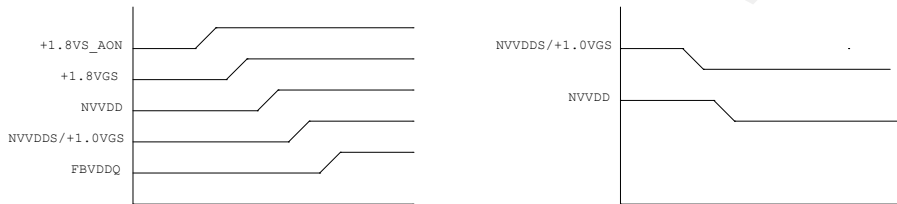
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|---|------------|------------------------------|------------|
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| Issued Date | 2015/02/26 | Deciphered Date | 2016/02/26 |
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| | | |
|---------------|---------------------------|---|
| Title | |  |
| PCH (9/9) VSS | | |
| Size B | Document Number | Rev 1.0 |
| Date: | Monday, December 19, 2016 | Sheet 22 of 75 |

N17E-G1 GPIO

| GPIO | I/O | ACTIVE | Function Description | I/O Termination |
|--------|-----|--------|--|------------------|
| GPIO0 | OUT | - | PWM Output to control NVVDD | |
| GPIO1 | OUT | - | FB Enable for GC6 2.1 | |
| GPIO2 | IN | - | GPU wake signal for GC6 2.1 | |
| GPIO3 | OUT | - | PWM Output to control the SRAM power supply | |
| GPIO4 | OUT | - | GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN | |
| GPIO5 | IN | N/A | Active low Frame Lock | |
| GPIO6 | OUT | - | Phase Shedding, NVVDD_PSI | |
| GPIO7 | OUT | N/A | Panel Backlight enable | |
| GPIO8 | OUT | - | Memory voltage Control | |
| GPIO9 | I/O | - | Active Low Thermal Alert | |
| GPIO10 | OUT | - | Memory VREF Control | (100K pull Down) |
| GPIO11 | OUT | - | Panel Power enable | |
| GPIO12 | IN | - | AC power detect or power supply overdraw input | (10K pull High) |
| GPIO13 | OUT | N/A | LCD Panel Backlight Enable | |
| GPIO14 | IN | N/A | Hot Plug Detect for IFPA | |
| GPIO15 | IN | N/A | Hot Plug Detect for IFPB | |
| GPIO16 | OUT | - | System side PCIe reset monitor | |
| GPIO17 | IN | N/A | Hot Plug Detect for IFPD | |
| GPIO18 | IN | N/A | Hot Plug Detect for IFPE | |
| GPIO19 | OUT | N/A | 3D Vision L/R Signal | |
| GPIO20 | | N/A | GCS_MODE | |
| GPIO21 | I/O | N/A | UNUSED | |
| GPIO22 | I/O | N/A | UNUSED | |
| GPIO23 | OUT | - | GPU PCIe self-reset control | |
| GPIO24 | IN | N/A | Hot Plug Detect for IFPF | |
| GPIO25 | | N/A | UNUSED | |
| GPIO26 | | N/A | UNUSED | |
| GPIO27 | IN | N/A | Hot Plug Detect for IFPC | |

N17E-G1 Power Sequence



- All power rail ramp up time should be larger than 40us and is recommended to be less than 6ms.
- T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Fgodd) must NOT exceed 4ms.
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.

- NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.
- All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.
- The previous power rail must ramp down to 10% before the next power rail can start ramping down.

| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] |
|--------|--------|--------|-------------|
| L | L | L | 00000 |
| L | H | L | 00010 |
| L | H | H | 00011 |
| H | H | L | 00110 |
| H | H | H | 00111 |

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

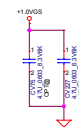
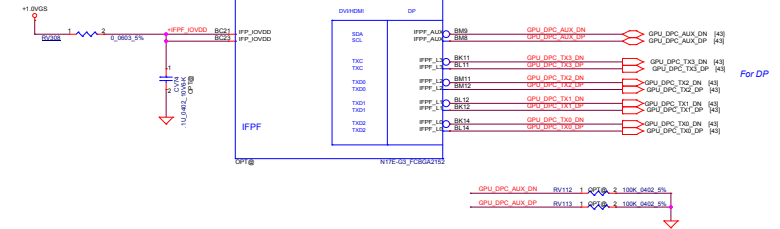
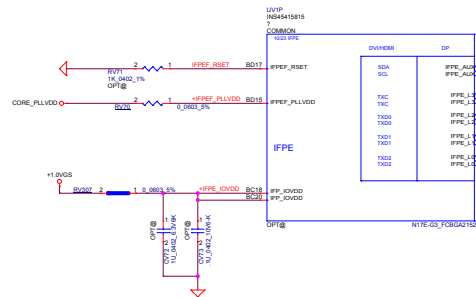
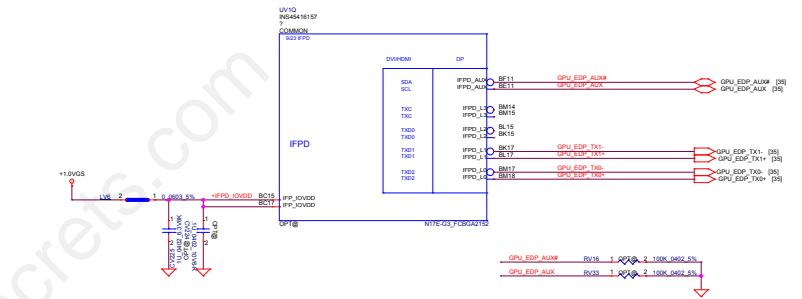
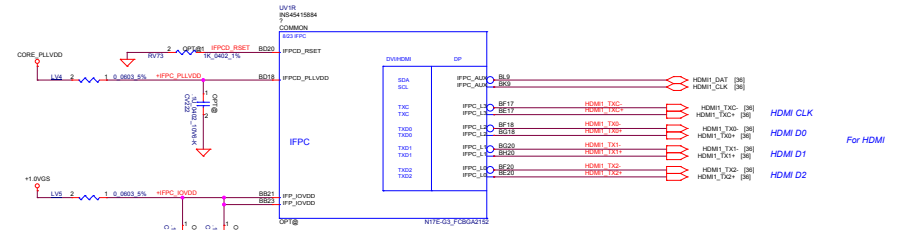
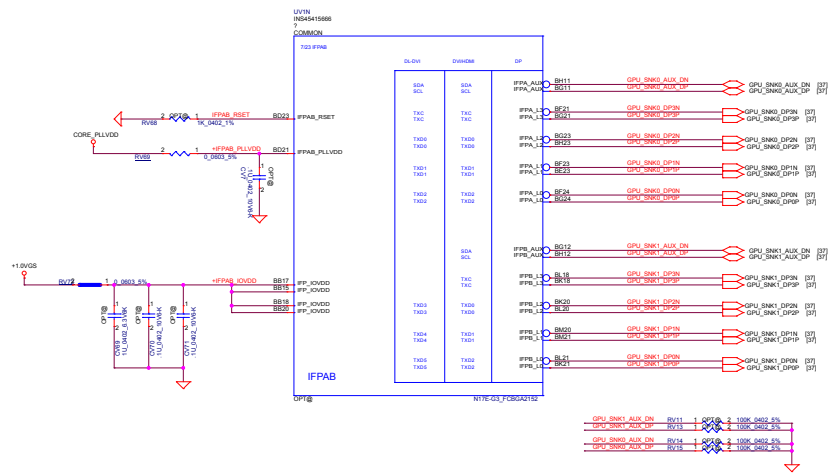
| ROM_SO | ROM_SI | ROM_SCLK | SOR_EXPOSED[3:0] |
|--------|--------|----------|------------------|
| L | L | L | 1111 DEFAULT |
| L | L | H | 1110 |
| L | H | L | 1101 |
| L | H | H | 1100 |
| H | L | L | 1011 |
| H | L | H | 1010 |
| H | H | L | 1001 |
| H | H | H | 1000 |
| L | L | M | 0111 |
| L | M | L | 0110 |
| L | M | H | 0101 |
| L | H | M | 0100 |
| H | L | M | 0011 |
| H | M | L | 0010 |
| H | M | H | 0001 |
| H | H | M | 0000 |

1:ENABLE 0:DISABLE
SOR0/1/2/3 ENABLE

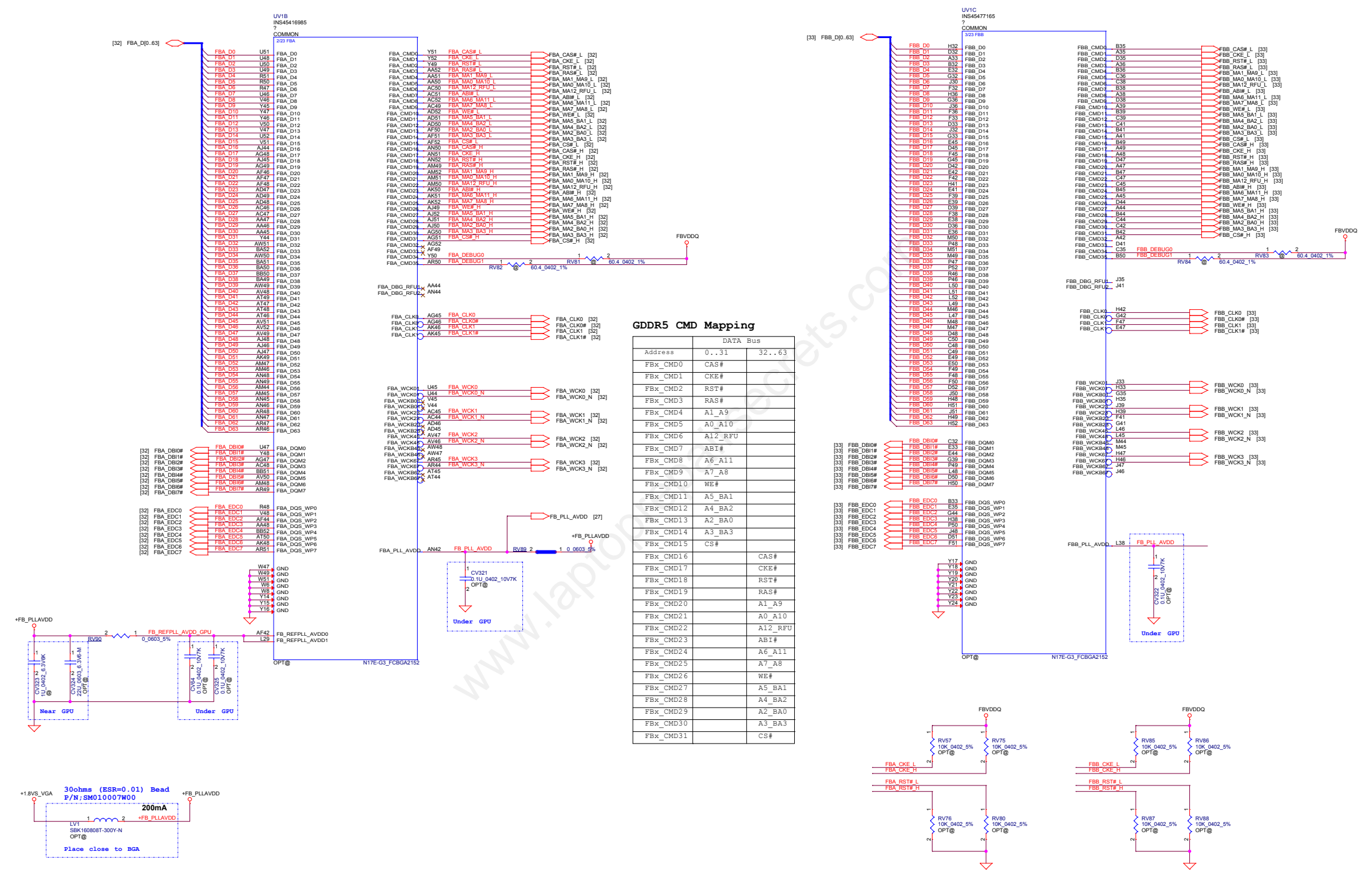
| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|--------|--------|--------|--------------|-----------|----------|------------|
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | 1 | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 DEFAULT |
| L | L | L | 0 | 0 | 0 | 0 |

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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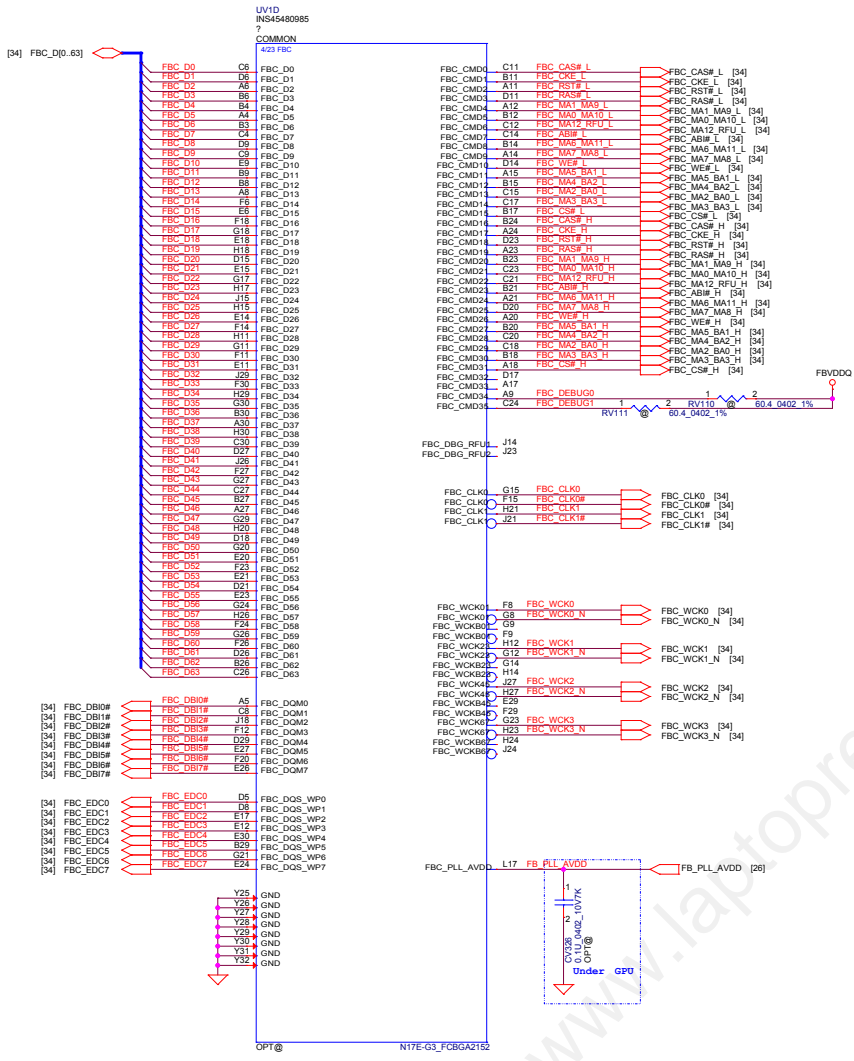
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| Security Classification | LC Future Center Secret Data | | This |
| Issued Date | 2015/02/26 | Displacement Date | 2016/00/13 |
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| Doc No | DY510/DY511 N178-G1 | | Rev 14 |
| Date | Monday, December 14, 2016 | Sheet | 25 of 75 |



GDDR5 CMD Mapping

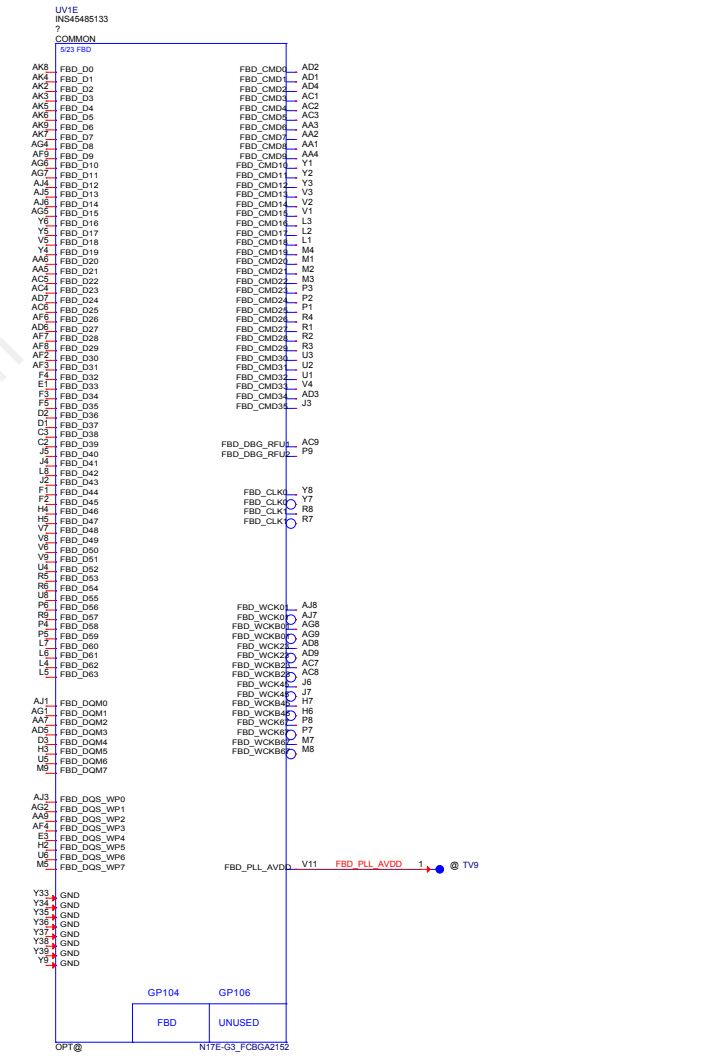
| Address | DATA Bus |
|-----------|----------|
| FBx_CMD0 | CAS# |
| FBx_CMD1 | CKE# |
| FBx_CMD2 | RST# |
| FBx_CMD3 | RAS# |
| FBx_CMD4 | A1_A9 |
| FBx_CMD5 | A0_A10 |
| FBx_CMD6 | A12_RFU |
| FBx_CMD7 | AB# |
| FBx_CMD8 | A6_A11 |
| FBx_CMD9 | A7_A8 |
| FBx_CMD10 | WE# |
| FBx_CMD11 | A5_BA1 |
| FBx_CMD12 | A4_BA2 |
| FBx_CMD13 | A2_BA0 |
| FBx_CMD14 | A3_BA3 |
| FBx_CMD15 | CS# |
| FBx_CMD16 | CAS# |
| FBx_CMD17 | CKE# |
| FBx_CMD18 | RST# |
| FBx_CMD19 | RAS# |
| FBx_CMD20 | A1_A9 |
| FBx_CMD21 | A0_A10 |
| FBx_CMD22 | A12_RFU |
| FBx_CMD23 | AB1# |
| FBx_CMD24 | A6_A11 |
| FBx_CMD25 | A7_A8 |
| FBx_CMD26 | WE# |
| FBx_CMD27 | A5_BA1 |
| FBx_CMD28 | A4_BA2 |
| FBx_CMD29 | A2_BA0 |
| FBx_CMD30 | A3_BA3 |
| FBx_CMD31 | CS# |

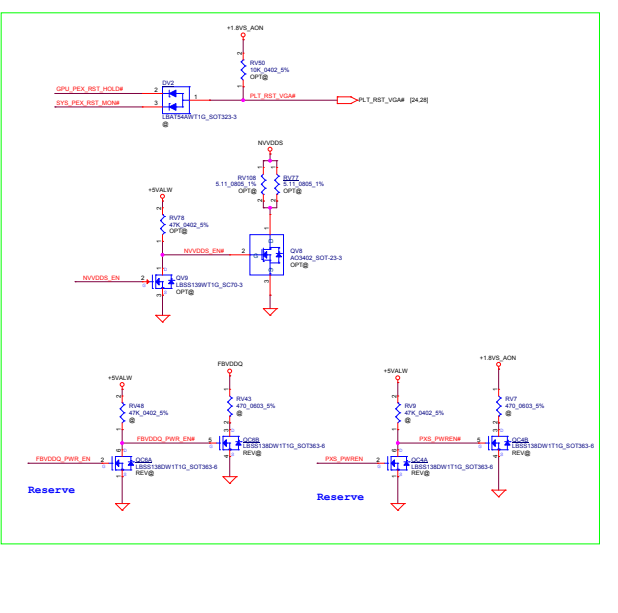
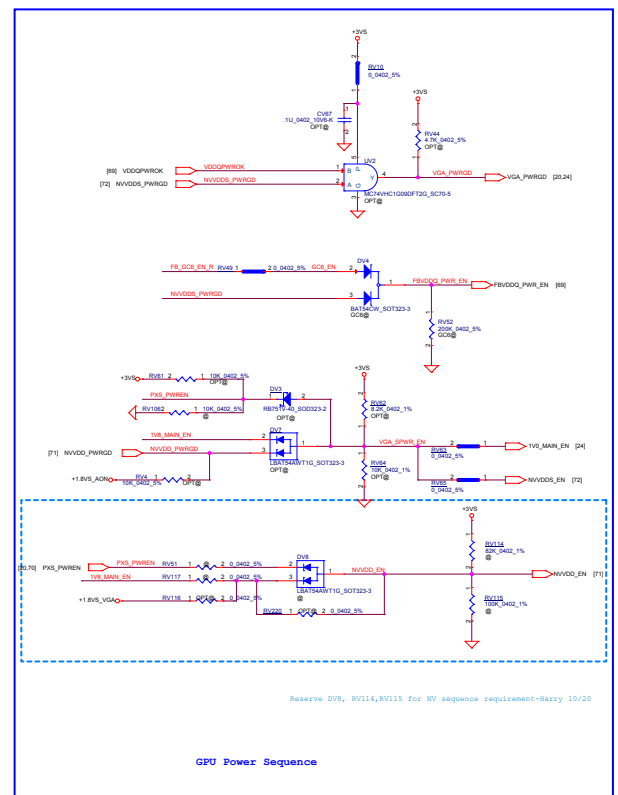
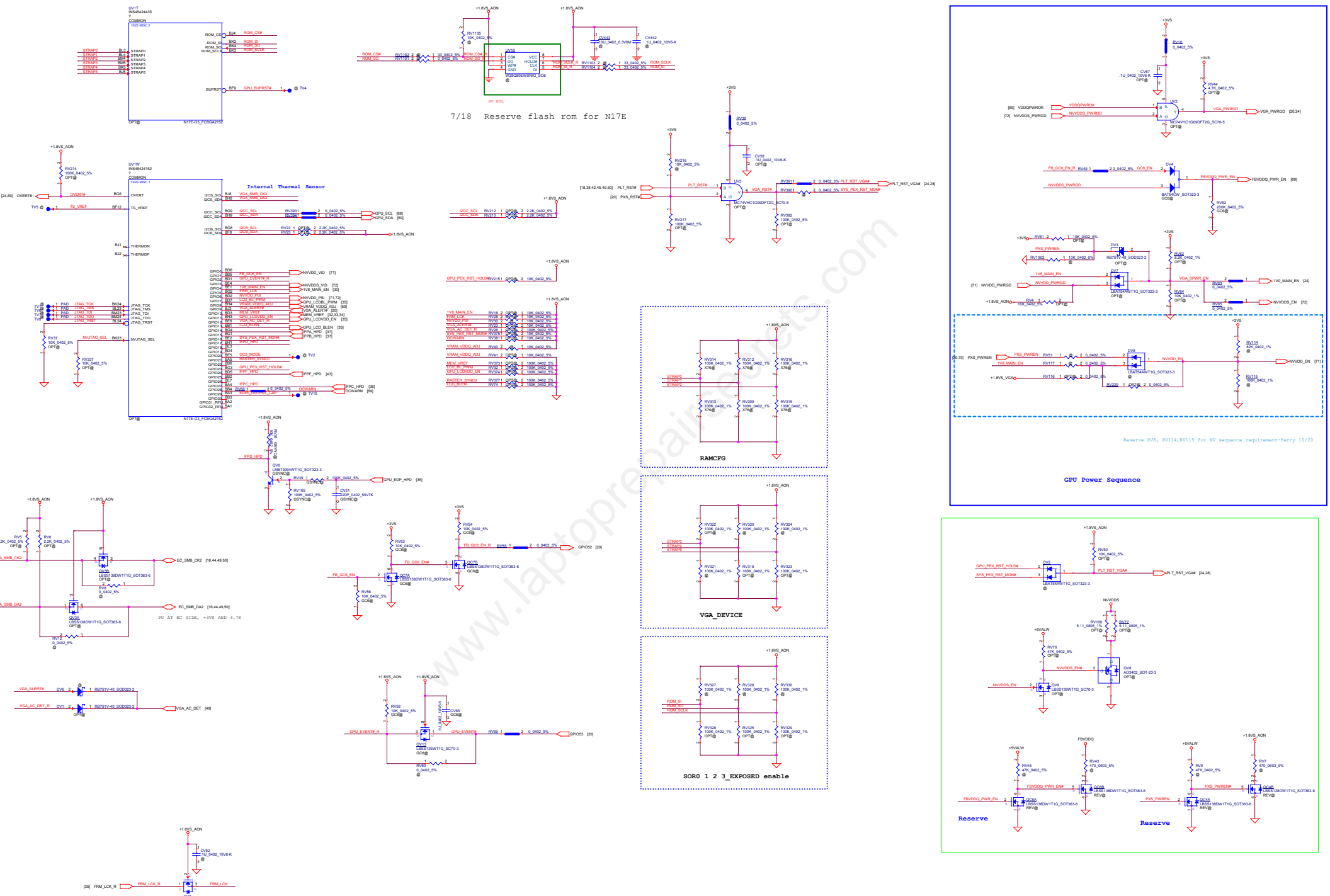
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| Security Classification | LC Future Center Secret Data | | Title | N17E-G1_VRAM_AB | |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | | |
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| Size | A2 | Document Number | DXS10/DY511 N17E-G1 | Rev | 1.0 |
| Date: | Monday, December 16, 2016 | Sheet | 26 | of | 76 |



GDDR5 CMD Mapping

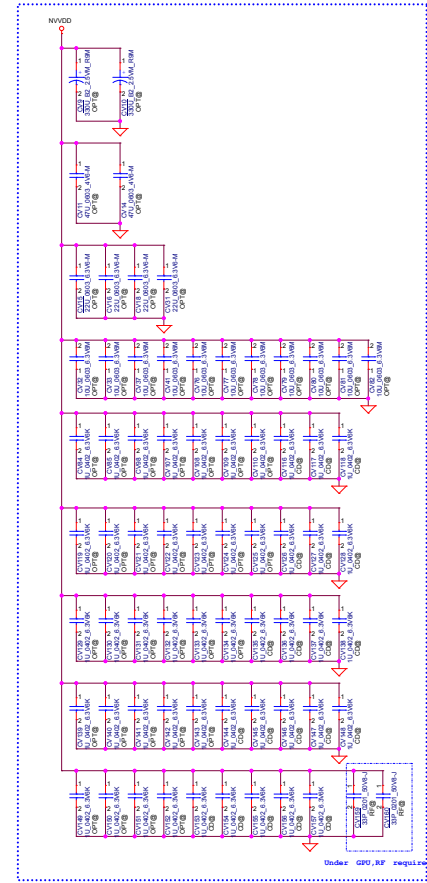
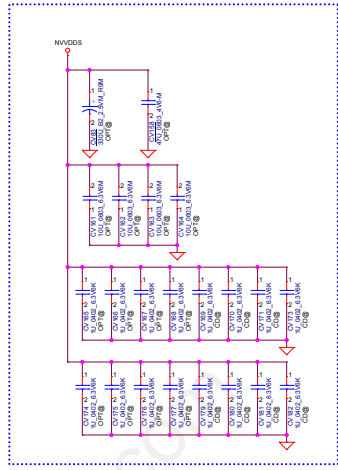
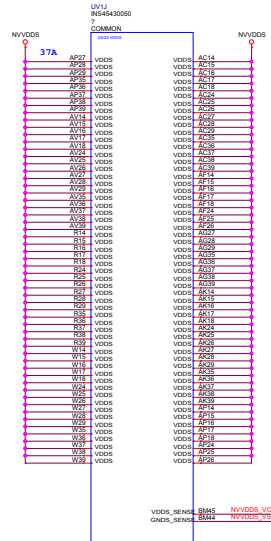
| Address | DATA Bus |
|-----------|----------|
| FBX_CMD0 | CAS# |
| FBX_CMD1 | CKE# |
| FBX_CMD2 | RST# |
| FBX_CMD3 | RAS# |
| FBX_CMD4 | A1_A9 |
| FBX_CMD5 | A0_A10 |
| FBX_CMD6 | A12_RFU |
| FBX_CMD7 | AB1# |
| FBX_CMD8 | A6_A11 |
| FBX_CMD9 | A7_A8 |
| FBX_CMD10 | WE# |
| FBX_CMD11 | A5_BA1 |
| FBX_CMD12 | A4_BA2 |
| FBX_CMD13 | A2_BA0 |
| FBX_CMD14 | A3_BA3 |
| FBX_CMD15 | CS# |
| FBX_CMD16 | CAS# |
| FBX_CMD17 | CKE# |
| FBX_CMD18 | RST# |
| FBX_CMD19 | RAS# |
| FBX_CMD20 | A1_A9 |
| FBX_CMD21 | A0_A10 |
| FBX_CMD22 | A12_RFU |
| FBX_CMD23 | AB1# |
| FBX_CMD24 | A6_A11 |
| FBX_CMD25 | A7_A8 |
| FBX_CMD26 | WE# |
| FBX_CMD27 | A5_BA1 |
| FBX_CMD28 | A4_BA2 |
| FBX_CMD29 | A2_BA0 |
| FBX_CMD30 | A3_BA3 |
| FBX_CMD31 | CS# |



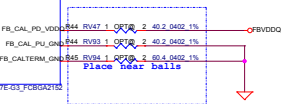
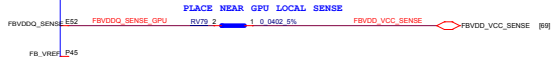
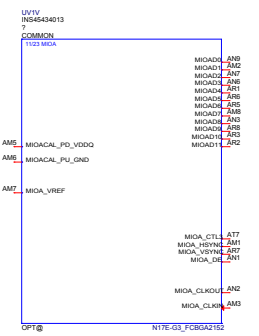
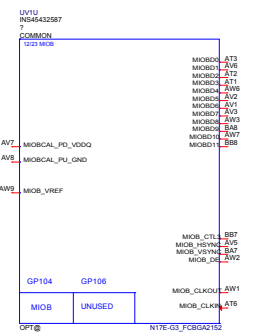
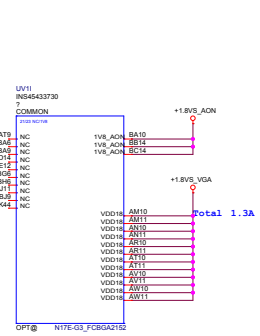
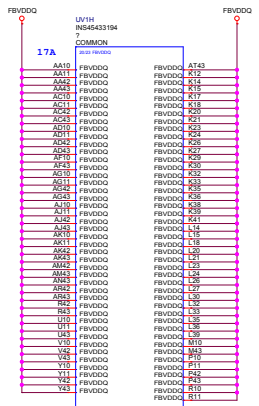




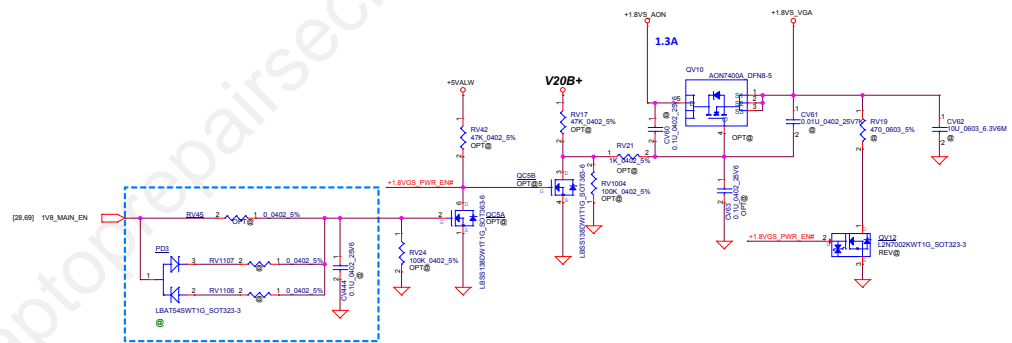
trace width: 16mil
 differential voltage sensing
 differential signal routing;



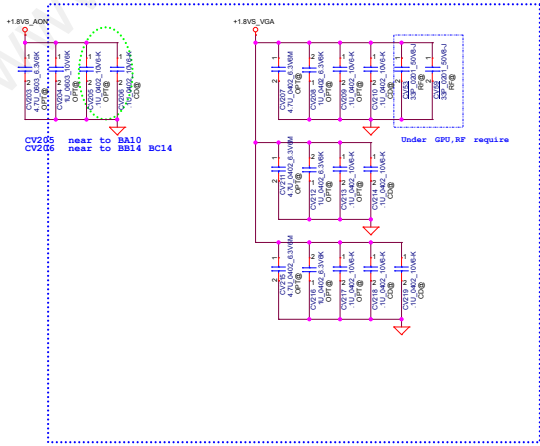
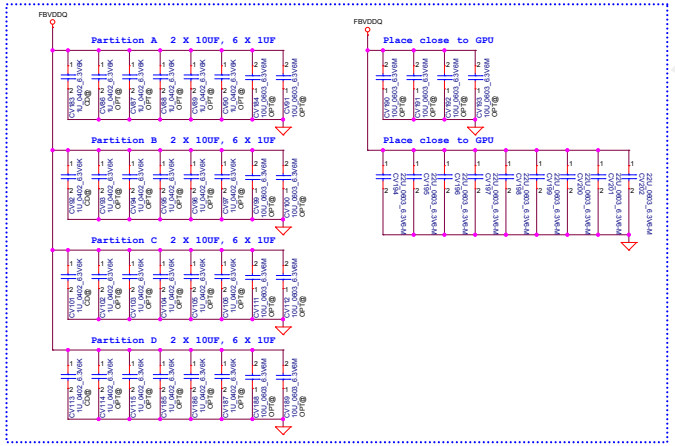
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|---|---------------------|------------------------------|------------|---------------------------|--|
| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | N17E-G1_POWER CORE | |
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| Size | Document Number | Rev | | 1.0 | |
| Color | DY510/DY511 N17E-G1 | Date | | Monday, December 15, 2015 | |
| Page | 28 | Sheet | | 21 of 78 | |

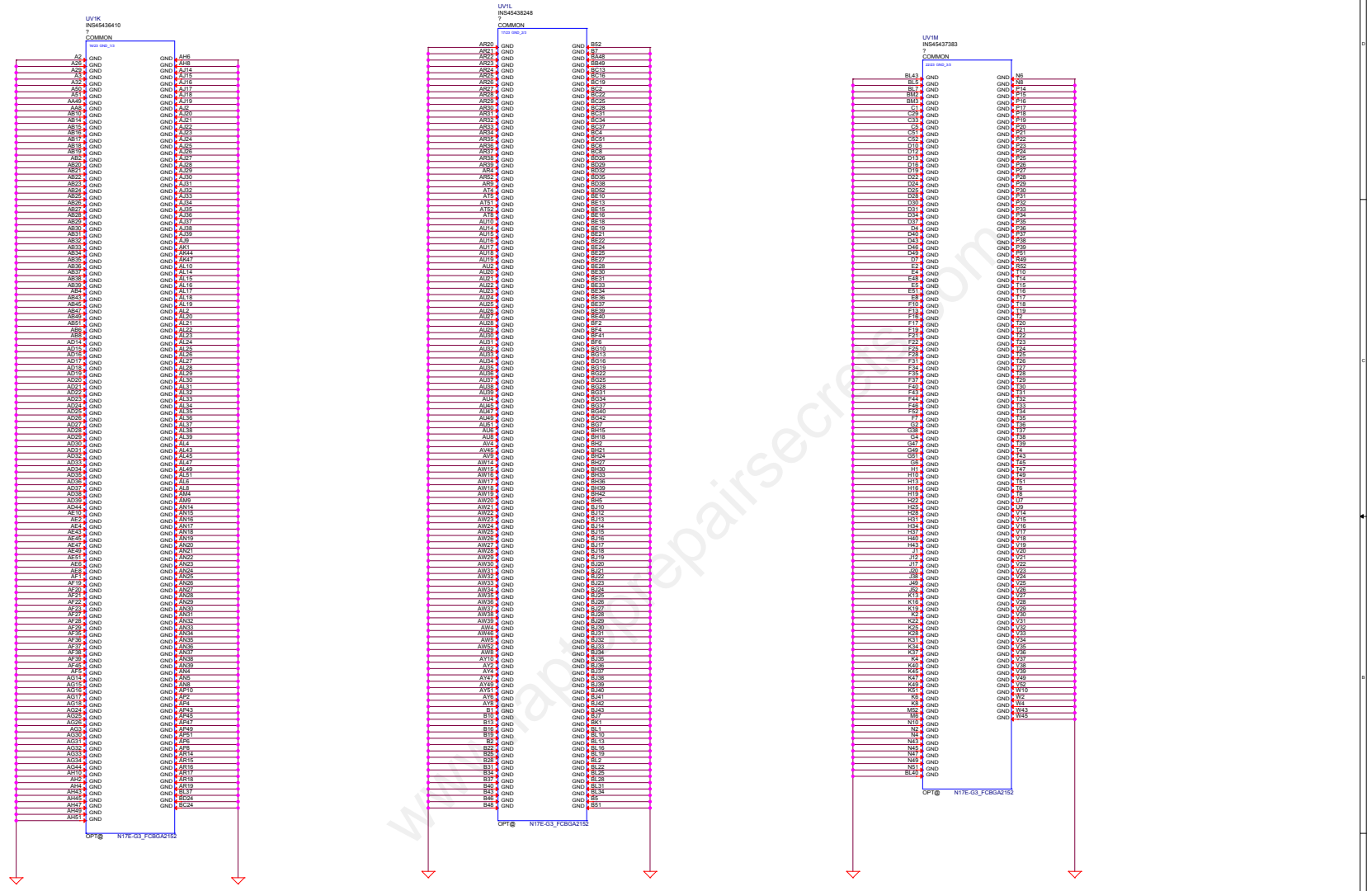


+1.8VS_AON TO +1.8VS_VGA



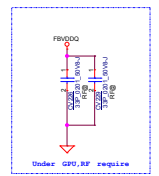
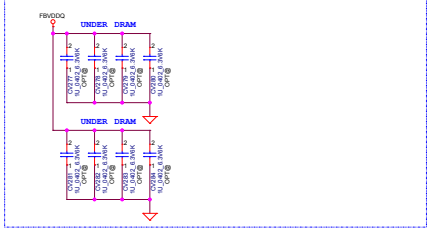
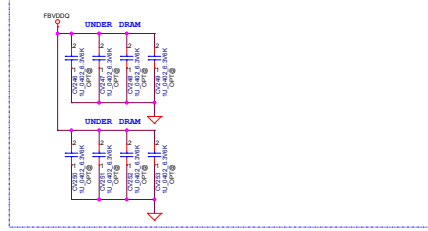
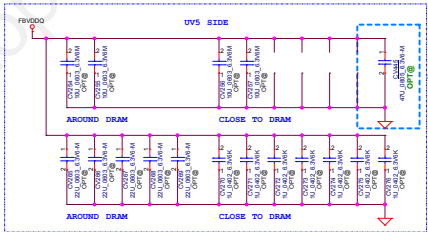
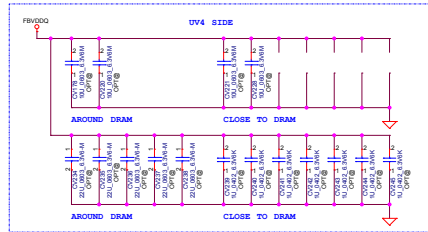
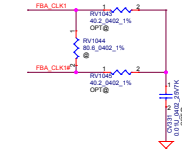
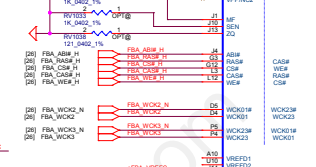
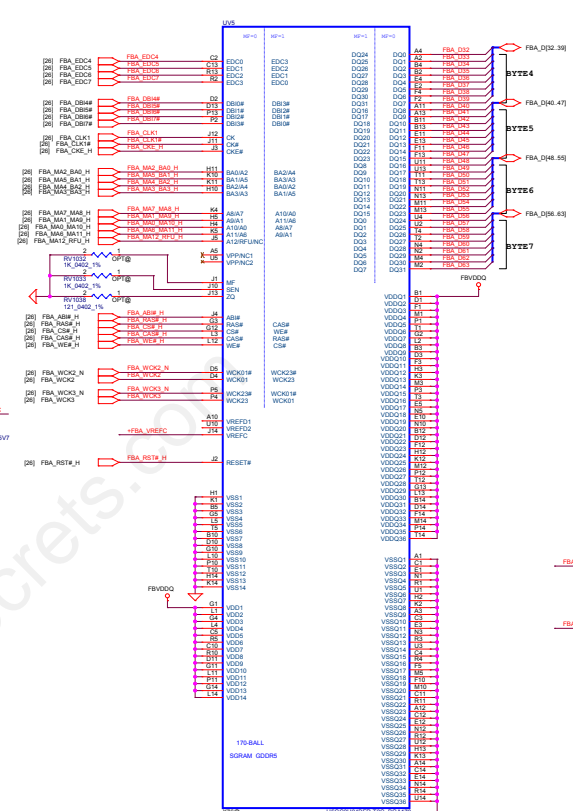
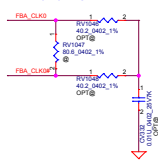
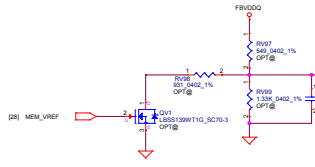
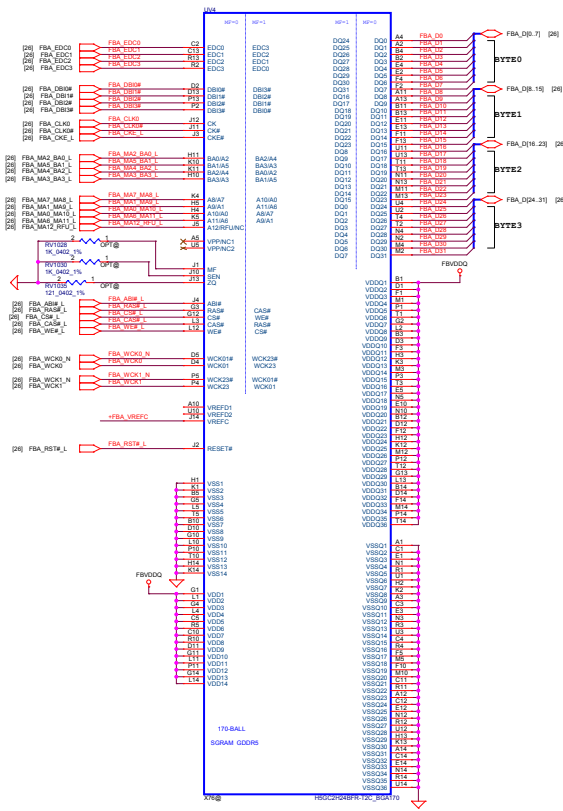
Reserve PD3, RV1107, RV1106, CV444 for NV sequence requirement-Harry 10/20





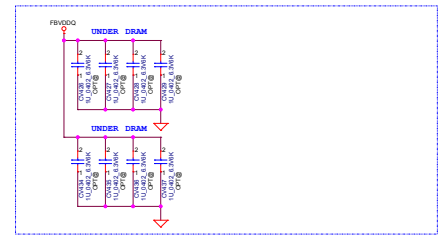
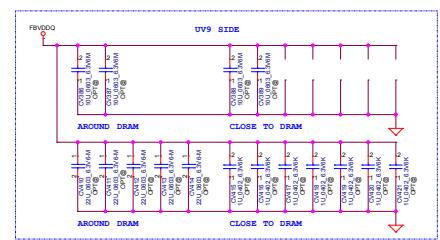
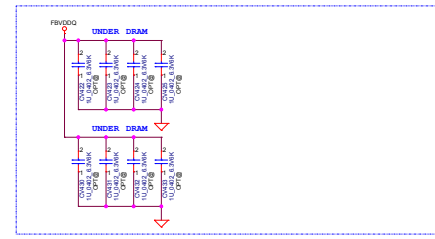
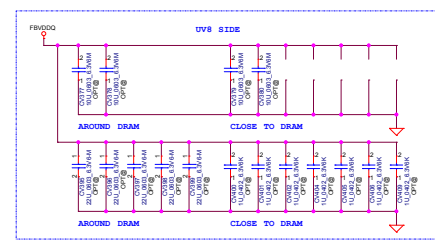
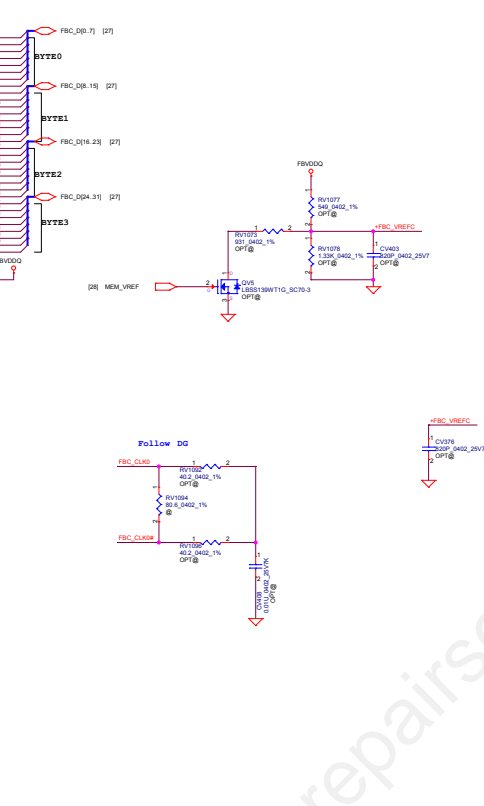
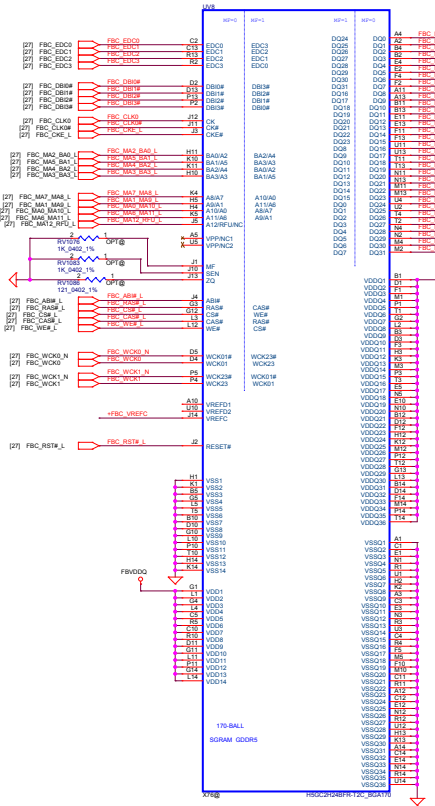
Memory - Lower 32 bits

Memory - Upper 32 bits



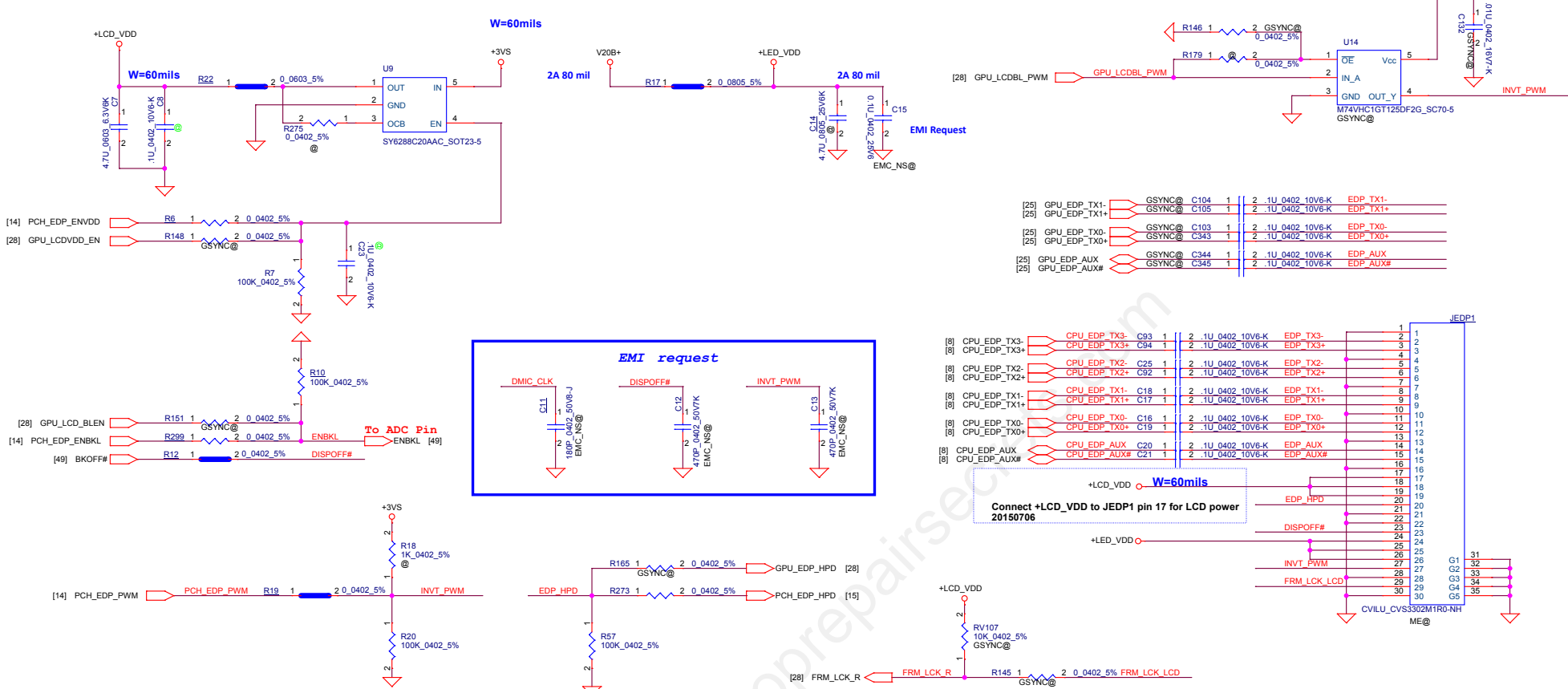
Memory Partition C - Lower 32 bits

Memory Partition C - Upper 32 bits



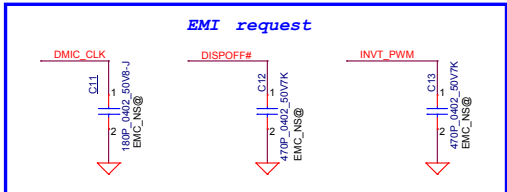
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| Issued Date | 2015/02/26 | Design/Draw Date | |
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LCD POWER CIRCUIT

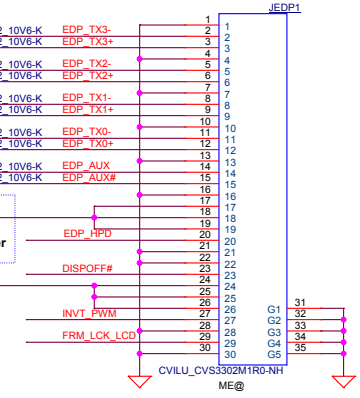


EMI Request

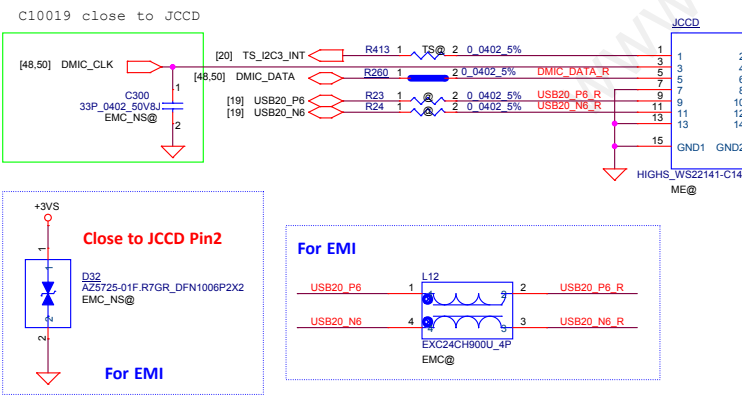
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|-------------------|-------------|---|---|-----------------|----------|
| [25] GPU_EDP_TX1- | GSYNC@ C104 | 1 | 2 | .1U_0402_10V6-K | EDP_TX1- |
| [25] GPU_EDP_TX1+ | GSYNC@ C105 | 1 | 2 | .1U_0402_10V6-K | EDP_TX1+ |
| [25] GPU_EDP_TX0- | GSYNC@ C103 | 1 | 2 | .1U_0402_10V6-K | EDP_TX0- |
| [25] GPU_EDP_TX0+ | GSYNC@ C343 | 1 | 2 | .1U_0402_10V6-K | EDP_TX0+ |
| [25] GPU_EDP_AUX | GSYNC@ C344 | 1 | 2 | .1U_0402_10V6-K | EDP_AUX |
| [25] GPU_EDP_AUX# | GSYNC@ C345 | 1 | 2 | .1U_0402_10V6-K | EDP_AUX# |



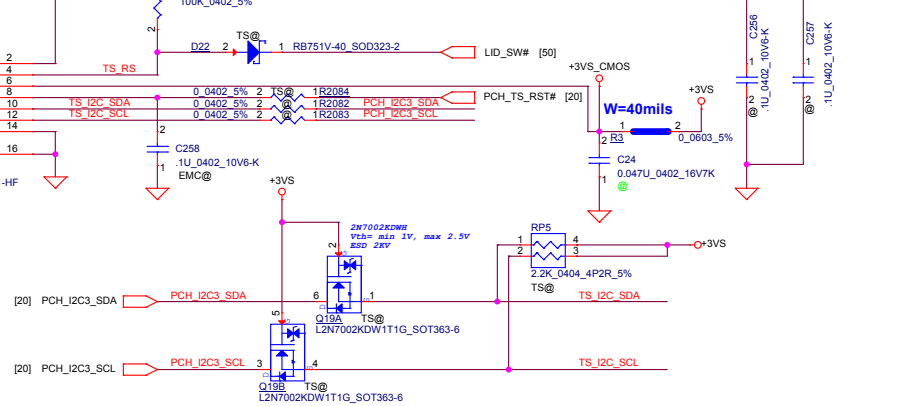
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|------------------|--------------|-----|---|---|-----------------|----------|
| [8] CPU_EDP_TX3- | CPU_EDP_TX3- | C93 | 1 | 2 | .1U_0402_10V6-K | EDP_TX3- |
| [8] CPU_EDP_TX3+ | CPU_EDP_TX3+ | C94 | 1 | 2 | .1U_0402_10V6-K | EDP_TX3+ |
| [8] CPU_EDP_TX2- | CPU_EDP_TX2- | C25 | 1 | 2 | .1U_0402_10V6-K | EDP_TX2- |
| [8] CPU_EDP_TX2+ | CPU_EDP_TX2+ | C92 | 1 | 2 | .1U_0402_10V6-K | EDP_TX2+ |
| [8] CPU_EDP_TX1- | CPU_EDP_TX1- | C18 | 1 | 2 | .1U_0402_10V6-K | EDP_TX1- |
| [8] CPU_EDP_TX1+ | CPU_EDP_TX1+ | C17 | 1 | 2 | .1U_0402_10V6-K | EDP_TX1+ |
| [8] CPU_EDP_TX0- | CPU_EDP_TX0- | C16 | 1 | 2 | .1U_0402_10V6-K | EDP_TX0- |
| [8] CPU_EDP_TX0+ | CPU_EDP_TX0+ | C19 | 1 | 2 | .1U_0402_10V6-K | EDP_TX0+ |
| [8] CPU_EDP_AUX | CPU_EDP_AUX | C20 | 1 | 2 | .1U_0402_10V6-K | EDP_AUX |
| [8] CPU_EDP_AUX# | CPU_EDP_AUX# | C21 | 1 | 2 | .1U_0402_10V6-K | EDP_AUX# |



CMOS Camera



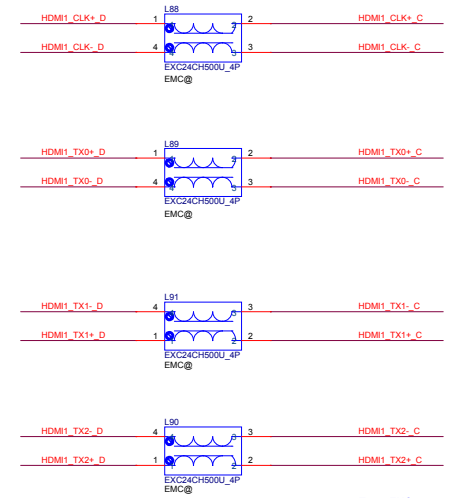
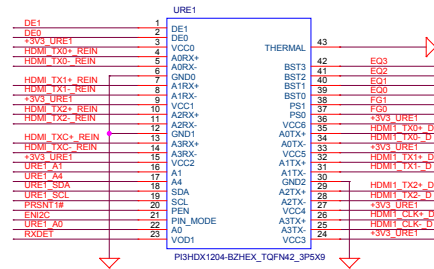
Touch Screen



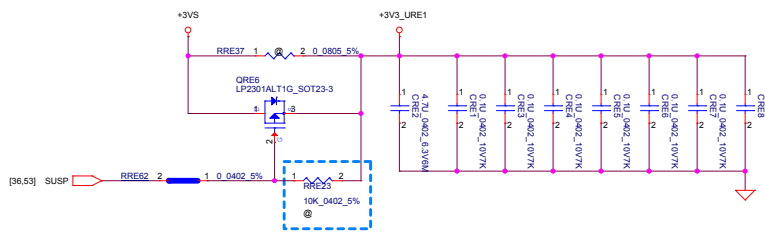
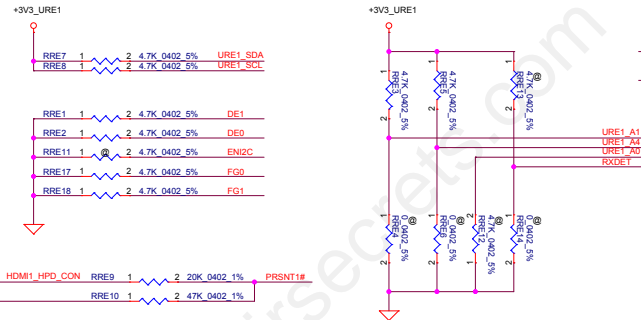
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|----------|-----------------|------------|-------|---|---|-----------------|----------------|
| HDMI D0 | [25] HDMI1_TX0+ | HDMI1_TX0+ | CRE25 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX0+ REIN |
| | [25] HDMI1_TX0- | HDMI1_TX0- | CRE26 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX0- REIN |
| HDMI D1 | [25] HDMI1_TX1+ | HDMI1_TX1+ | CRE27 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX1+ REIN |
| | [25] HDMI1_TX1- | HDMI1_TX1- | CRE28 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX1- REIN |
| HDMI D2 | [25] HDMI1_TX2+ | HDMI1_TX2+ | CRE29 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX2+ REIN |
| | [25] HDMI1_TX2- | HDMI1_TX2- | CRE30 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TX2- REIN |
| HDMI CLK | [25] HDMI1_TXC+ | HDMI1_TXC+ | CRE31 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TXC+ REIN |
| | [25] HDMI1_TXC- | HDMI1_TXC- | CRE32 | 1 | 2 | 0.1u 0402_10V7K | HDMI_TXC- REIN |



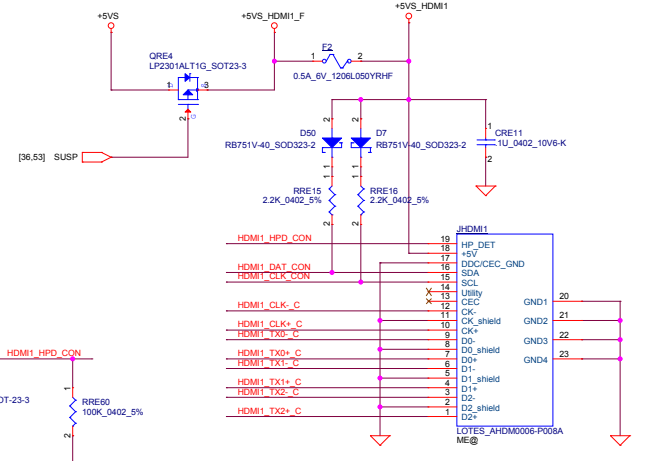
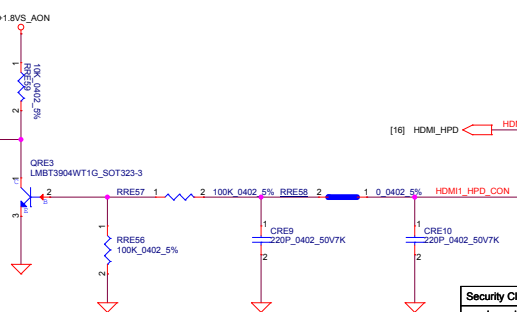
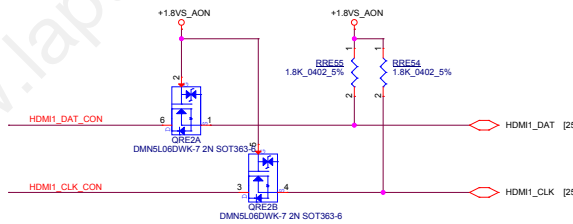
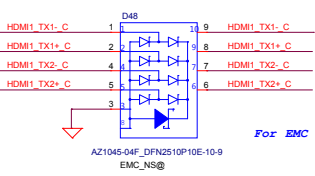
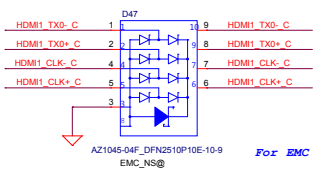
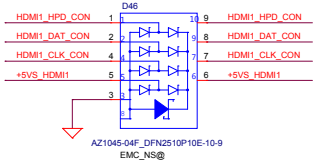
Reserve I2C & SM BUS for HDMI re-driver



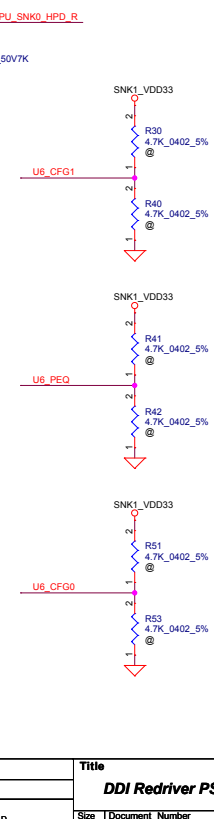
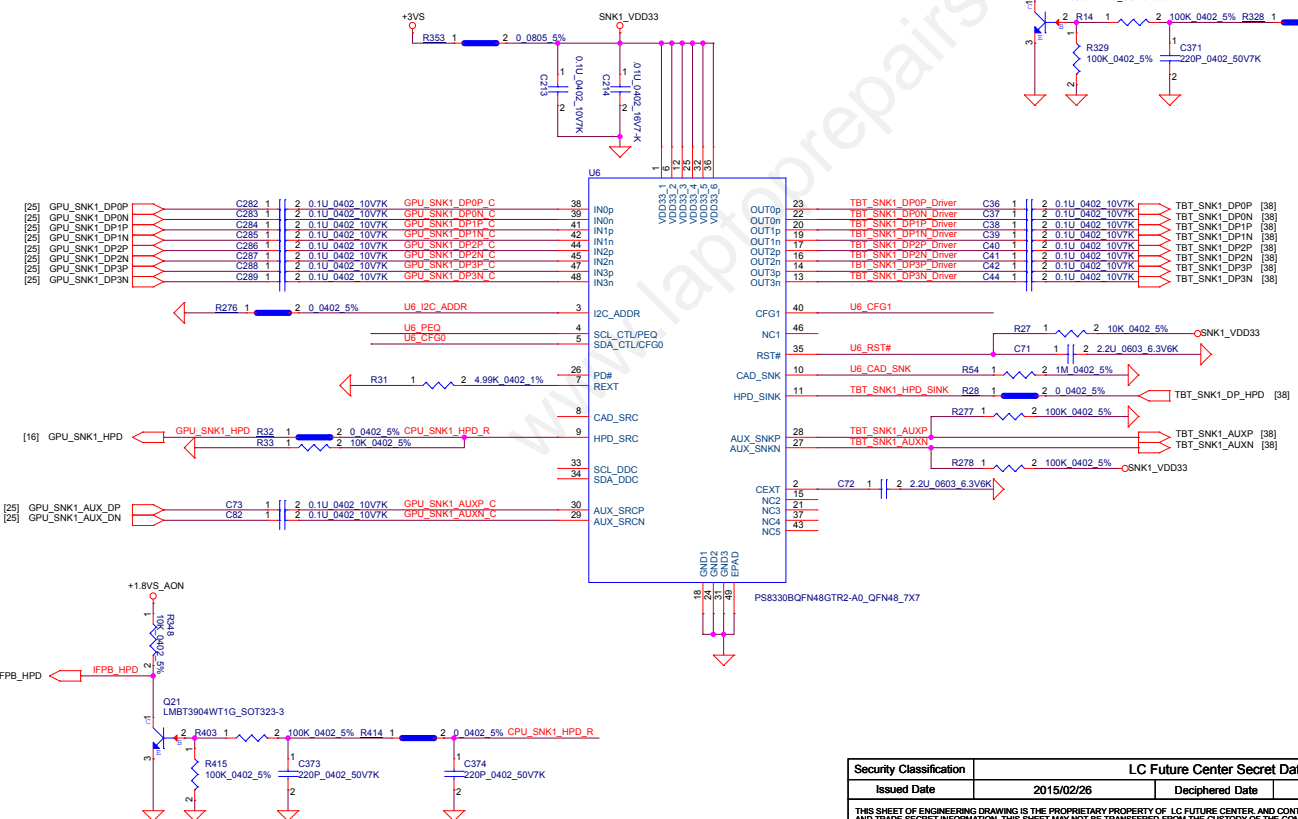
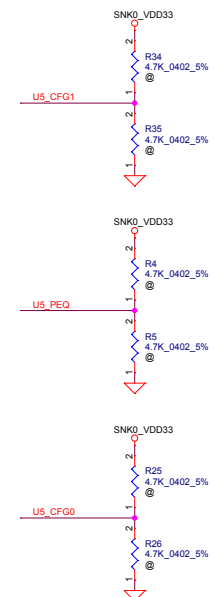
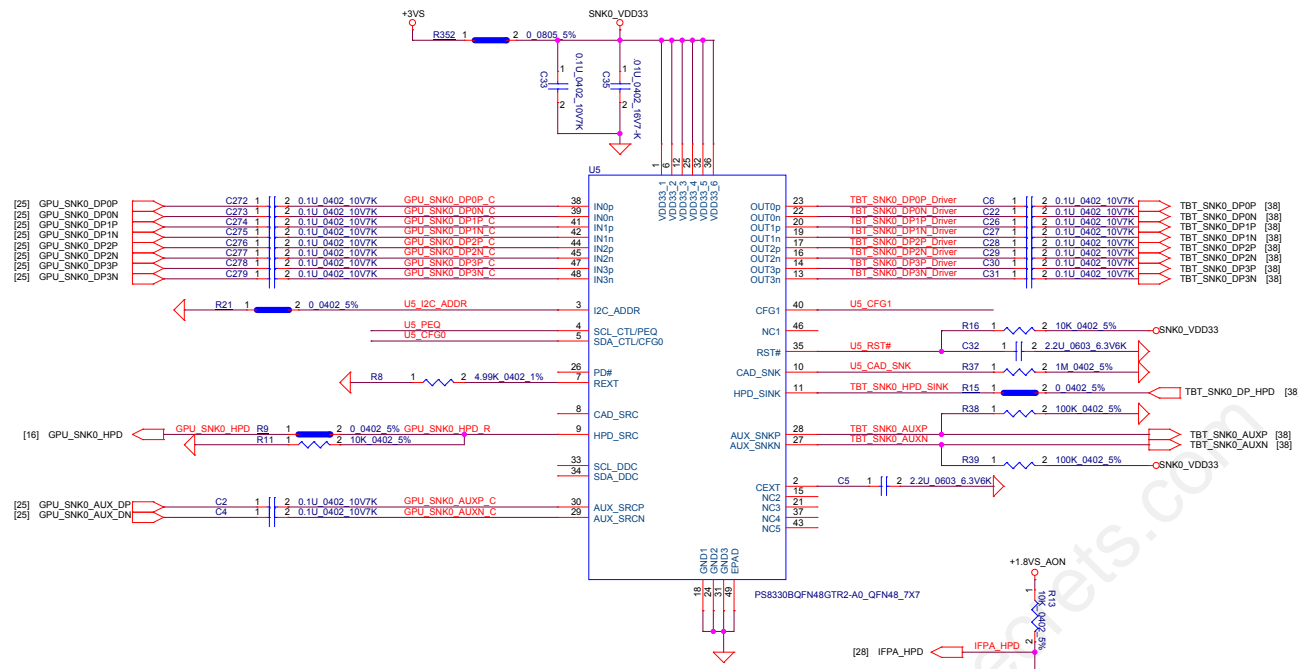
For EMC



Reserve follow HDMI certification requirement

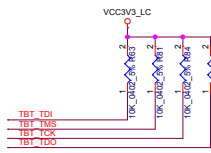


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| Security Classification | LC Future Center Secret Data | | Title | HDMI_CONN | |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | | |
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| Size | A2 | Document Number | DY510/DY511 N17E-G1 | Rev | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet | 36 | of | 76 |

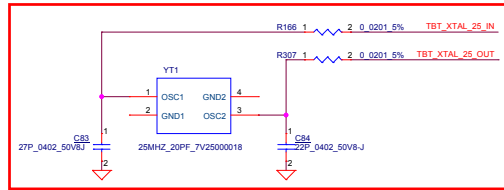


| Security Classification | LC Future Center Secret Data | | Title | |
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| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | DDI Redriver PS8330 |
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| Size C | Document Number | Rev 1.0 | | |
| Date: | DY510/DY511 N17E-G1 | Monday, December 19, 2016 | Sheet 37 of 75 | |

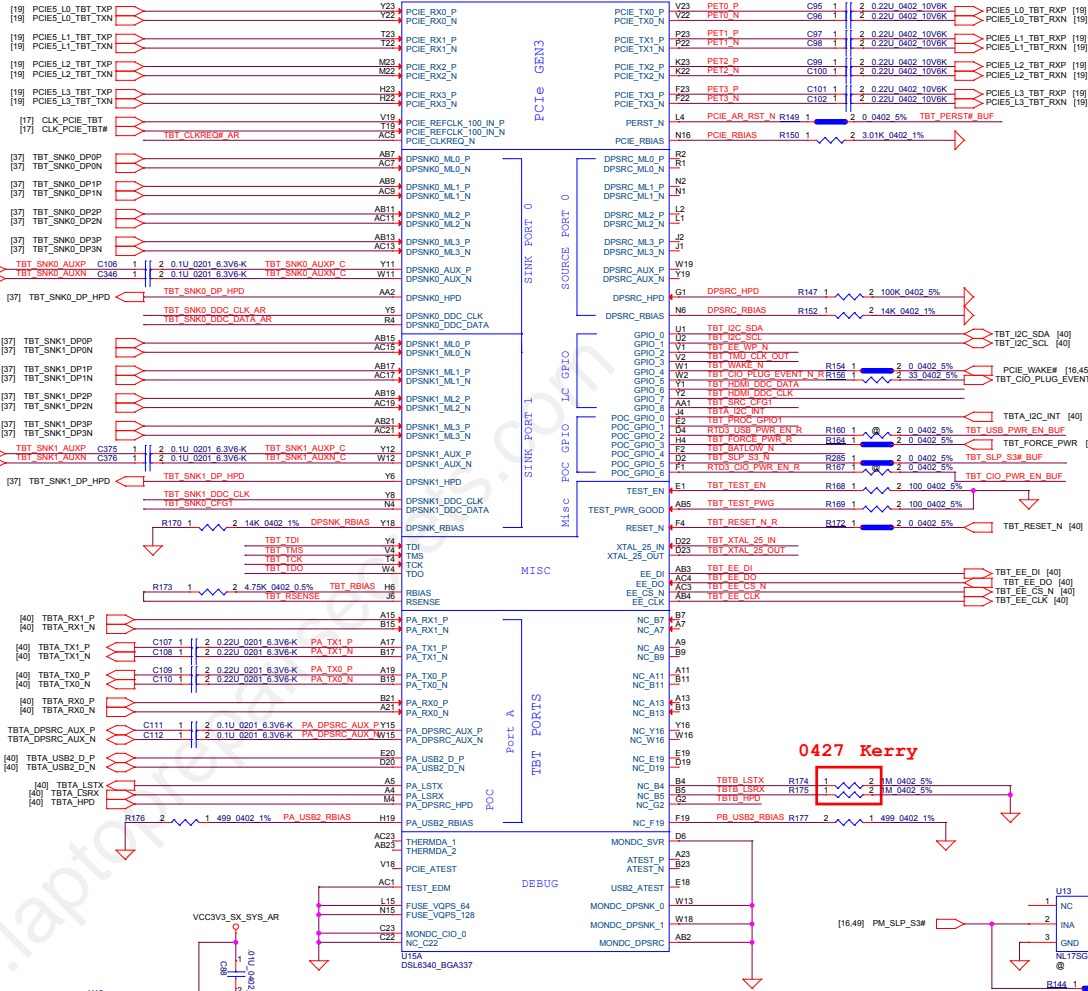
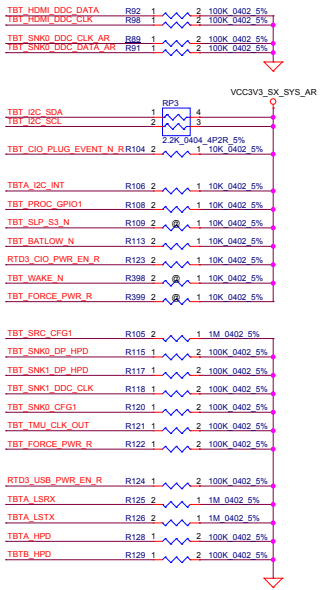
JTAG



XTAL



GPIO



0427 Kerry

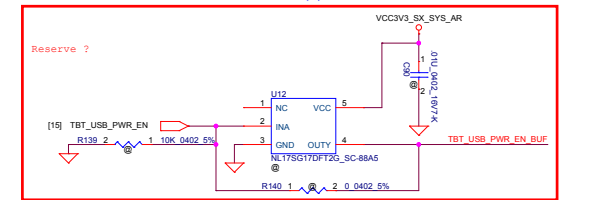
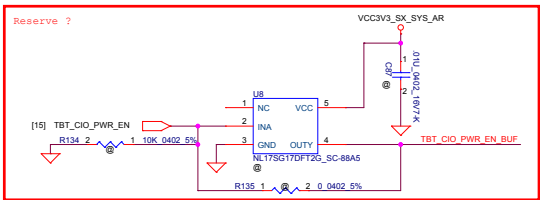
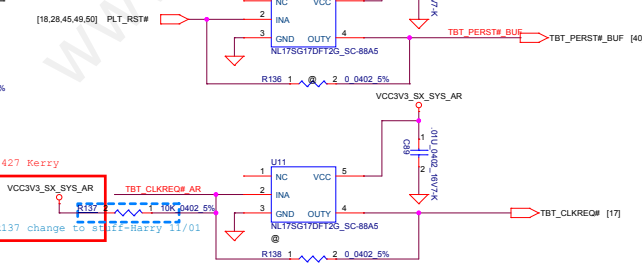
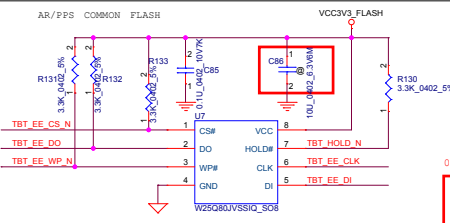
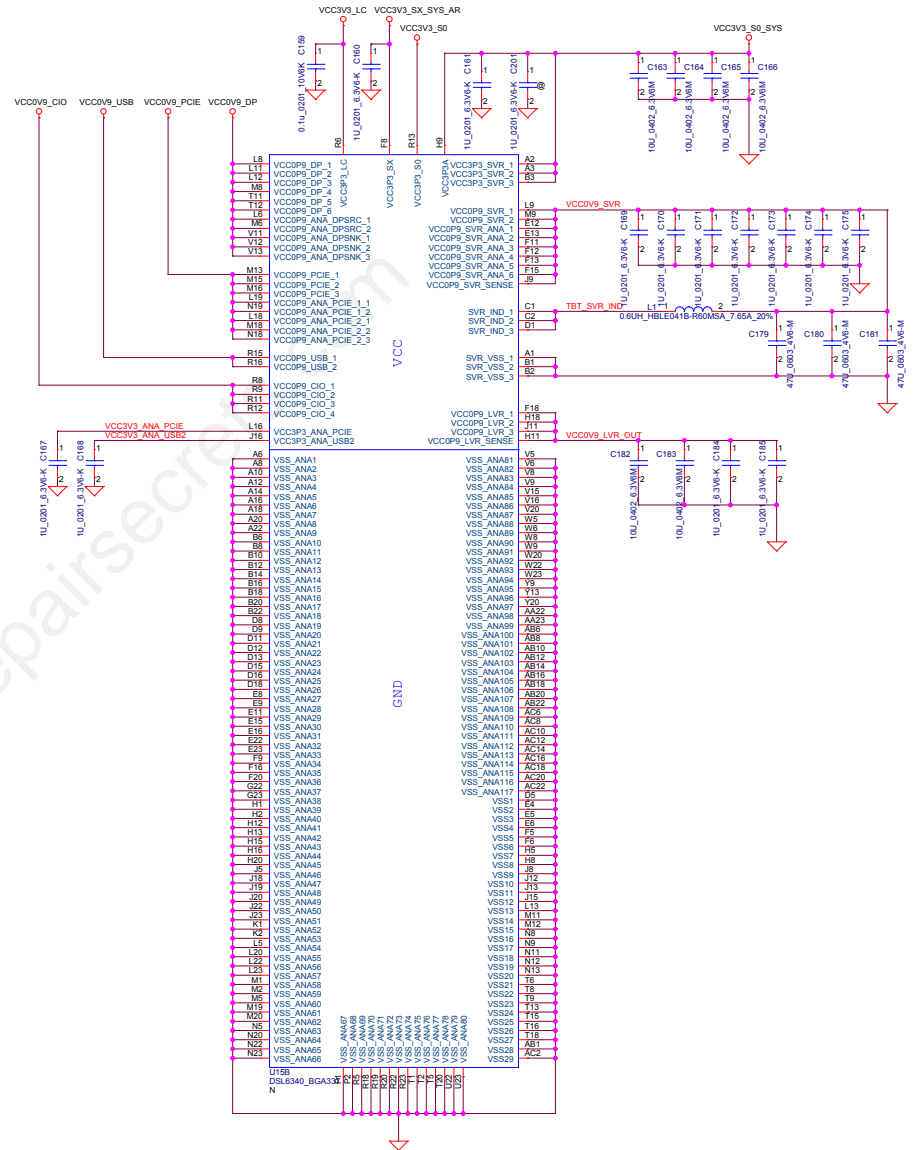
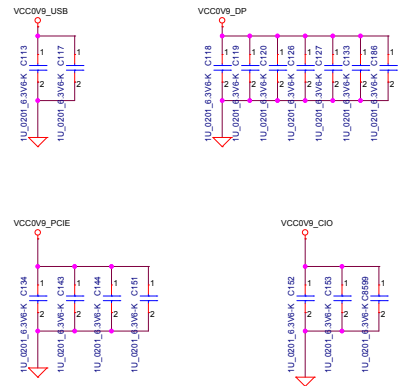


Table with 4 columns: Security Classification, LC Future Center Secret Data, Title (USB TYPE-C Controller), and Issued Date (2015/02/26). Includes a footer with document number DY510/DY511 N17E-G1 and date Monday, December 19, 2016.



Option 1 for wake support over TBT:
 1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
 2. Make sure VCC0V9_SX_SYS_AR can support AR maximum power consumption.
 3. Simple Bios implementation

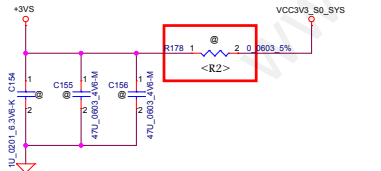
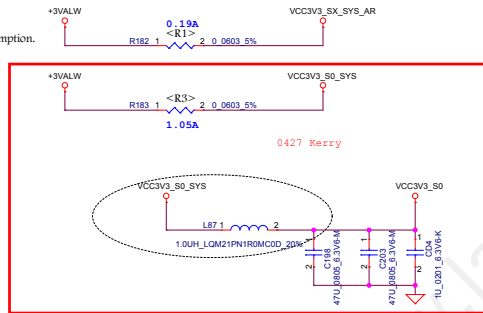
Option 2 for wake support over TBT:
 1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
 2. Bios need to implement Sx entry pre-notice flow by PCIeTBT.

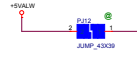
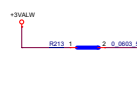
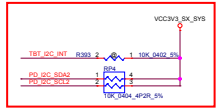
No wake support at all from AR
 1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

40KHz LC Filter to reduce VCC0V9_S0_TBT ripple

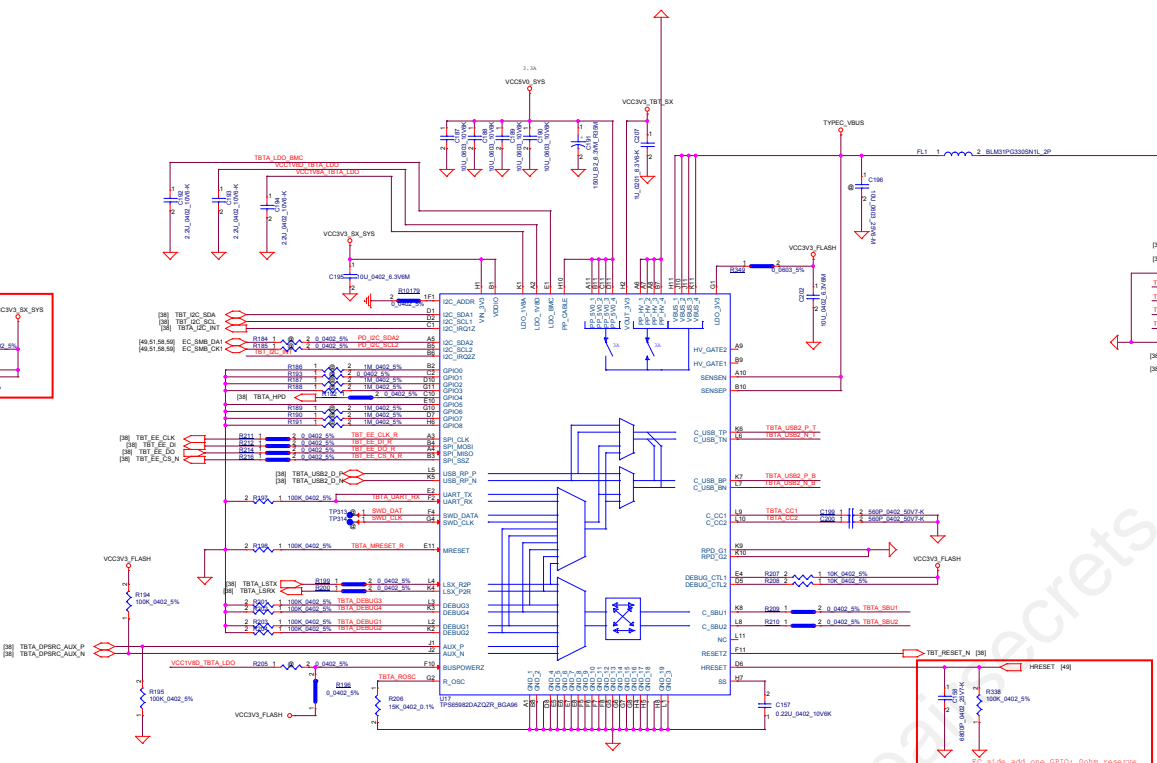
L (LQM18FN1R0MFDH):
 IDC < 0.20hm
 IDC > 0.2A

C (GRM188R60J476ME15):
 Need to notice the capacitance at 3.3 Vdc

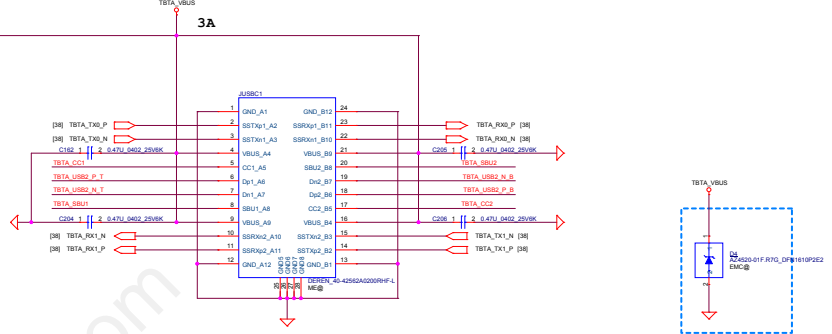




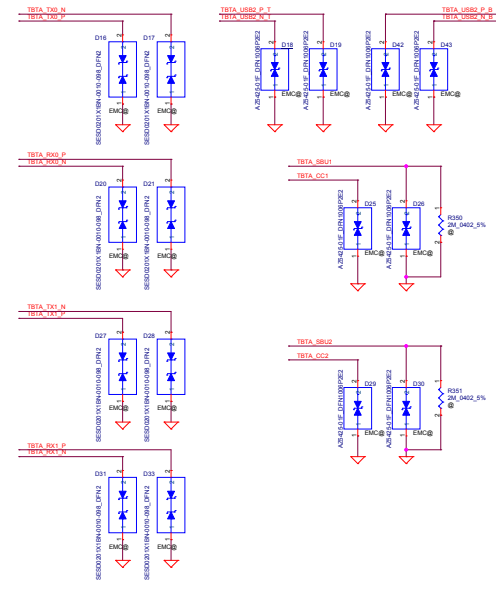
Please note MRESETN of L is active or EC setting



USB TYPE C Receptacle

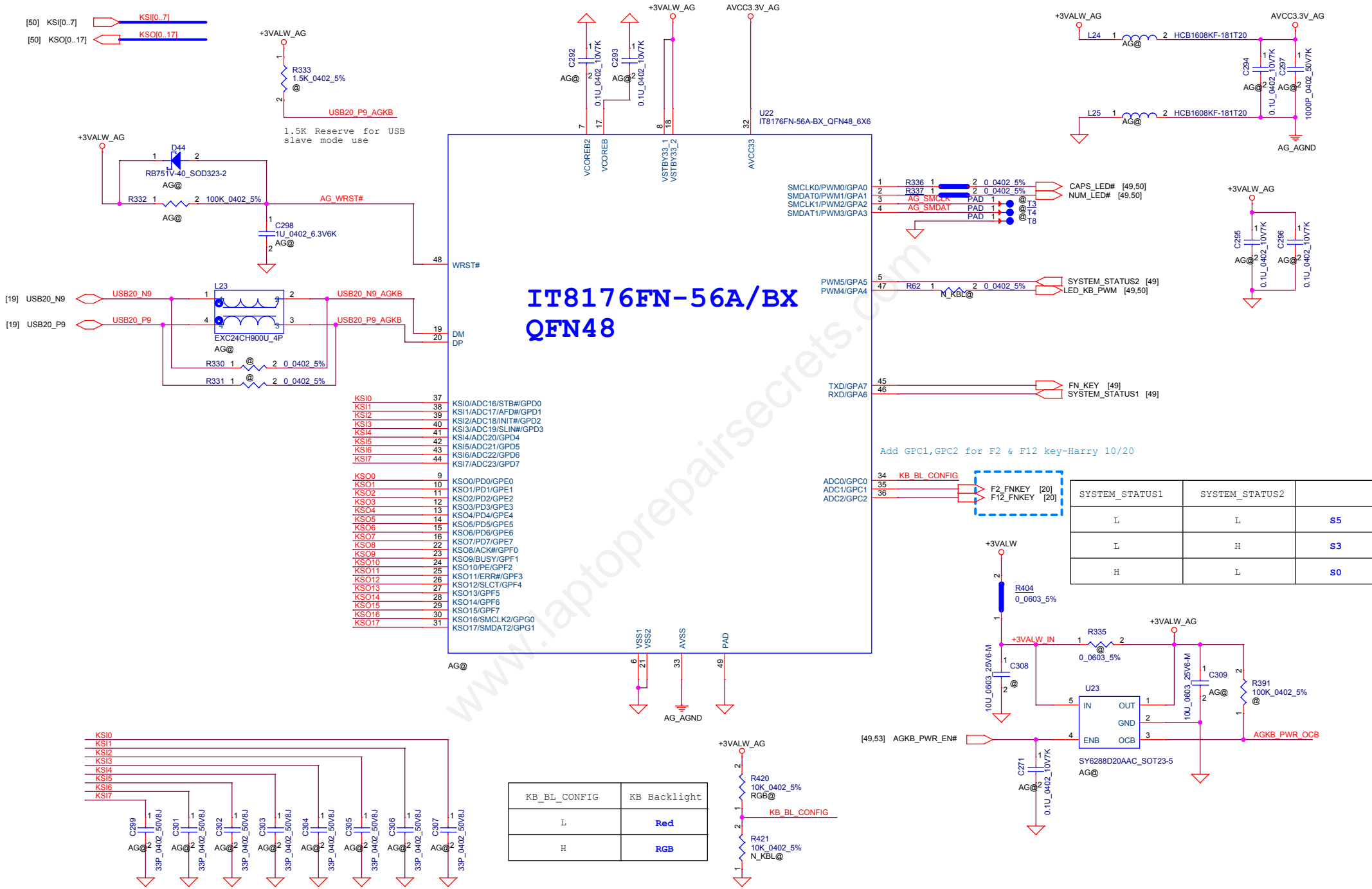


Change D4 from A25725 to A24520 -Harry 10/20



| | | | | | |
|--|-------------|------------------------------|------------|-----------------|----|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2015/02/26 | Design/Rev Date | 2016/02/26 | USB TYPE-C Port | |
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| Doc No | DY510/DY511 | Rev | M17E-G1 | Page | 14 |
| <small>LC Future Center</small> | | | | | |

IT8176FN-56A/BX QFN48



- KSI0 37 KSI0/ADC16/STB#/GPD0
- KSI1 38 KSI1/ADC17/AFD#/GPD1
- KSI2 39 KSI2/ADC18/INIT#/GPD2
- KSI3 40 KSI3/ADC19/SLIN#/GPD3
- KSI4 41 KSI4/ADC20/GPD4
- KSI5 42 KSI5/ADC21/GPD5
- KSI6 43 KSI6/ADC22/GPD6
- KSI7 44 KSI7/ADC23/GPD7
- KSO0 9 KSO0/PD0/GPE0
- KSO1 10 KSO1/PD1/GPE1
- KSO2 11 KSO2/PD2/GPE2
- KSO3 12 KSO3/PD3/GPE3
- KSO4 13 KSO4/PD4/GPE4
- KSO5 14 KSO5/PD5/GPE5
- KSO6 15 KSO6/PD6/GPE6
- KSO7 16 KSO7/PD7/GPE7
- KSO8 22 KSO8/ACK#/GPF0
- KSO9 23 KSO9/BUSY/GPF1
- KSO10 24 KSO10/PE/GPF2
- KSO11 25 KSO11/ERR#/GPF3
- KSO12 26 KSO12/SLCT/GPF4
- KSO13 27 KSO13/GPF5
- KSO14 28 KSO14/GPF6
- KSO15 29 KSO15/GPF7
- KSO16 30 KSO16/SMCLK2/GPG0
- KSO17 31 KSO17/SMDAT2/GPG1

| SYSTEM_STATUS1 | SYSTEM_STATUS2 | |
|----------------|----------------|----|
| L | L | S5 |
| L | H | S3 |
| H | L | S0 |

| KB_BL_CONFIG | KB Backlight |
|--------------|--------------|
| L | Red |
| H | RGB |


| | | | | |
|---|------------------------------|-----------------|------------|---|
| Security Classification | LC Future Center Secret Data | | Title |  Anti-ghost KB |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 | |
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TABLE : CPU ITP DEBUG REPORT

| | No use | Individual Port | DCI 2.0 w/o connector |
|-------|--------|-----------------|-----------------------|
| R591 | NO ASM | NO ASM | ASM |
| R593 | NO ASM | NO ASM | ASM |
| R594 | NO ASM | NO ASM | ASM |
| R595 | NO ASM | NO ASM | ASM |
| R596 | NO ASM | NO ASM | ASM |
| R657 | NO ASM | NO ASM | ASM |
| R658 | NO ASM | NO ASM | ASM |
| R102 | NO ASM | ASM | NO ASM |
| R597 | NO ASM | ASM | NO ASM |
| R9907 | NO ASM | ASM | ASM |
| JXDP1 | NO ASM | ASM | NO ASM |
| C70 | NO ASM | ASM | NO ASM |
| R96 | NO ASM | ASM | NO ASM |
| R101 | NO ASM | ASM | NO ASM |
| R9909 | NO ASM | ASM | ASM |
| R9910 | NO ASM | ASM | ASM |
| R9916 | NO ASM | ASM | ASM |
| R99 | NO ASM | ASM | ASM |
| R9912 | NO ASM | ASM | ASM |
| R9934 | NO ASM | ASM | ASM |
| R9930 | NO ASM | ASM | ASM |
| R9931 | NO ASM | ASM | ASM |
| R9932 | NO ASM | ASM | ASM |
| R9933 | NO ASM | ASM | ASM |

LOGIC

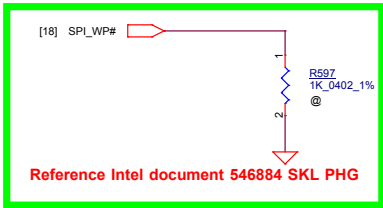
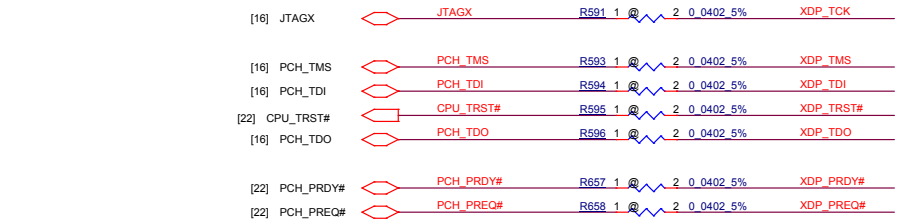
TABLE : PCH ITP DEBUG REPORT

| | No use | Individual Port | DCI 2.0 w/o connector |
|-------|--------|-----------------|-----------------------|
| R93 | NO ASM | ASM | NO ASM |
| JXDP1 | NO ASM | ASM | NO ASM |
| R9917 | NO ASM | ASM | NO ASM |
| R101 | NO ASM | ASM | NO ASM |
| R9908 | NO ASM | ASM | NO ASM |
| R9911 | NO ASM | ASM | NO ASM |
| R9913 | NO ASM | ASM | NO ASM |
| R9915 | NO ASM | ASM | NO ASM |

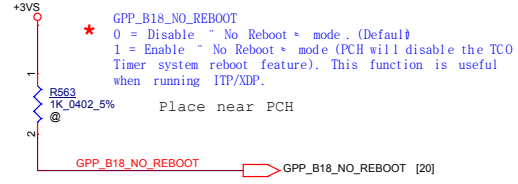
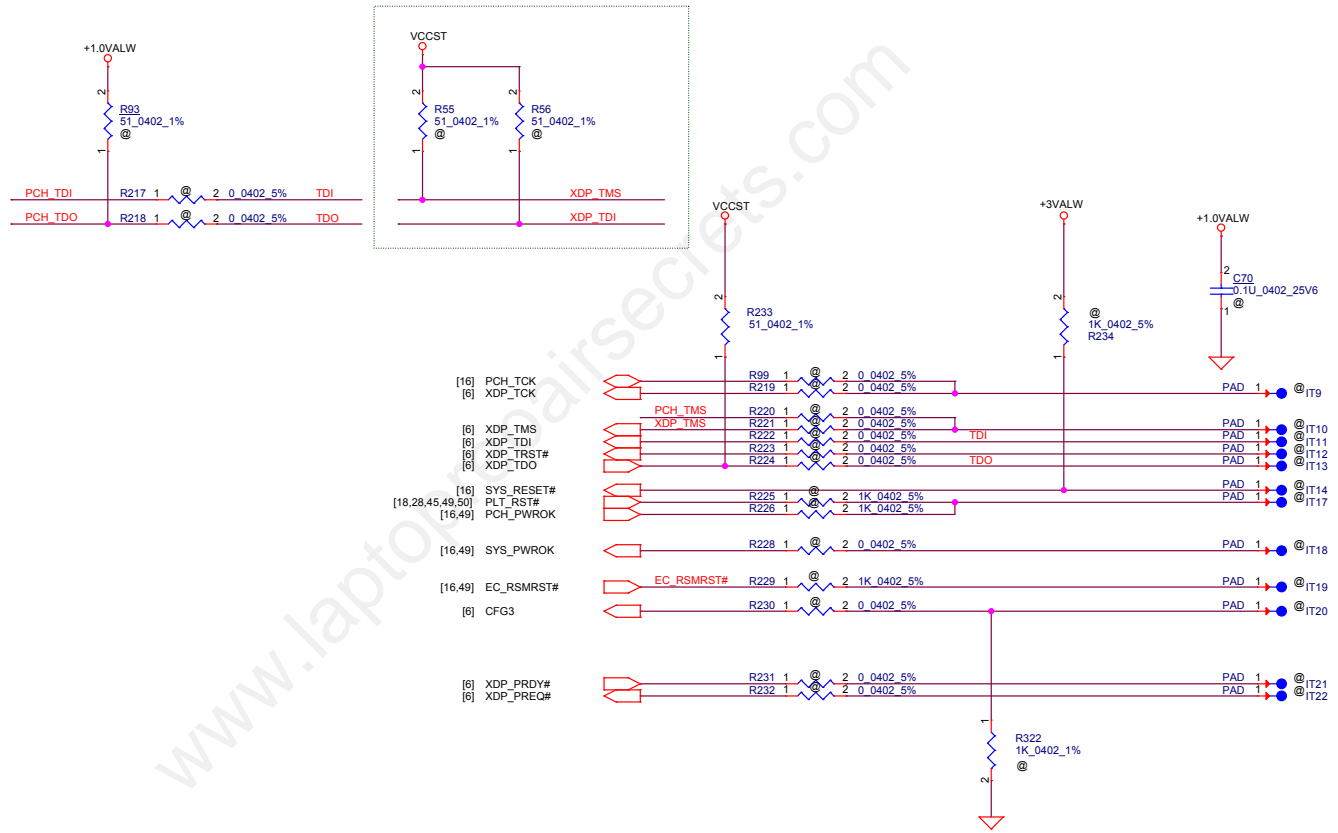
LOGIC

TABLE : Functional Strap

| GPP_B18/GSPI0_MOSI (No Reboot) | R563 |
|--|--------|
| HIGH Enable "No Reboot" Mode | ASM |
| LOW Disable "No Reboot" Mode (Default) | NO ASM |



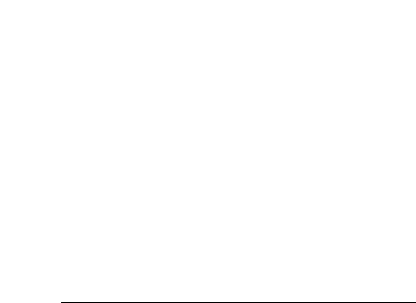
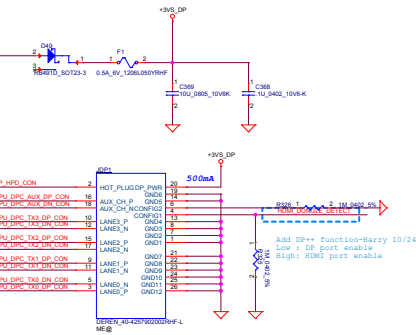
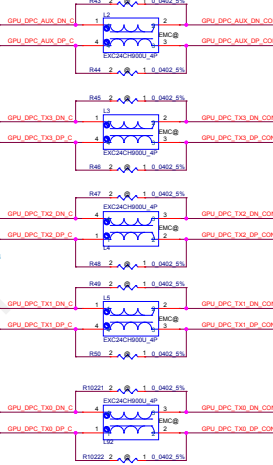
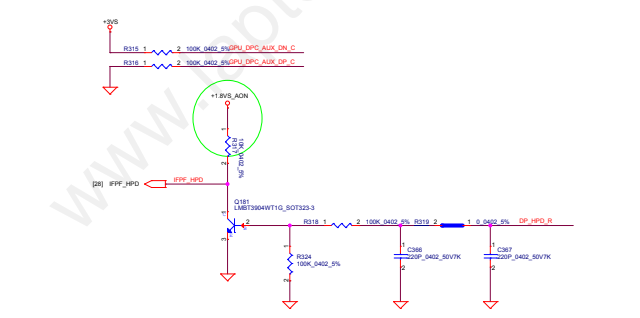
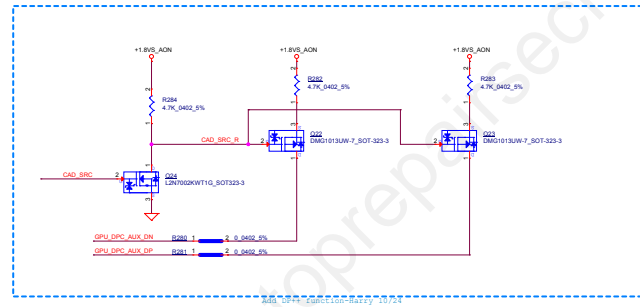
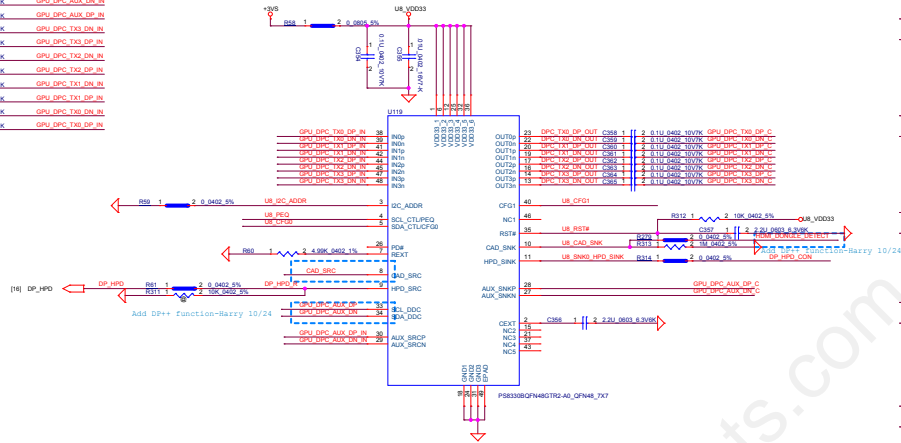
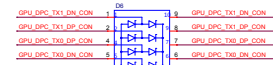
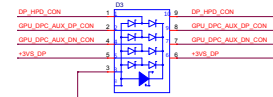
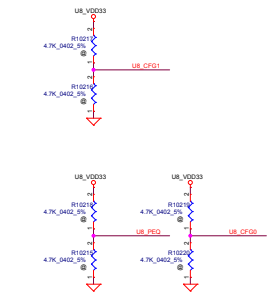
Reference Intel document 546884 SKL PHG



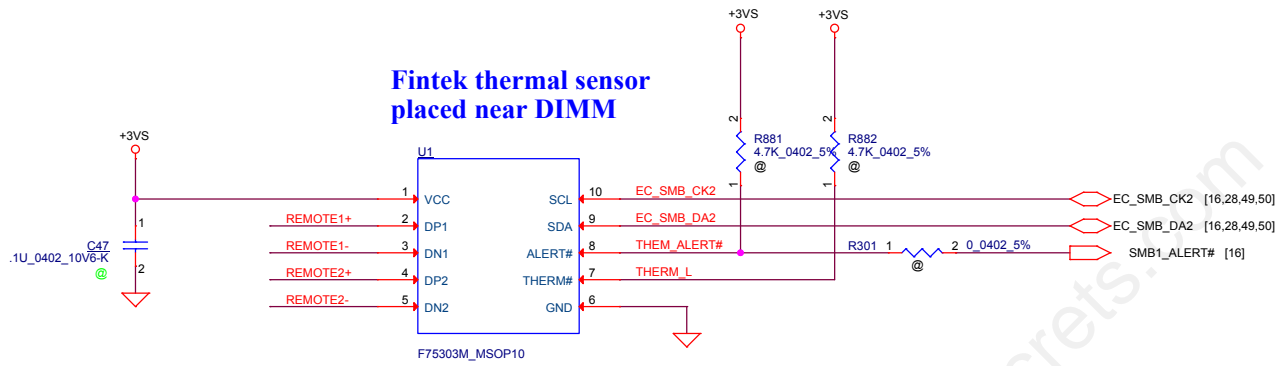
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|--------|---------------------------|----------------|
| Custom | DY510/DY511 N17E-G1 | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet 42 of 75 |

| | | | | | | |
|--------------------|----------------|------|---|---|-----------------|-------------------|
| [D] GPU_DPC_AUX_DN | GPU_DPC_AUX_DN | C34 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_AUX_DN_IN |
| [D] GPU_DPC_AUX_DP | GPU_DPC_AUX_DP | C341 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_AUX_DP_IN |
| [D] GPU_DPC_TX3_DN | GPU_DPC_TX3_DN | C342 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX3_DN_IN |
| [D] GPU_DPC_TX3_DP | GPU_DPC_TX3_DP | C347 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX3_DP_IN |
| [D] GPU_DPC_TX2_DN | GPU_DPC_TX2_DN | C348 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX2_DN_IN |
| [D] GPU_DPC_TX2_DP | GPU_DPC_TX2_DP | C349 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX2_DP_IN |
| [D] GPU_DPC_TX1_DN | GPU_DPC_TX1_DN | C350 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX1_DN_IN |
| [D] GPU_DPC_TX1_DP | GPU_DPC_TX1_DP | C351 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX1_DP_IN |
| [D] GPU_DPC_TX5_DN | GPU_DPC_TX5_DN | C352 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX5_DN_IN |
| [D] GPU_DPC_TX5_DP | GPU_DPC_TX5_DP | C353 | 1 | 2 | 0.1U_0402_100YK | GPU_DPC_TX5_DP_IN |

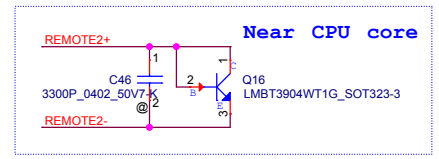
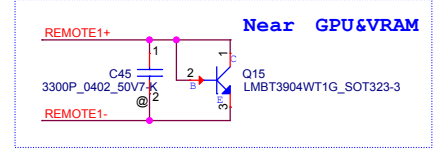


| | | | |
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| Issued Date | 2013/09/06 | Design Date | 2016/06/13 |
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| Doc No | DY510/DY511 M17E-G1 | Rev | 14 |
| Date | Monday, December 15, 2016 | Sheet | 43 of 73 |



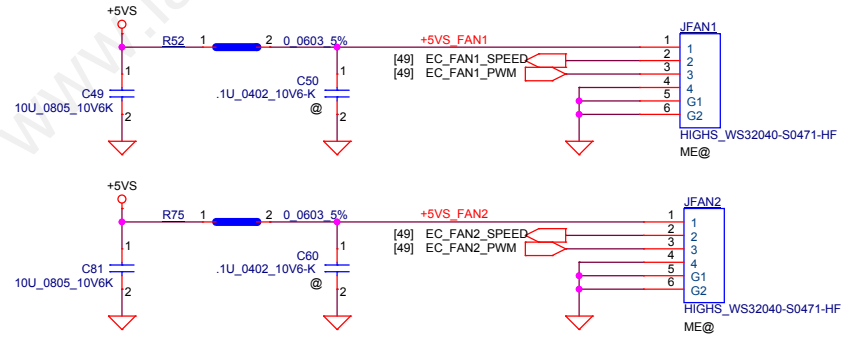
Fintek thermal sensor placed near DIMM

REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



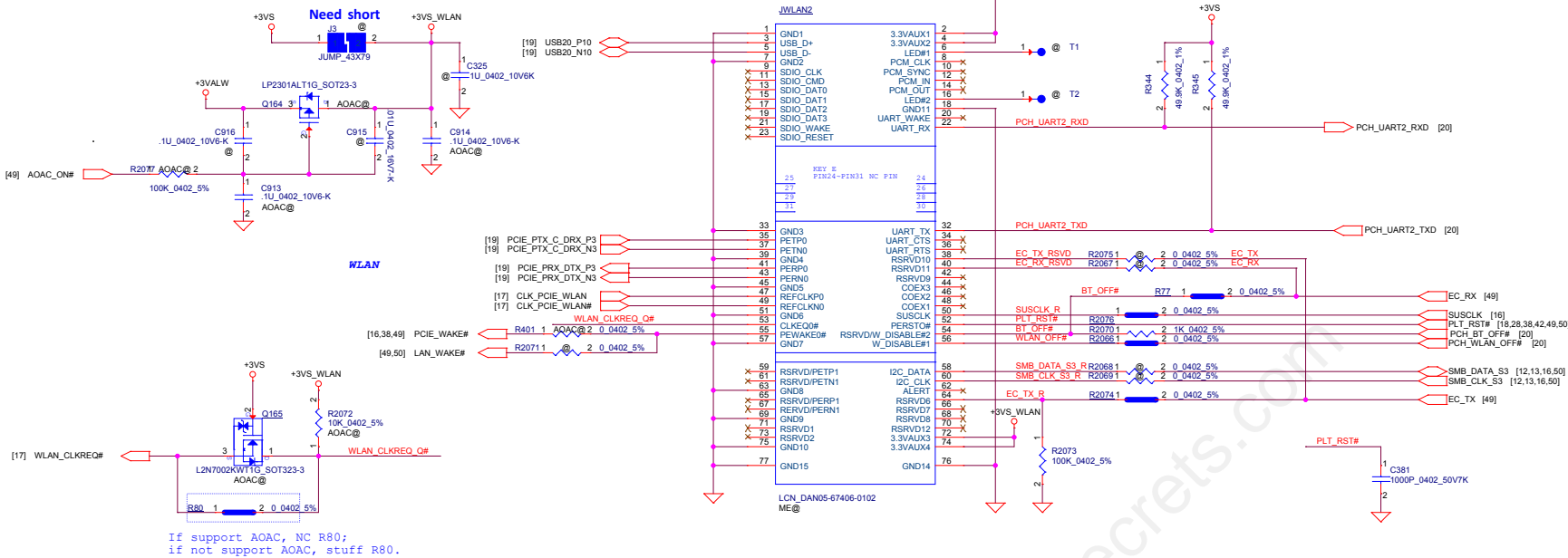
FAN Conn

Address 1001_101xb

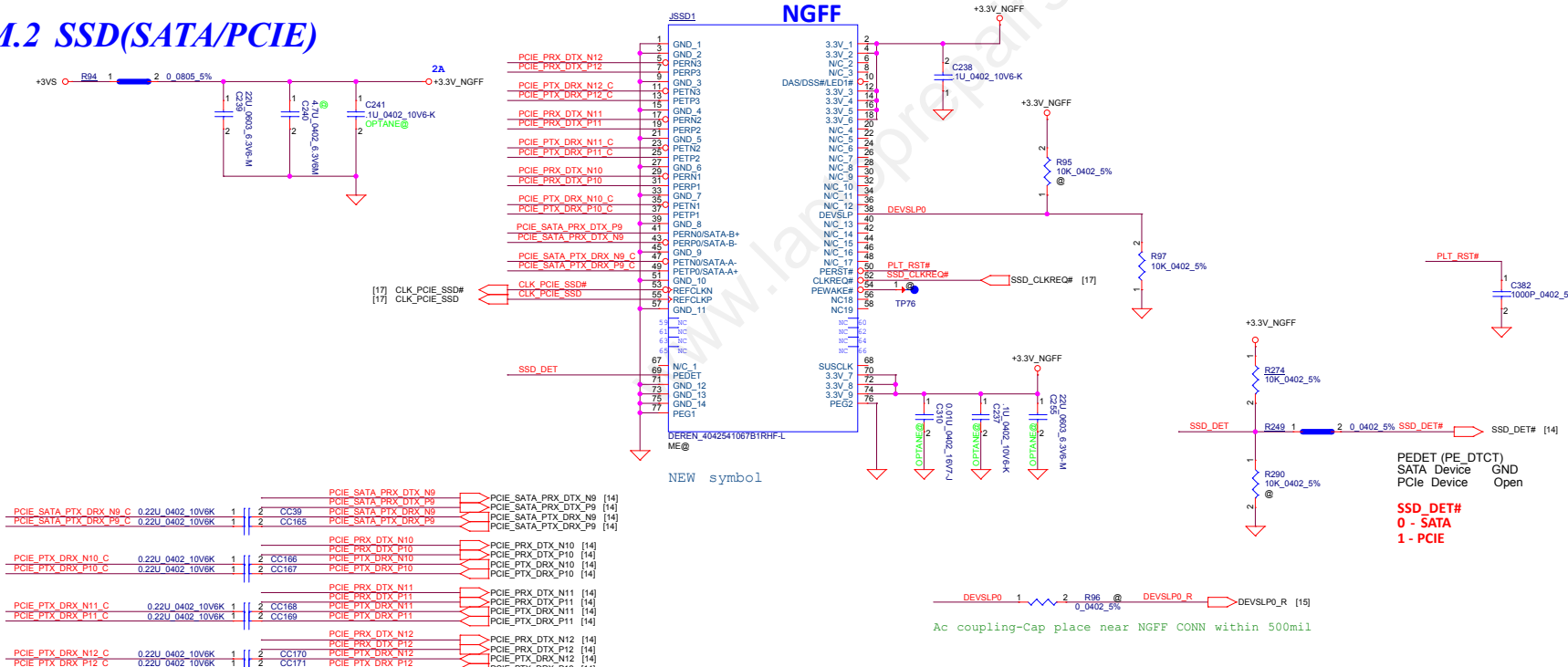


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Mini-Express Card(WLAN/WiMAX)

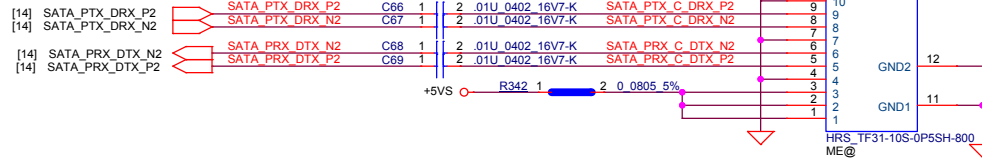
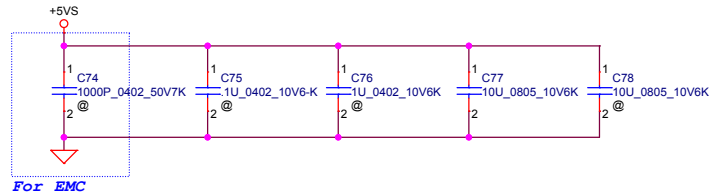


M.2 SSD(SATA/PCIE)

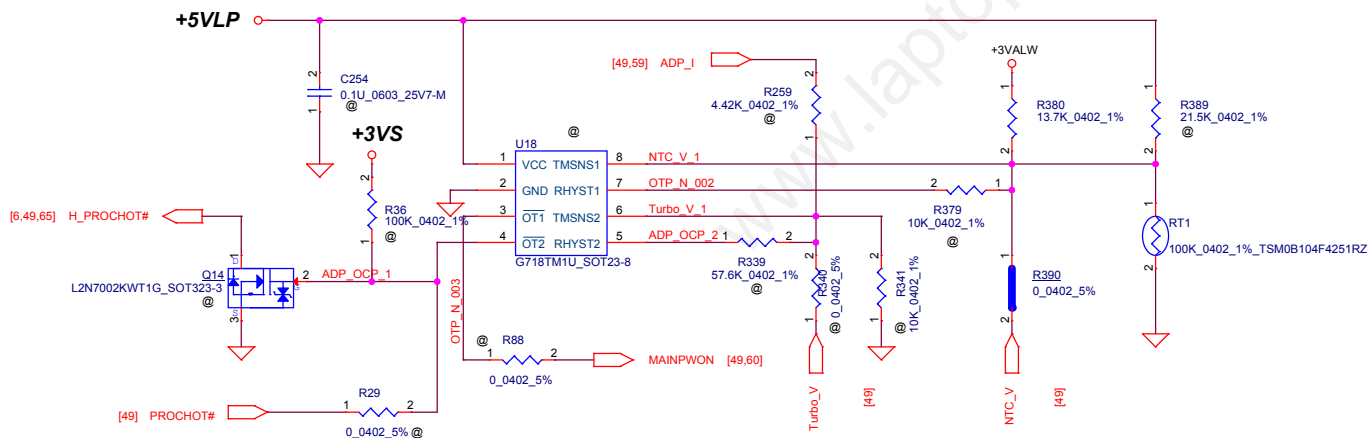
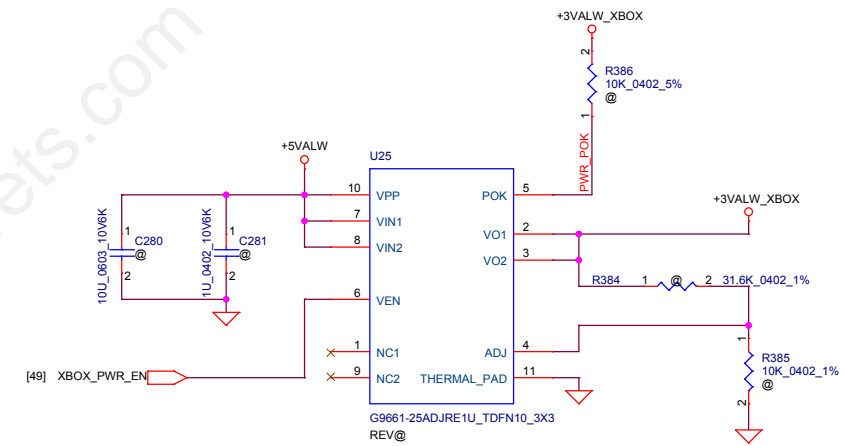
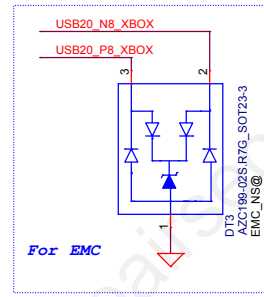
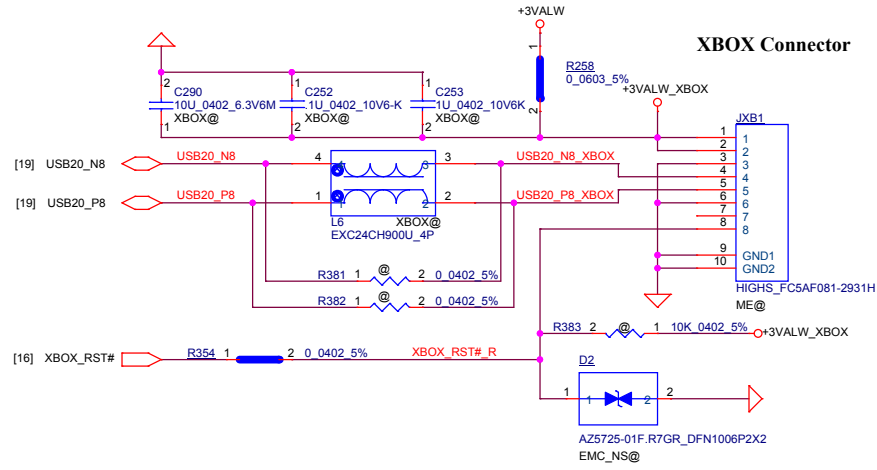


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| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 |
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| Size | Document Number | Rev | 1.0 |
| Custom | DY510/DY511 N17E-G1 | | |
| Date: | Monday, December 18, 2016 | Sheet | 45 of 75 |

SATA HDD Conn.



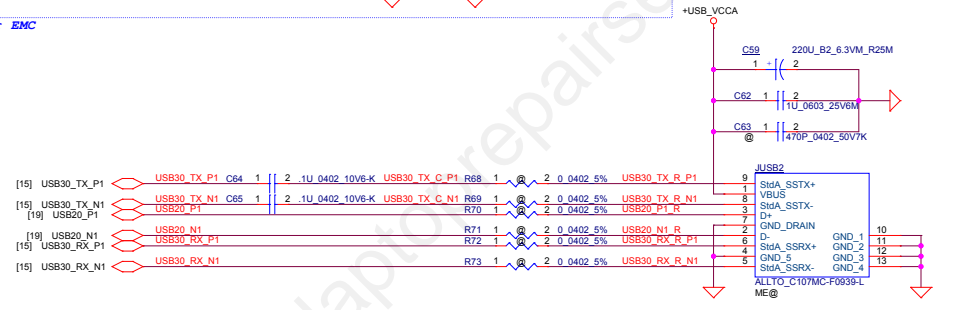
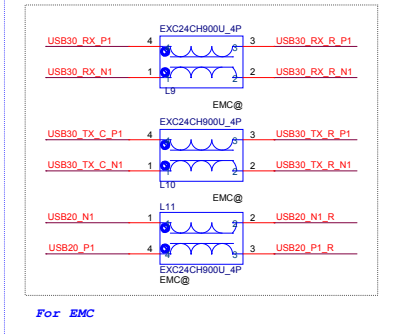
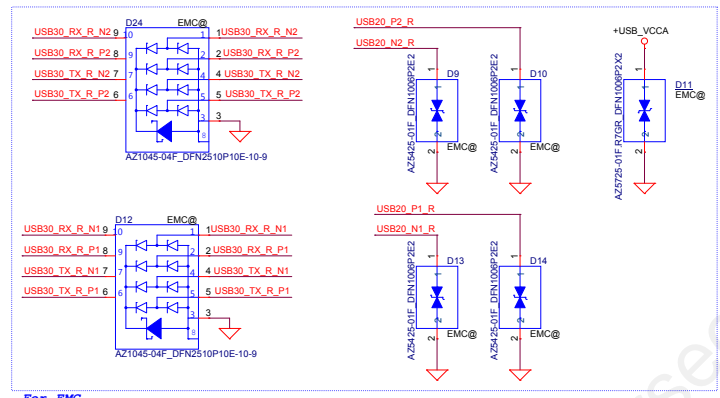
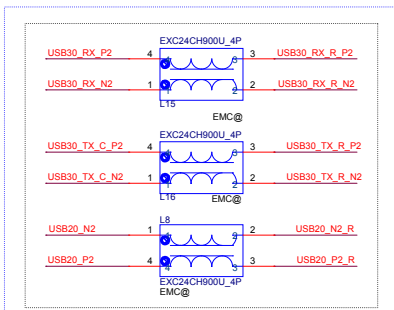
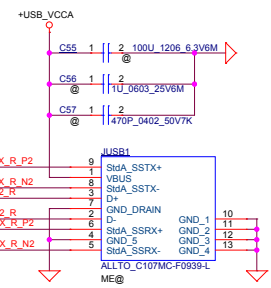
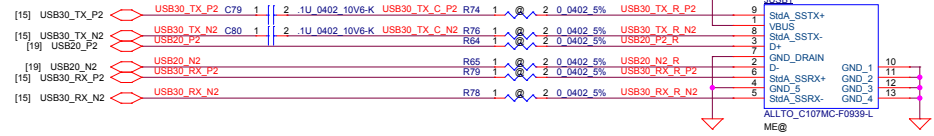
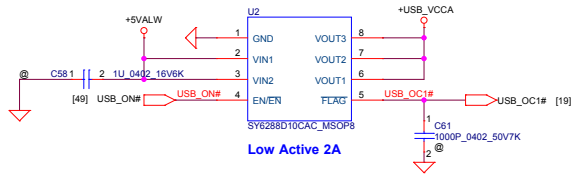
XBOX Connector

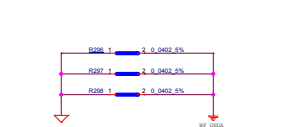
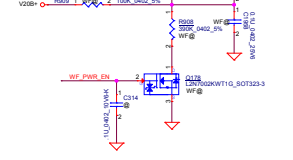
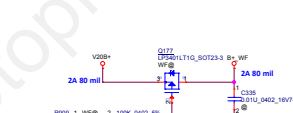
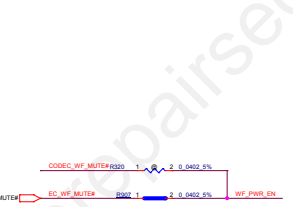
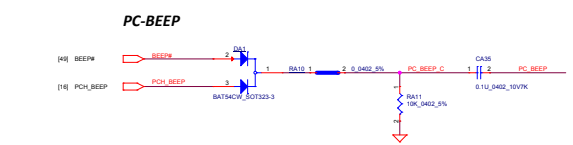
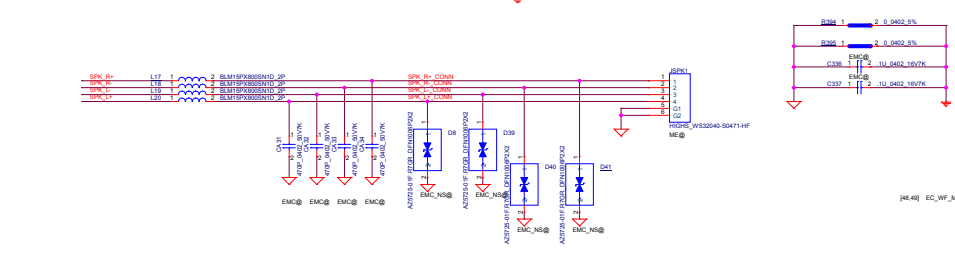
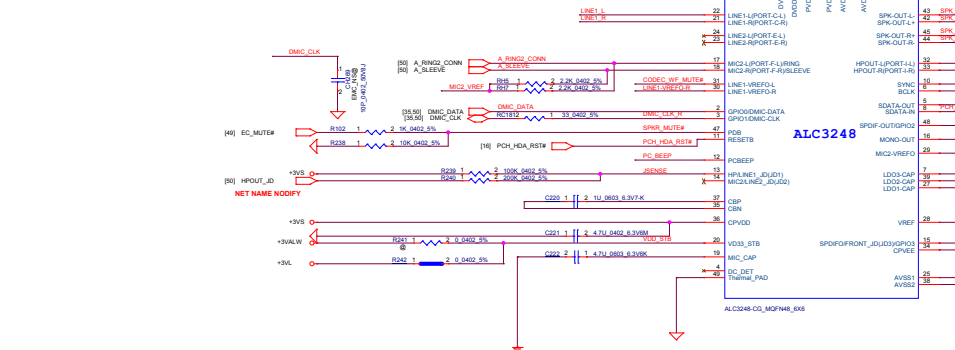
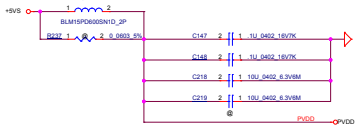


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| | | |
|---------------|---------------------------|----------------|
| Title | | |
| HDD/XBOX CONN | | |
| Size | Document Number | Rev |
| Custom | DY510/DY511 N17E-G1 | |
| Date: | Monday, December 19, 2016 | Sheet 46 of 75 |

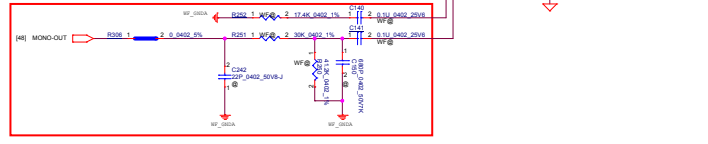
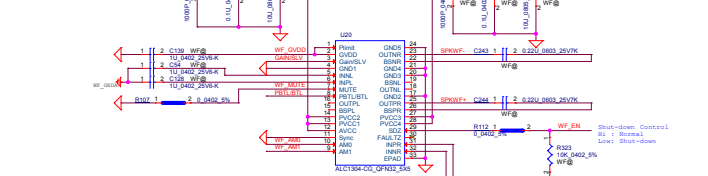
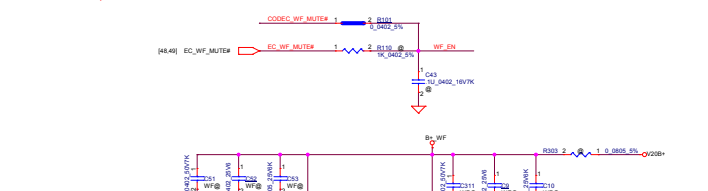
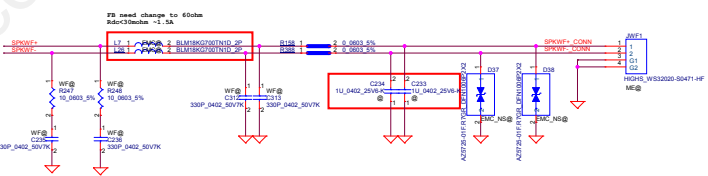
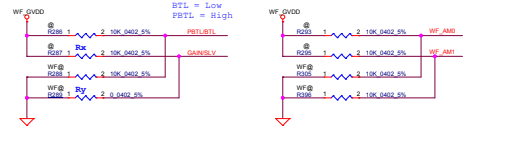
LEFT SIDE USB3.0 PORT X2

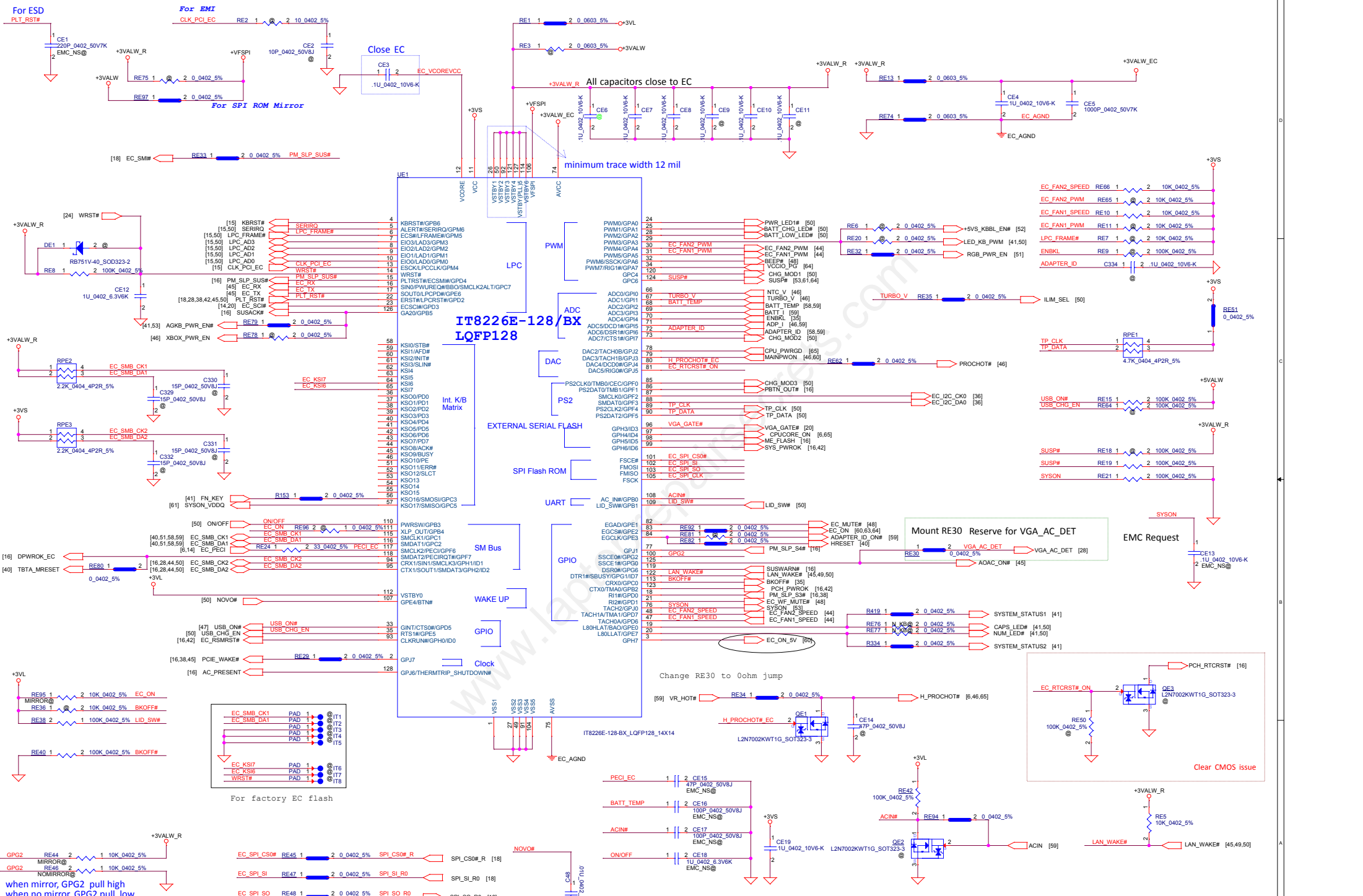




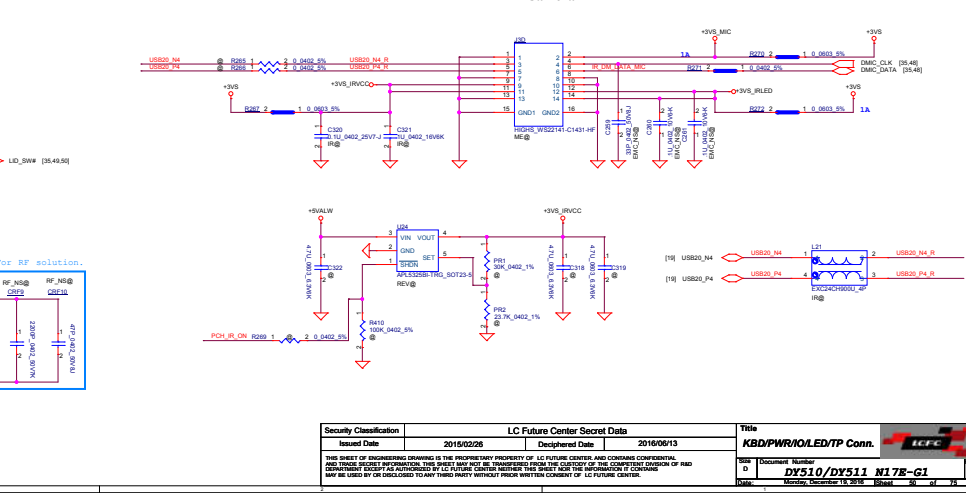
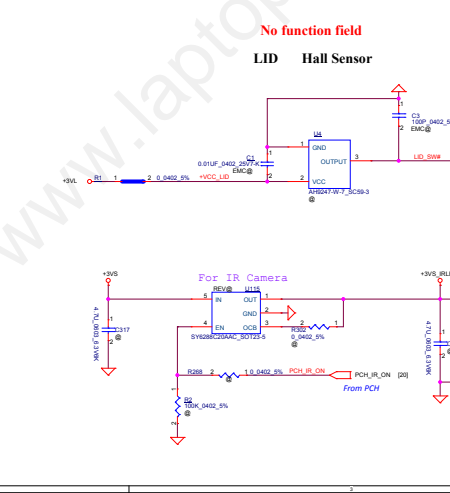
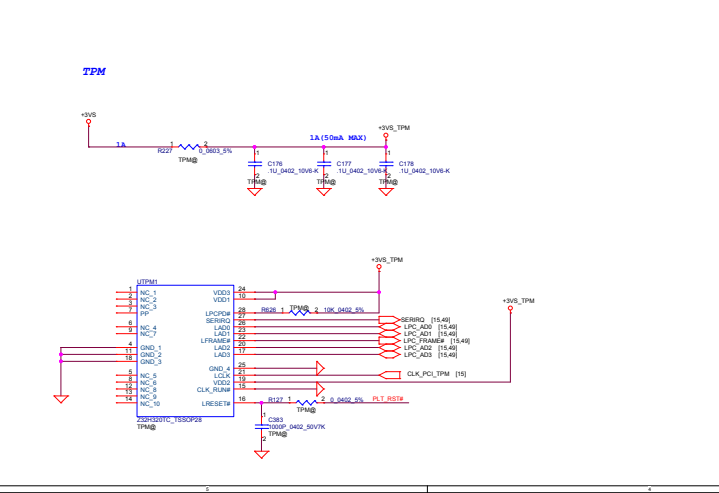
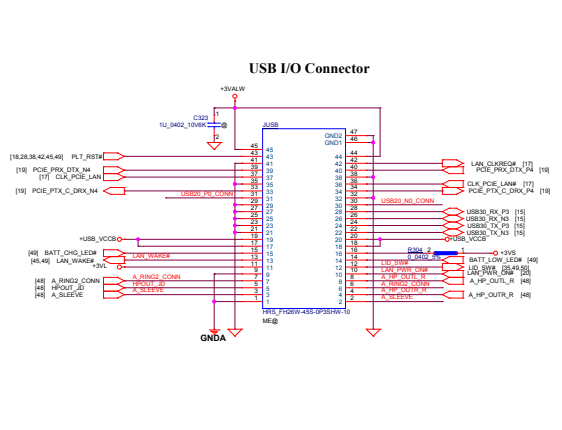
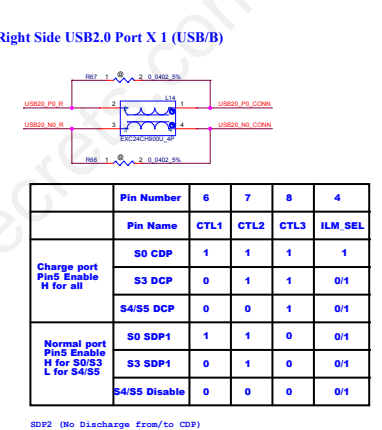
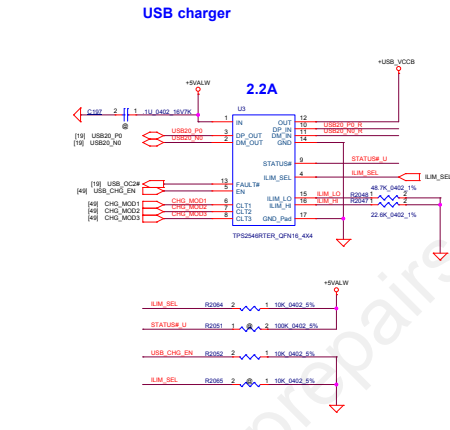
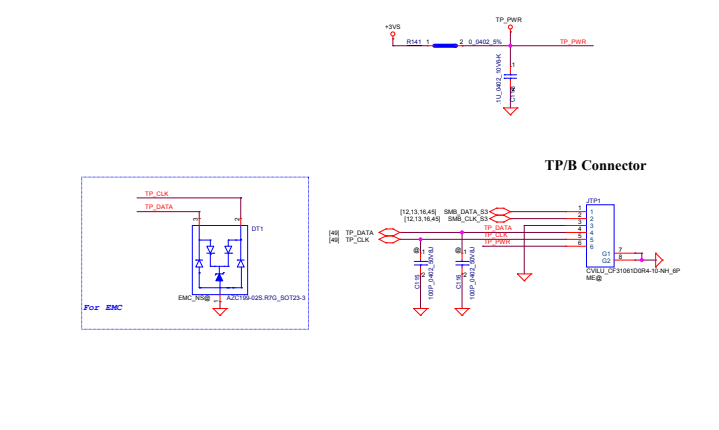
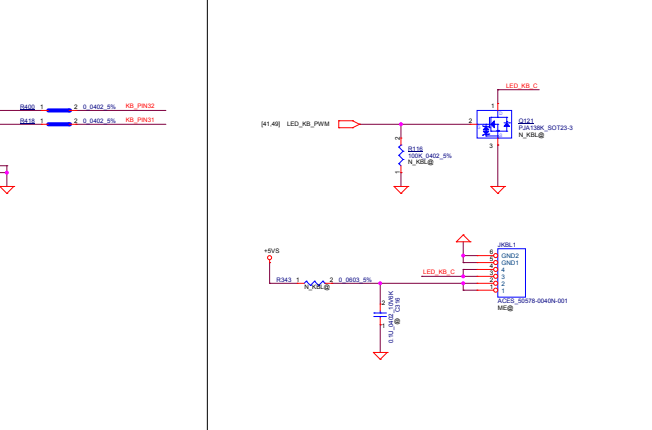
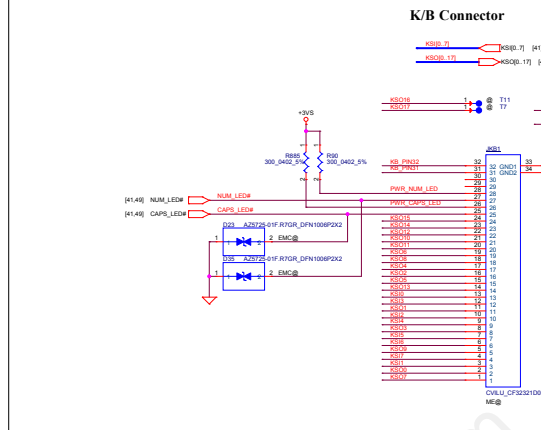
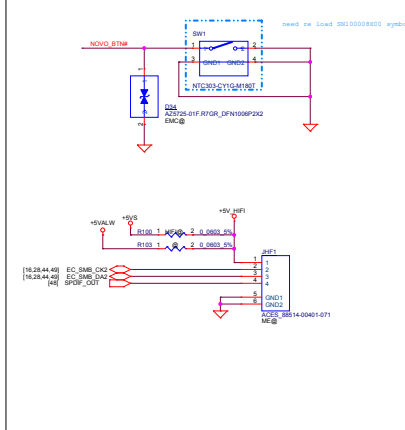
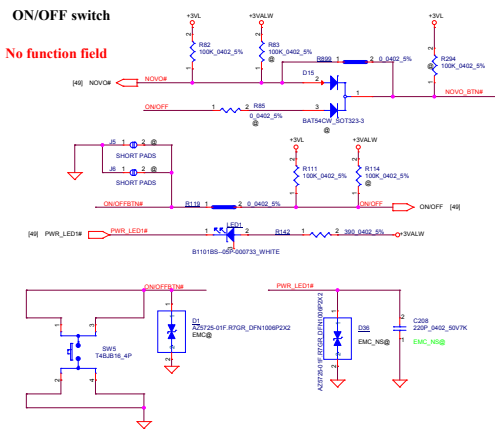
| Mode | Min | Max | Fs | Fs |
|--------|------|-----|------|------|
| Master | 256k | 512 | 44.1 | 48 |
| | 256k | 768 | 44.1 | 48 |
| | 256k | 432 | 25.5 | 28.8 |
| Slave | 256k | 512 | 44.1 | 48 |
| | 256k | 432 | 44.1 | 48 |
| | 256k | 258 | 25.5 | 28.8 |

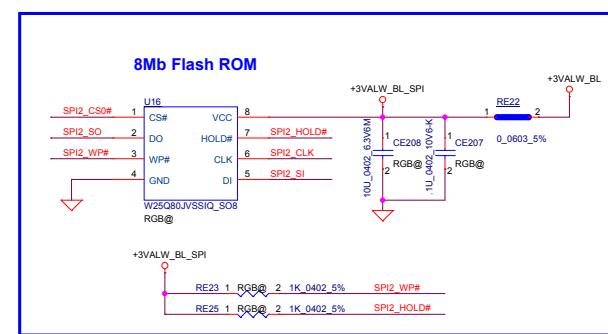
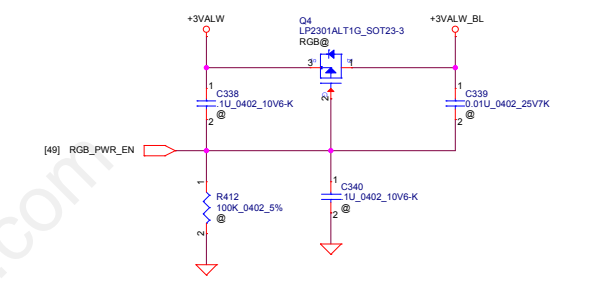
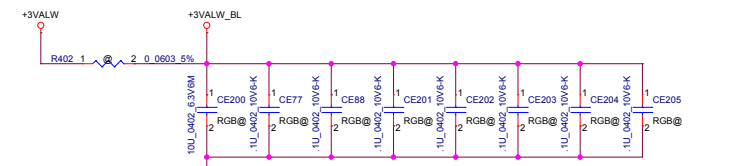
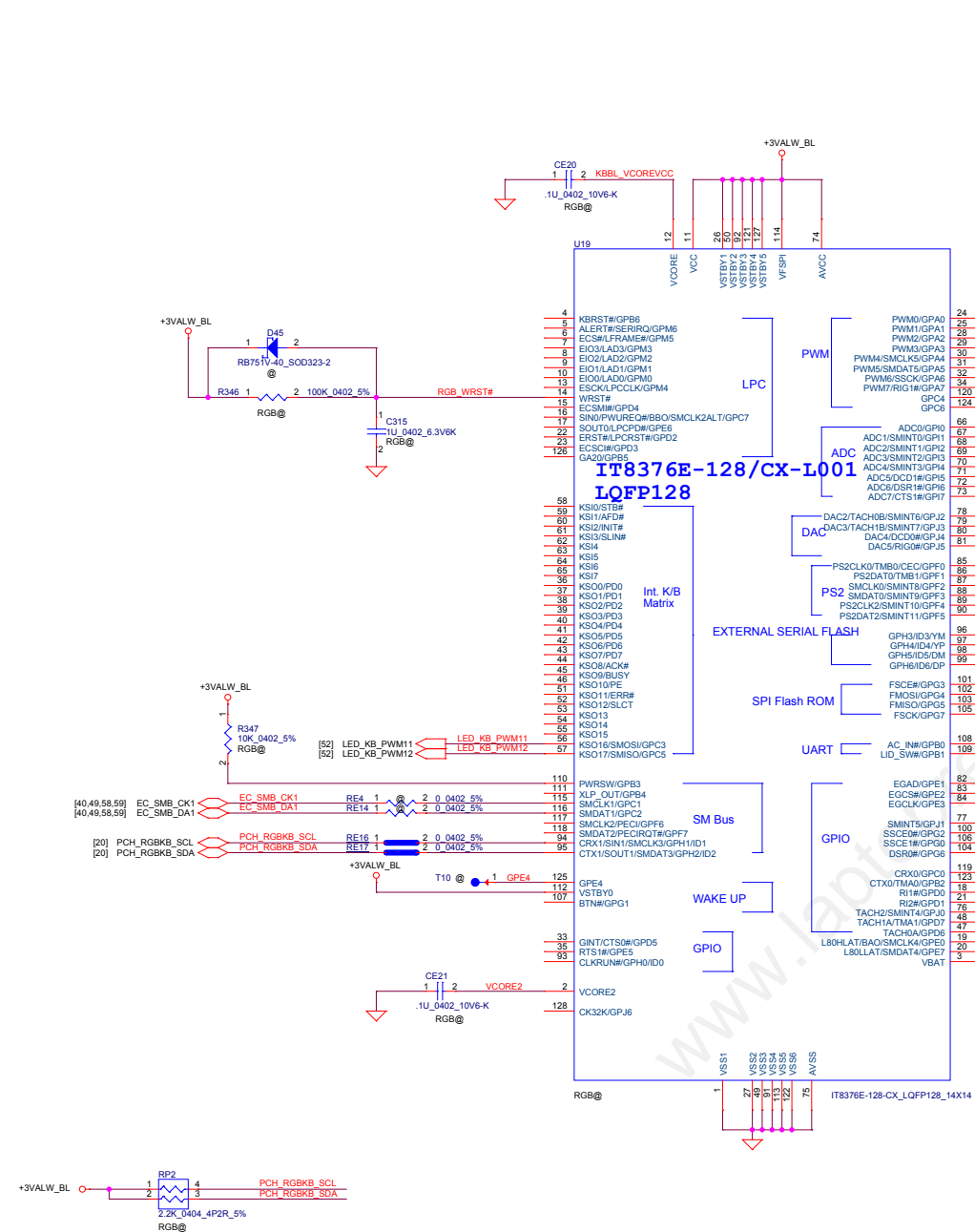
| Mode | Min | Max | Frequency (kHz) | FS |
|------|-----|------|-----------------|----|
| Low | 300 | 432 | 44.1 | 48 |
| | 375 | 500 | 44.1 | 48 |
| High | 450 | 630 | 44.1 | 48 |
| | 750 | 1050 | 44.1 | 48 |



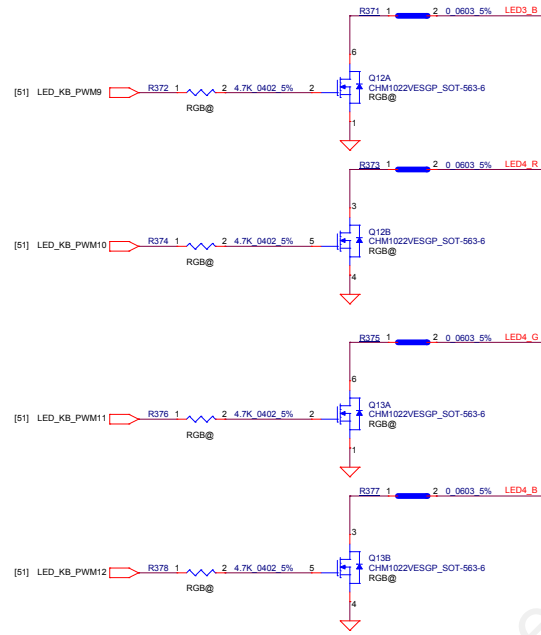
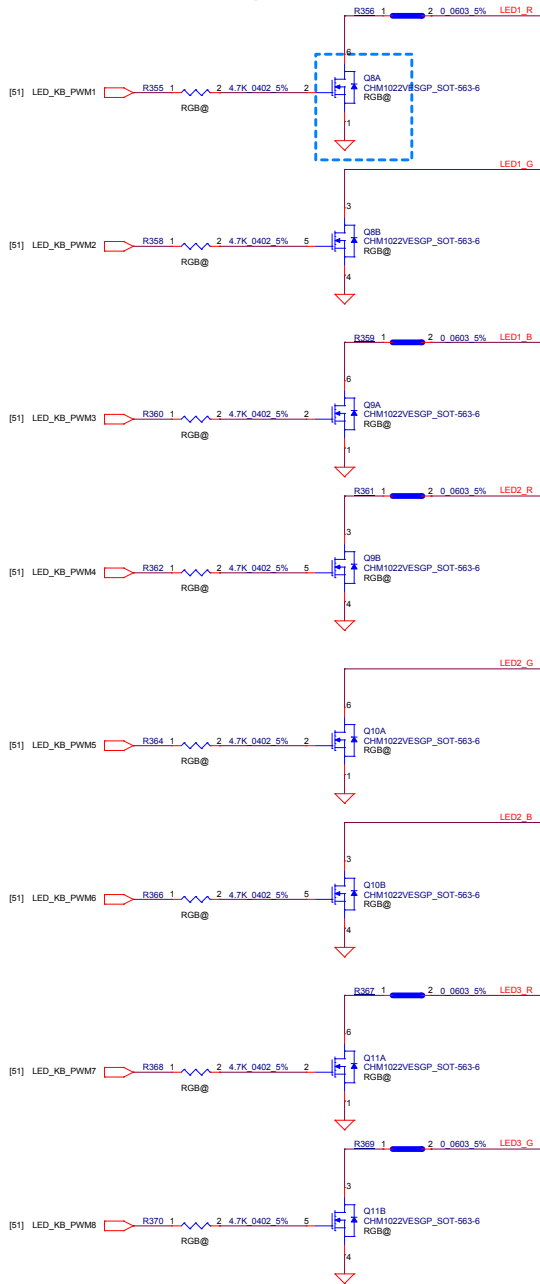


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|---|------------------------------|-----------------|---|
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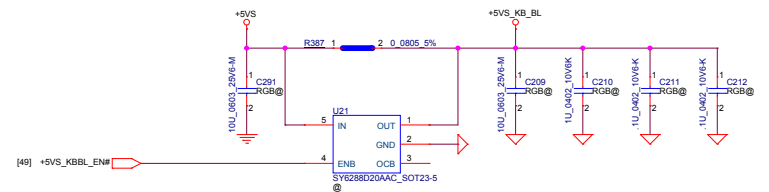
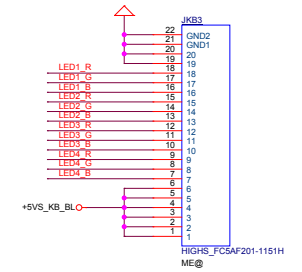




need reload symbol for SB000018E00
-Harry 10/20



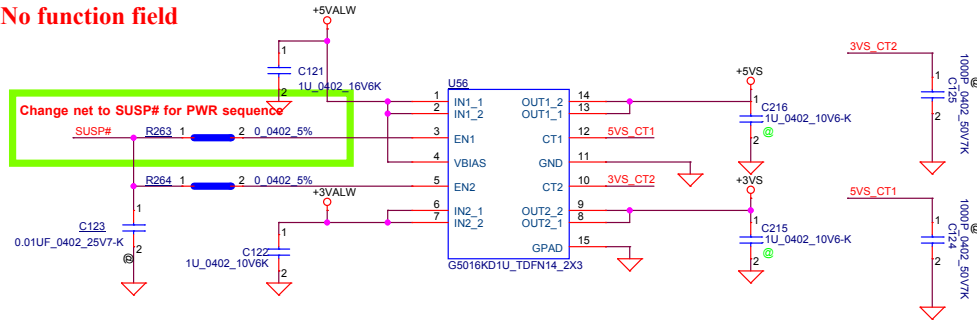
RGB KB BL CONN.



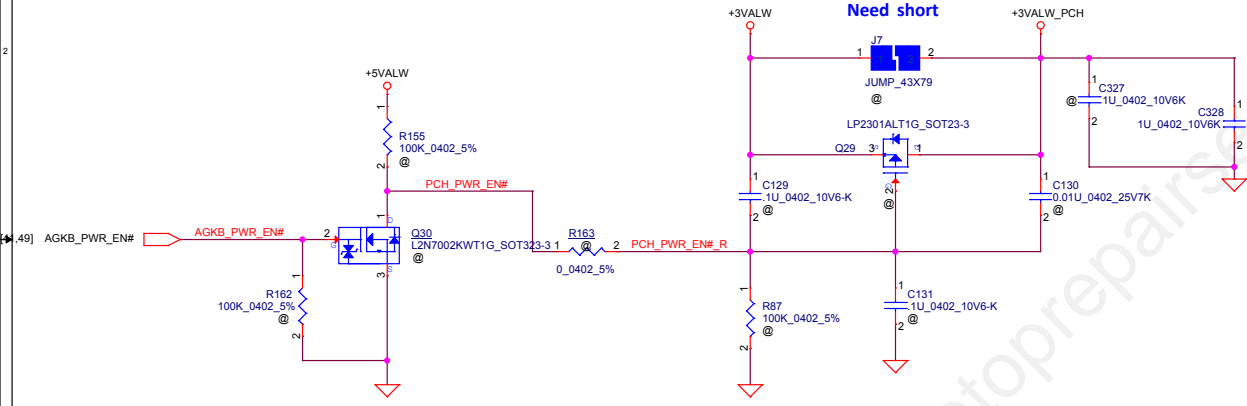
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| Issued Date | 2015/02/26 | Deciphered Date | 2016/06/13 |
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| Sheet | Document Number | Rev | 1.0 |
| 42 | DY510/DY511 N17E-G1 | | |
| Date: | Monday, December 18, 2016 | Sheet | 62 of 76 |

+5VALW to +5VS

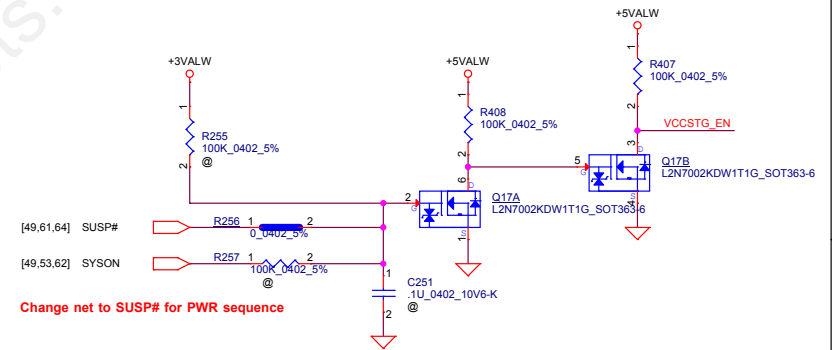
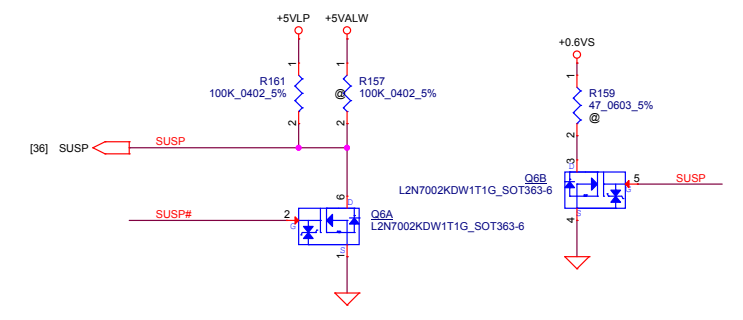
No function field



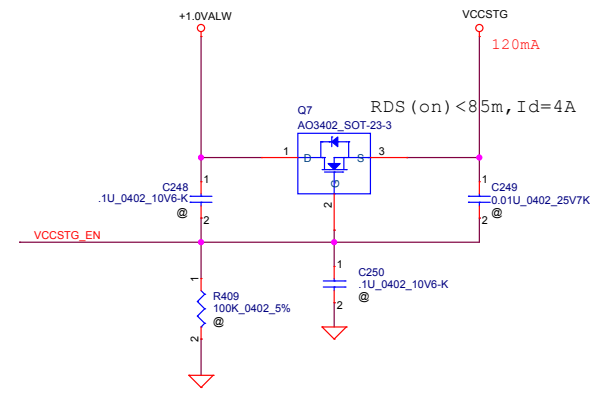
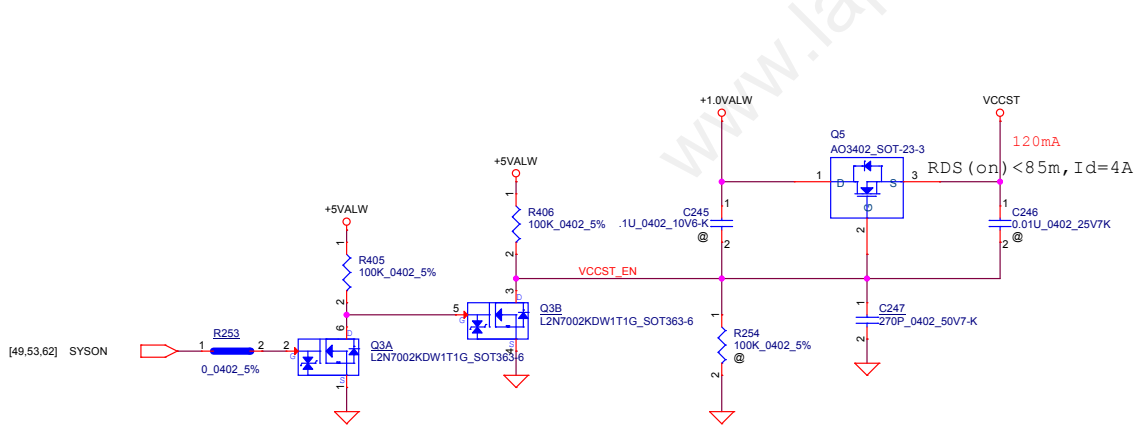
LP2301ALT1G
 $R_{ds}=110\text{m}\Omega$
 $V_{GS}=4.5V, I_D=2.8A$
 $V_{GS(th)}=1V_{Max}$



Need short



Change net to SUSP# for PWR sequence




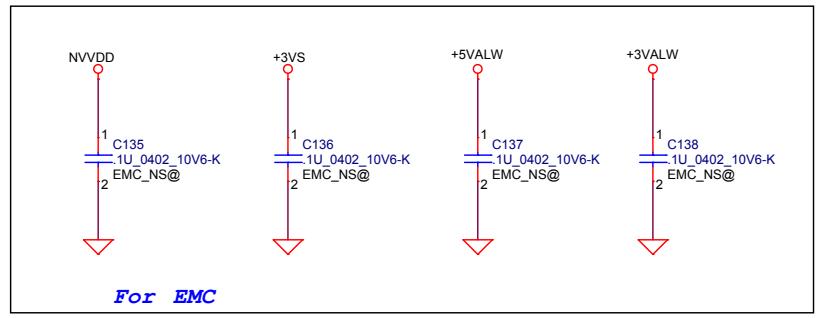
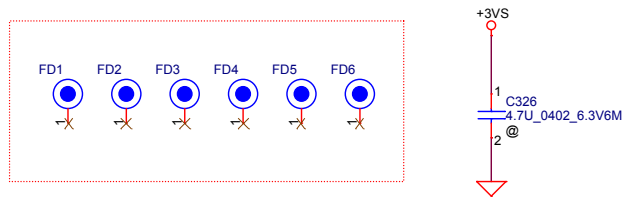
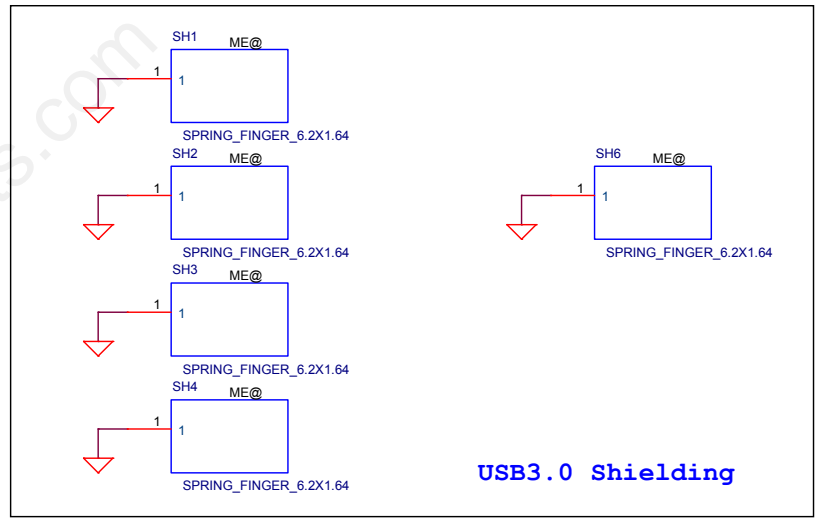
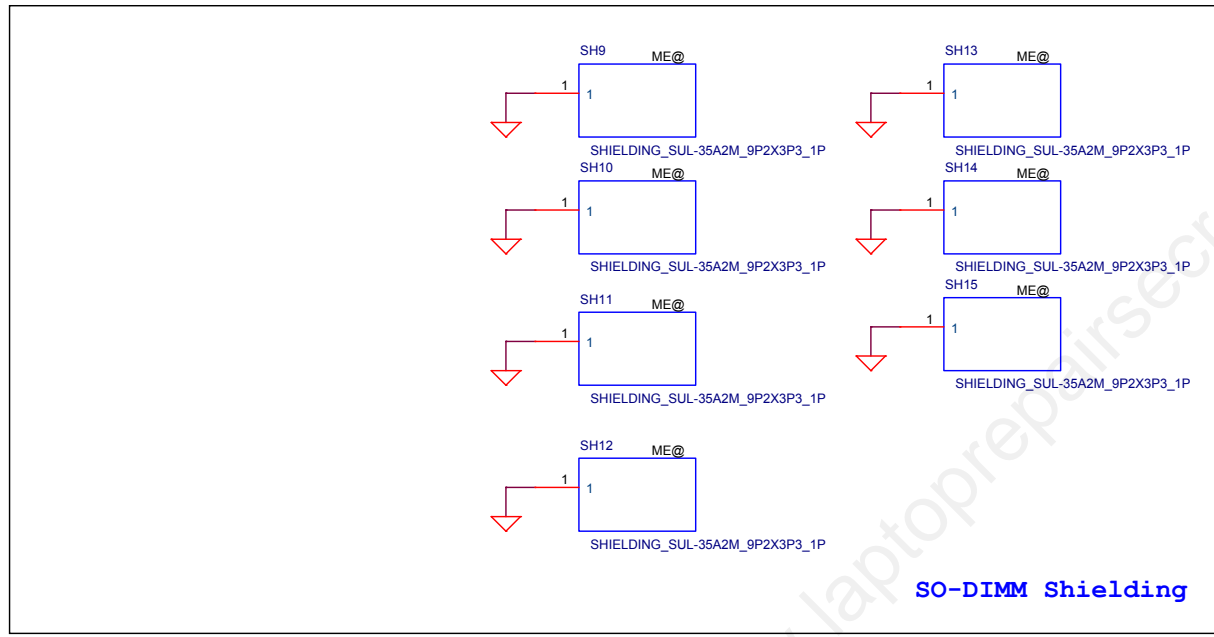
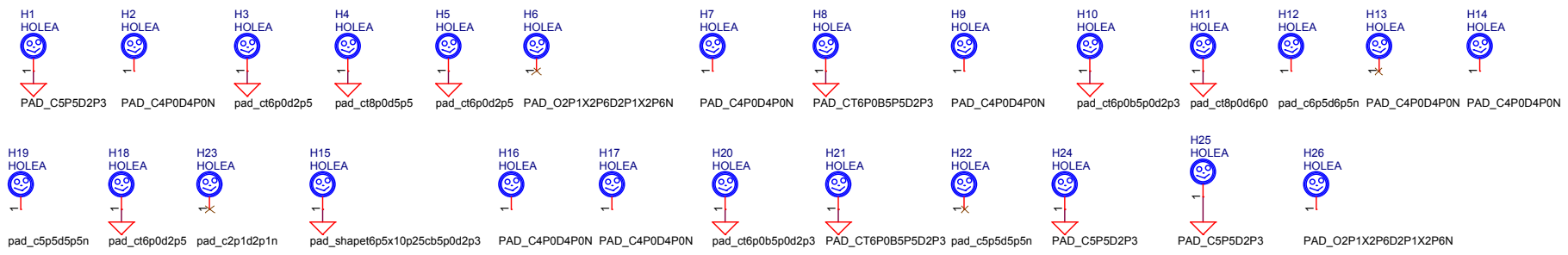
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|--|------------------------------|-----------------|
| Security Classification | LC Future Center Secret Data | |
| Issued Date | 2015/02/26 | Deciphered Date |
| | | 2016/06/13 |
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| | | |
|--------|---------------------------|----------------|
| Title | DC V TO VS INTERFACE | |
| Size | Document Number | Rev |
| Custom | DY510/DY511 N17E-G1 | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet 53 of 75 |



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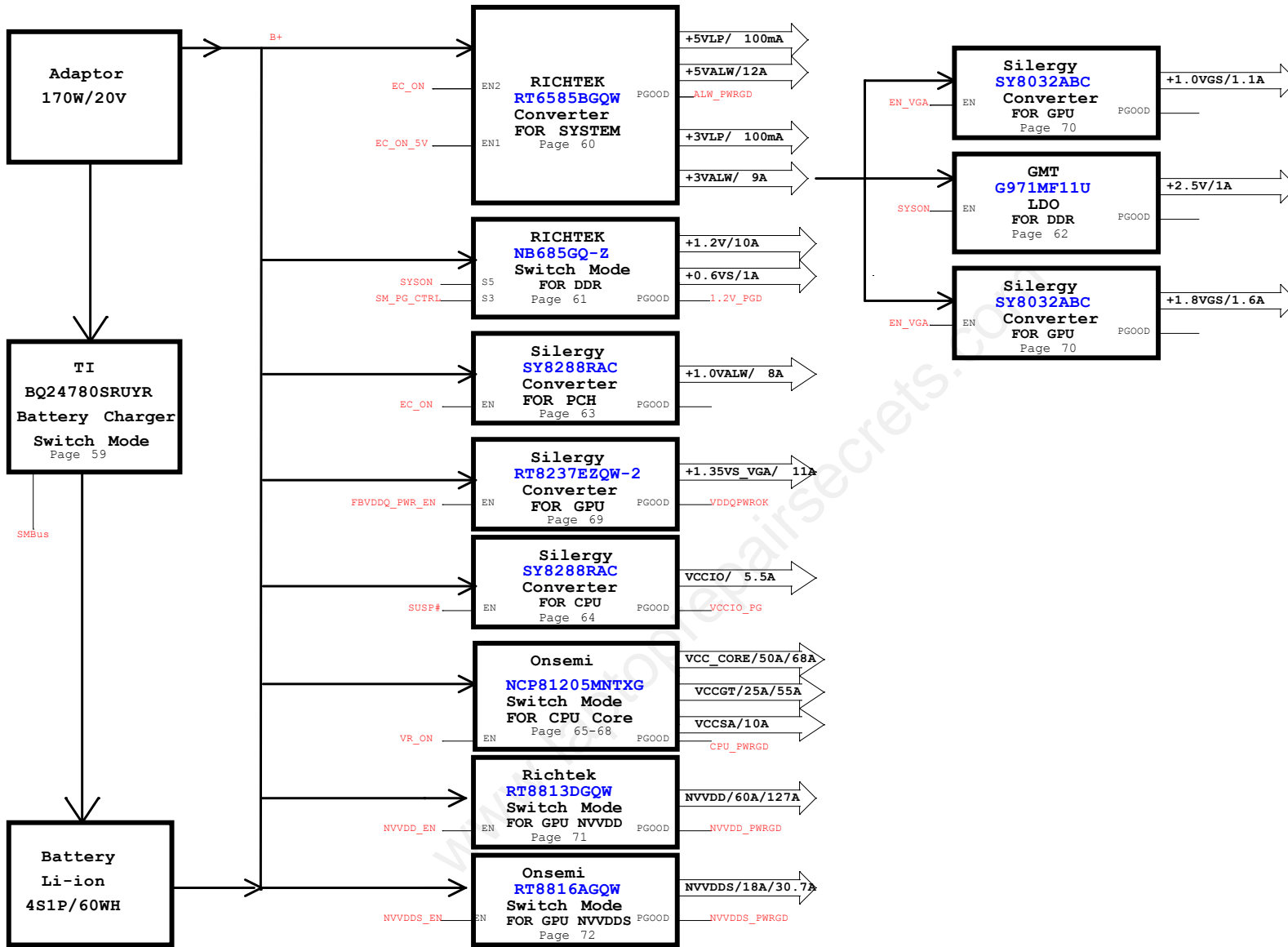
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| Security Classification | LC Future Center Secret Data | | | Title |  | | |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/02/26 | Virtual symbol | | | |
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| | | | | | Date: | Monday, December 18, 2016 | Sheet 54 of 75 |




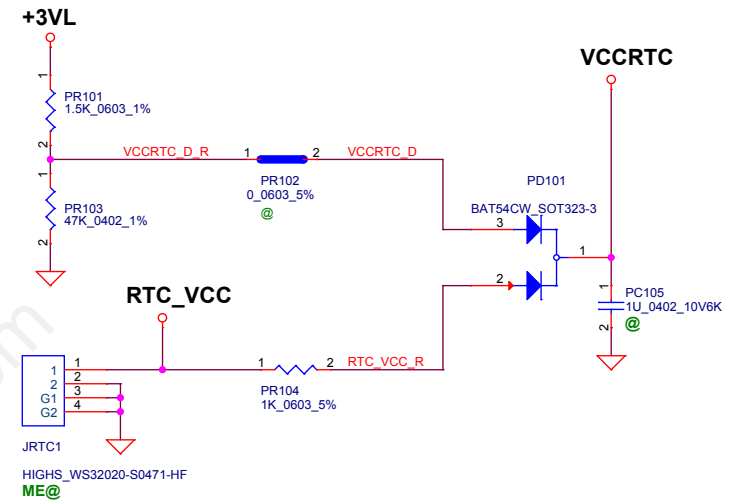
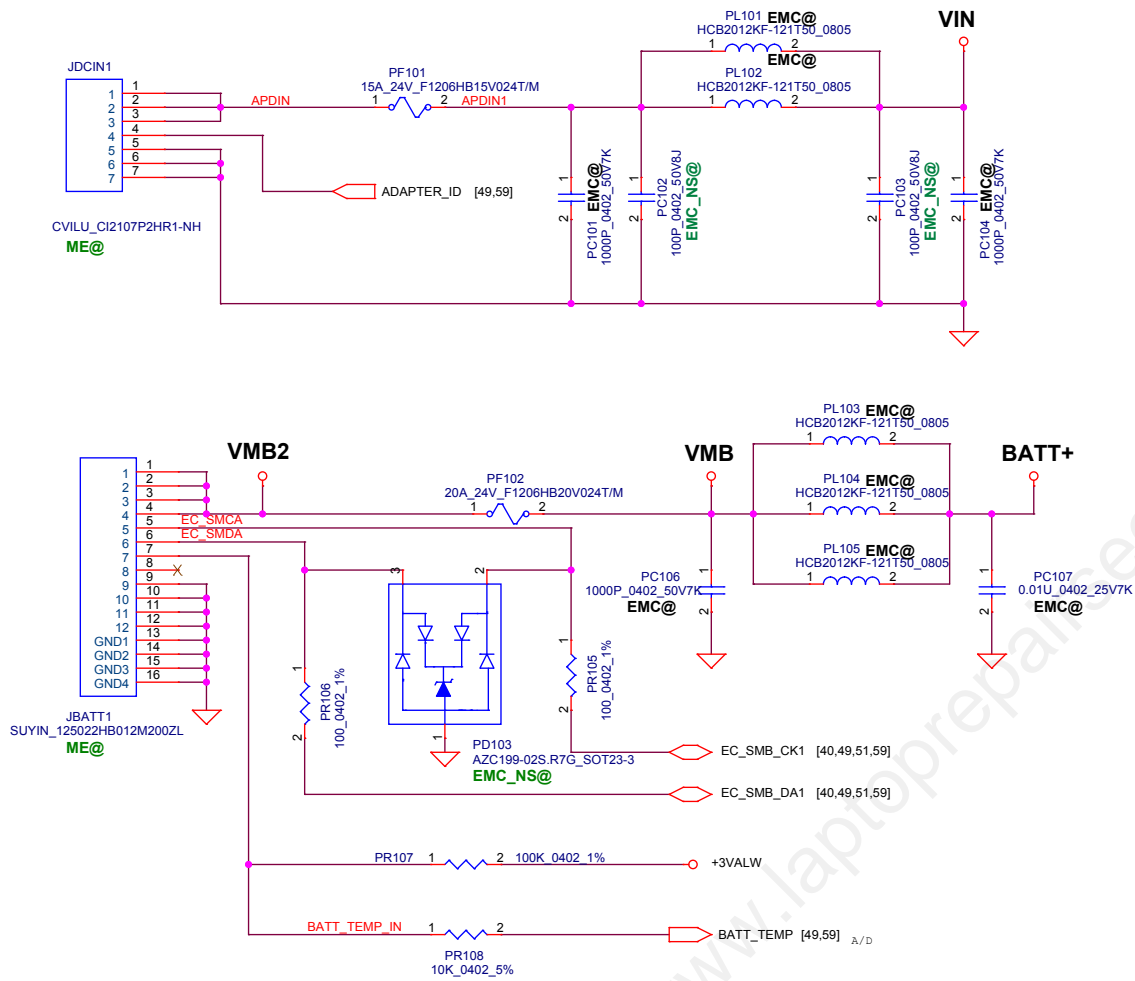
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| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2015/02/26 | Deciphered Date | 2016/02/26 | Hole | |
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| | | | | DY510/DY511 | |
| | | | | Date: | Monday, December 19, 2016 |
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| Issued Date | 2016/02/26 | Displacement Date | 2016/02/26 |
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| | | | <small>Rev</small> 1/1 |
| | | | <small>Date</small> Monday, December 15, 2015 <small>Sheet</small> 01 of 01 |

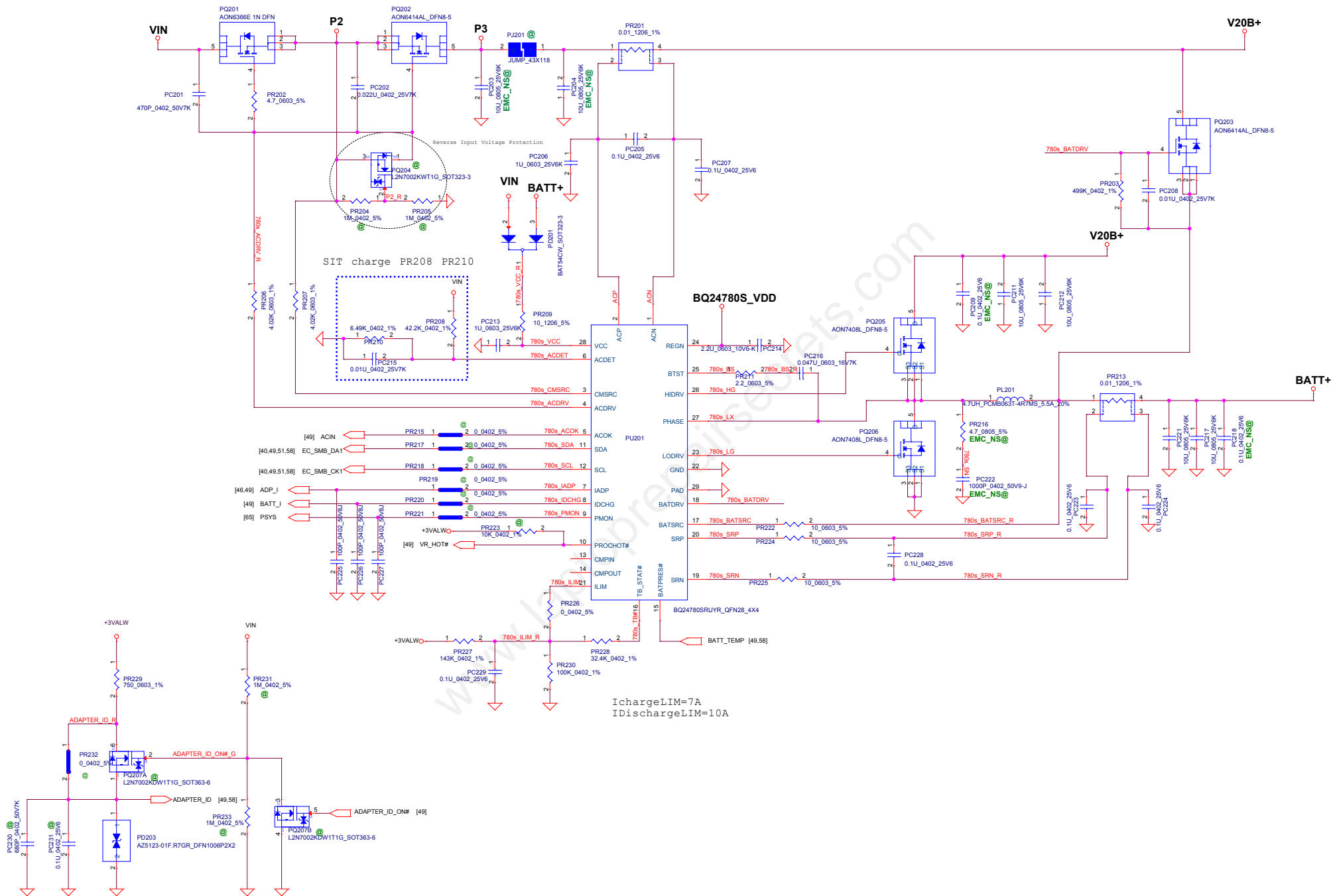


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| Issued Date | 2015/02/26 | Deciphered Date | 2016/02/26 | |
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| | | | | Rev 1.0 |

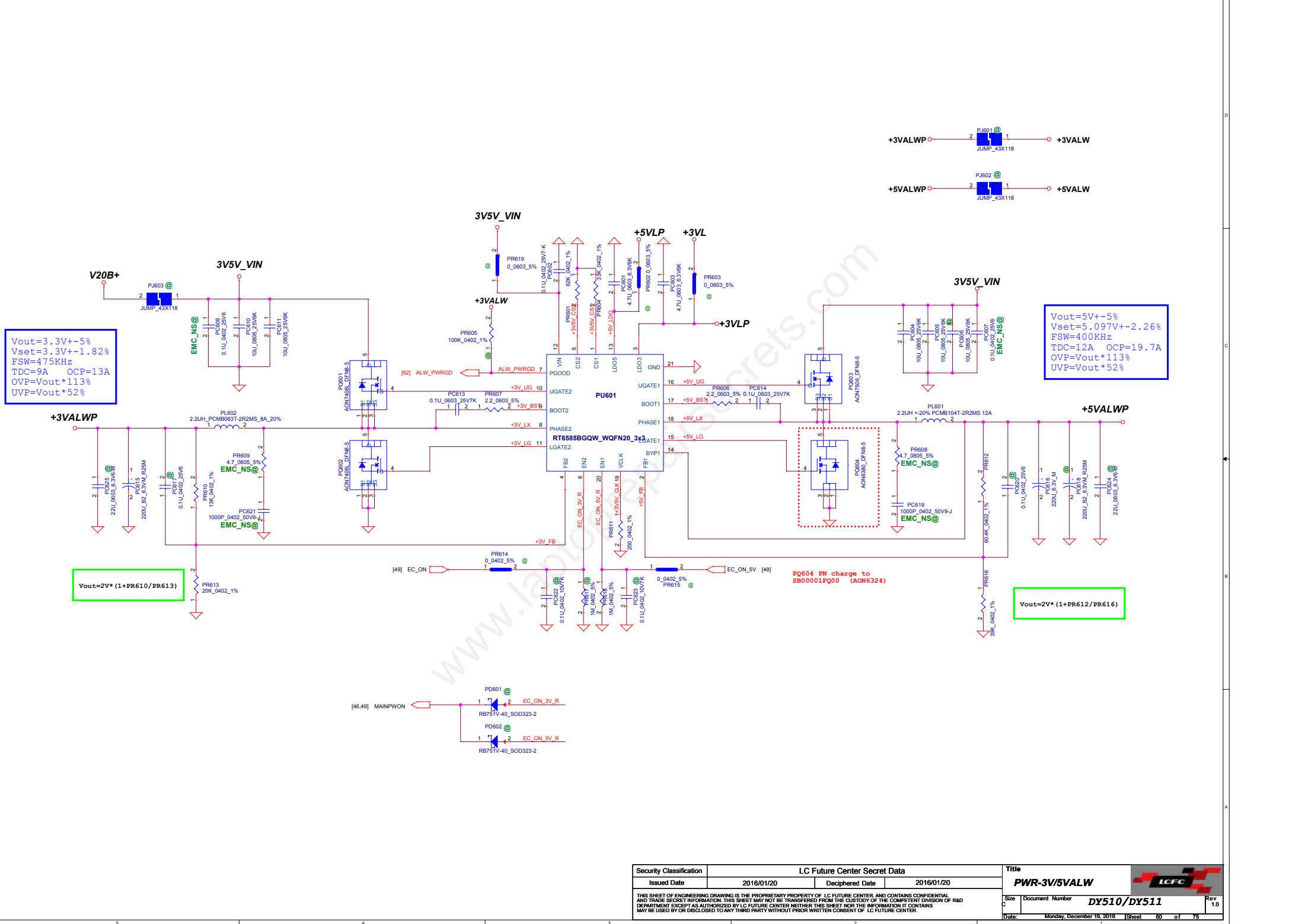


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|---|---------------------------|------------|--|------------------------------|----|------------|----|--------------------------|----|---------|
| Issued Date | | 2016/01/20 | | Deciphered Date | | 2016/01/20 | | PWR-DCIN /BATT/ RTC CONN | | |
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| Date: | Monday, December 19, 2016 | | | Sheet | 58 | | of | | 75 | |





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| Issued Date | 2016/01/20 | Deciphered Date | 2016/01/20 | |
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$V_{out} = 3.3V \pm 5\%$
 $V_{set} = 3.3V \pm 1.82\%$
 $FSW = 475KHz$
 $TDC = 9A$ $OCp = 13A$
 $OVP = V_{out} * 113\%$
 $UVP = V_{out} * 52\%$

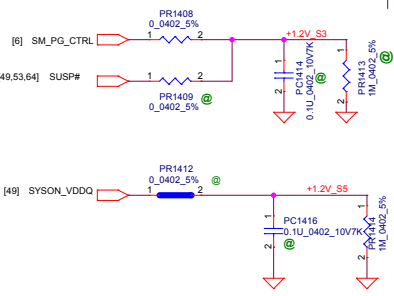
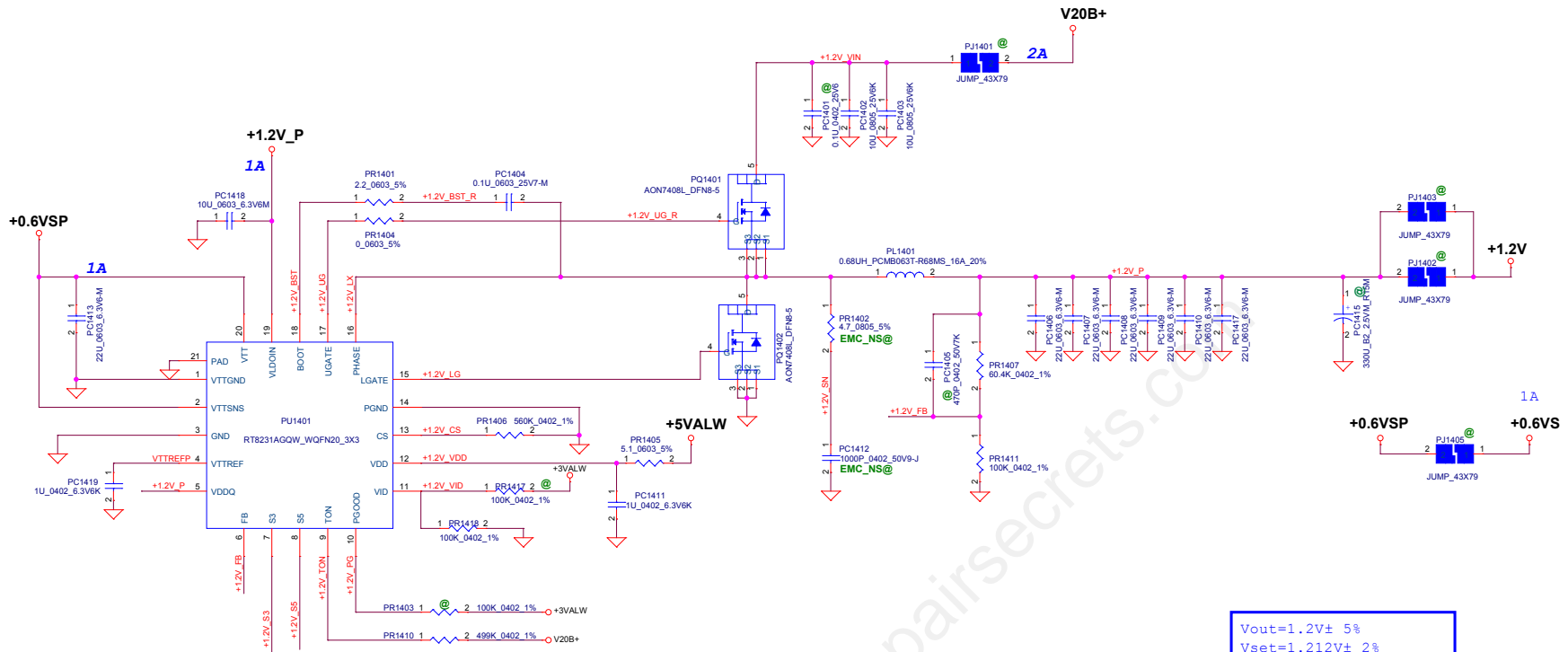
$V_{out} = 5V \pm 5\%$
 $V_{set} = 5.097V \pm 2.26\%$
 $FSW = 400KHz$
 $TDC = 12A$ $OCp = 19.7A$
 $OVP = V_{out} * 113\%$
 $UVP = V_{out} * 52\%$

$V_{out} = 2V * (1 + PR610 / PR613)$

$V_{out} = 2V * (1 + PR612 / PR616)$

PQ604 FN charge to SB00001FQ00 (AON6324)

| | | | | |
|---|------------------------------|-----------------|------------|--|
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| Issued Date | 2016/01/20 | Deciphered Date | 2016/01/20 | |
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| Date: Monday, December 19, 2016 | | | | Sheet 60 of 75 |

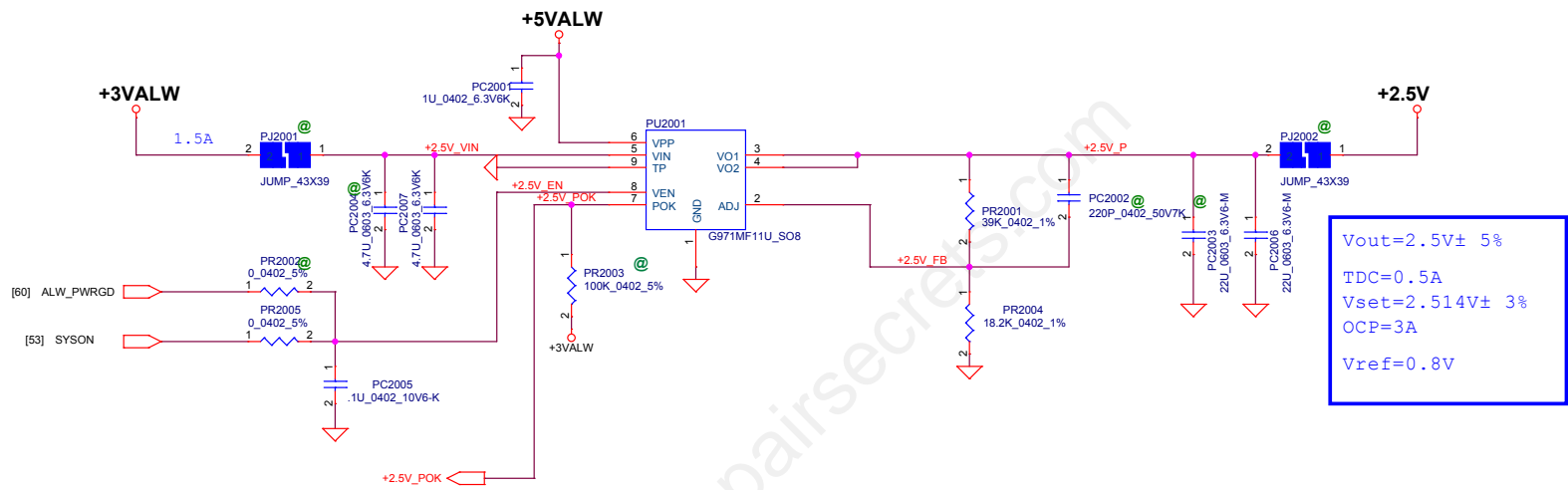


$V_{out}=1.2V \pm 5\%$
 $V_{set}=1.212V \pm 2\%$
 $OCP=11.6A$
 $V_{ref}=0.6V$
 $OVP=(1.25 \sim 1.35) * V_{ref}$
 $UVP=(0.7 \sim 0.8) * V_{ref}$
 $F_{sw}=508KHZ$

$V_{out}=0.6V \pm 5\%$
 $OCP=1.5A$
 $VTT=1/2VDDQ$


| STATE | EN1 | EN2 | VDDQ | VTT_REFP | VTT |
|-------|-----|-----|------|----------|------------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |

Note: S3 - sleep ; S5 - power off

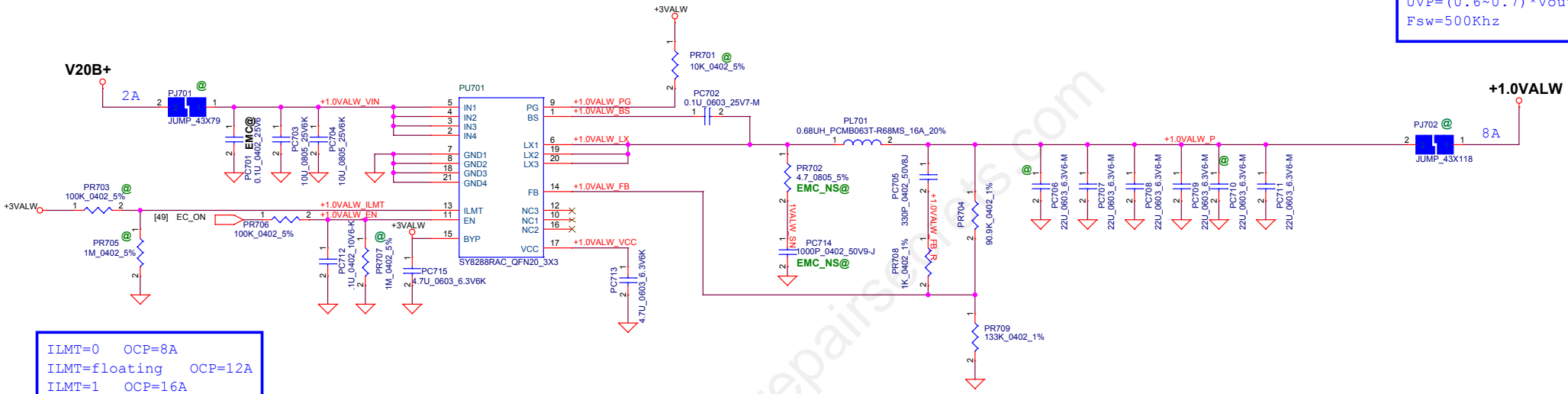


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| | | |
|----------|---------------------------|---|
| Title | |  |
| PWR-2.5V | | |
| Size | Document Number | Rev |
| Custom | DY510/DY511 | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet 62 of 75 |

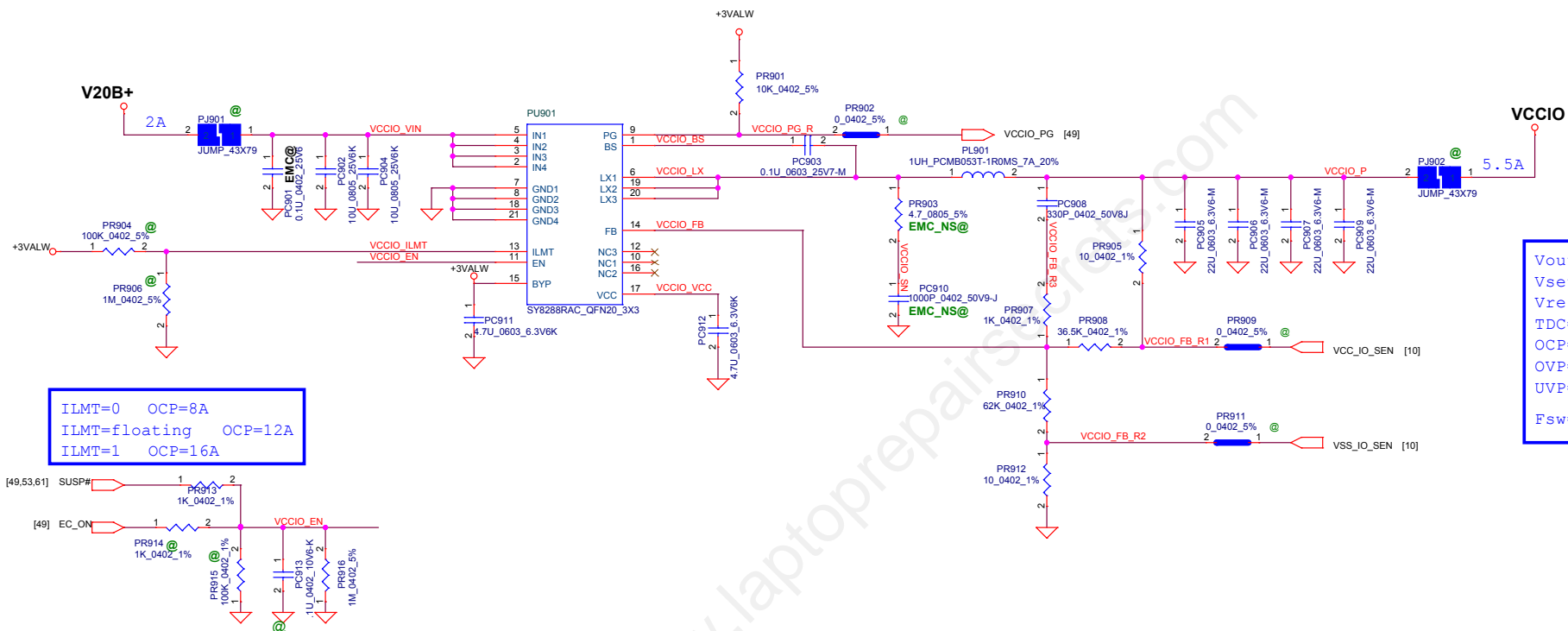
Vout=1.00V± 3%
 Vset=1.01V± 1.88%
 Vref=0.6V
 TDC=8A
 OCP=12A
 OVP=(1.15~1.25) *Vout
 UVP=(0.6~0.7) *Vout
 Fsw=500Khz



ILMT=0 OCP=8A
 ILMT=floating OCP=12A
 ILMT=1 OCP=16A

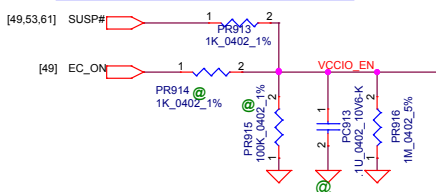
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|--|---------------------------|------------------------------|------------|-------------|-----|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2016/01/20 | Deciphered Date | 2016/01/20 | PWR-1.0VALW | |
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| Size | Document Number | DY510/DY511 | | Rev | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet | 63 of 75 | | |



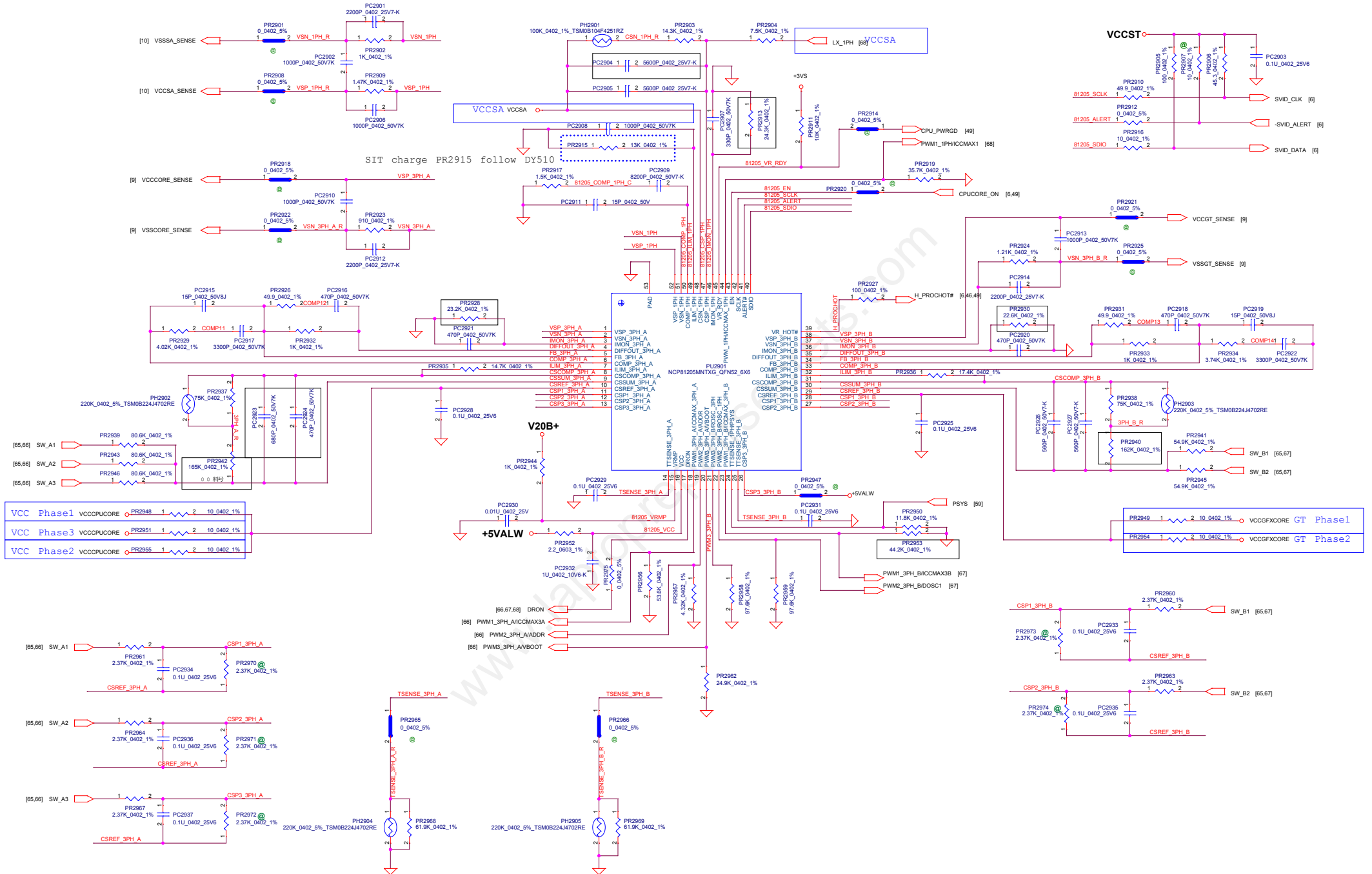


ILMT=0 OCP=8A
 ILMT=floating OCP=12A
 ILMT=1 OCP=16A

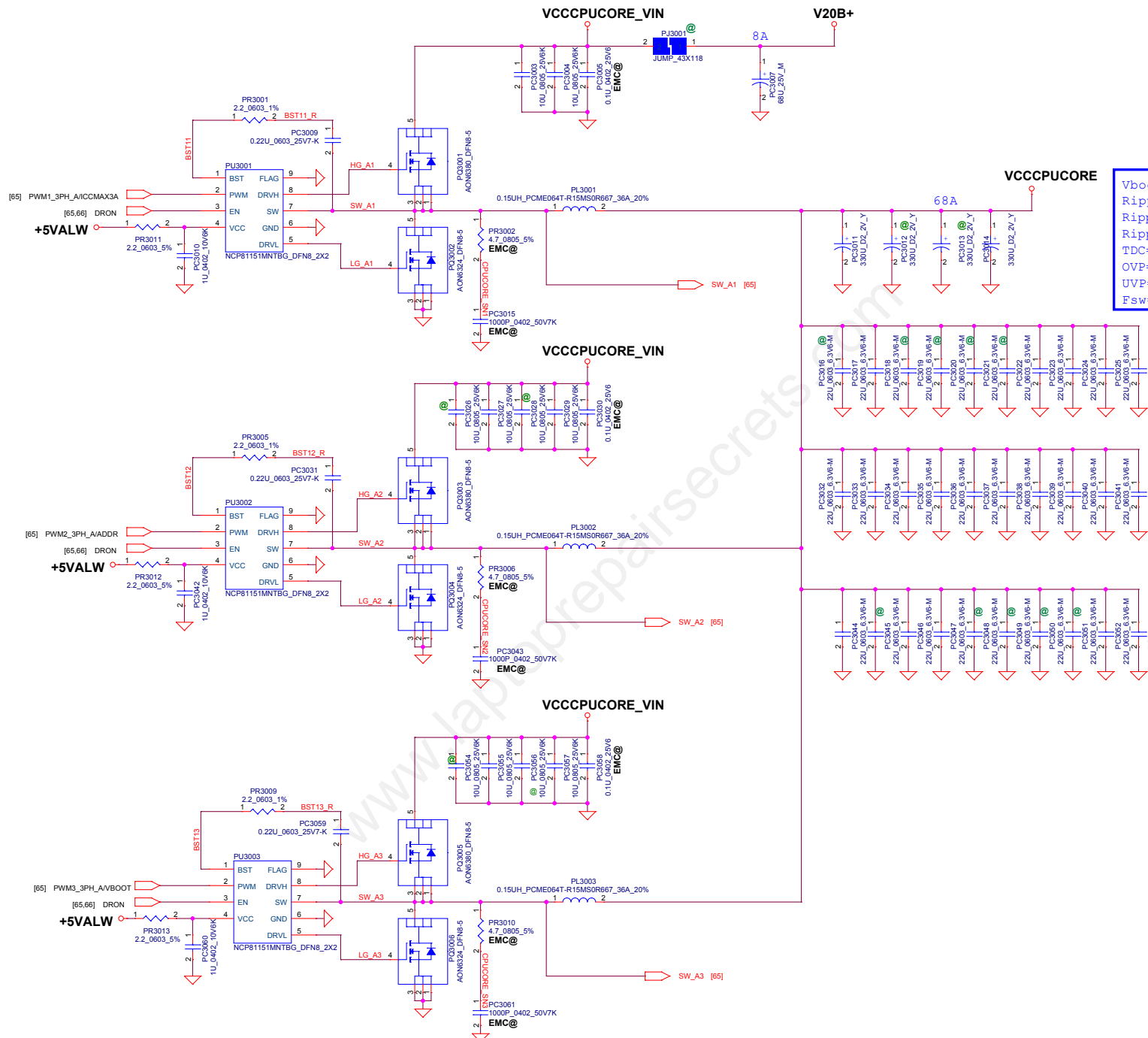
Vout=0.95V± 50mV
 Vset=0.953V± 1.78%
 Vref=0.6V
 TDC=5.5A
 OCP=12A
 OVP=(1.15~1.25)*Vout
 UVP=(0.6~0.7)*Vout
 Fsw=500Khz



| | | | | | |
|--|---------------------------|------------------------------|------------|-----------|-----|
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| Issued Date | 2016/01/20 | Deciphered Date | 2016/01/20 | PWR-VCCIO | |
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| Size | Document Number | DY510/DY511 | | Rev | 1.0 |
| Date: | Monday, December 19, 2016 | Sheet | 64 | of | 75 |

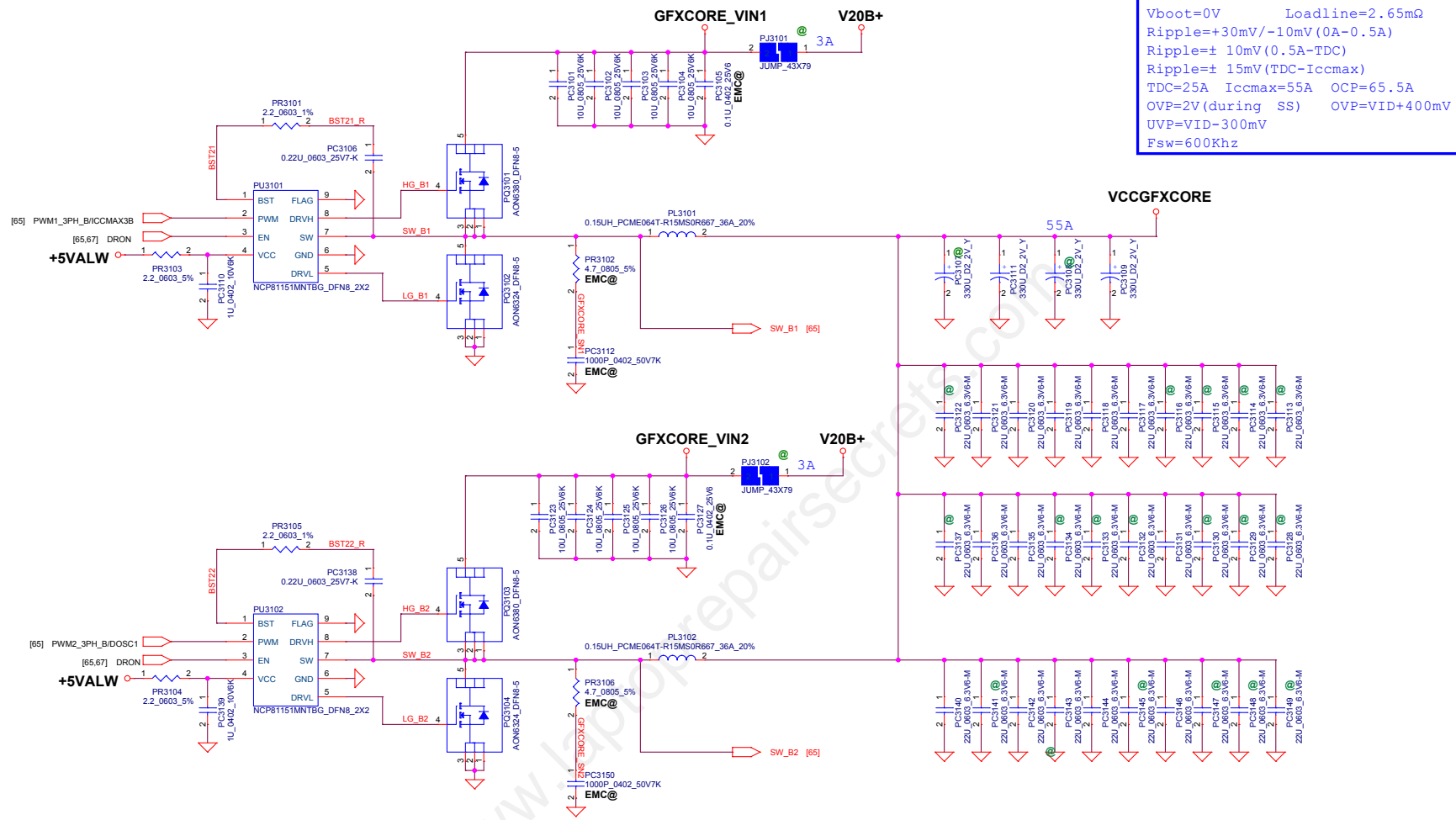


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|---|-----------------|---------------------------|------------|------------------------------|-------|-------|--|
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| Size | Document Number | DY510/DY511 | | Rev | 1.0 | | |
| Custom | Date | Monday, December 18, 2016 | Sheet | 65 | of 75 | | |




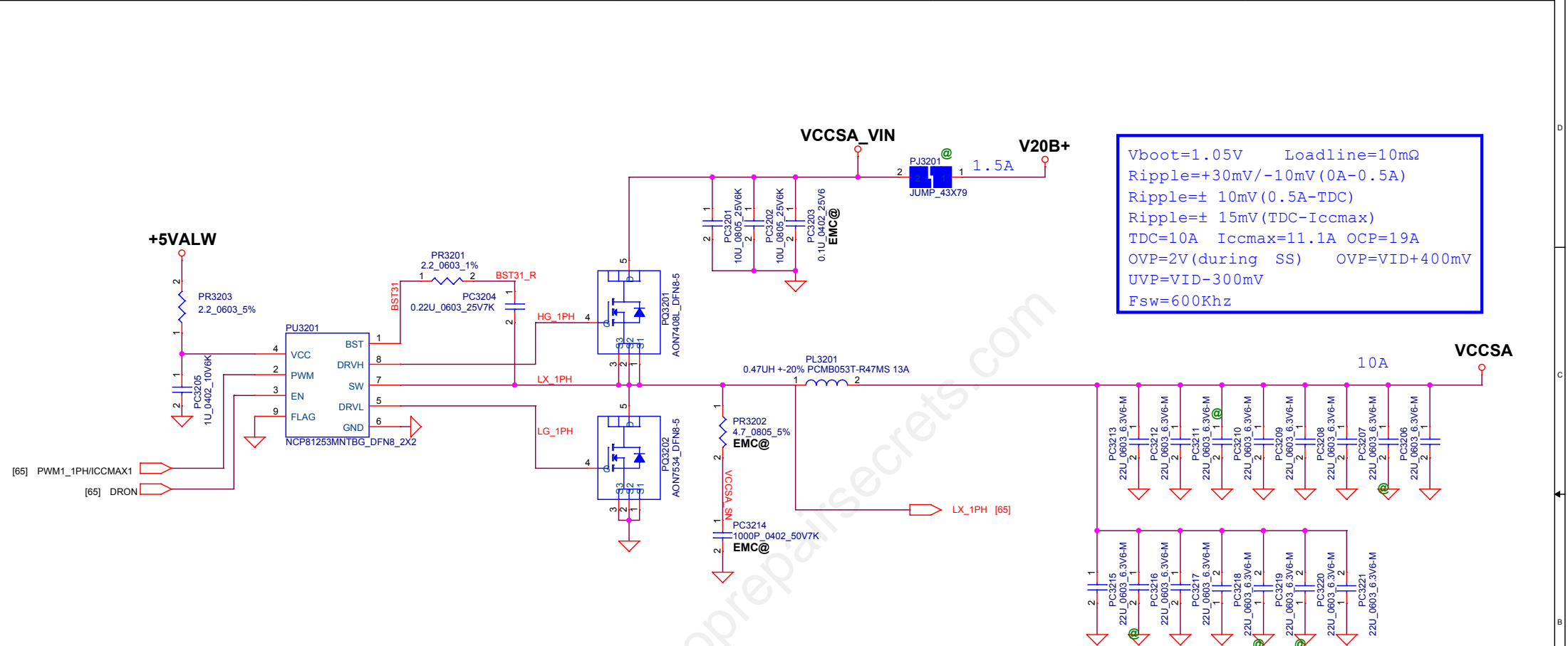
Vboot=0V Loadline=1.8mΩ
 Ripple=+30mV/-10mV (0A-0.5A)
 Ripple=± 10mV (0.5A-TDC)
 Ripple=± 15mV (TDC-Iccmax)
 TDC=50A Iccmax=68A OCP=81.5A
 OVP=2V (during SS) OVP=VID+400mV
 UVP=VID-300mV
 Fsw=600Khz

| | | | | |
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| Issued Date | 2016/01/20 | Deciphered Date | 2016/01/20 | |
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Vboot=0V Loadline=2.65mΩ
 Ripple=+30mV/-10mV (0A-0.5A)
 Ripple=± 10mV (0.5A-TDC)
 Ripple=± 15mV (TDC-Iccmax)
 TDC=25A Iccmax=55A OCP=65.5A
 OVP=2V (during SS) OVP=VID+400mV
 UVP=VID-300mV
 Fsw=600Khz

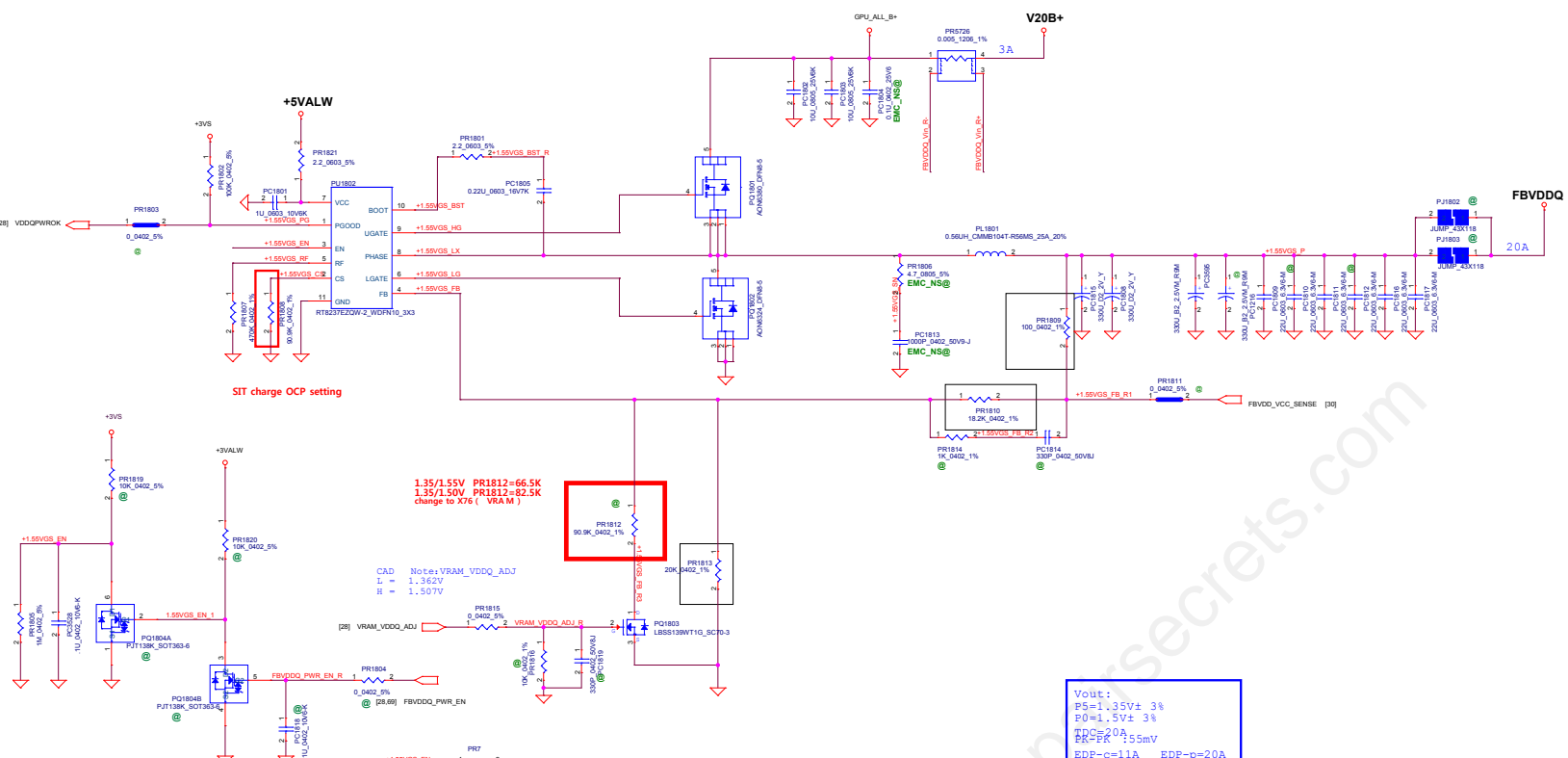
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Vboot=1.05V Loadline=10mΩ
 Ripple=+30mV/-10mV(0A-0.5A)
 Ripple=± 10mV(0.5A-TDC)
 Ripple=± 15mV(TDC-Iccmax)
 TDC=10A Iccmax=11.1A OCP=19A
 OVP=2V(during SS) OVP=VID+400mV
 UVP=VID-300mV
 Fsw=600Khz

22u-0603 Power 12PCS, 2PCS change to CC140 CC138

| | | | | | |
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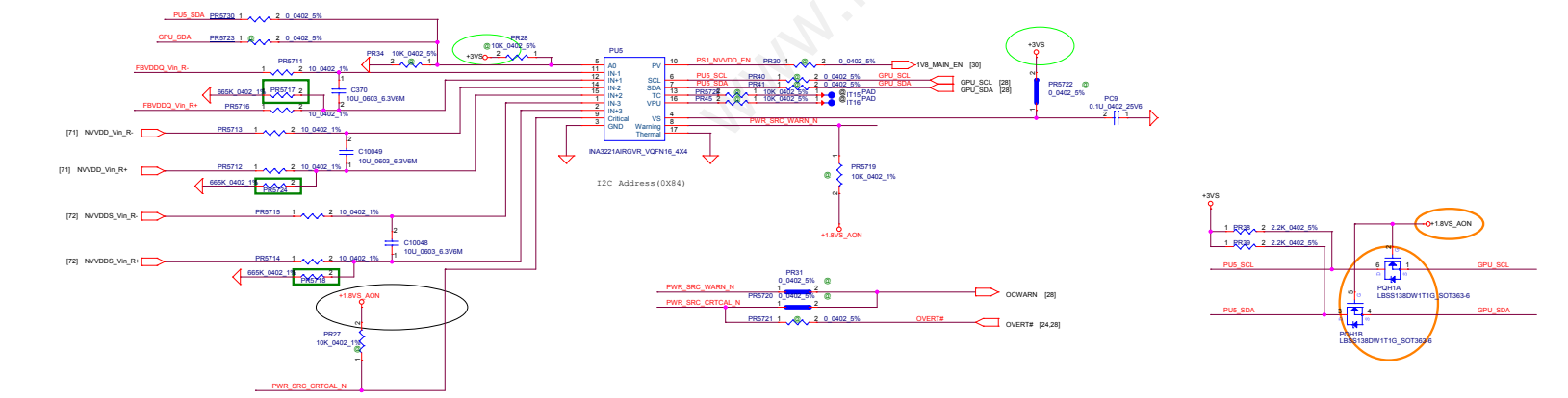


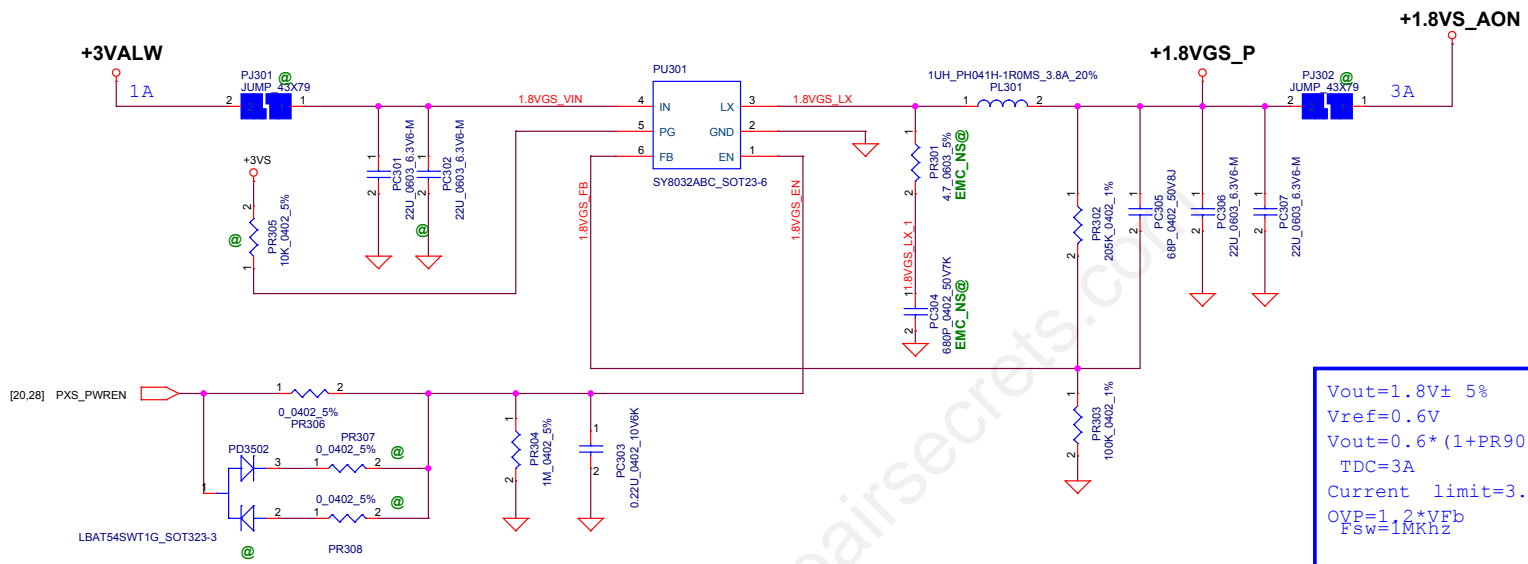
| RRF | Fsw (kHz) |
|-----|-----------|
| 39 | 290 |
| 100 | 340 |
| 200 | 380 |
| 400 | 430 |

Note: TRM RRF to GND
CCK RRF to PG00D

Table 7. INA3221 Address Pins and Slave Addresses

| Bit | SLAVE ADDRESS |
|------|----------------------|
| ADR0 | 10000000 |
| ADR1 | 10000001 |
| ADR2 | 10000001 |
| ADR3 | 10000010 0X04 |
| ADR4 | 10000011 |





$V_{out} = 1.8V \pm 5\%$
 $V_{ref} = 0.6V$
 $V_{out} = 0.6 * (1 + PR902 / PR906)$
 $TDC = 3A$
 $Current\ limit = 3.5A$
 $OVP = 1.2 * V_{fb}$
 $F_{sw} = 1MKHz$

| | | | |
|-------------------------|------------------------------|-----------------|------------|
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| | | | |
|-------|------------|--|--|
| Title | PWR-1.8VGS | | |
|-------|------------|--|--|

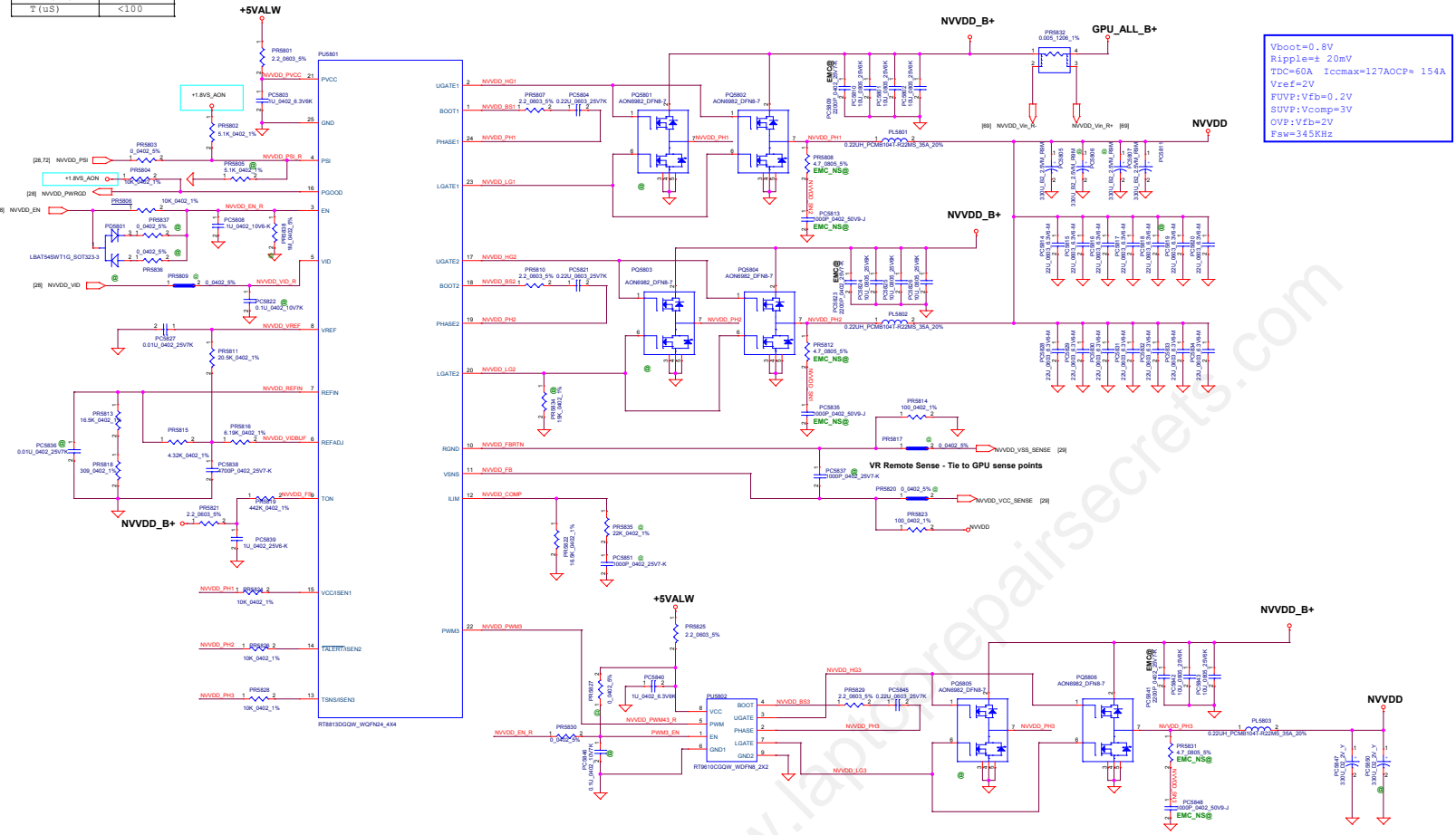


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| PWM-VID Specification | Config | Component Value |
|-----------------------|--------|-------------------------------|
| Vmin (V) | 0.3 | R1 (K Ω) PR5816 6.19 |
| Vmax (V) | 1.3 | R2 (K Ω) PR5811 20.5 |
| Vstep (mV) | 0.8 | R3 (K Ω) PR5815 4.32 |
| N (level) | 160 | R4 (K Ω) PR5813 16.5 |
| Fpwm (KHz) | 675 | R5 (K Ω) PR5818 0.309 |
| Tdmin (ns) | 9.26 | C (nF) PC5838 4.7 |
| T (us) | <100 | |

| PSI Level | Power Mode | Phase Configuration |
|---------------|------------|---------------------|
| PS1<0.4V | PSH | 1Phase DEM |
| 0.8V<PSI<1V | PS0 | 1Phase FCCM |
| 1.4V<PSI<5.5V | PS1 | 3Phase FCCM |



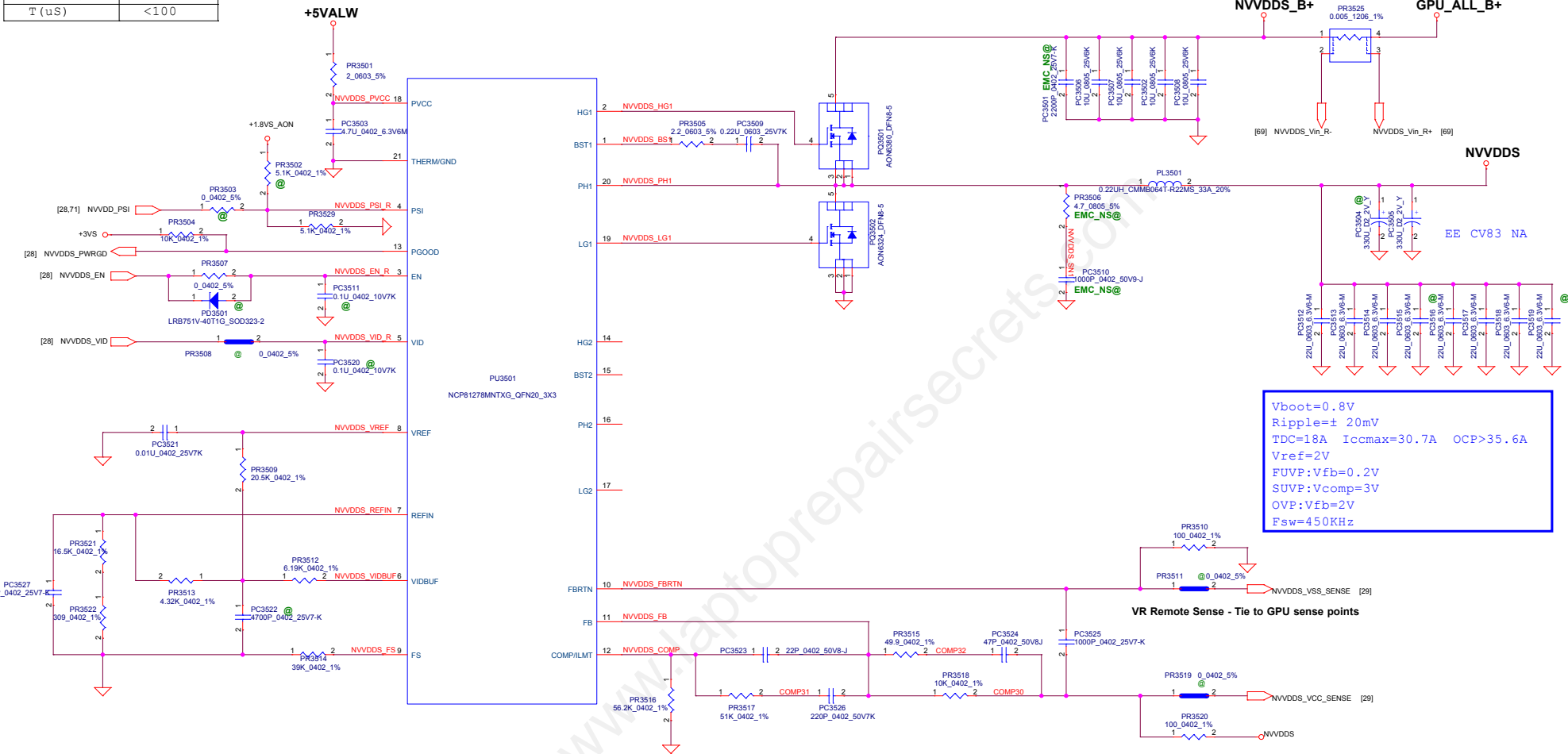
Vboot=0.8V
 Ripple=t 20mV
 TDC=60A Iccmax=127AOCPS= 154A
 Vrfe=2V
 FVFP;Vfb=0.2V
 SUIP;Vcomp=3V
 OVP;Veb=2V
 Fsw=345KHz

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| Doc No | Doc No | Rev |
| Date | Modify/Revise | Page |

| PWM-VID Specification | |
|-----------------------|--------|
| | Config |
| Vmin (V) | 0.3 |
| Vmax (V) | 1.3 |
| Vboot (V) | 0.8 |
| Vstep (mV) | 6.25 |
| N (level) | 160 |
| Fpwm (KHz) | 675 |
| Tdmin (nS) | 9.26 |
| T (uS) | <100 |


| Component Value | | |
|------------------|--------|-------|
| R1 (K Ω) | PR9440 | 6.19 |
| R2 (K Ω) | PR9434 | 20.5 |
| R3 (K Ω) | PR9436 | 4.32 |
| R4 (K Ω) | PR9437 | 16.5 |
| R5 (K Ω) | PR9431 | 0.309 |
| C (nF) | PC1277 | 4.7 |

| PSI Level | Power Mode | Phase Configuration |
|-------------------|------------|---------------------|
| Connected to PVCC | PSH | 2Phase Auto CCM/DCM |
| High | PS0 | 2Phase FCCM |
| Intermediate | PS1 | 2Phase Auto CCM |
| Low | PS2 | 1Phase Auto CCM/DCM |




Vboot=0.8V
 Ripple=±20mV
 TDC=18A Iccmax=30.7A OCP>35.6A
 Vref=2V
 FUVF:Vfb=0.2V
 SUIP:Vcomp=3V
 OVP:Vfb=2V
 Fsw=450KHz

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