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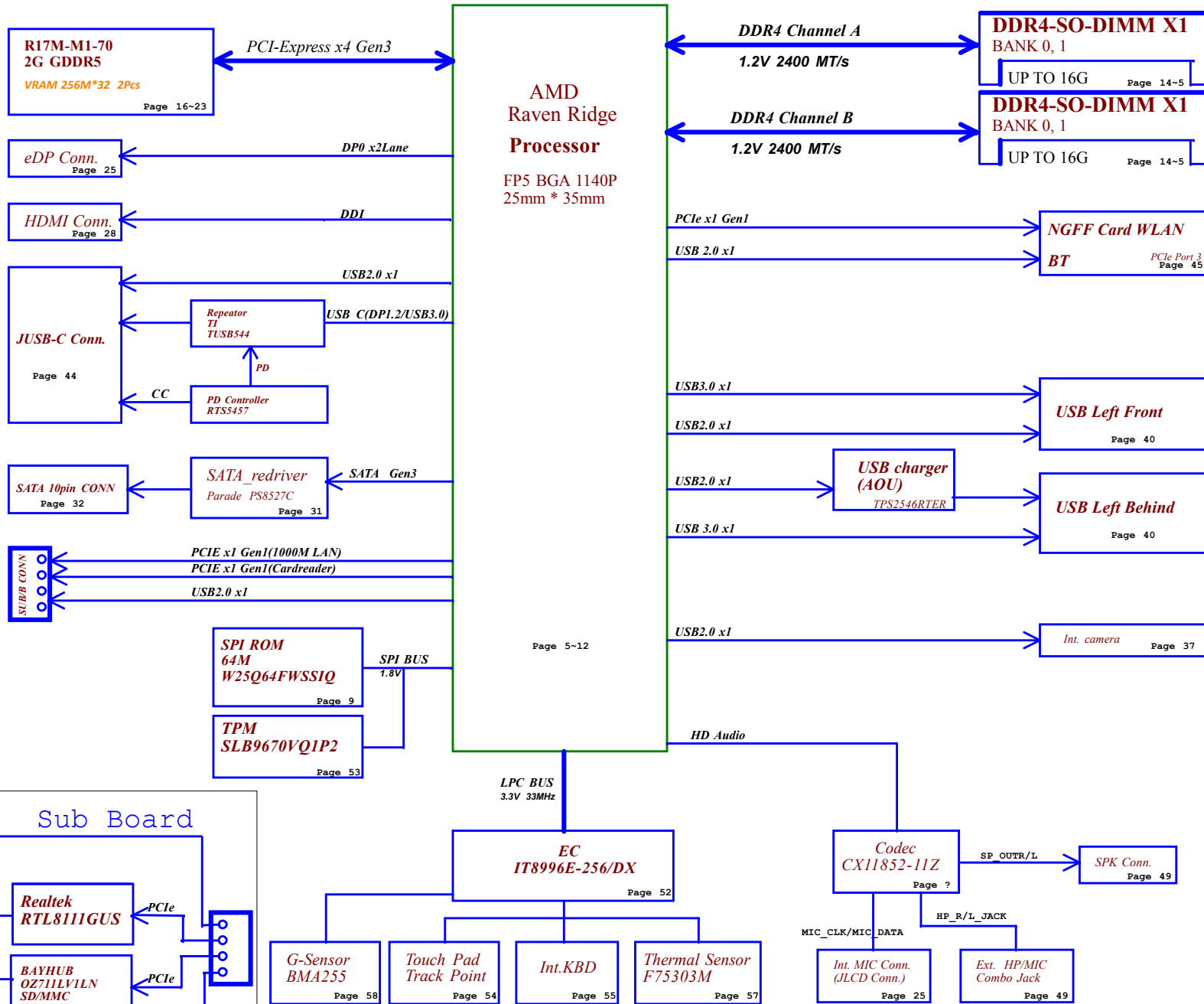
RAVEN EX85 Rev0.1 Schematic

*AMD Raven Ridge FP5 Processor with DDR4
R17M-M1-70 with DDR5 2GB*

2017-3-30 Rev0.1

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AMD Raven Ridge FP5



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	B9+	+3VALW	+1.2V	+5VS +3VS +1.5VS +0.9VS_VDDP +0.6VS +VDDCR_SOC +VDDC_VDD +VGA_CORE +3.3VGS +1.8VGS +1.35VGS +0.95VGS
State		+5VALW	+2.5V	
		+1.8VALW		
		+0.9VALW_VDDP		
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_A#	SLP_S3#	SLP_S5#	EC_ON	SUSP#
S0		HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF

USB2 Port

Port	Device
0	USBC
1	USB3 port1
2	USB3 port2
3	USB2 port1
4	USB (WLAN)
5	Int. Camera

USB3 Port

Port	Device
0	USB Type-C
1	USB3 port1
2	USB3 port2
3	X
4	X

PCIE Port

Port	Device
0	LAN
1	CardReader
2	WLAN
3	X
4	X
5	X
	GFX0 GPU
	GFX1 GPU
	GFX2 GPU
	GFX3 GPU

SATA Port

Port	Device
1	HDD
2	X

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	APU	CP Module	Charge	PD	G-Sensor	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8986F +3VL	X	V +3VL	X	X	X	X	X	V +3VL	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8986F +3VALW	X	X	X	X	X	X	X	X	V +3VALW	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8986F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VS	X	X	X	V +3VS	X
EC_SMB_CK4 EC_SMB_DA4	IT8986F +3VL	X	X	X	X	X	X	X	X	X	X	V

APU I2C

APU Port	Net	Device
I2C2_SCL/SDA	APU_SMB0CLK/SDA	DIMM1/DIMM2
I2C3_SCL/SDA	APU_SMB1_CLK/SDA	TOUCHPAD
SIC/SID	EC_SMB_CK3/DA3	Conn EC
USBC_I2C_SCL/SDA	EC_SMB_CK2/DA2	PD




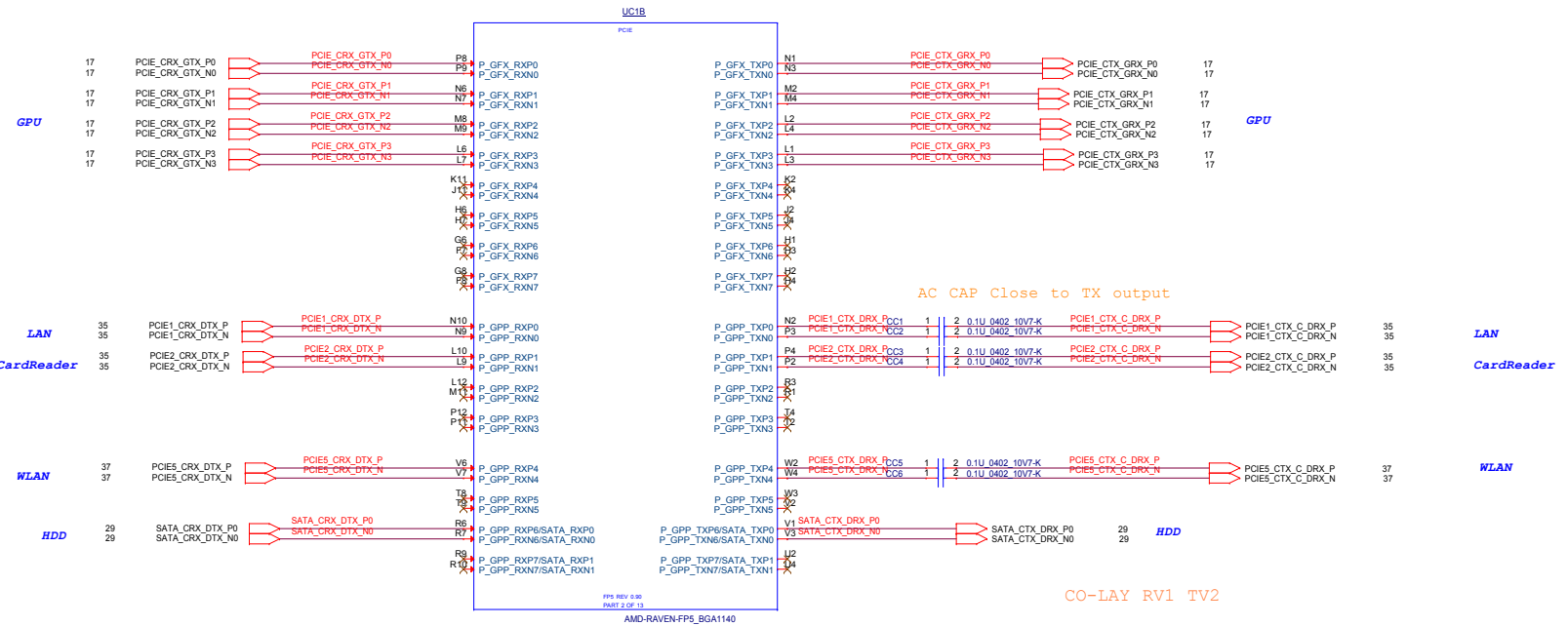
APPLY PCB PN

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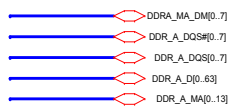
BOM Structure Table

BOM Structure	NOTE
HDT@	For HDT AMD debug port
LPC@	For LPC AMD debug port
PX@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module (TPM)
UMA@	UMA SKU ID
CD@	COST DOWN
EMC_NS@	EMC Reserves
ME@	ME Connector
RF@	For RF function
EMC@	For EMI function
RF_NS@	reserves RF component
RF_PXNS@	VGA reserves RF component
14@	14 inch
15@	15 inch

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UC1A

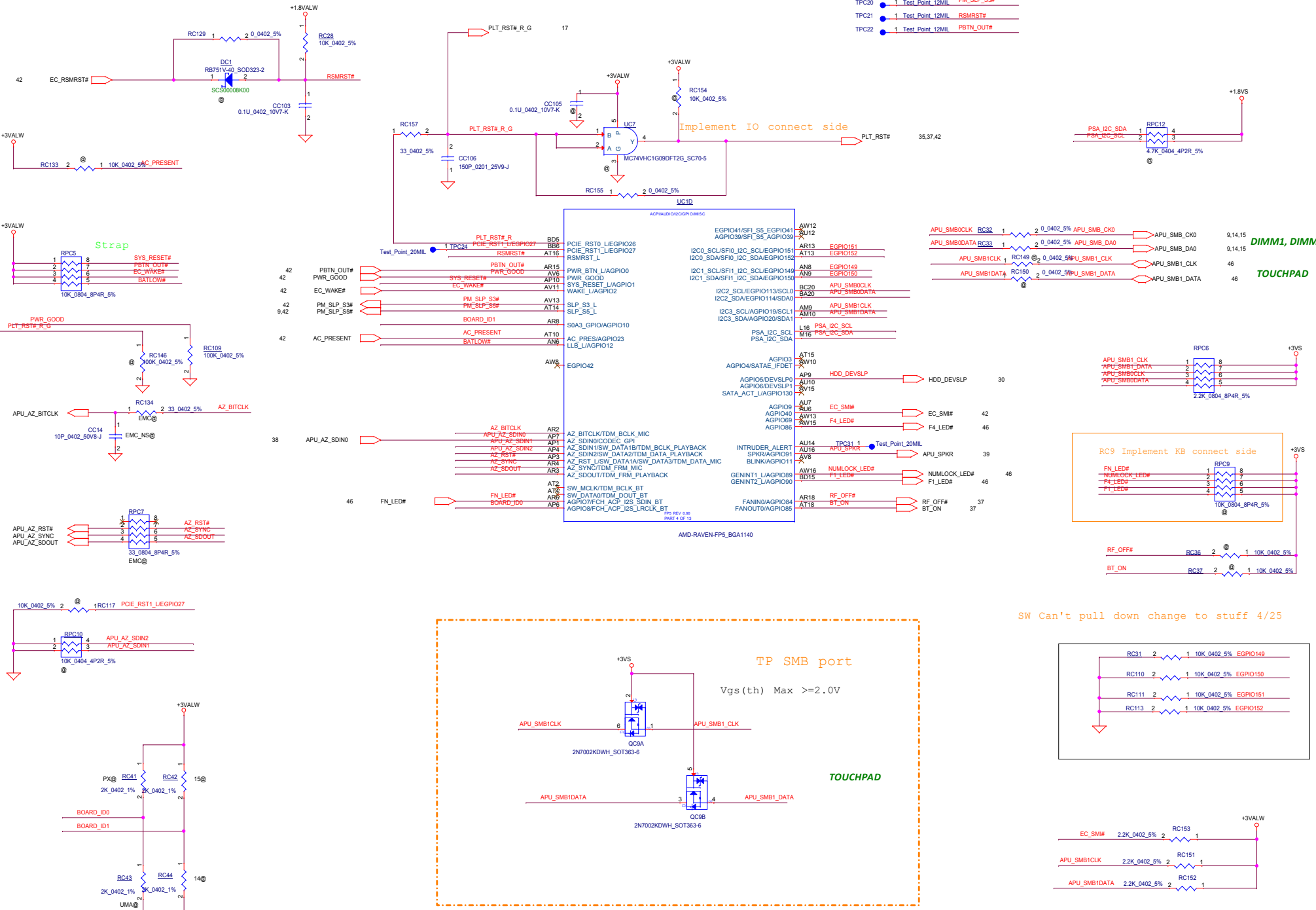
UC1I

MEMORY A		MEMORY B	
DDR_A_MA0	AF25	MA_ADD0MAB_CS0	J21
DDR_A_MA1	AE23	MA_ADD1RSVD	K21
DDR_A_MA2	AE21	MA_ADD2RSVD	F23
DDR_A_MA3	AE24	MA_ADD3RSVD	H23
DDR_A_MA4	AE26	MA_ADD4RSVD	G20
DDR_A_MA5	AE27	MA_ADD5RSVD	F20
DDR_A_MA6	AE27	MA_ADD6RSVD	J22
DDR_A_MA7	AE22	MA_ADD7MAB_CA3	J23
DDR_A_MA8	AE21	MA_ADD8MAB_CA4	K23
DDR_A_MA9	AE22	MA_ADD9MAB_CA1	G25
DDR_A_MA10	AE24	MA_ADD10MAB_CK0	F26
DDR_A_MA11	AE23	MA_ADD11MAB_CA5	L24
DDR_A_MA12	AE25	MA_ADD12MAB_CA2	D26
DDR_A_MA13	AE27	MA_ADD13_BANK2RSVD	D26
DDR_A_MA14	AE25	MA_ADD14MAB_CA2	L24
DDR_A_MA15	AE23	MA_ADD15MAB_CA4	K25
DDR_A_MA16	AE26	MA_ADD16MAB_CA3	K27
DDR_A_MA17	AE25	MA_ADD17MAB_CA2	M25
DDR_A_MA18	AE23	MA_ADD18MAB_CA0	M27
DDR_A_MA19	AE21	MA_ADD19MAB_CA0	P27
DDR_A_MA20	AE21	MA_ADD20MAB_CA0	T24
DDR_A_MA21	AE21	MA_ADD21MAB_CA0	L27
DDR_A_MA22	AE21	MA_ADD22MAB_CA0	M24
DDR_A_MA23	AE21	MA_ADD23MAB_CA0	P25
DDR_A_MA24	AE21	MA_ADD24MAB_CA0	M22
DDR_A_MA25	AE21	MA_ADD25MAB_CA0	N21
DDR_A_MA26	AE21	MA_ADD26MAB_CA0	V21
DDR_A_MA27	AE21	MA_ADD27MAB_CA0	L21
DDR_A_MA28	AE21	MA_ADD28MAB_CA0	A21
DDR_A_MA29	AE21	MA_ADD29MAB_CA0	R23
DDR_A_MA30	AE21	MA_ADD30MAB_CA0	T21
DDR_A_MA31	AE21	MA_ADD31MAB_CA0	N22
DDR_A_MA32	AE21	MA_ADD32MAB_CA0	A27
DDR_A_MA33	AE21	MA_ADD33MAB_CA0	A25
DDR_A_MA34	AE21	MA_ADD34MAB_CA0	A27
DDR_A_MA35	AE21	MA_ADD35MAB_CA0	A26
DDR_A_MA36	AE21	MA_ADD36MAB_CA0	A24
DDR_A_MA37	AE21	MA_ADD37MAB_CA0	A23
DDR_A_MA38	AE21	MA_ADD38MAB_CA0	A23
DDR_A_MA39	AE21	MA_ADD39MAB_CA0	A23
DDR_A_MA40	AE21	MA_ADD40MAB_CA0	A23
DDR_A_MA41	AE21	MA_ADD41MAB_CA0	A23
DDR_A_MA42	AE21	MA_ADD42MAB_CA0	A23
DDR_A_MA43	AE21	MA_ADD43MAB_CA0	A23
DDR_A_MA44	AE21	MA_ADD44MAB_CA0	A23
DDR_A_MA45	AE21	MA_ADD45MAB_CA0	A23
DDR_A_MA46	AE21	MA_ADD46MAB_CA0	A23
DDR_A_MA47	AE21	MA_ADD47MAB_CA0	A23
DDR_A_MA48	AE21	MA_ADD48MAB_CA0	A23
DDR_A_MA49	AE21	MA_ADD49MAB_CA0	A23
DDR_A_MA50	AE21	MA_ADD50MAB_CA0	A23
DDR_A_MA51	AE21	MA_ADD51MAB_CA0	A23
DDR_A_MA52	AE21	MA_ADD52MAB_CA0	A23
DDR_A_MA53	AE21	MA_ADD53MAB_CA0	A23
DDR_A_MA54	AE21	MA_ADD54MAB_CA0	A23
DDR_A_MA55	AE21	MA_ADD55MAB_CA0	A23
DDR_A_MA56	AE21	MA_ADD56MAB_CA0	A23
DDR_A_MA57	AE21	MA_ADD57MAB_CA0	A23
DDR_A_MA58	AE21	MA_ADD58MAB_CA0	A23
DDR_A_MA59	AE21	MA_ADD59MAB_CA0	A23
DDR_A_MA60	AE21	MA_ADD60MAB_CA0	A23
DDR_A_MA61	AE21	MA_ADD61MAB_CA0	A23
DDR_A_MA62	AE21	MA_ADD62MAB_CA0	A23
DDR_A_MA63	AE21	MA_ADD63MAB_CA0	A23
DDR_A_MA64	AE21	MA_ADD64MAB_CA0	A23
DDR_A_MA65	AE21	MA_ADD65MAB_CA0	A23
DDR_A_MA66	AE21	MA_ADD66MAB_CA0	A23
DDR_A_MA67	AE21	MA_ADD67MAB_CA0	A23
DDR_A_MA68	AE21	MA_ADD68MAB_CA0	A23
DDR_A_MA69	AE21	MA_ADD69MAB_CA0	A23
DDR_A_MA70	AE21	MA_ADD70MAB_CA0	A23
DDR_A_MA71	AE21	MA_ADD71MAB_CA0	A23
DDR_A_MA72	AE21	MA_ADD72MAB_CA0	A23
DDR_A_MA73	AE21	MA_ADD73MAB_CA0	A23
DDR_A_MA74	AE21	MA_ADD74MAB_CA0	A23
DDR_A_MA75	AE21	MA_ADD75MAB_CA0	A23
DDR_A_MA76	AE21	MA_ADD76MAB_CA0	A23
DDR_A_MA77	AE21	MA_ADD77MAB_CA0	A23
DDR_A_MA78	AE21	MA_ADD78MAB_CA0	A23
DDR_A_MA79	AE21	MA_ADD79MAB_CA0	A23
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DDR_A_MA81	AE21	MA_ADD81MAB_CA0	A23
DDR_A_MA82	AE21	MA_ADD82MAB_CA0	A23
DDR_A_MA83	AE21	MA_ADD83MAB_CA0	A23
DDR_A_MA84	AE21	MA_ADD84MAB_CA0	A23
DDR_A_MA85	AE21	MA_ADD85MAB_CA0	A23
DDR_A_MA86	AE21	MA_ADD86MAB_CA0	A23
DDR_A_MA87	AE21	MA_ADD87MAB_CA0	A23
DDR_A_MA88	AE21	MA_ADD88MAB_CA0	A23
DDR_A_MA89	AE21	MA_ADD89MAB_CA0	A23
DDR_A_MA90	AE21	MA_ADD90MAB_CA0	A23
DDR_A_MA91	AE21	MA_ADD91MAB_CA0	A23
DDR_A_MA92	AE21	MA_ADD92MAB_CA0	A23
DDR_A_MA93	AE21	MA_ADD93MAB_CA0	A23
DDR_A_MA94	AE21	MA_ADD94MAB_CA0	A23
DDR_A_MA95	AE21	MA_ADD95MAB_CA0	A23
DDR_A_MA96	AE21	MA_ADD96MAB_CA0	A23
DDR_A_MA97	AE21	MA_ADD97MAB_CA0	A23
DDR_A_MA98	AE21	MA_ADD98MAB_CA0	A23
DDR_A_MA99	AE21	MA_ADD99MAB_CA0	A23
DDR_A_MA100	AE21	MA_ADD100MAB_CA0	A23

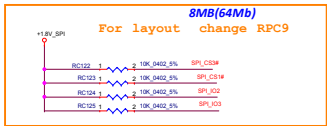
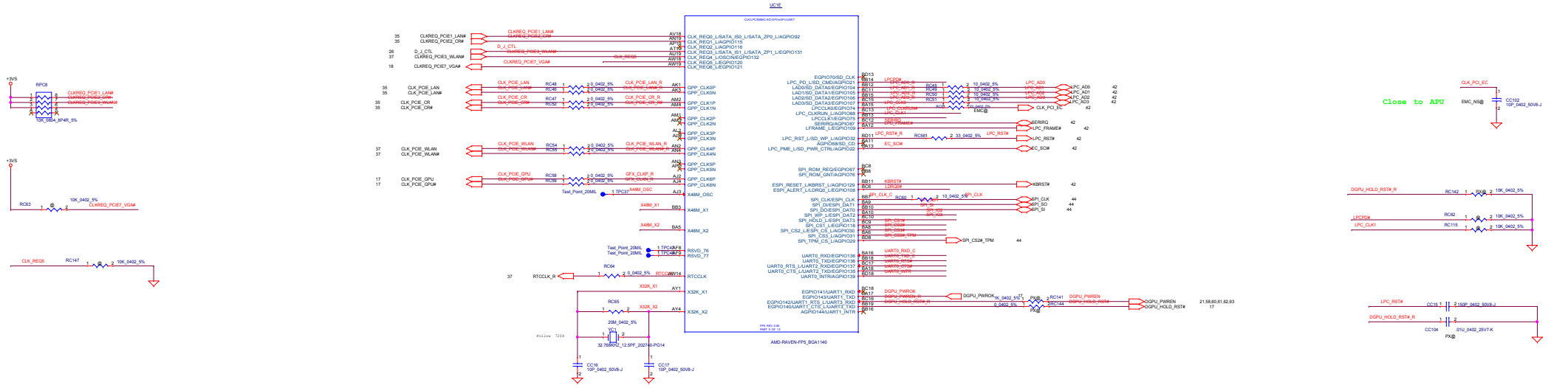
MEMORY A		MEMORY B	
DDR_B_MA0	AG30	MB_ADD0MAB_CS0	B21
DDR_B_MA1	AG30	MB_ADD1RSVD	D21
DDR_B_MA2	AG30	MB_ADD2RSVD	B23
DDR_B_MA3	AG31	MB_ADD3RSVD	D23
DDR_B_MA4	AG30	MB_ADD4RSVD	A20
DDR_B_MA5	AG30	MB_ADD5RSVD	C20
DDR_B_MA6	AG30	MB_ADD6RSVD	F22
DDR_B_MA7	AG31	MB_ADD7MAB_CA3	C22
DDR_B_MA8	AG31	MB_ADD8MAB_CA4	M24
DDR_B_MA9	AG30	MB_ADD9MAB_CA1	D24
DDR_B_MA10	AG30	MB_ADD10MAB_CK0	A25
DDR_B_MA11	AG31	MB_ADD11MAB_CA5	B27
DDR_B_MA12	AG31	MB_ADD12MAB_CA2	C27
DDR_B_MA13	AG31	MB_ADD13_BANK2RSVD	C23
DDR_B_MA14	AG31	MB_ADD14MAB_CA2	B24
DDR_B_MA15	AG30	MB_ADD15MAB_CA4	C26
DDR_B_MA16	AG30	MB_ADD16MAB_CA3	B27
DDR_B_MA17	AG31	MB_ADD17MAB_CA0	C30
DDR_B_MA18	AG31	MB_ADD18MAB_CA0	E29
DDR_B_MA19	AG31	MB_ADD19MAB_CA0	H29
DDR_B_MA20	AG31	MB_ADD20MAB_CA0	H31
DDR_B_MA21	AG31	MB_ADD21MAB_CA0	A28
DDR_B_MA22	AG31	MB_ADD22MAB_CA0	D28
DDR_B_MA23	AG31	MB_ADD23MAB_CA0	F31
DDR_B_MA24	AG31	MB_ADD24MAB_CA0	G30
DDR_B_MA25	AG31	MB_ADD25MAB_CA0	J29
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DDR_B_MA83	AG31	MB_ADD83MAB_CA0	A31
DDR_B_MA84	AG31	MB_ADD84MAB_CA0	B31
DDR_B_MA85	AG31	MB_ADD85MAB_CA0	D31
DDR_B_MA86	AG31	MB_ADD86MAB_CA0	F31
DDR_B_MA87	AG31	MB_ADD87MAB_CA0	H31
DDR_B_MA88	AG31	MB_ADD88MAB_CA0	H33
DDR_B_MA89	AG31	MB_ADD89MAB_CA0	A31
DDR_B_MA90	AG31	MB_ADD90MAB_CA0	B31
DDR_B_MA91	AG31	MB_ADD91MAB_CA0	D31
DDR_B_MA92	AG31	MB_ADD92MAB_CA0	F31
DDR_B_MA93	AG31	MB_ADD93MAB_CA0	H31
DDR_B_MA94	AG31	MB_ADD94MAB_CA0	H33
DDR_B_MA95	AG31	MB_ADD95MAB_CA0	A31
DDR_B_MA96	AG31	MB_ADD96MAB_CA0	B31
DDR_B_MA97	AG31	MB_ADD97MAB_CA0	D31
DDR_B_MA98	AG31	MB_ADD98MAB_CA0	F31
DDR_B_MA99	AG31	MB_ADD99MAB_CA0	H31
DDR_B_MA100	AG31	MB_ADD100MAB_CA0	H33

Vinafix

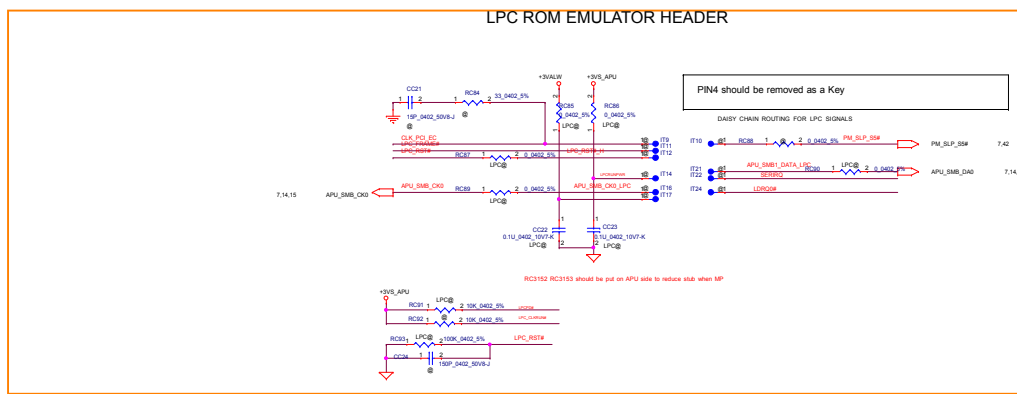
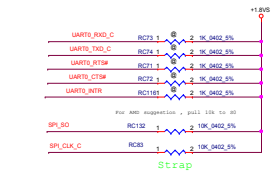
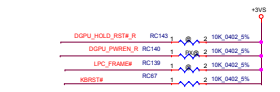
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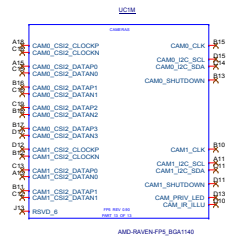


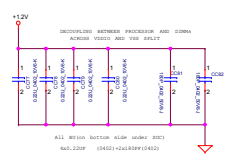
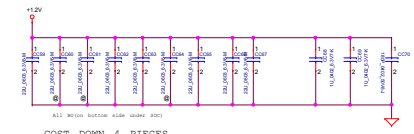
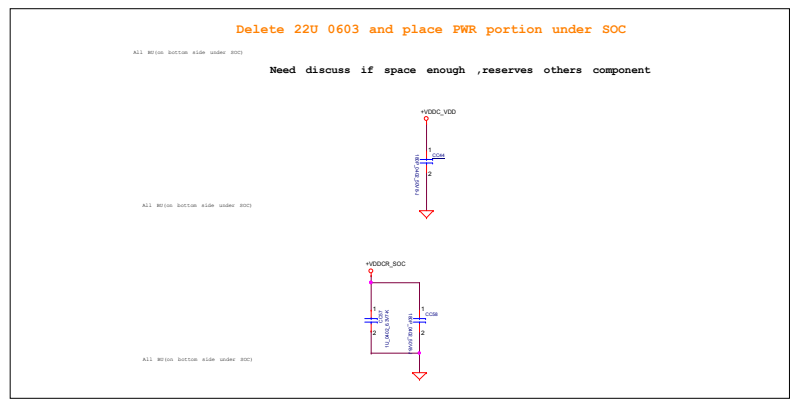
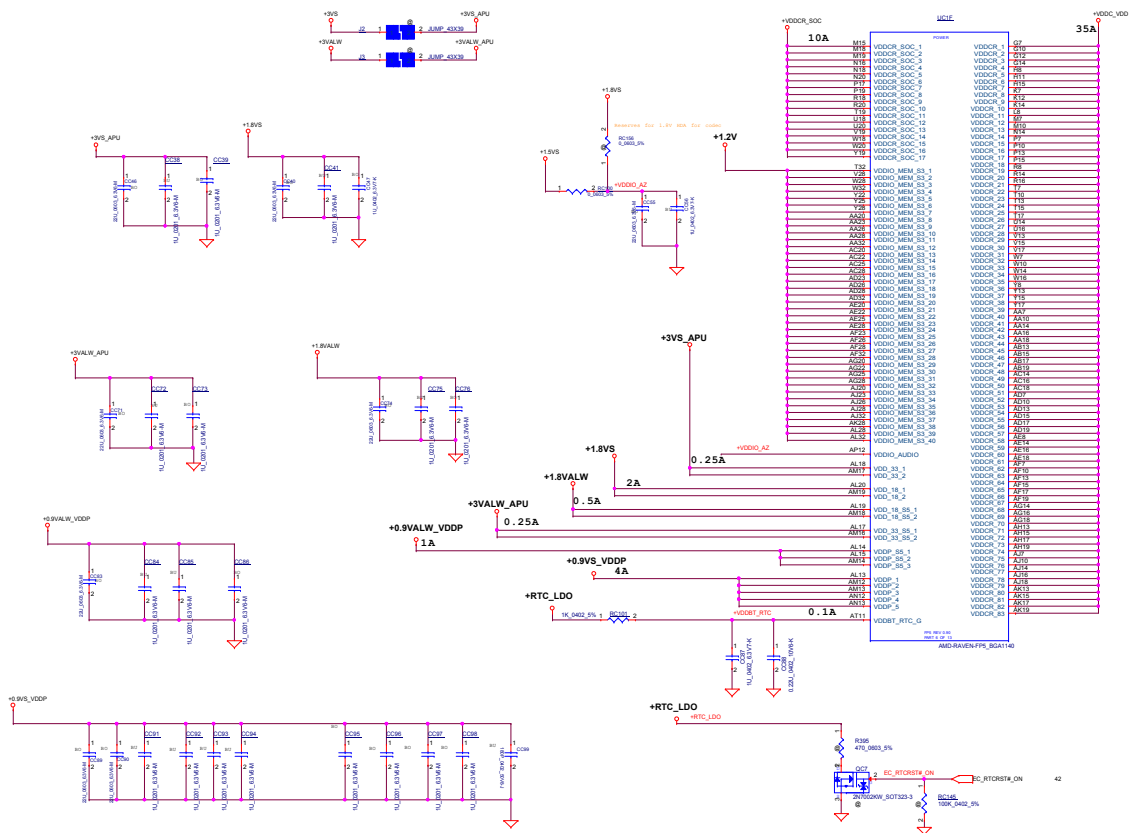
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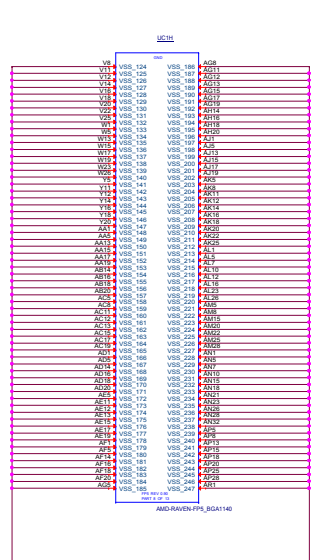
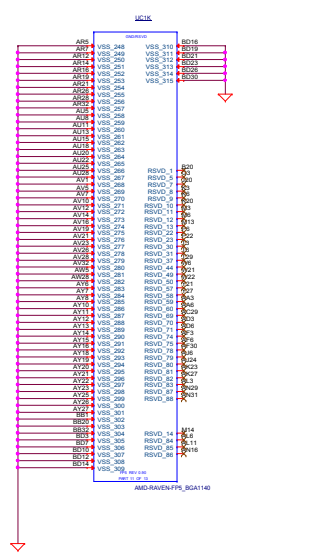
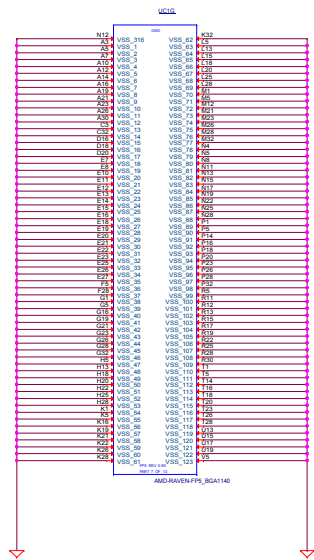


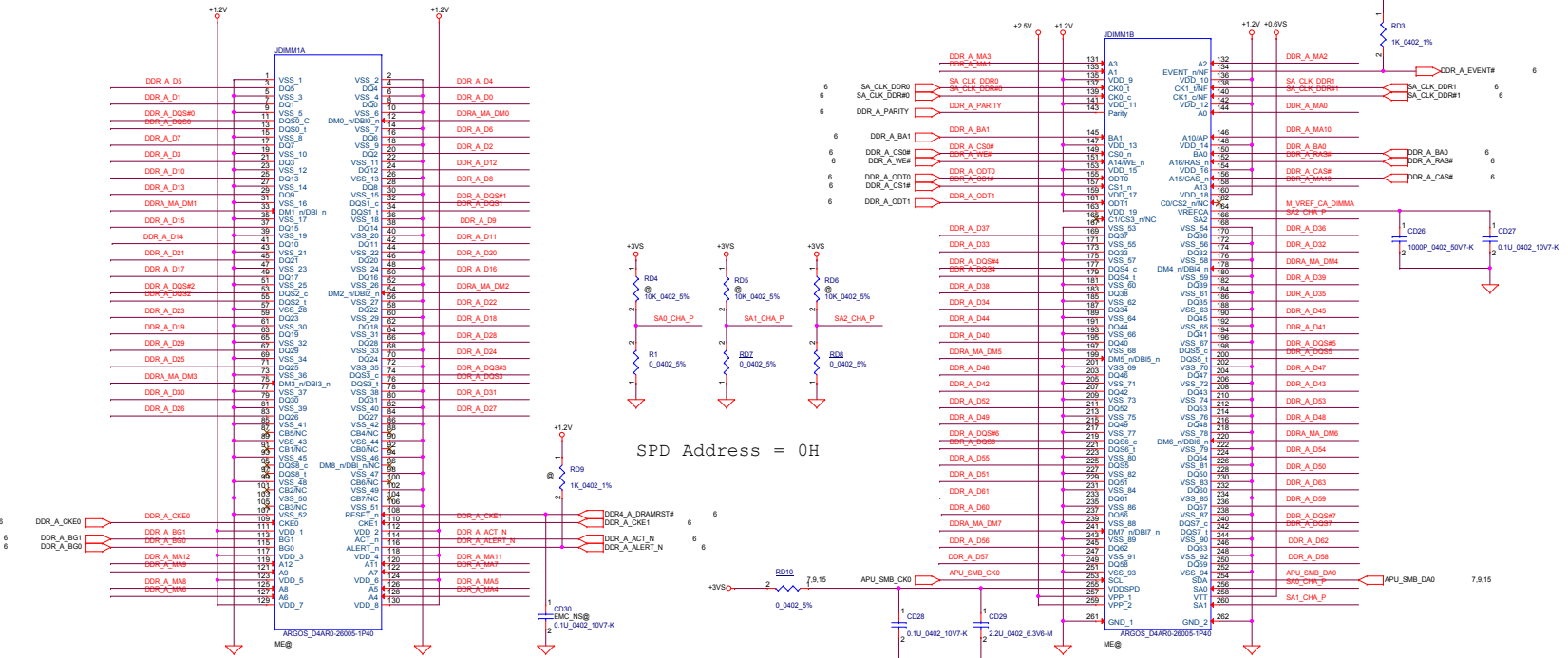
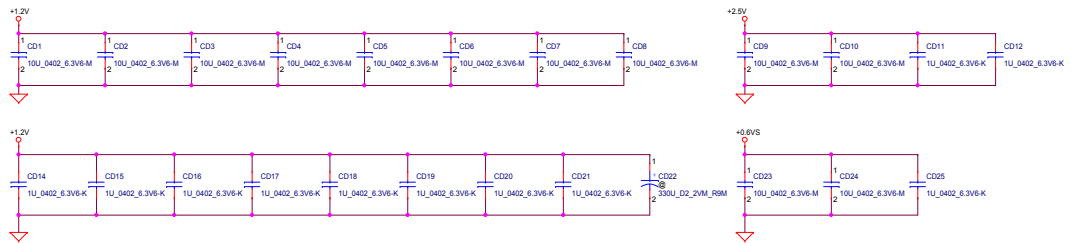
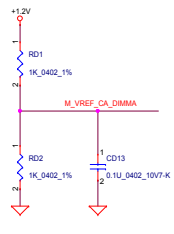
change YC2 PN change to S21000M00, manual modify PN to S31000M00

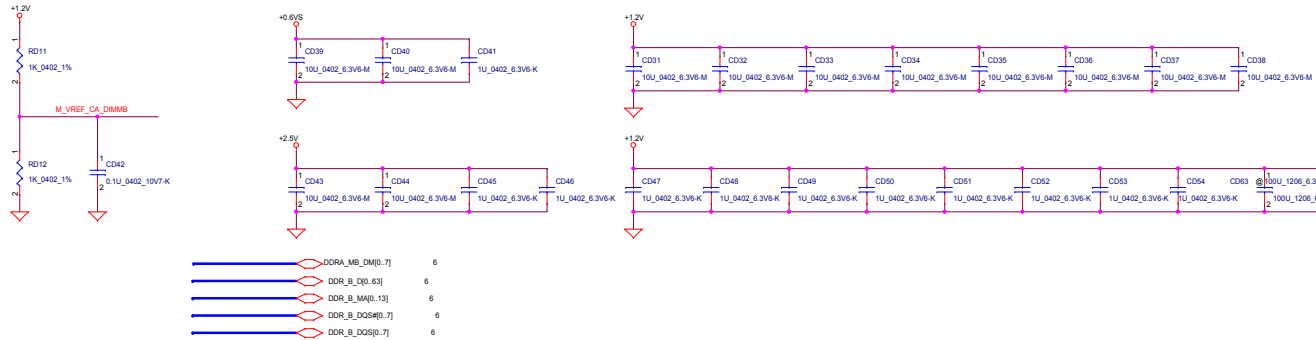




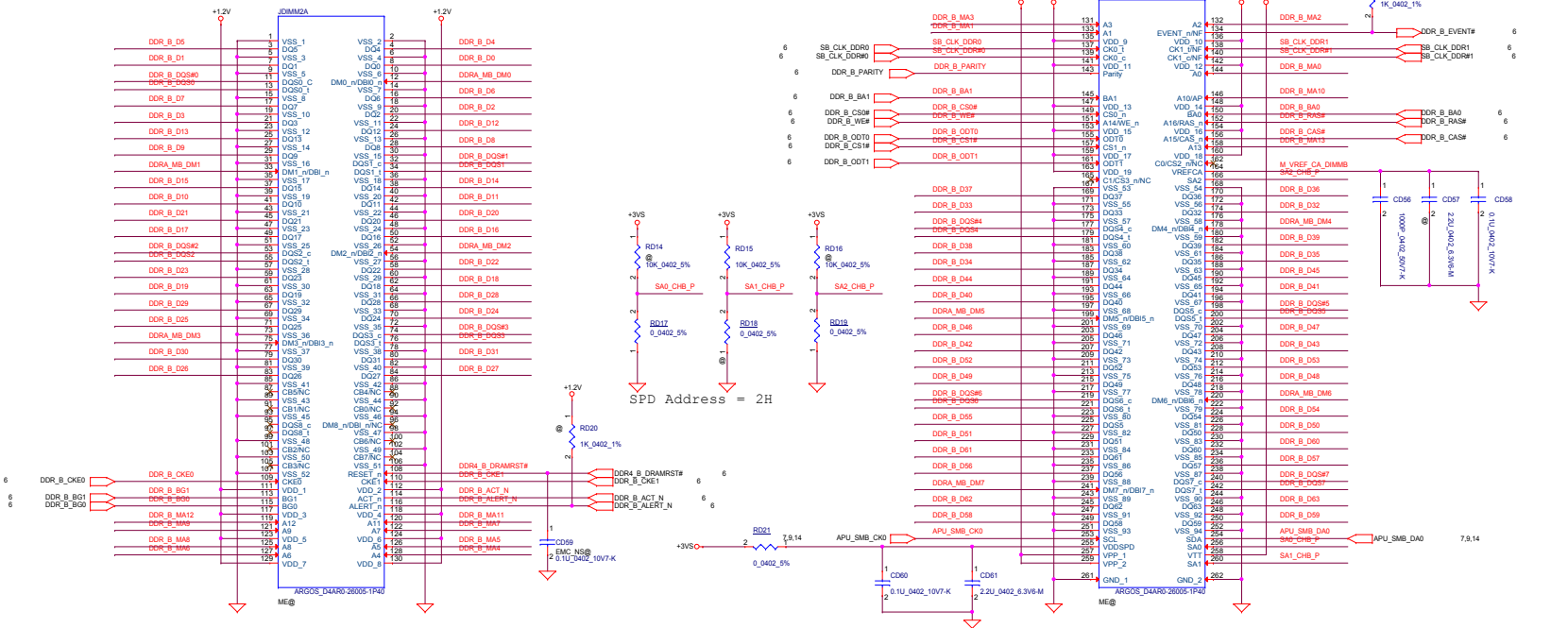








Layout Note:
Place Close DIMMs



Power-Up/Down Sequence

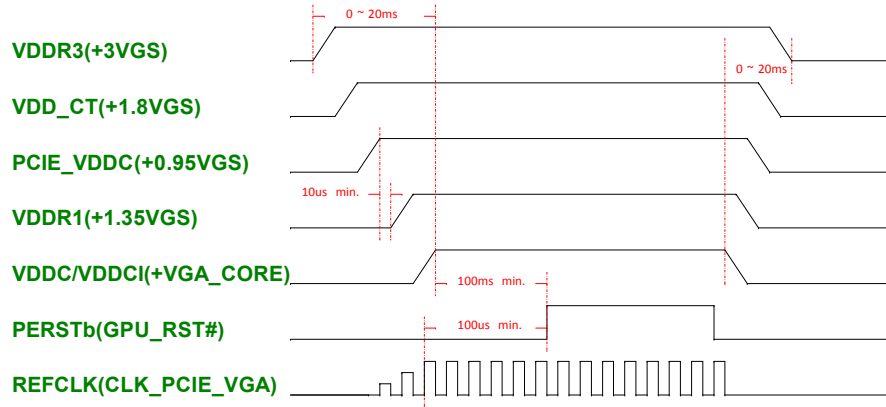
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/ μ s). For power down, reversing the ramp-up sequence is recommended.

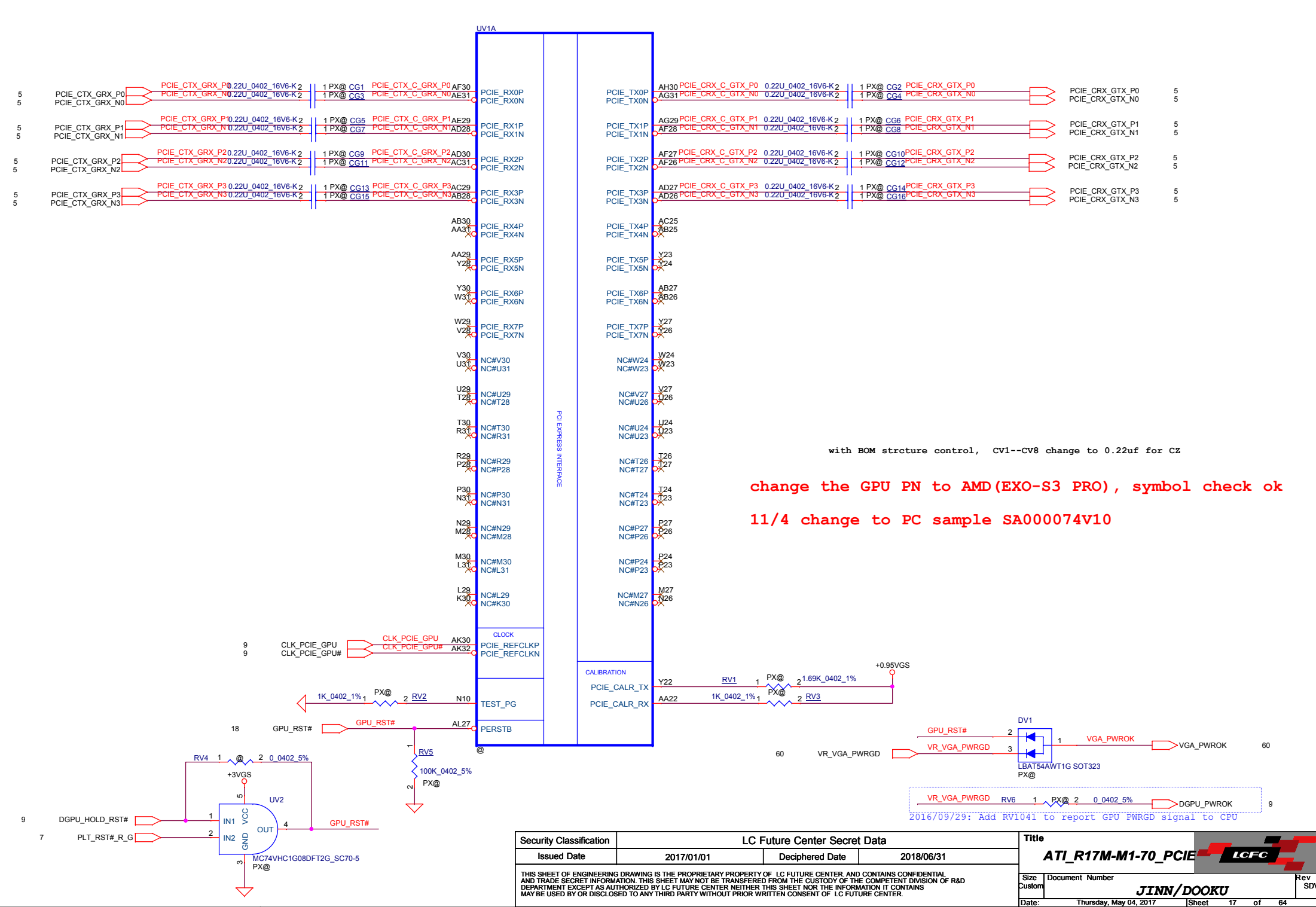


VRAM ID config

Memory Type	VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70	
	100	4.53K	4.99K	
	111	4.75K	NC	
	110	3.4K	10K	
8Gb GDDR5 512M x 32	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70:A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

3 Hynix H5GC8H24MJR-R0C
Samsung K4G80325FB-HC28
Micron MT51J256M32HF-70:A

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with BOM structure control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok
 11/4 change to PC sample SA000074V10

2016/09/29: Add RV1041 to report GPU PWRGD signal to CPU

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ATI_R17M-M1-70_PCIE		
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UV1F

NC_VARY_BL
NC_DIGON

AB11
AB12

+VGA_CORE

NC_UPHYAB_TMDPA_TX0N ΔL15
 NC_UPHYAB_TMDPA_TX0P ΔK14
 NC_UPHYAB_TMDPA_TX1N ΔH16
 NC_UPHYAB_TMDPA_TX1P ΔJ15
 NC_UPHYAB_TMDPA_TX2N ΔL17
 NC_UPHYAB_TMDPA_TX2P ΔK16
 NC_UPHYAB_TMDPA_TX3N ΔH18
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 NC_TXOUT_L3P ΔL19
 NC_TXOUT_L3N ΔK18

TMDP

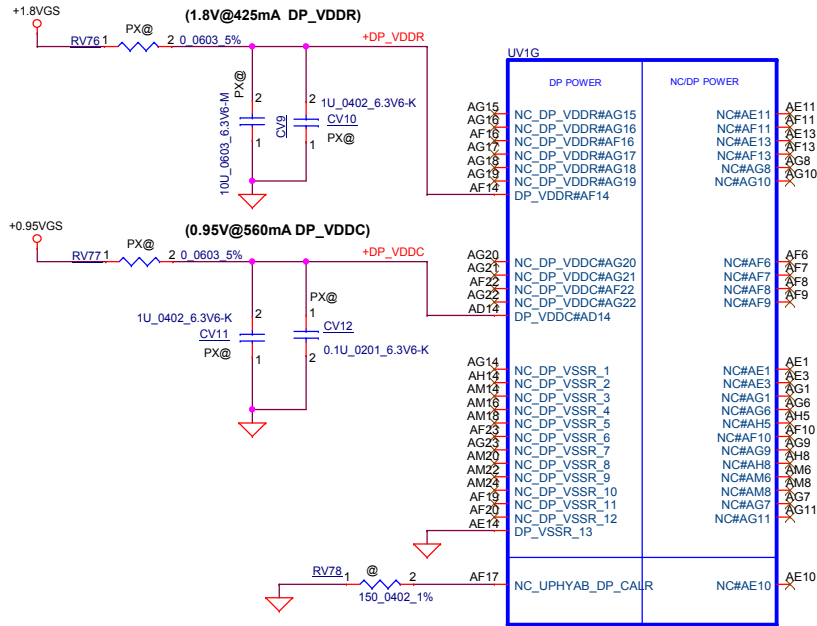
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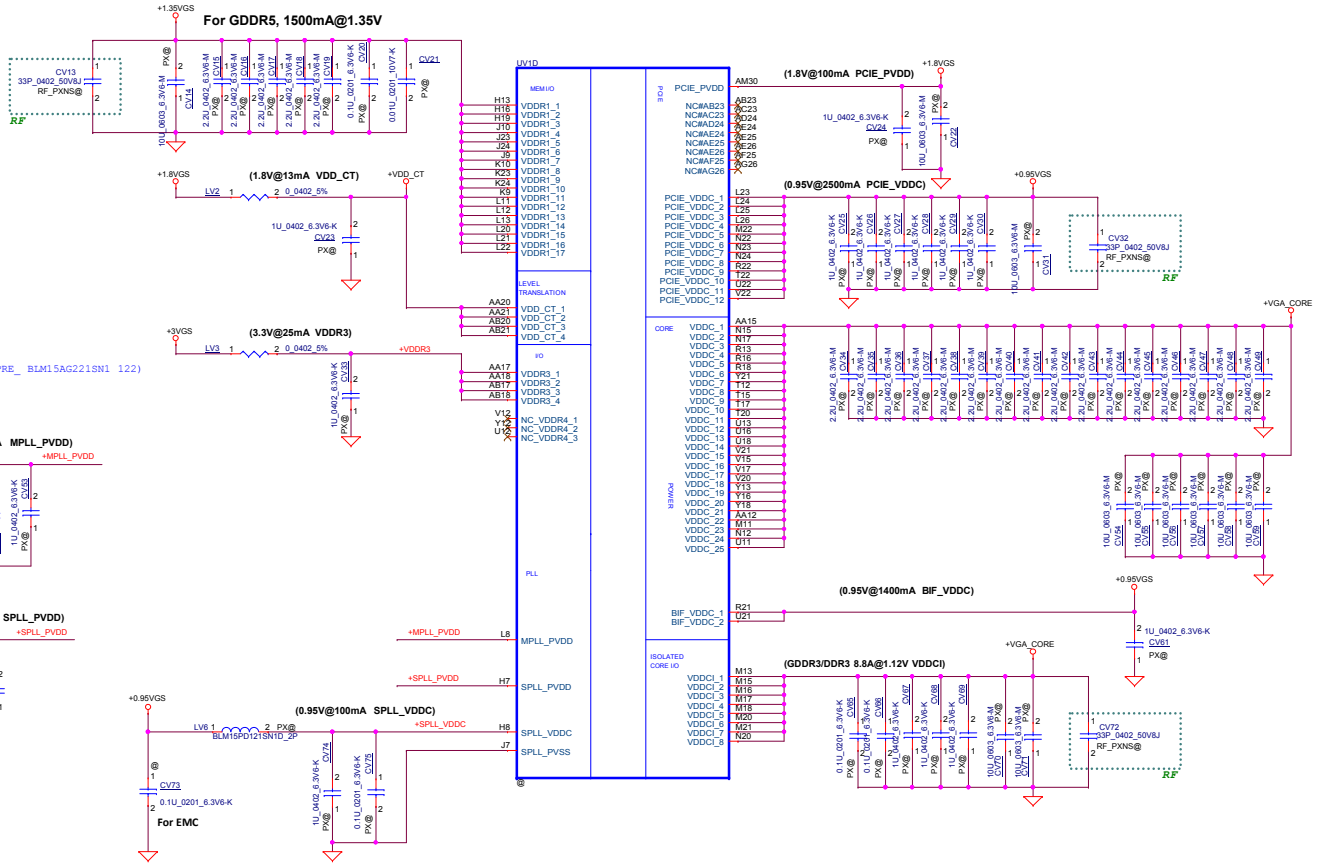
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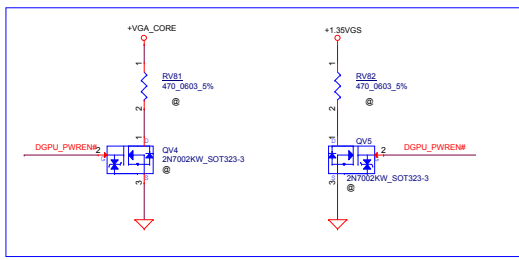
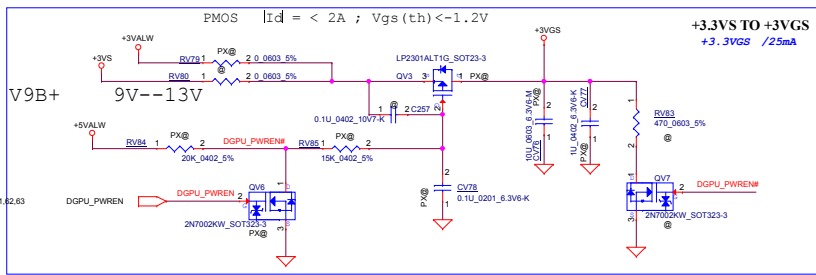
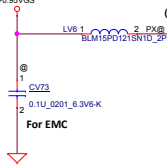
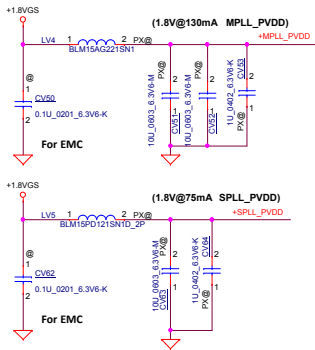
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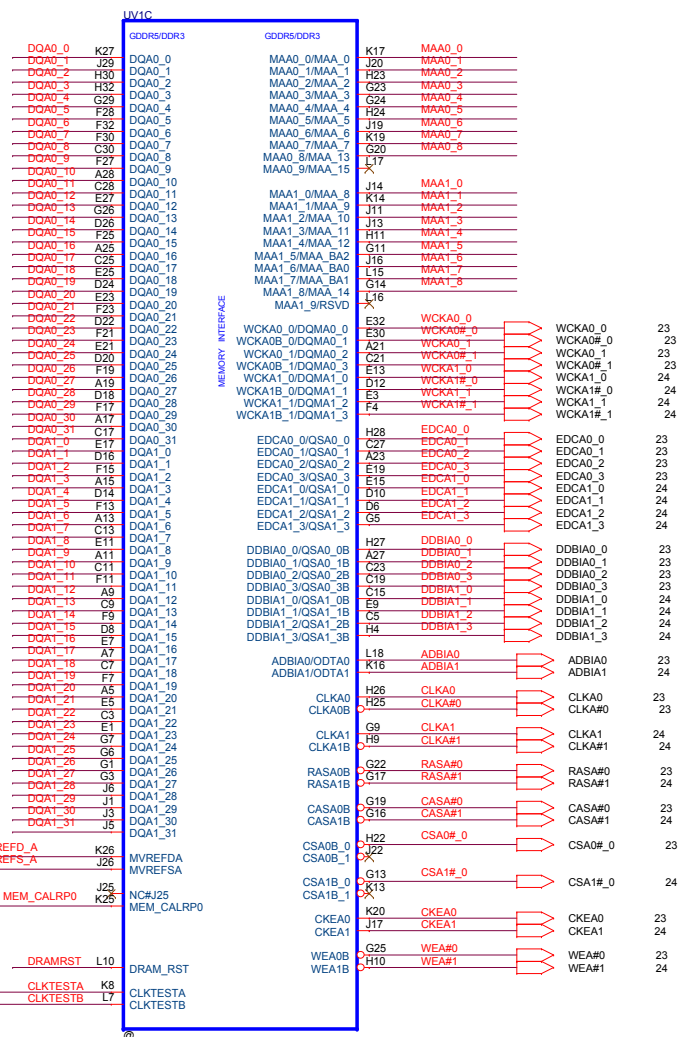
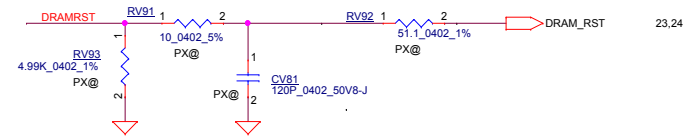
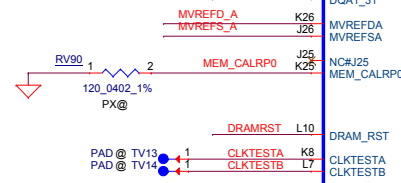
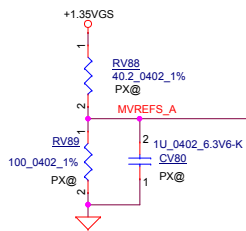
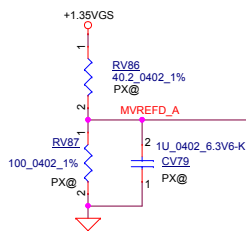
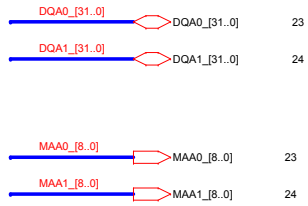


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change LV4 to SM01000M00 (S_SUPPTE_BLM15AG221SN1 122) as DFC suggest, footprint with MURAT_BLM15PD121SND_2P





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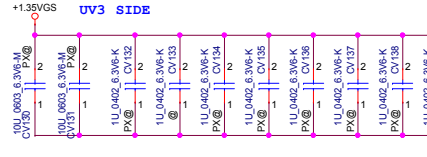
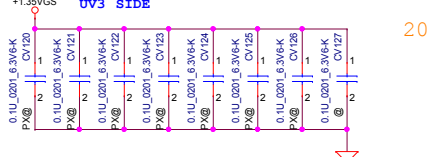
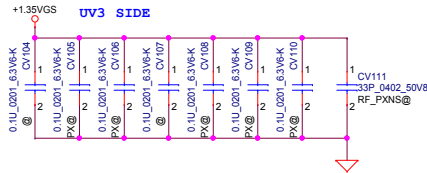
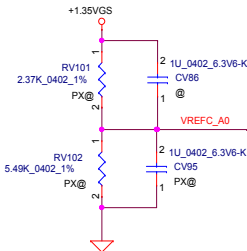
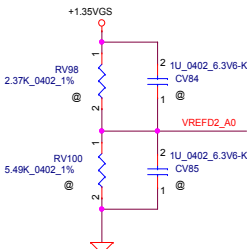
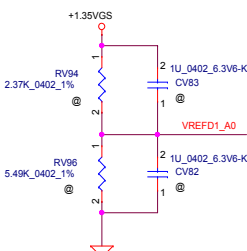
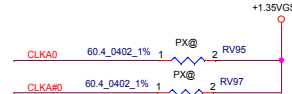
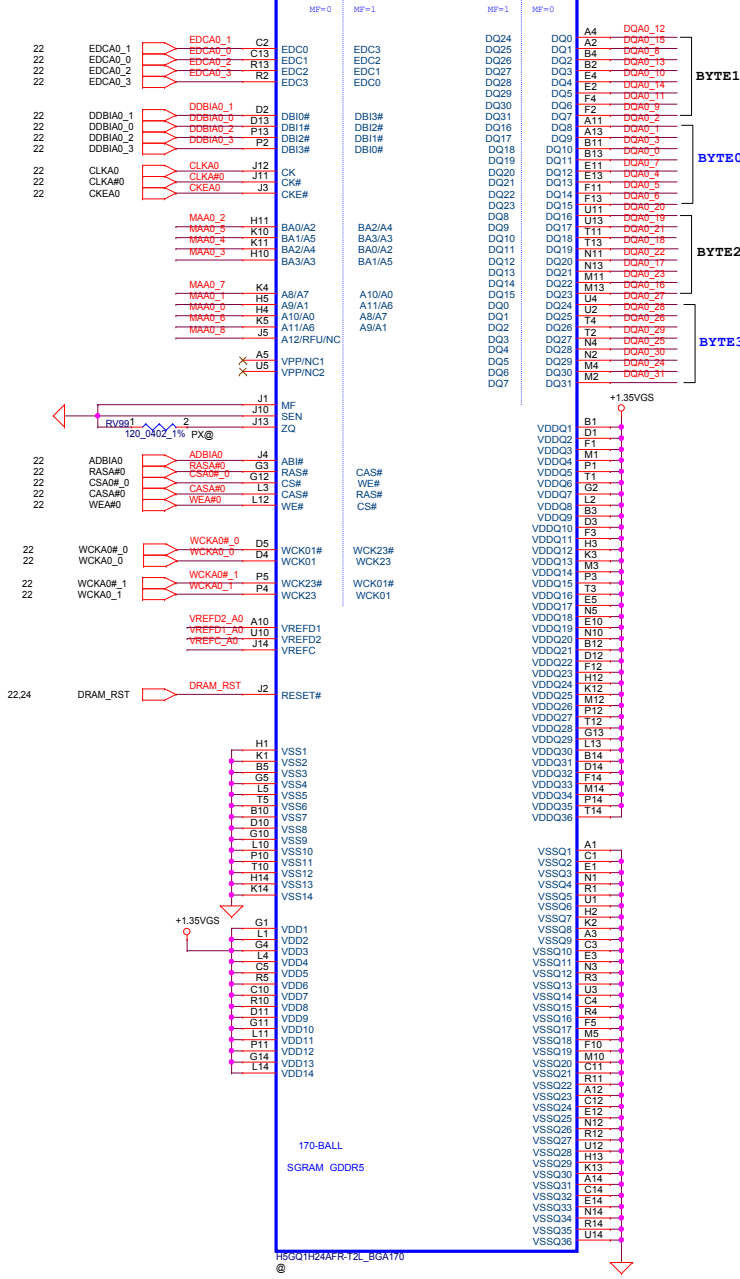
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Lower 32 bits



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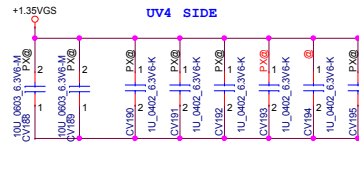
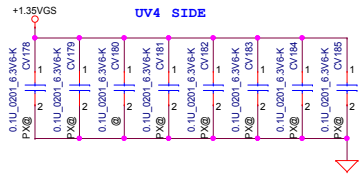
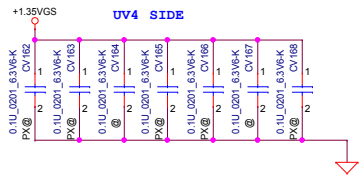
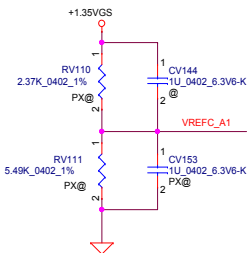
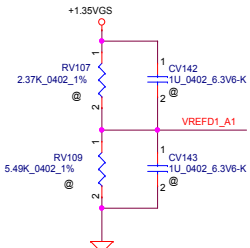
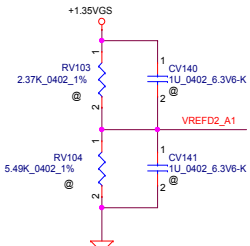
UV3



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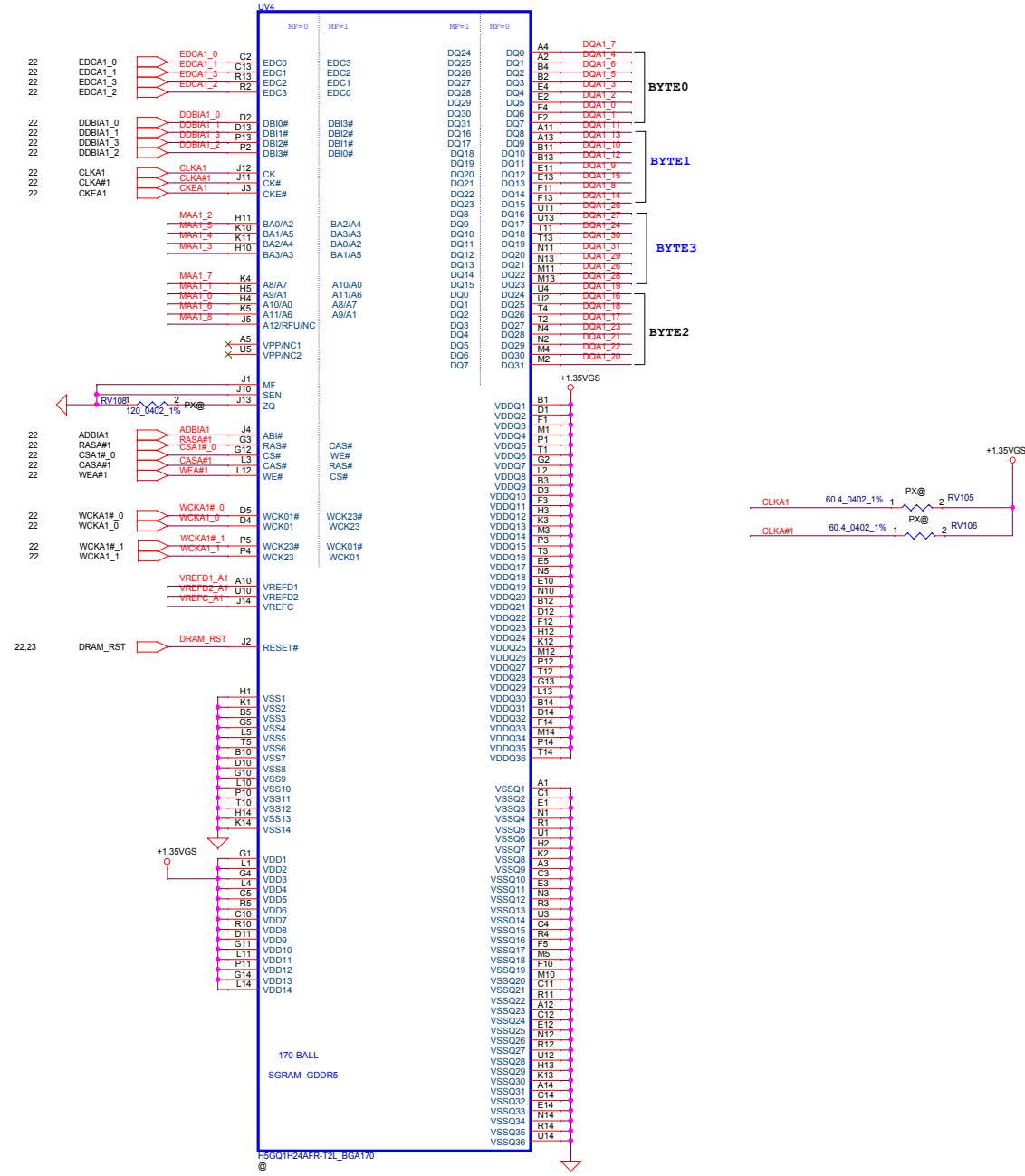
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Upper 32 bits




20% Down

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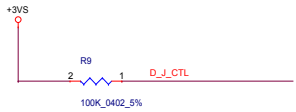
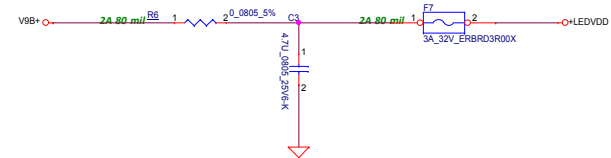
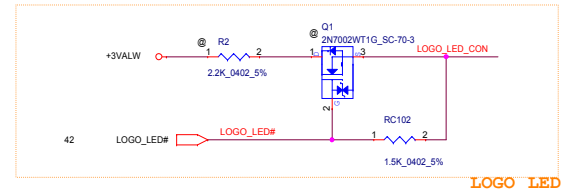
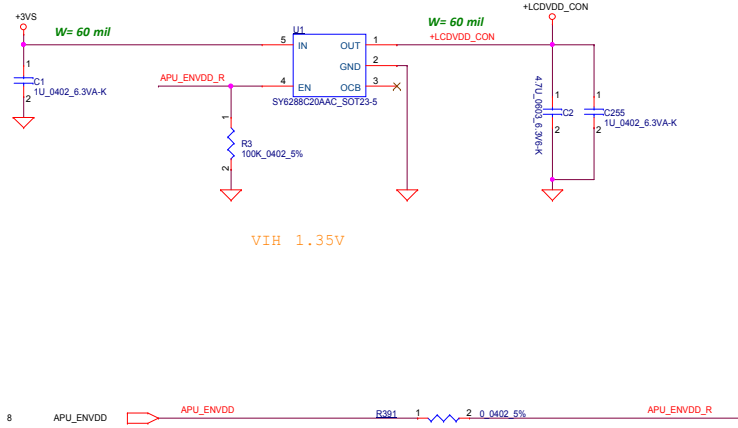


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170-BALL SGRAM GDDR5			Rev SDV
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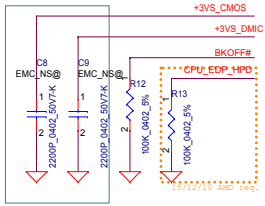
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LCDVDD Circuit



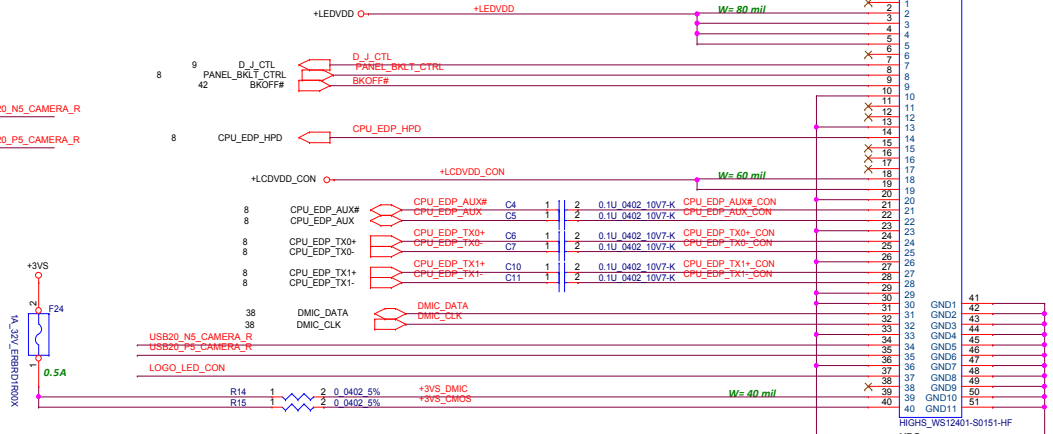
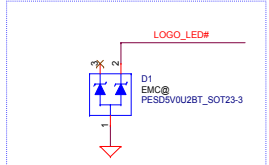
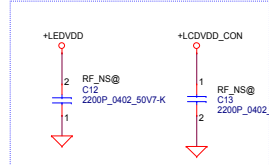
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D_J_CTL	NC	GND

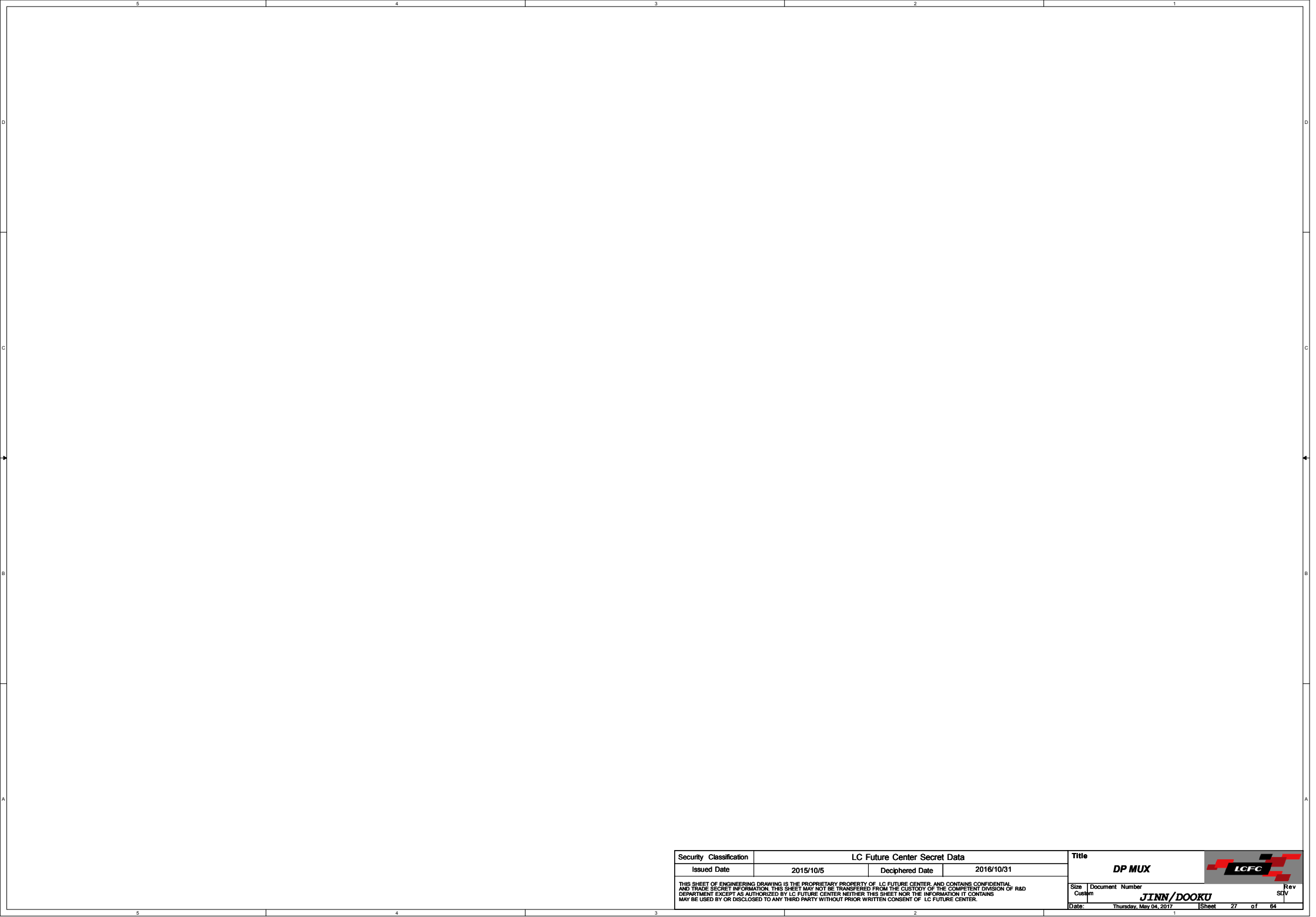
eDP/CMOS/LOGO-LED CONN.




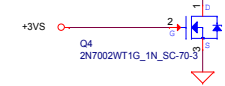
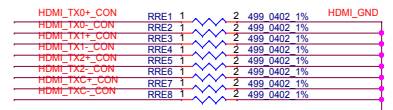
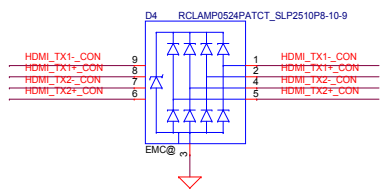
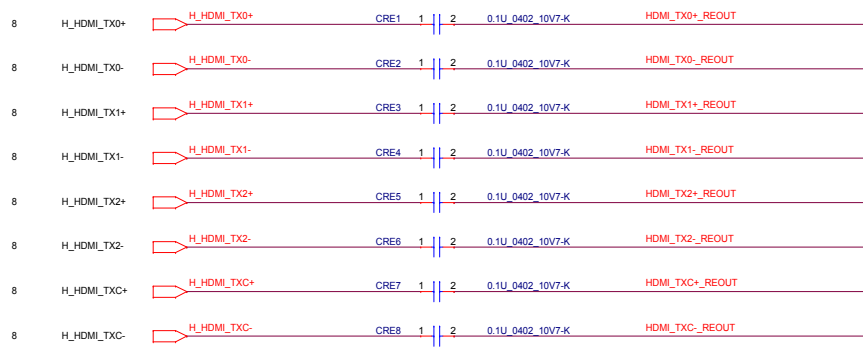
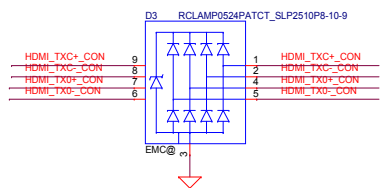
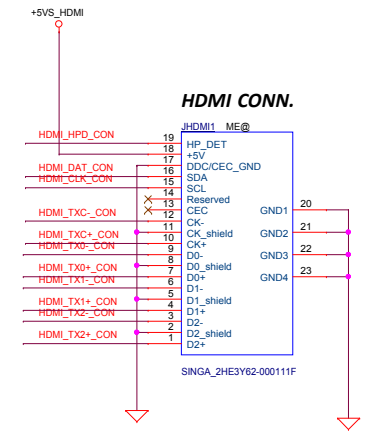
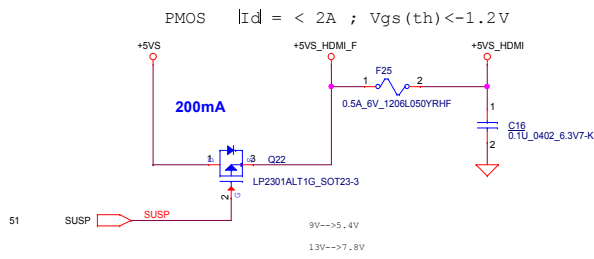
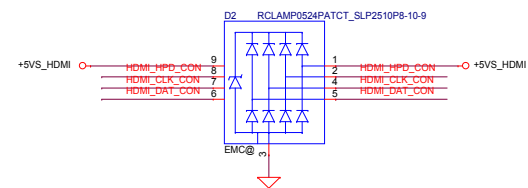
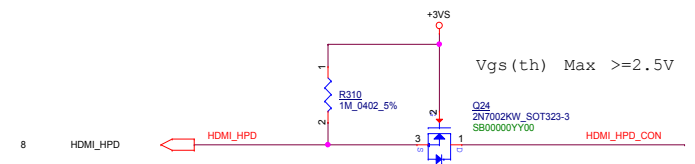
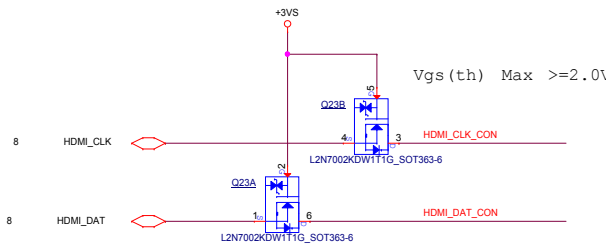
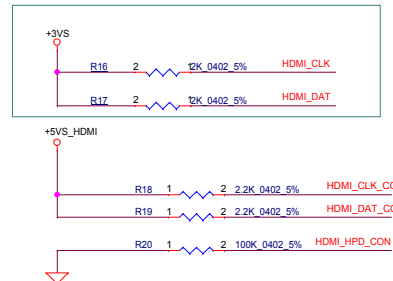
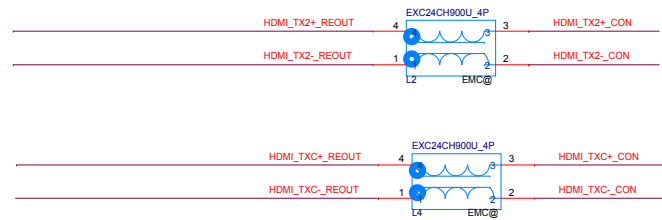
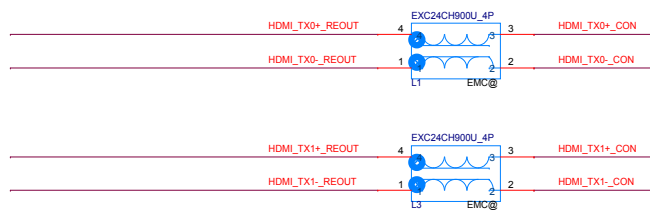
EMC request. Close to JLCD

ESD request



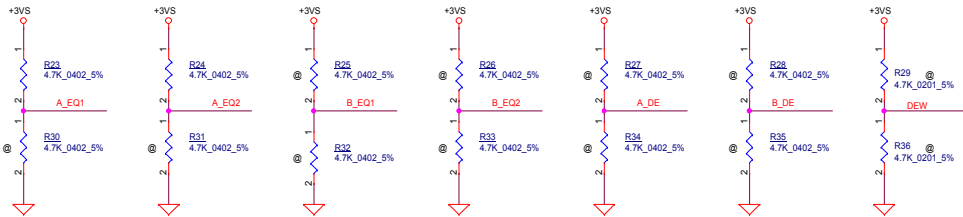
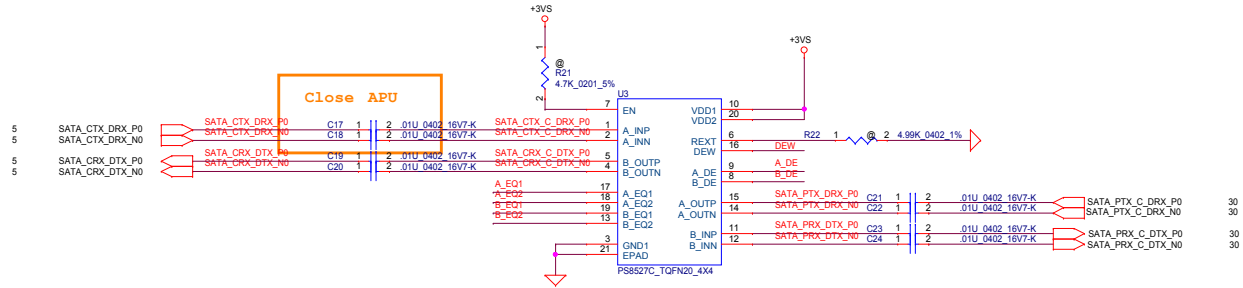


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Issued Date	2015/10/5	Deciphered Date	2016/10/31	
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Date:	Thursday, May 04, 2017		Sheet	27 of 84



Need two gerbout about SATA redriver and no redriver 0324

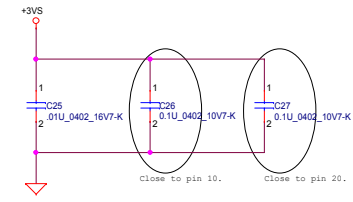
SATA HDD Redriver



Equalization level setting for Channel x(x=A/B), internally tied to VDDP2
 [x_EQ2, x_EQ1] ==
 L/M: for channel loss up to 0.4dB
 L/L: for channel loss up to 0.4dB
 L/R: for channel loss up to 14.4dB
 M/M: for channel loss up to 12.5dB (default)
 M/L: for channel loss up to 9.4dB
 M/R: for channel loss up to 13.7dB
 H/M: for channel loss up to 6.2dB
 H/L: for channel loss up to 11.2dB
 H/H: for channel loss up to 5dB

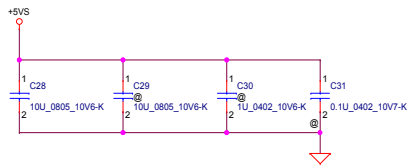
De-emphasis level setting for Channel x(x=A/B), internally tied to VDDP2
 [x_DE] ==
 M: -3.5dB (default)
 L: 0dB
 H: -6dB

De-emphasis width adjustment, internally pulled down:
 [DEW] ==
 M: for SATA3 (default)
 L: for SATA3
 H: for SATA2

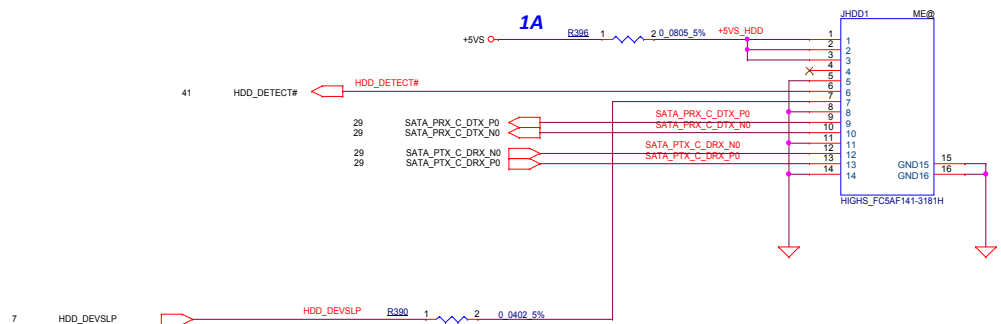


Follow Vendor suggest

SATA HDD CONN.



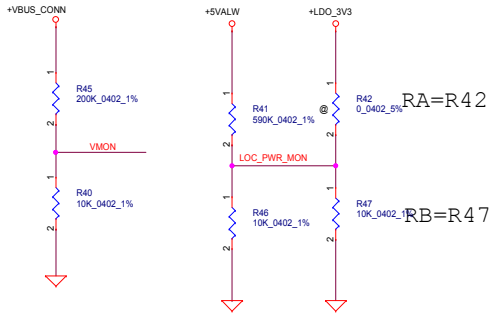
SATA HDD CONN.



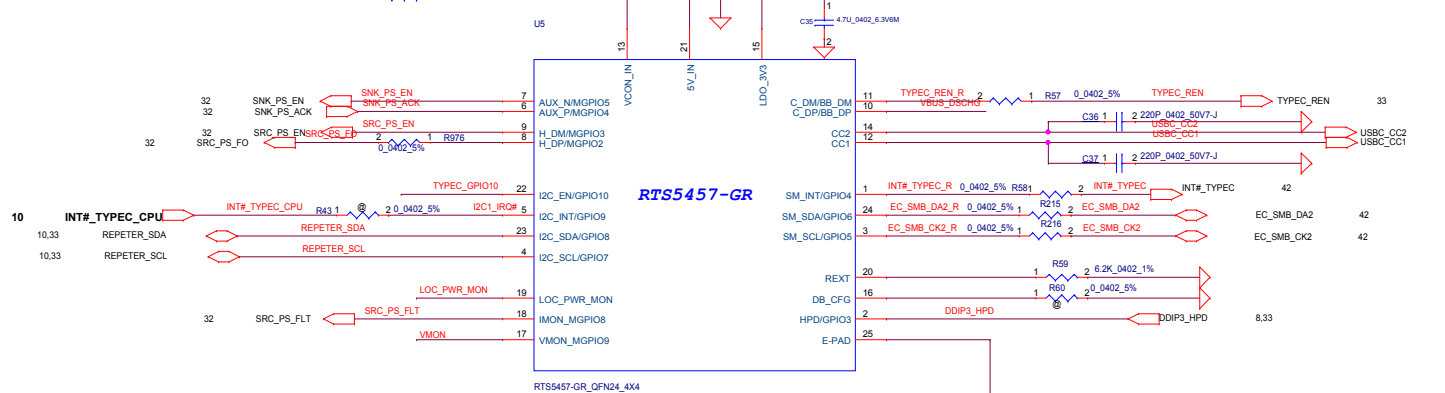
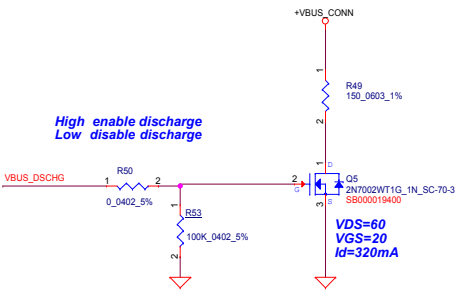
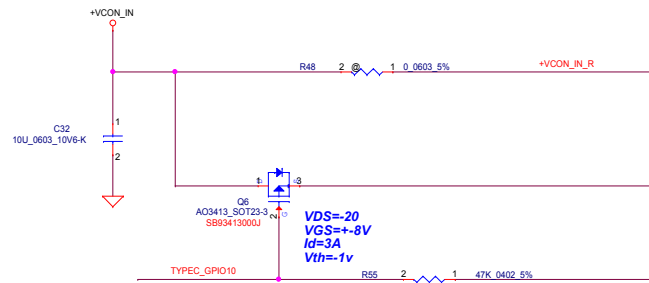
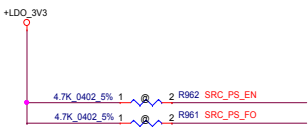
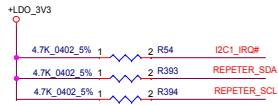
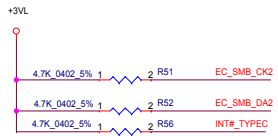
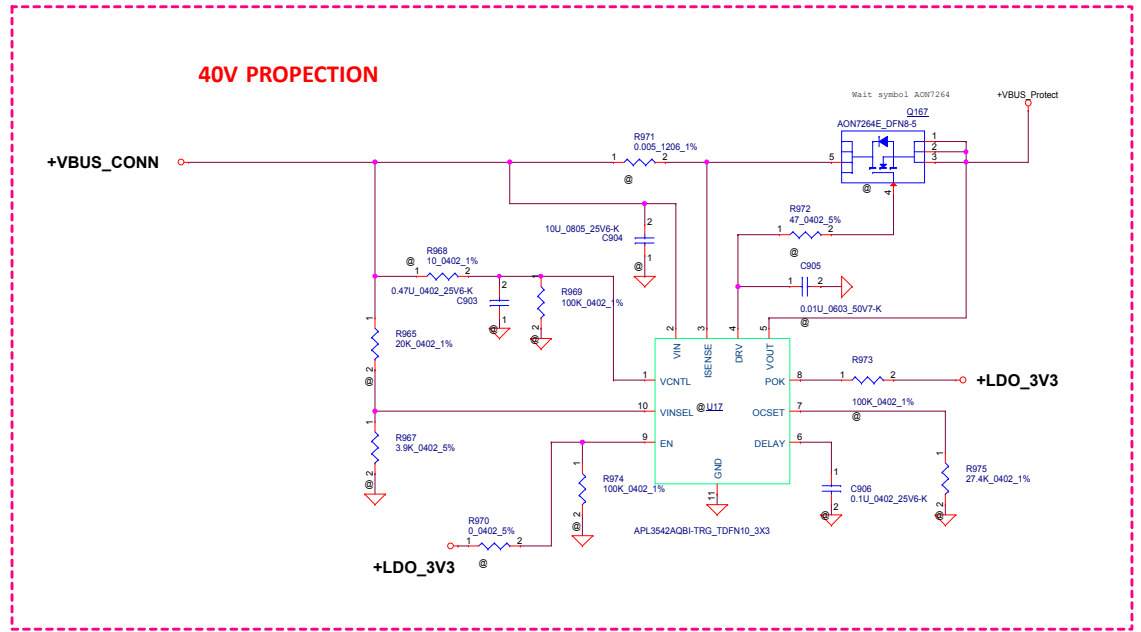
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2017/01/01	Deciphered Date	2018/06/31	SATA HDD	
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Size	C	Document Number	JINN/DOORU		Rev
Date	Thursday, May 04, 2017	Sheet	39	of	64

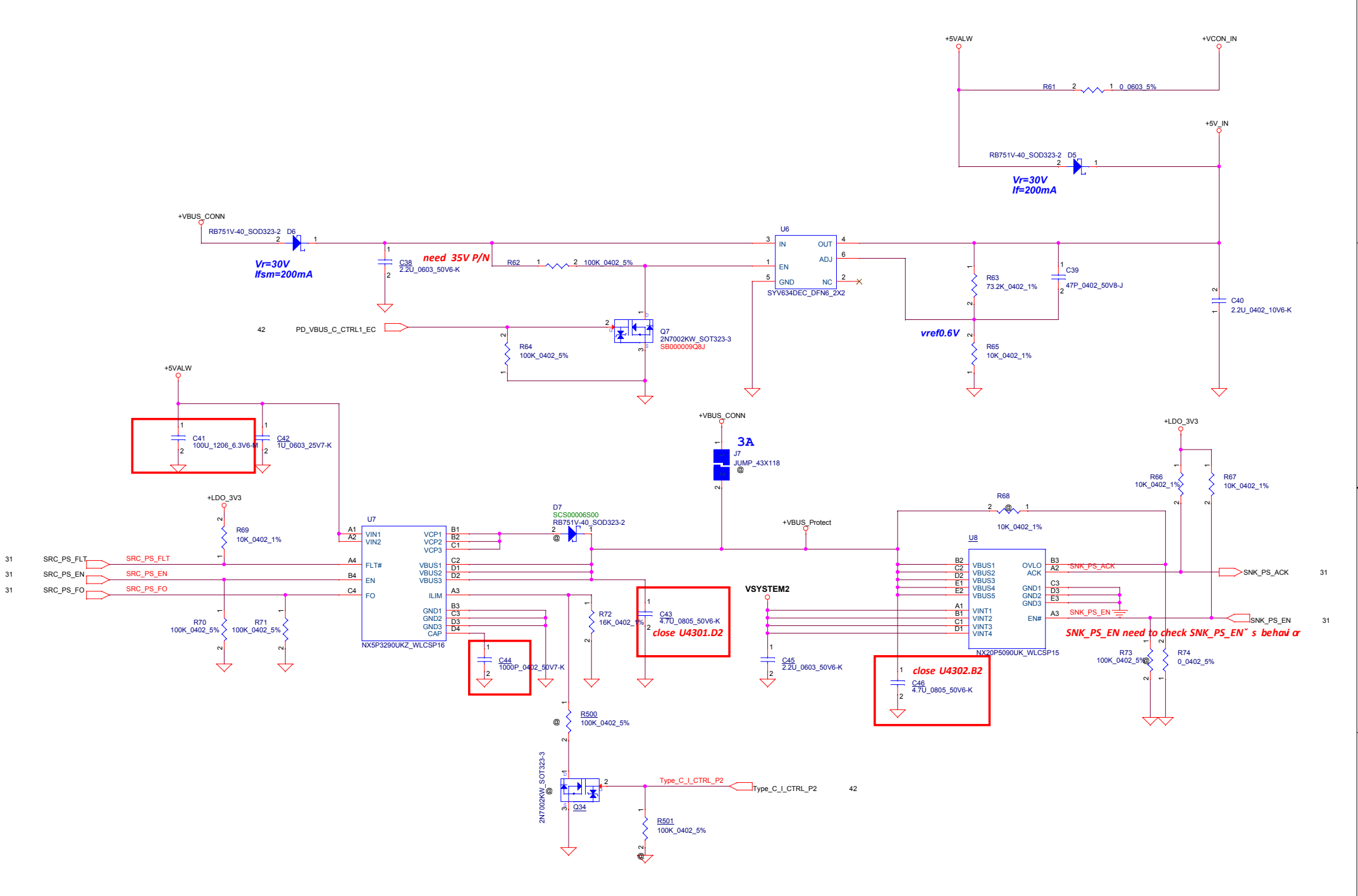


SDV



Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



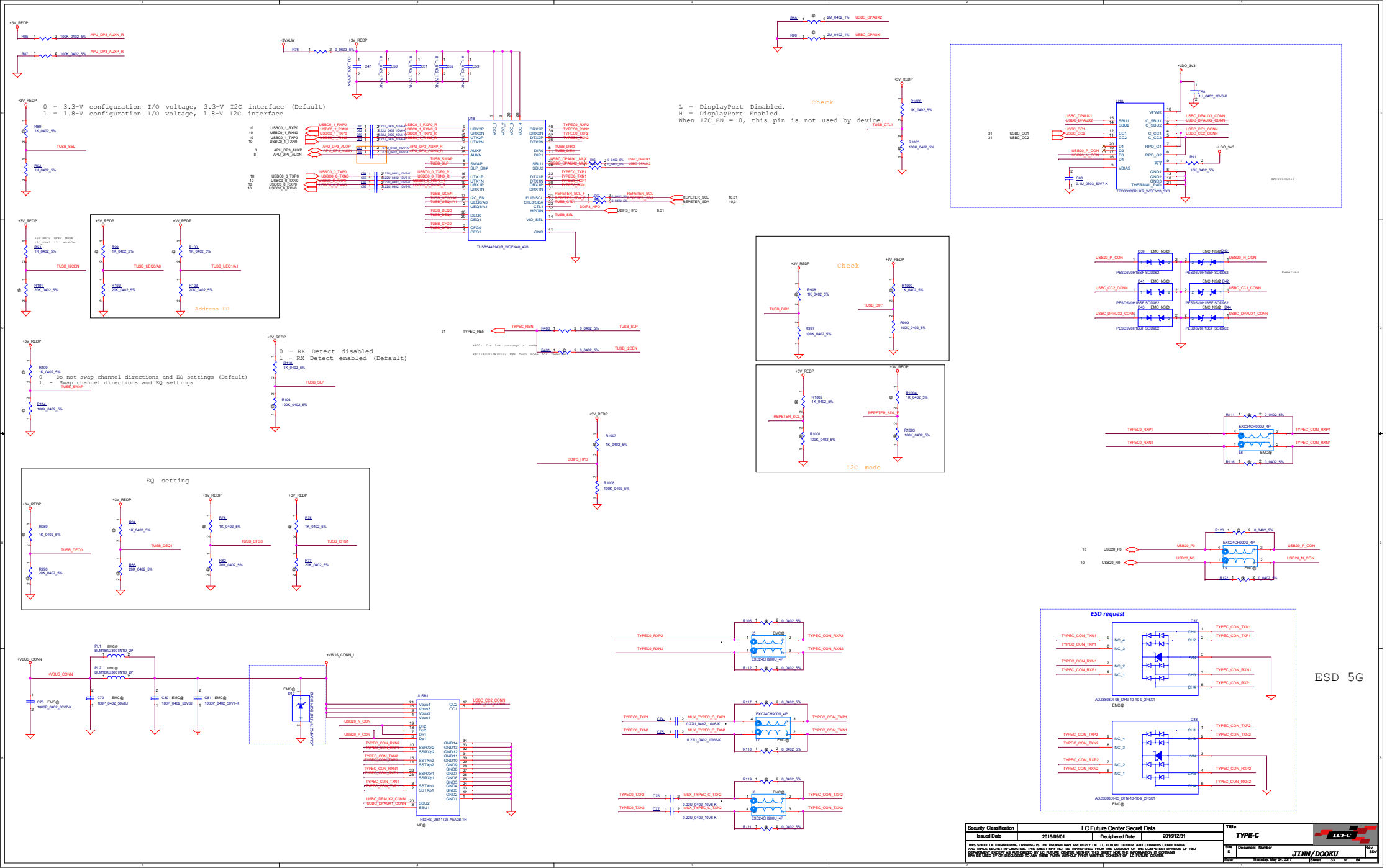


31
31
31

31
31
31

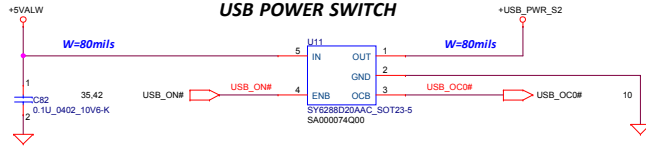
SNK_PS_EN need to check SNK_PS_EN's behavior

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/01/12	Deciphered Date	2016/01/12	RTS5455/POWER SWITCH	
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Size	Document	Number	EE480 NM-B421		Rev
Date:	Thursday, May 04, 2017	Sheet	32	of	64

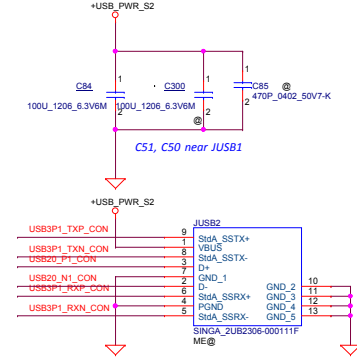
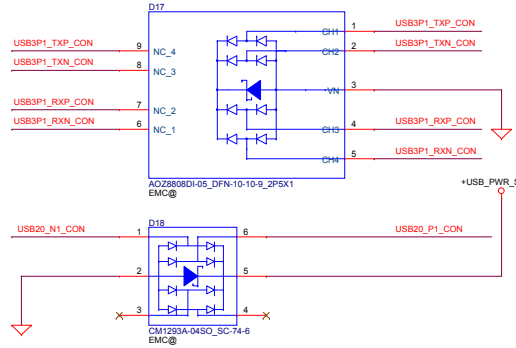
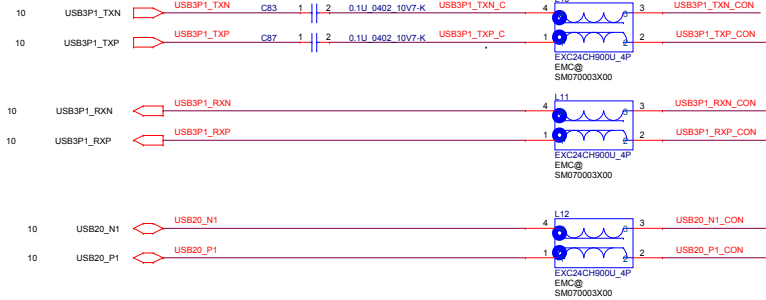


On Board (LEFT-Front)

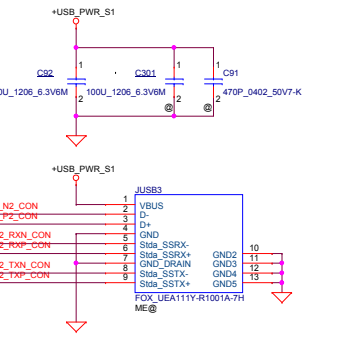
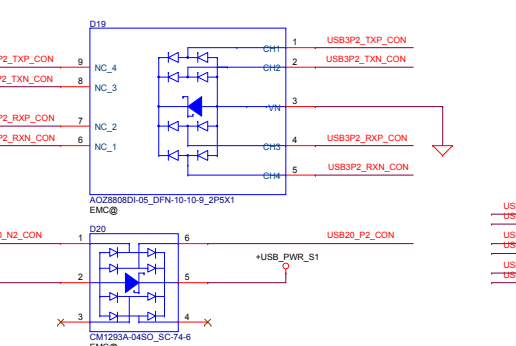
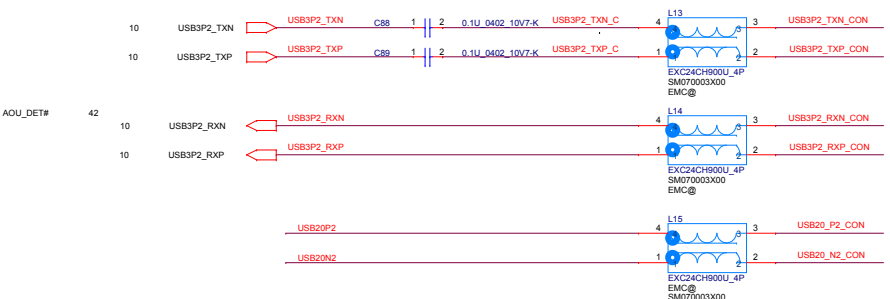
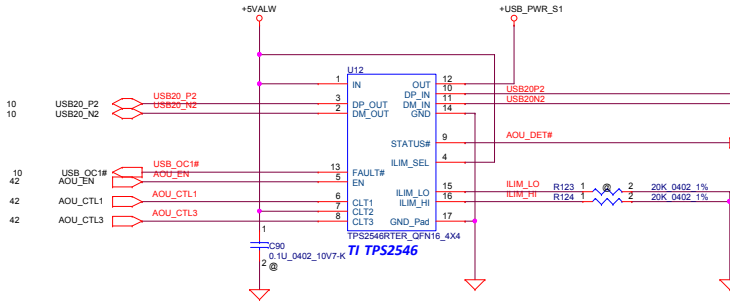
USB POWER SWITCH



Vendor	LCFC P/N	Description
SILGERY	SA000074Q00	S IC SY6288D20AAC SOT23 5P POWER SWITCH
GMT	SA000079400	S IC G517F2T111U SOT-23 5P POWER SWITCH



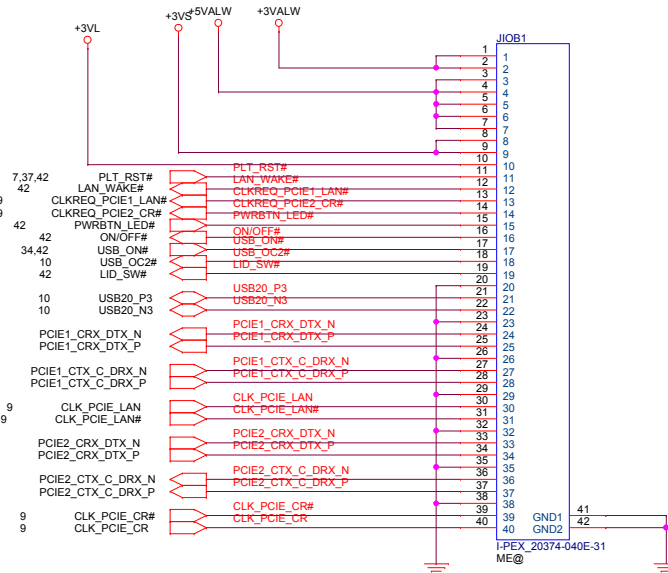
On Board (LEFT-Back)



CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCB OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

IO_40_Pin conn


USB2.0
GBE LAN PHY
Card Reader



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Issued Date	2015/01/12	Deciphered Date
		2016/01/12
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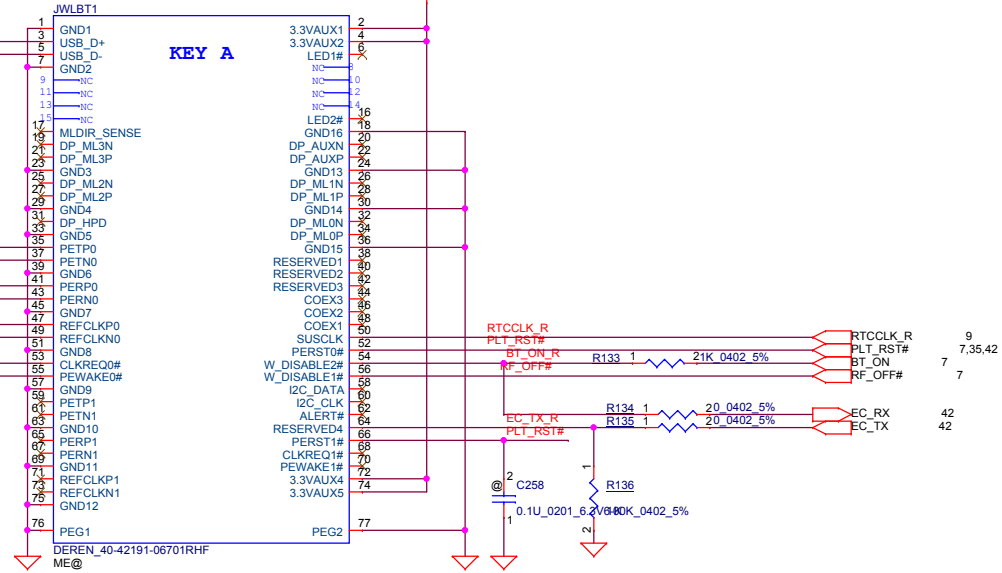
Title		
IO BOARD CONN		
Size	Document Number	Rev
Custom		SDV
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Issued Date	2015/10/5	Deciphered Date	2014/12/05	Switch		
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				Custom	JINN/DOOKU	SDV
				Date:	Thursday, May 04, 2017	Sheet 36 of 64

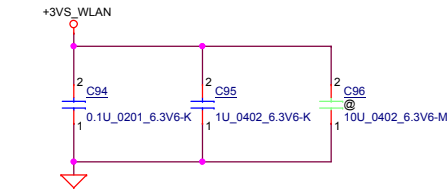
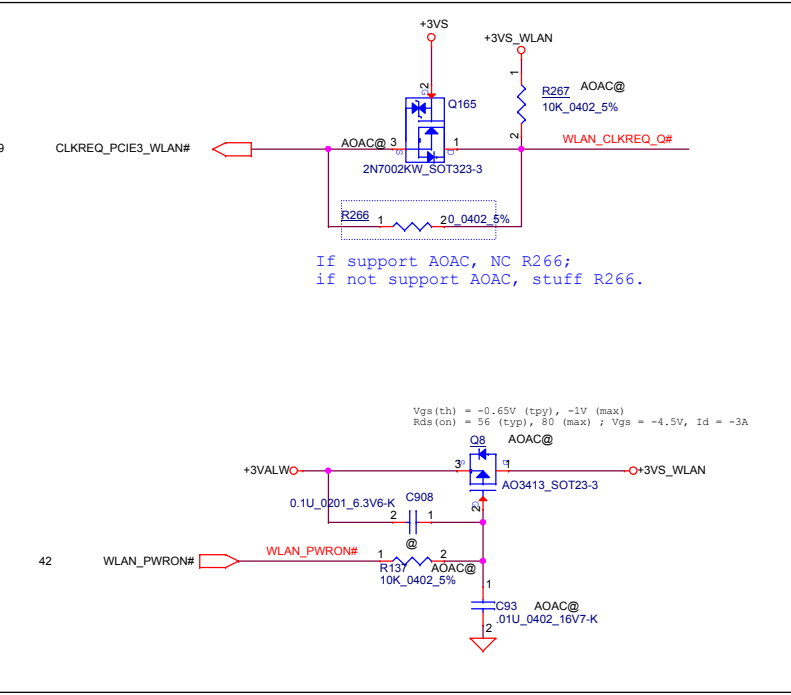
TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR

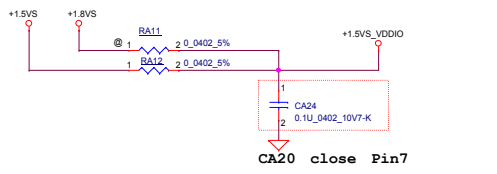
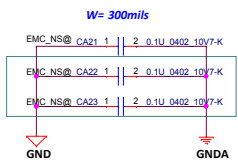
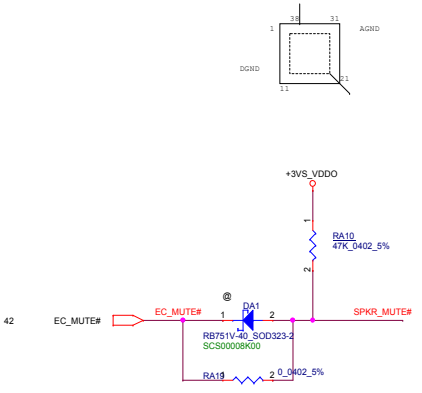
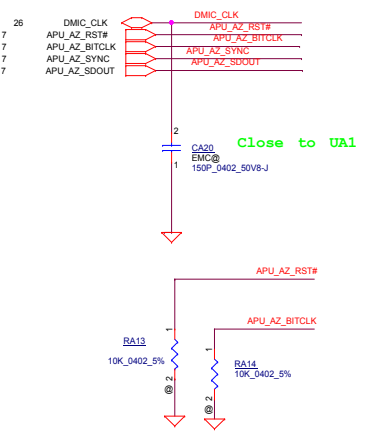
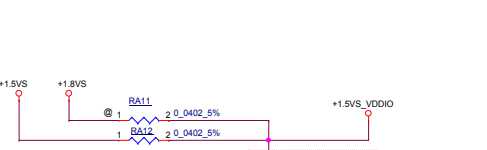
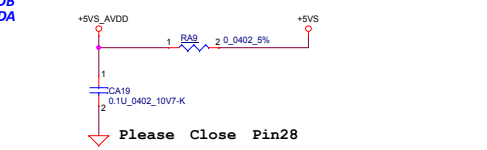
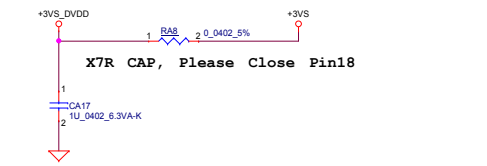
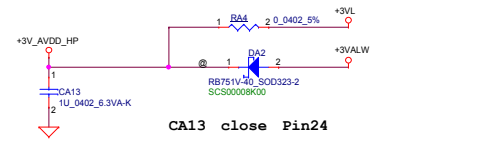
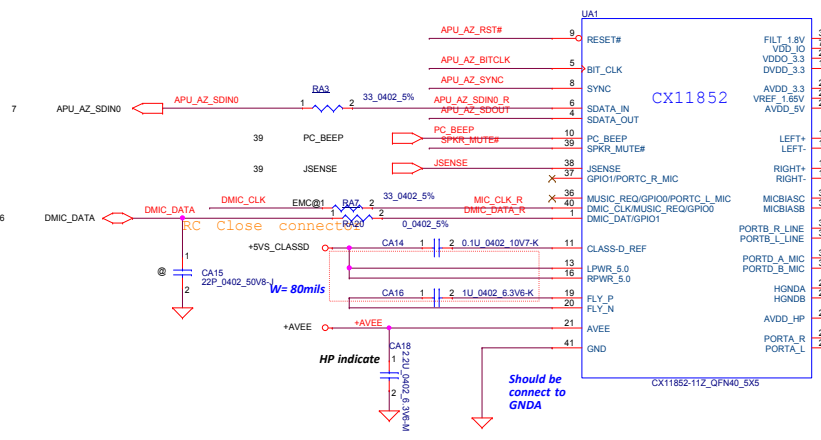
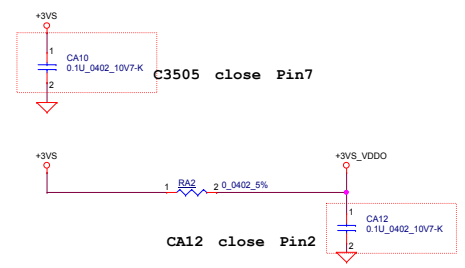
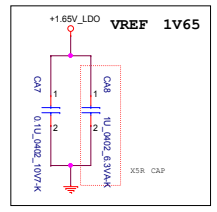
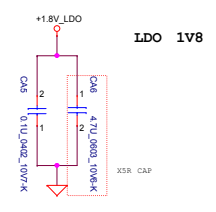
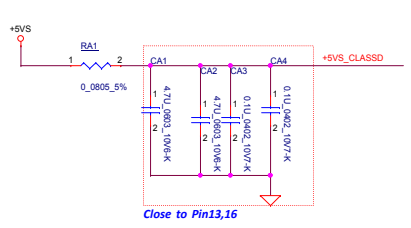


PLACE NEAR J32

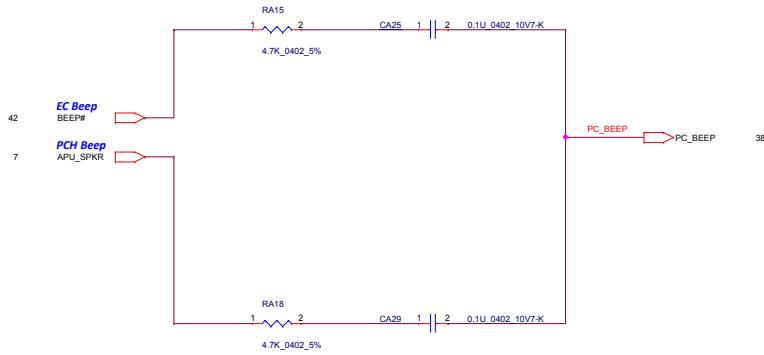
CHECK 0324



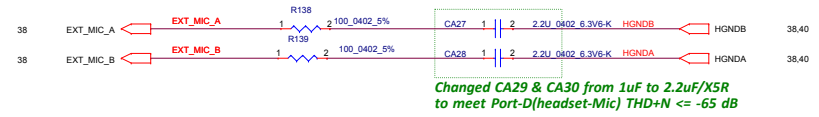
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Issued Date	2015/11/02	Deciphered Date	2015/08/10	
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Size	Document Number	JINN/DOOKU		SDV
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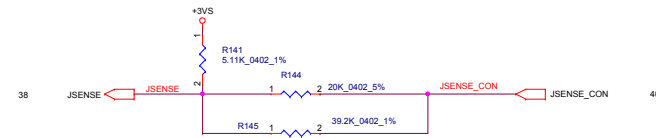
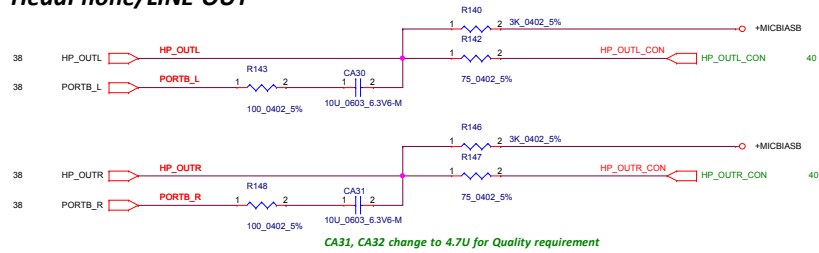
PC BEEP



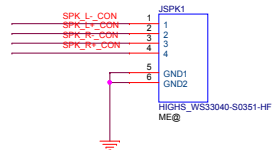
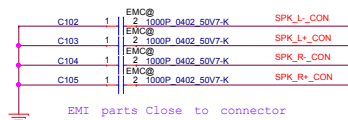
EXT. MIC/LINE IN Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A



HeadPhone/LINE OUT



SPK CONN.



Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/1/02	Deciphered Date	2015/8/10

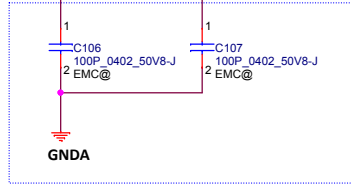
AUDIO CONNECTOR		Rev
Size	Document Number	Rev
Quantity	C	5
Date:	Thursday, May 14, 2017	Sheet 39 of 64

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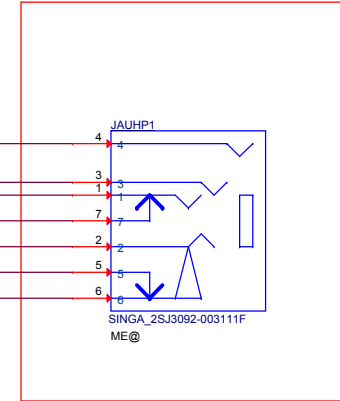


JINN/DOOKU

38,39 HGND B ← HGND B
 38,39 HGND A ← HGND A
 HP_OUTL_CON ← HP_OUTL_CON
 39 HP_OUTR_CON ← HP_OUTR_CON
 39 JSENSE_CON ← JSENSE_CON

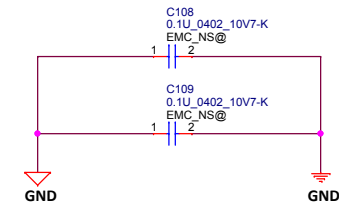
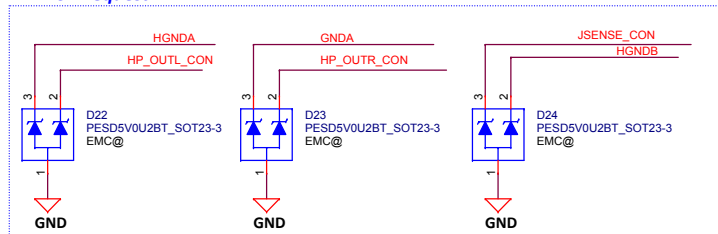


Vendor suggestion. Reserve for EMI.
 Close to JAUHP.

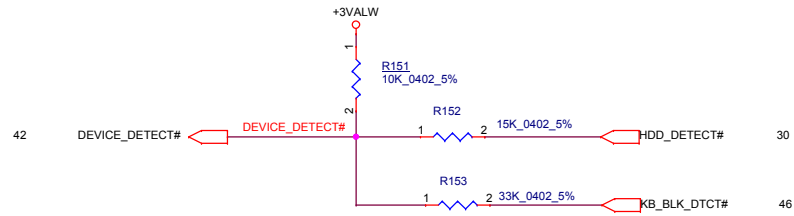


NEED CHECK PIN DEFINE

ESD request



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Issued Date	2015/11/02	Deciphered Date	2015/8/10	
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Size	Document Number	JINN/DOOKU		Rev
Custom				SDV
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Add KB DETECT Ned check

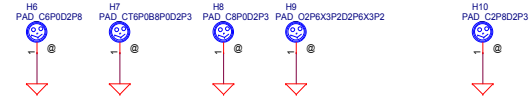
Vcc	3.3V															
R409	10K +/- 1%															
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V	2.87V	0.26V	1.82V	2.27V	2.45V	2.00V	1.64V	1.558V		
HDD_DETECT#	V	V	V	X	X	X	X	V	V	X	X	X	V	V		
KB_BLK_DTCT#	X	V	X	X	V	X	X	V	X	V	X	V	X	V		
	X	X	V	V	X	X	X	V	X	X	V	V	V	X		
	X	X	X	X	X	X	V	X	V	V	V	V	V	V		

Screw Hole

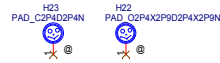
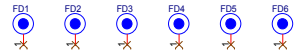
CPU



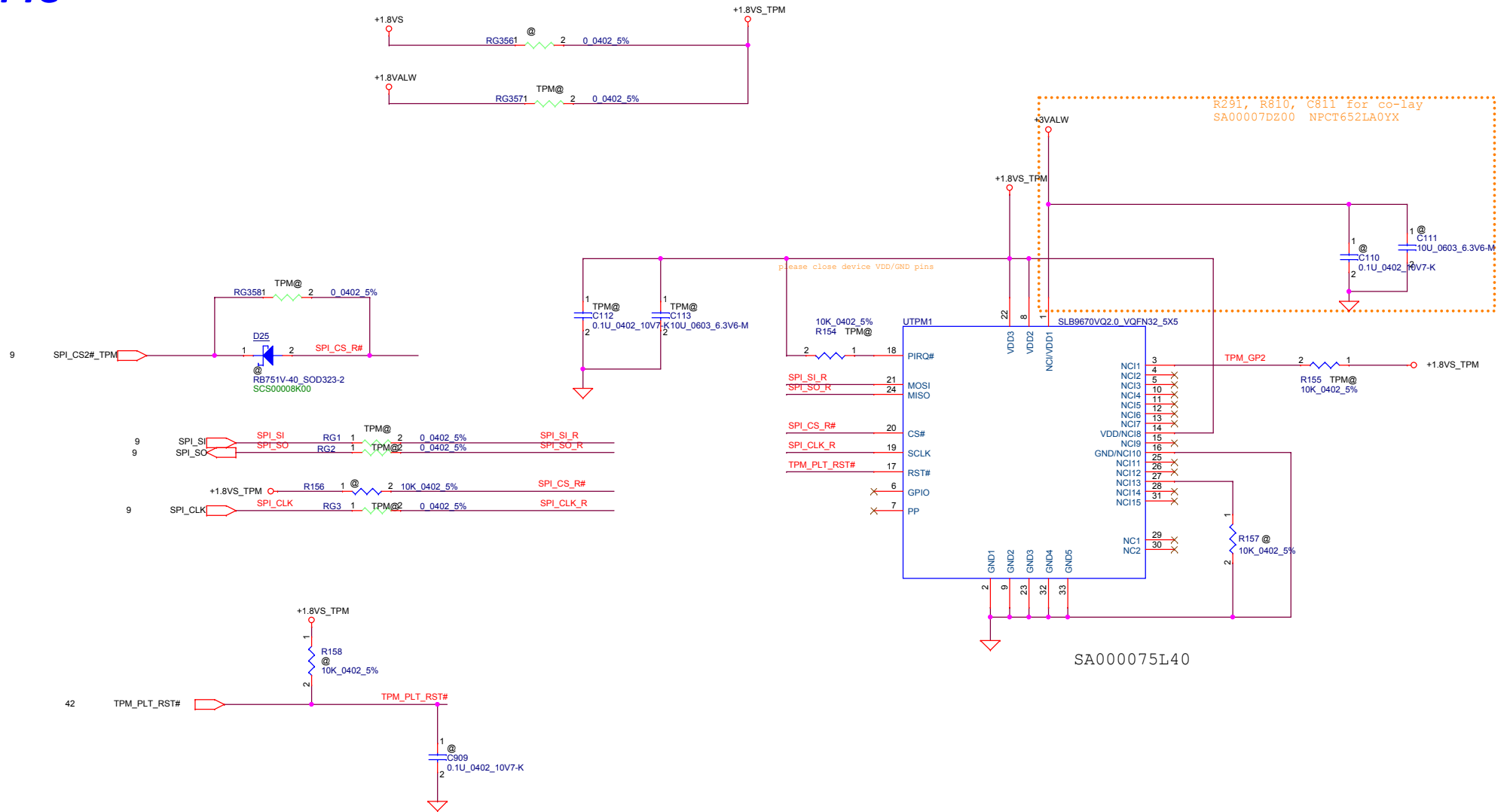
WLNN



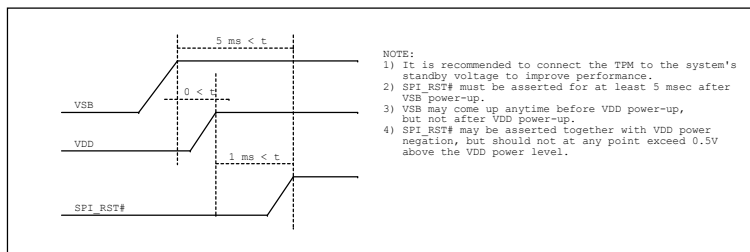
PCB Federal Mark PAD




TPM IC



NOTE:
Check timing sequence in SDV phase.



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Size	Document Number	JINN/DOOKU		Rev
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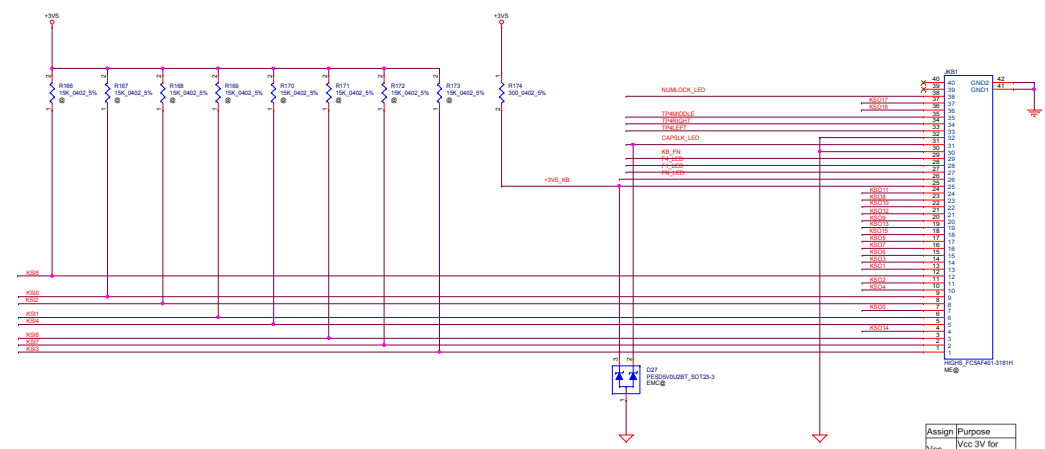
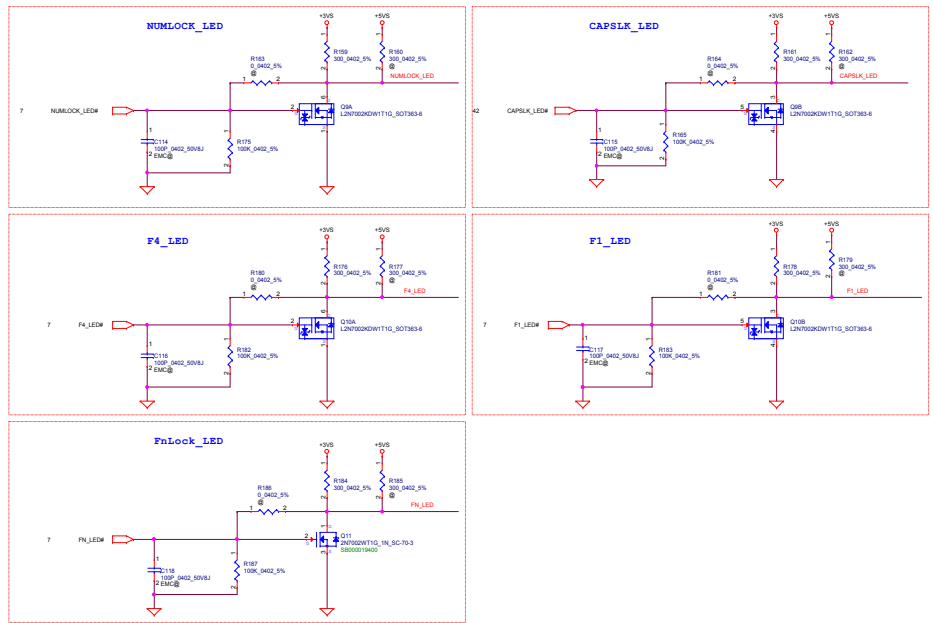
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/11/02	Deciphered Date	2015/8/10	TOUCH PAD/FPR/Smart Card	
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<small>DATE: Thursday, May 14, 2017</small>				<small>Sheet 45 of 54</small>	



JINN/DOOKU



Keyboard CONN



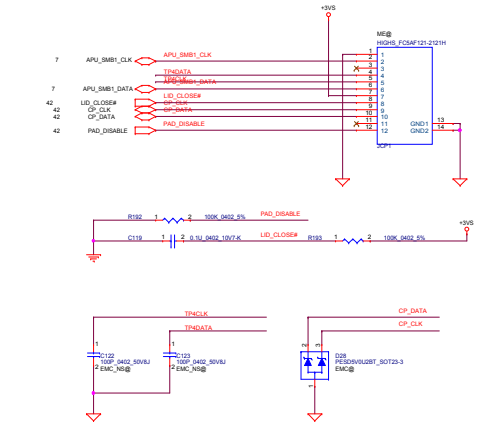
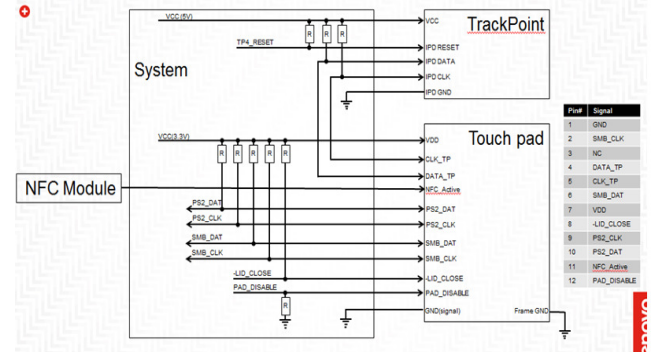
Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	LED4
30	LED5
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLk
LED5	LED for NumLock

Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Click Pad

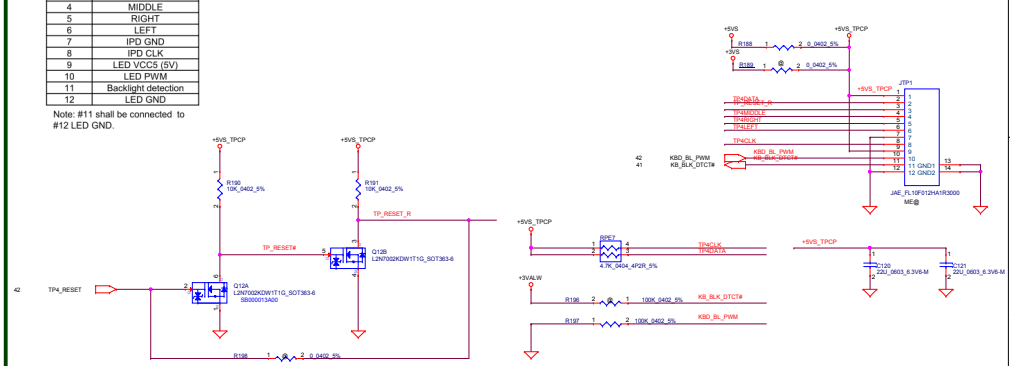
反



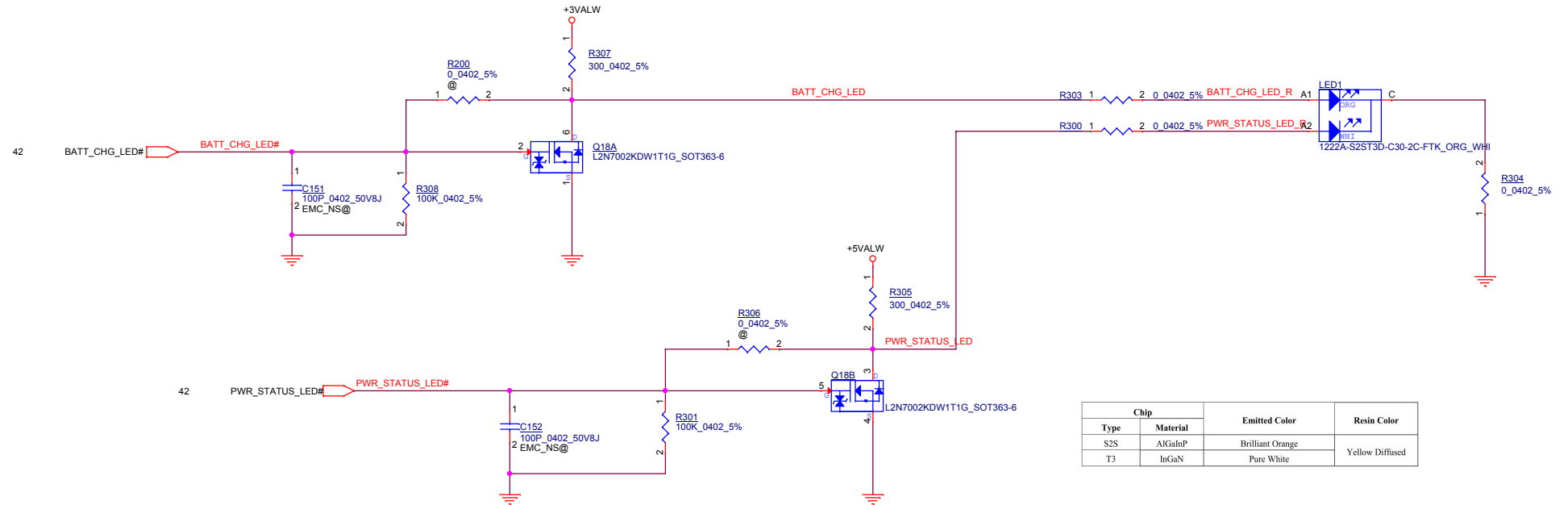
Track Point

Pin #	Assign
1	VCC5 (5V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND

Note: #11 shall be connected to #12 LED GND.



POWER ADAPTER Bi-COLOR (ORANGE/WHITE)

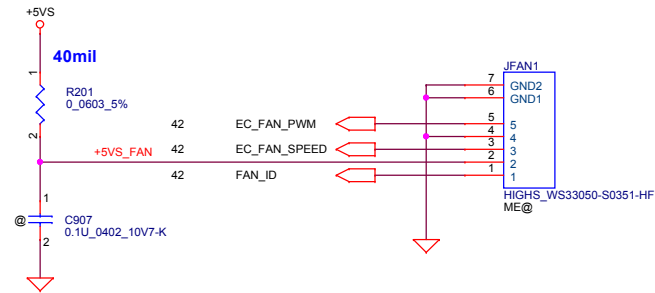



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Issued Date	2015/11/02	Deciphered Date	2015/8/10
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Title		JINN/DOOKU	Rev SDV
POWER LED			
Size	Document Number		
Custom			
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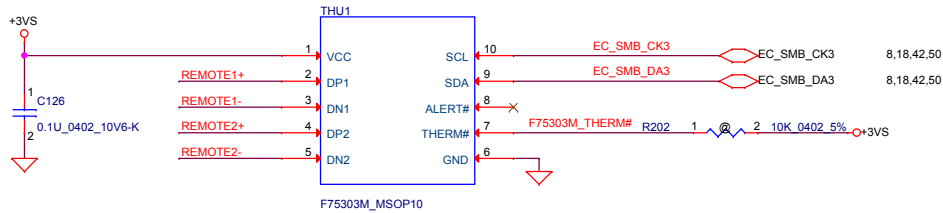


FAN CONN.



Security Classification	LC Future Center Secret Data		Title		
Issued Date	2015/11/02	Deciphered Date	2015/8/10		FAN CONNECTOR
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**Thermal Sensor
placed near by VRAM**

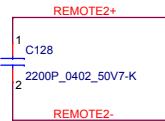
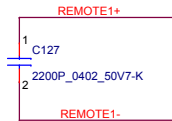


Address 1001_101xb

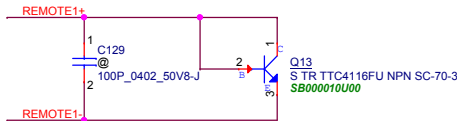
Internal pull up 1.2K to 1.5V

R for init i d t her n d s h ut do w n t e mp

Close to U1

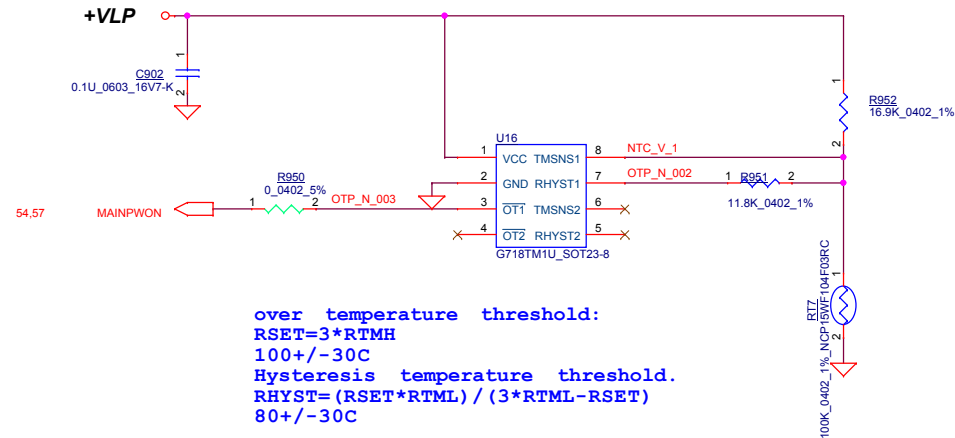
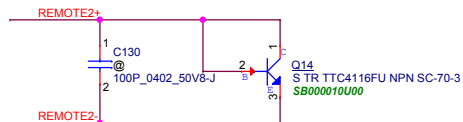


Close to +VCC_CORE




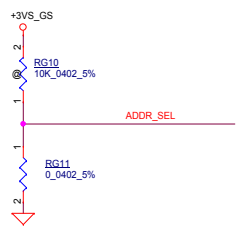
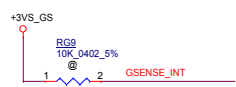
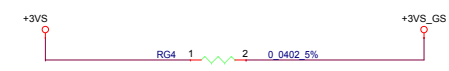
**REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"**

Close JDIMM1&JDIMM2

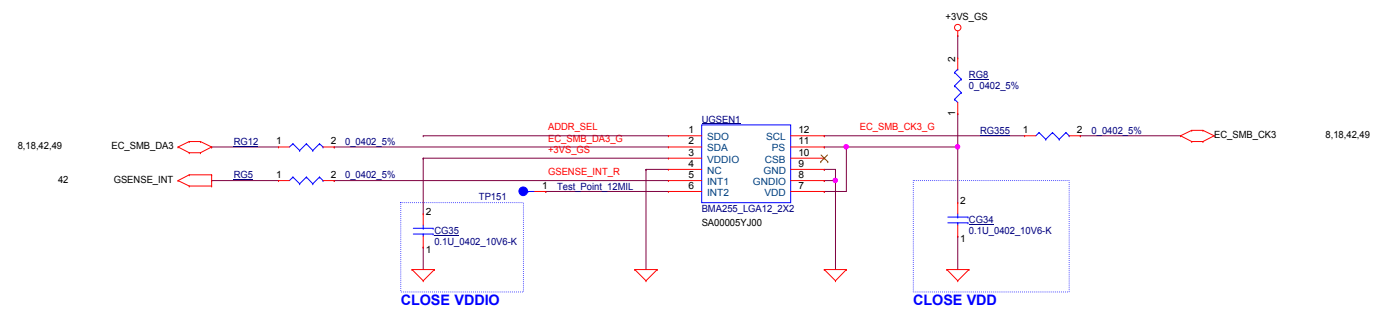


**over temperature threshold:
RSET=3*RTMH
100+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML) / (3*RTML-RSET)
80+/-30C**

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	Thermal Sensor	
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APS G-Sensor

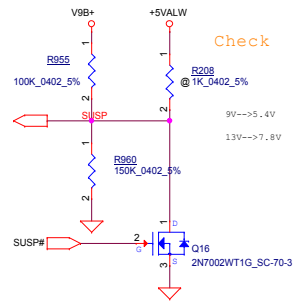


Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00

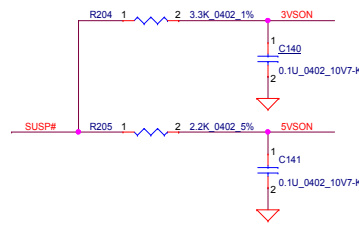
P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

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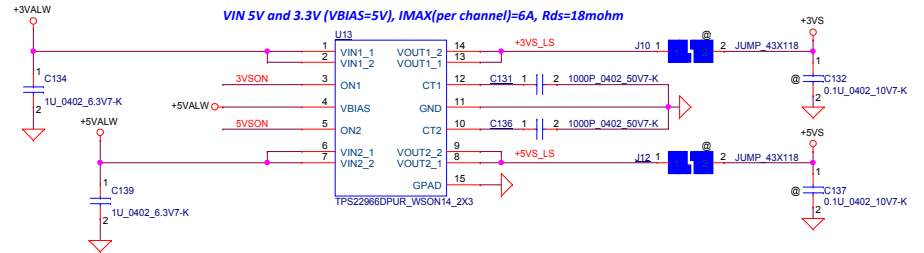
Check 5VLP



Check



**3/5VS load Switch
+5VALW To +5VS
+3VALW To +3VS**

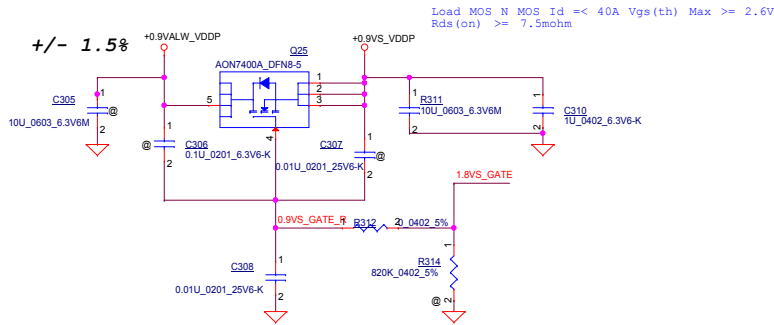


VIN 5V and 3.3V (VBIAS=5V), I_{MAX}(per channel)=6A, R_{DS}=18mohm

+0.9VALW_VDDP to +VDDP 10A request

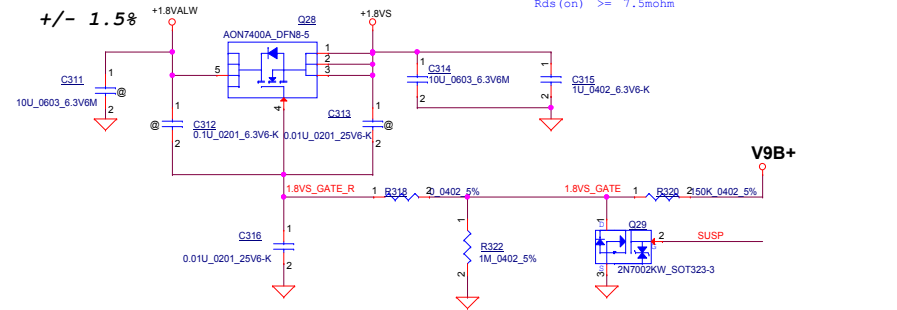
V9B+ 9V--13V

SB000013Q00, SB00001B300 AON7400



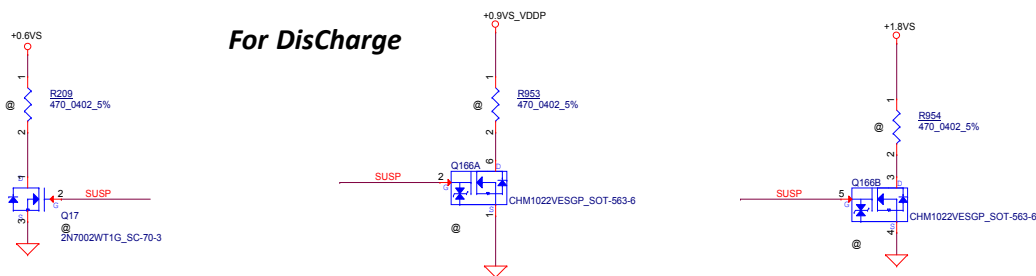
Load MOS N MOS Id <= 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

+1.8VALW to +1.8VS 2A request

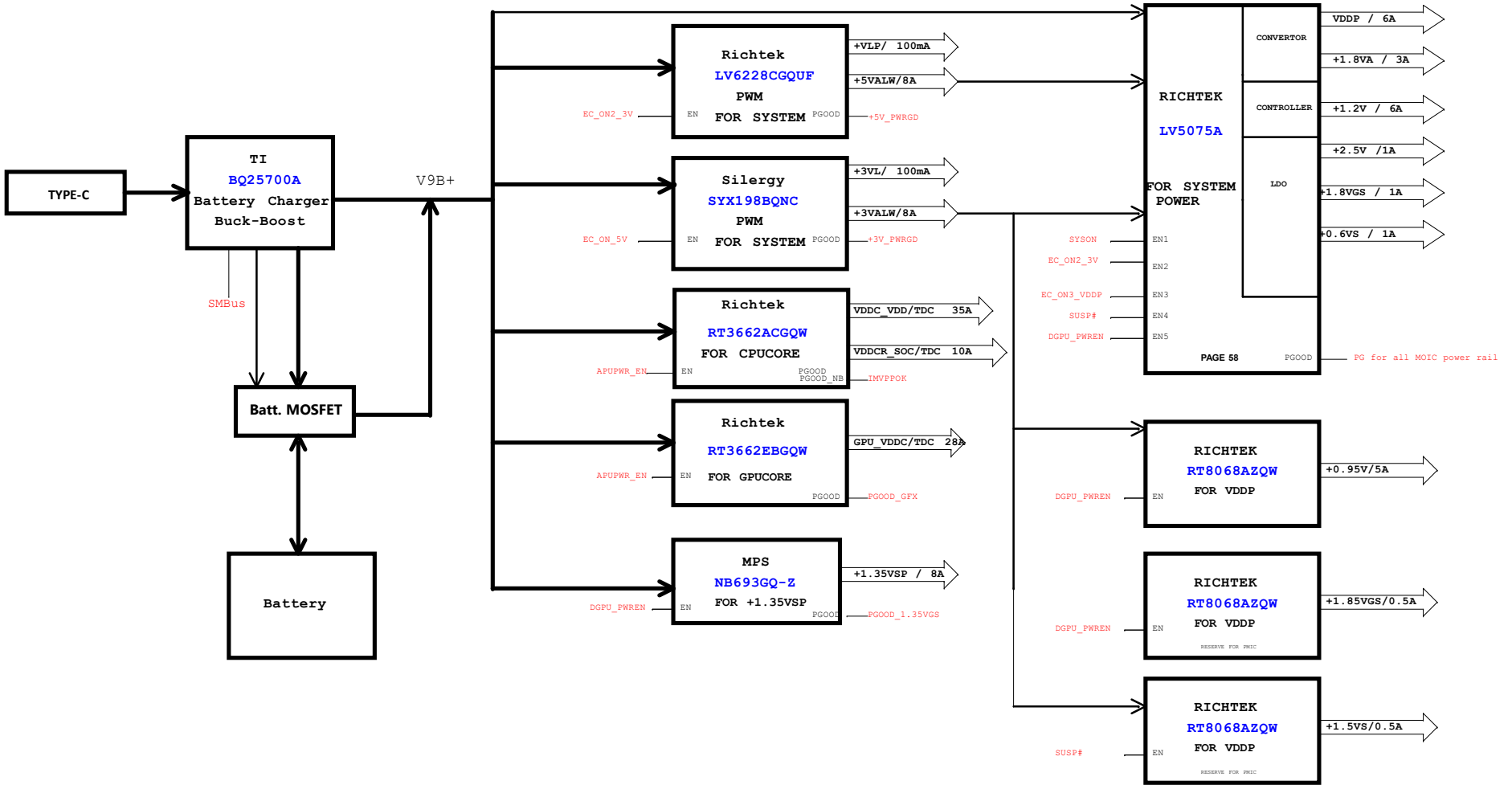


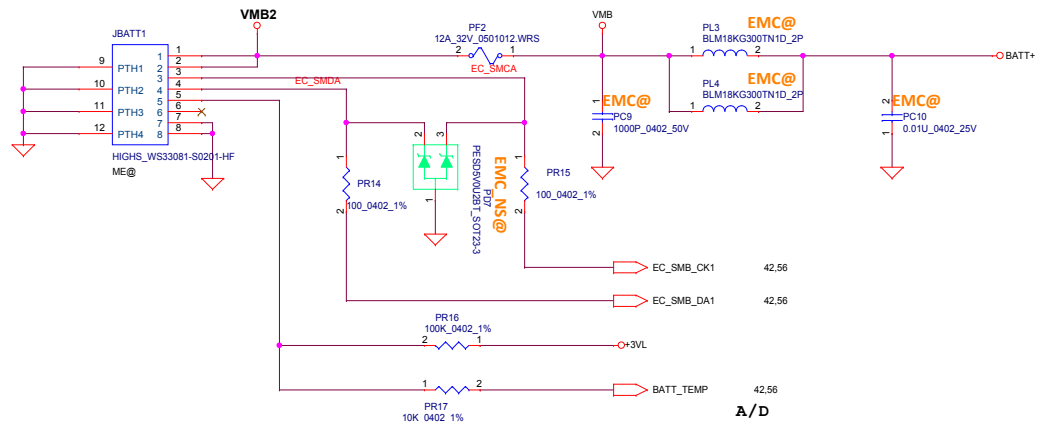
Load MOS N MOS Id <= 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

For DisCharge




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	3VS/5VS/1.1VS/VDDIO_RUN	
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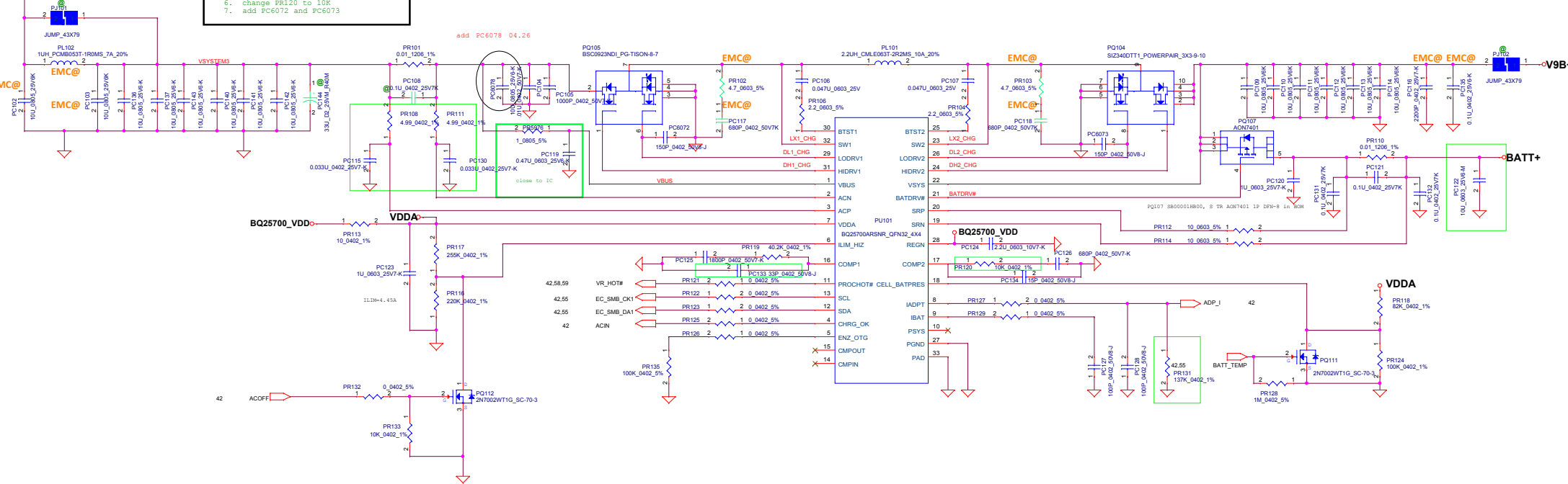


A/D

<Variant Name>

Security Classification	LC Future Center Secret Data		Title	 BATTERY CONN/PH1	Size Custom Document Number JINN/DOOKU Rev 1.0
Issued Date	2017/03/14	Deciphered Date	2017/03/01		
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VSYSTEM2



follow TI change:
 1. change PC115 and PC130 to 0.0330
 2. change PR108 and PR111 to 4.990hm
 3. add PR5976
 4. change PC133 to 33P
 5. change PR131 to 137K
 6. change PR120 to 10K
 7. add PC6072 and PC6073

add PC6078 04.26

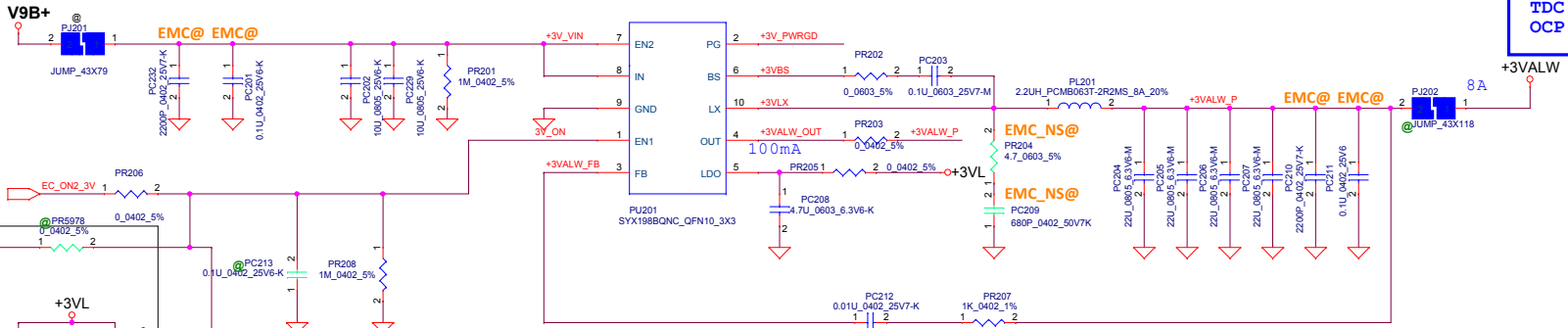
close to IC

<Variant Name>

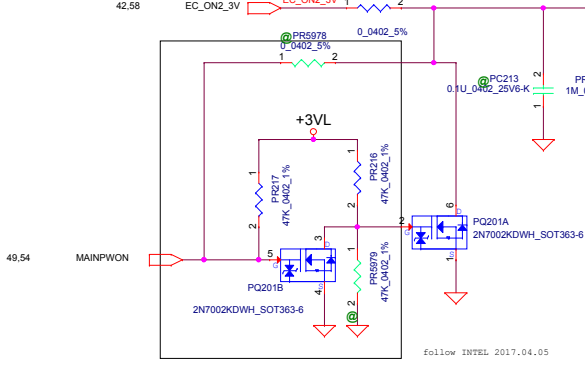
Security Classification	LC Future Center Secret Data		Title
Issued Date	2017/03/14	Deciphered Date	2017/03/01
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CHARGER

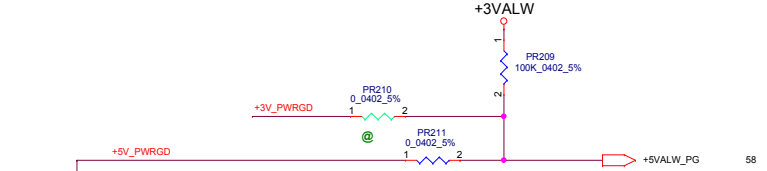
JINN/DOOKU



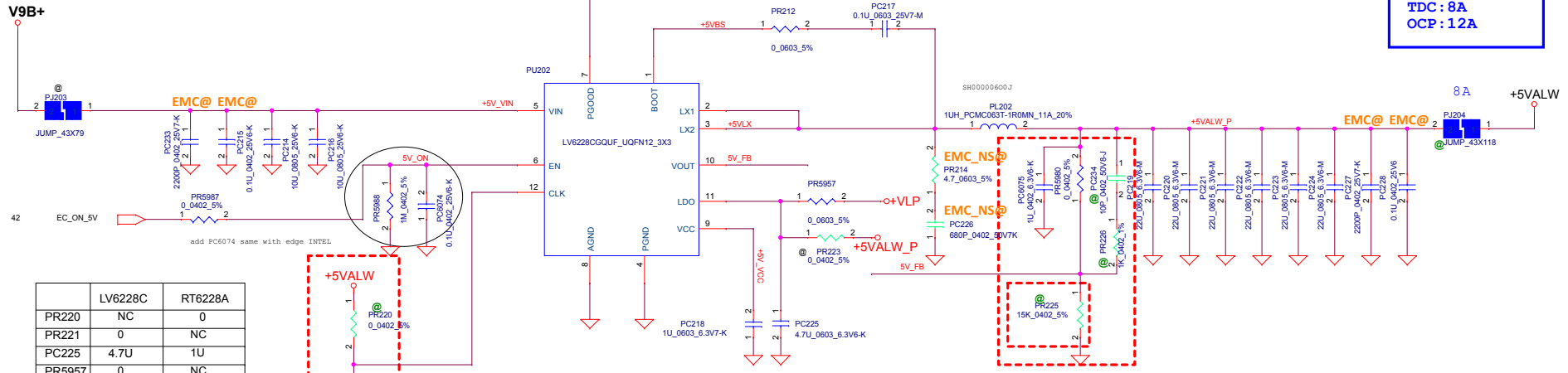
+3VALW
FSW=750 KHz
TDC : 8A
OCF : 11A



Follow INTEL 2017.04.05



+5VALW
FSW=750 KHz
TDC : 8A
OCF : 12A



add PC6074 same with edge INTEL

FOLLOW INTEL 2017.04.14

FOLLOW INTEL 2017.04.14

	LV6228C	RT6228A
PR220	NC	0
PR221	0	NC
PC225	4.7U	1U
PR5957	0	NC
PR223	NC	0
PR5980	0	115K
PR225	NC	15K
PC234	NC	10P
PR226	NC	1K
PC6075	1U	NC

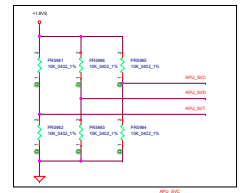
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Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/14	Deciphered Date	2017/03/01

Title	3VALWP/5VALWP		
Size	Document Number	Rev	1.0
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SVC	BVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V



3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

3662_VREF

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3662_VREF

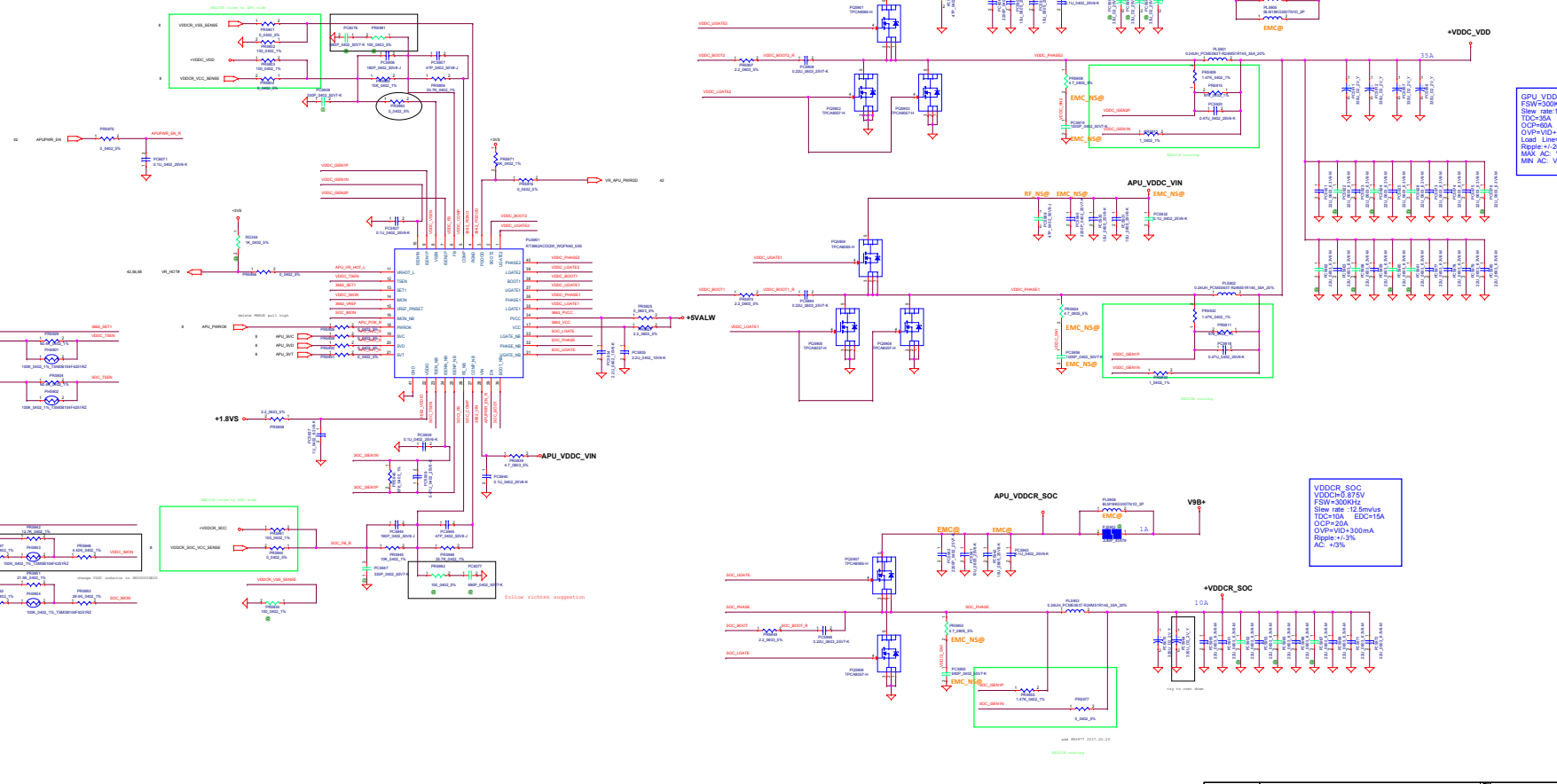
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3662_VREF

3662_VREF

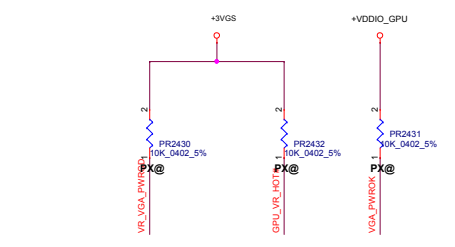
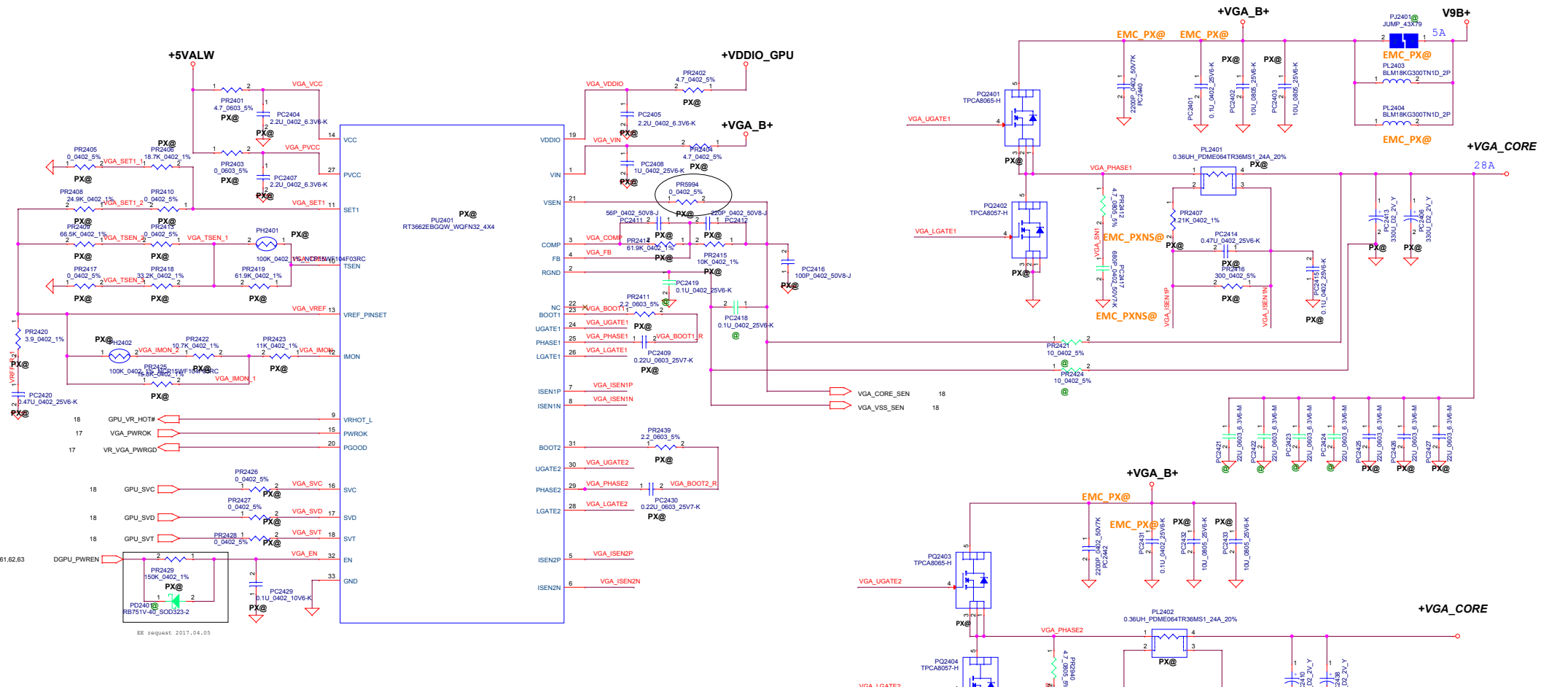
3662_VREF

3662_VREF

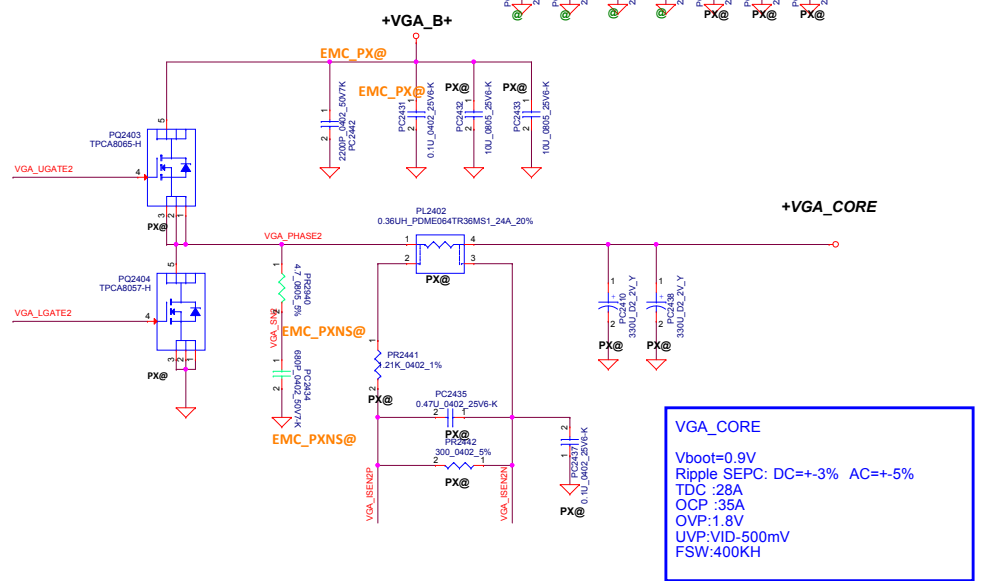


GPU_VDDC
FSW=300kHz
Slew rate: 12.5mV/us
TDC=35A EDC=45A
OC=70A
OVP=VID+300mV
Load Line=0.5mV/mA
Rpsle=+1.20mV
MAX AC: VID_VDDC +120mV
MIN AC: VID_VDDC -80mV

VDDCR_SOC
VDDCR=0.875V
FSW=300kHz
Slew rate: 12.5mV/us
TDC=15A EDC=15A
OC=20A
OVP=VID+300mV
Rpsle=+1.20mV
AC: +3%

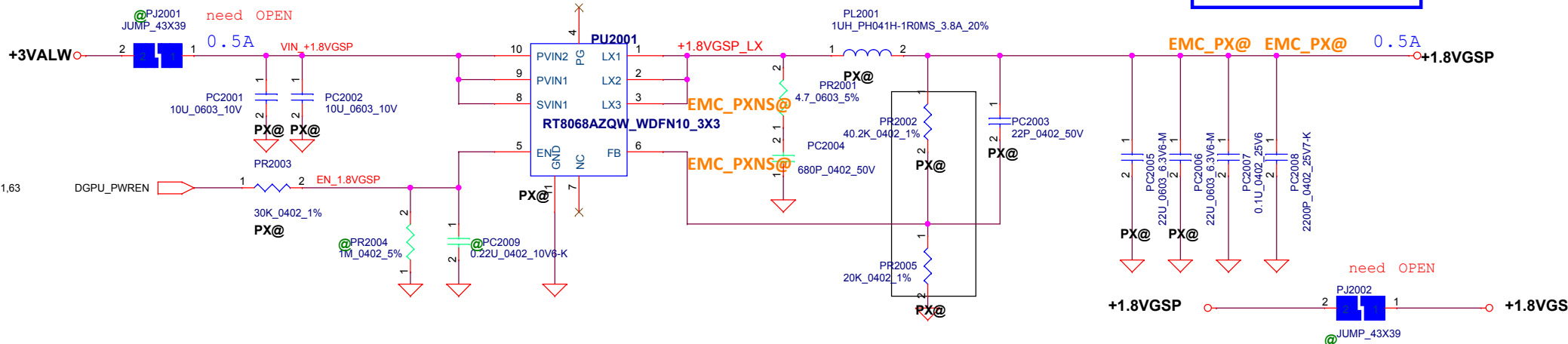


SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



VGA_CORE

Vboot=0.9V
 Ripple SEPC: DC=+3% AC=+5%
 TDC :28A
 OCP :35A
 OVP:1.8V
 UVP:VID-500mV
 FSW:400KH




Vout=1.8V± 3%
 TDC=0.5A
 Vset=1.806V± 3%
 OCP=3A
 Vref=0.6V
 FSW=1MHZ

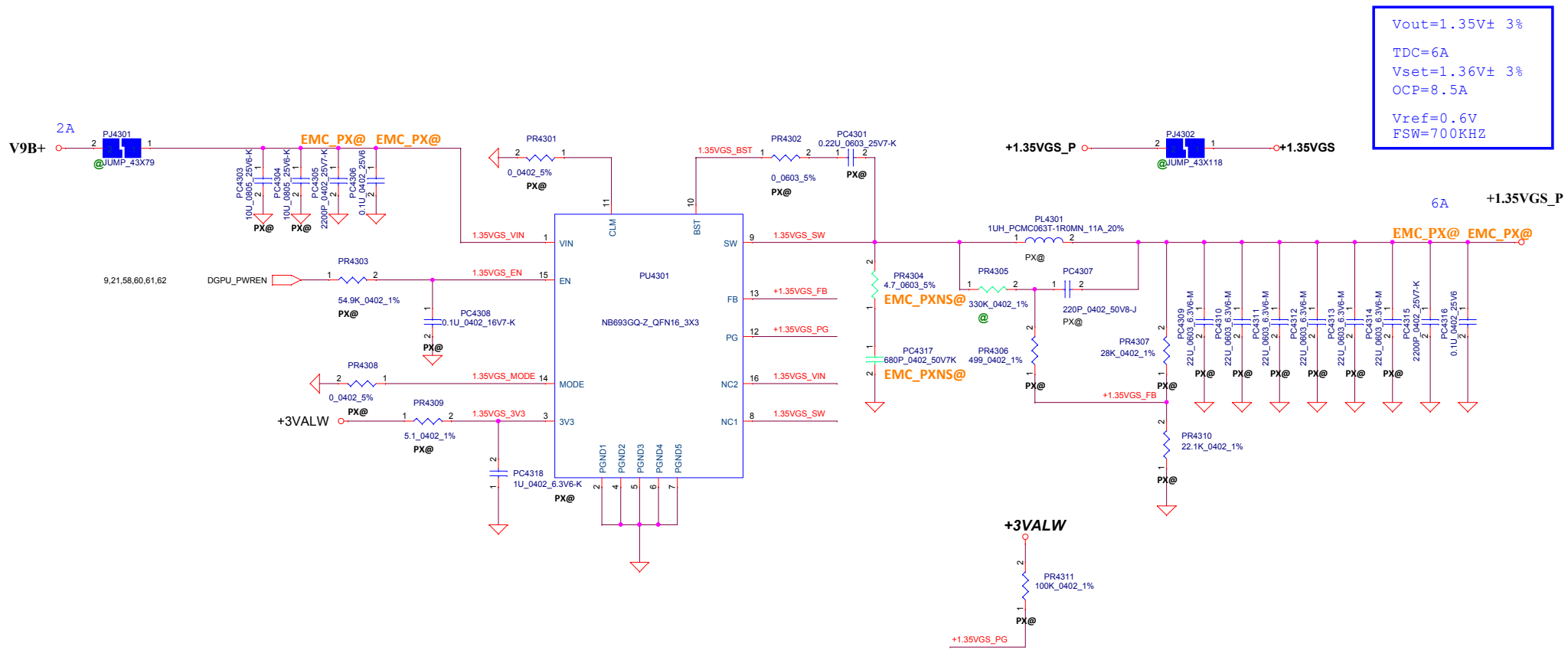
Reserve for PMIC

Security Classification	LC Future Center Secret Data		
Issued Date	2017/03/14	Deciphered Date	2017/03/01

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Title		
+1.8VGS		
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JINN/DOOKU



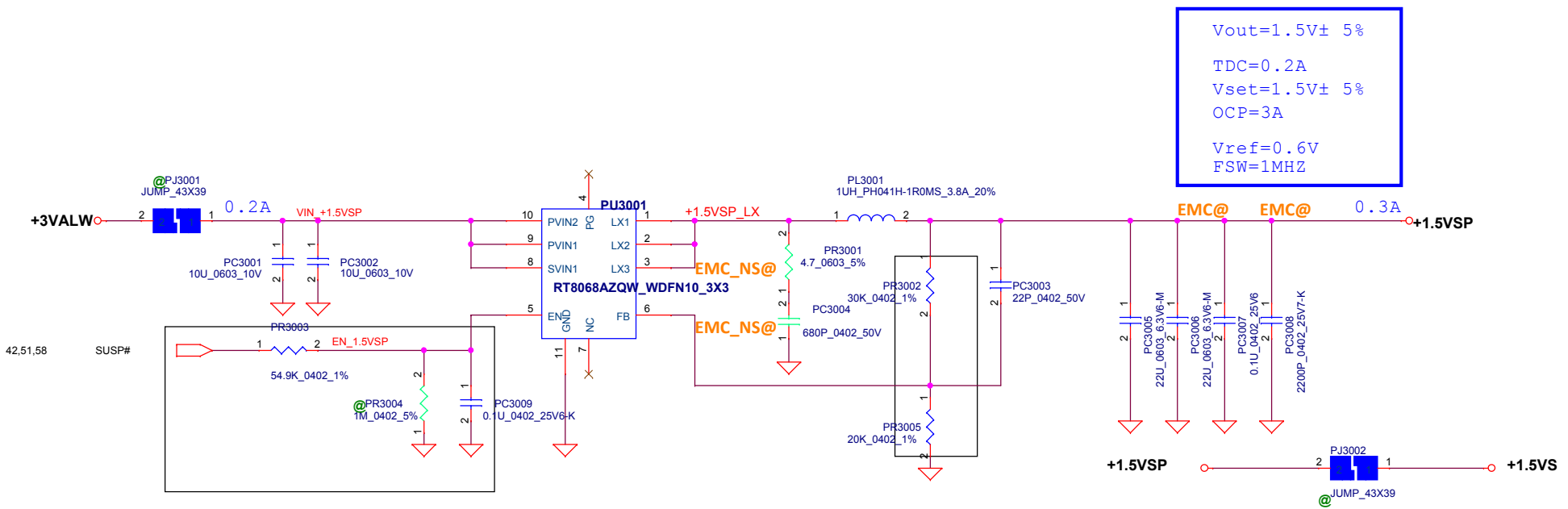
Vout=1.35V± 3%
 TDC=6A
 Vset=1.36V± 3%
 OCP=8.5A
 Vref=0.6V
 FSW=700KHZ

<Variant Name>

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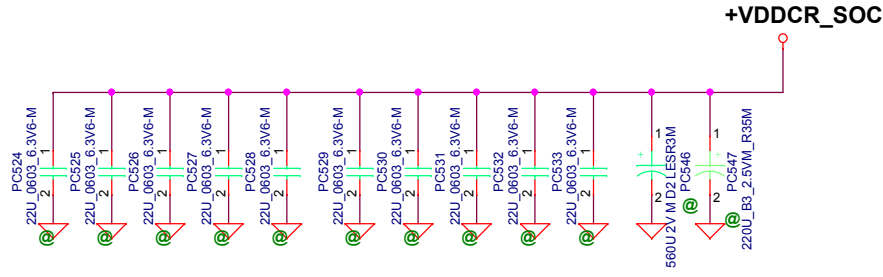
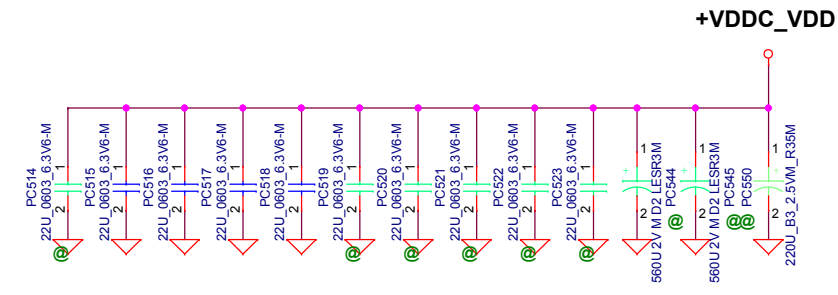
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