


LCFC Confidential

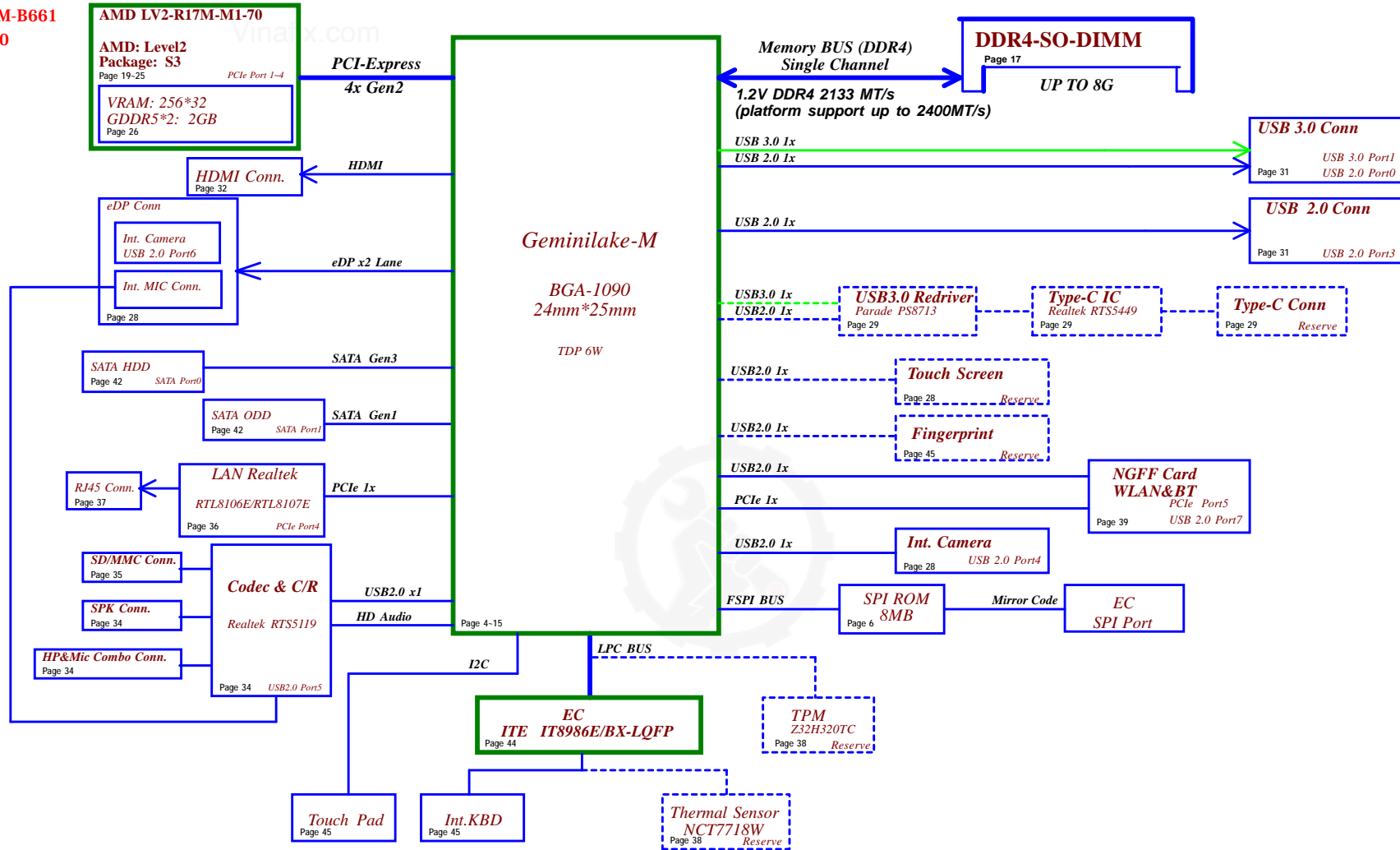
330-IGM M/B EG431/EG532 Schematics Document Intel Geminilake M-Processor with DDR4 + AMD LV2-R17M-M1-70 GPU

2018-03-02

REV:1.0

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2013/08/08	Deciphered Date	2014/01/21	Cover Page			
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					Date:	Friday, March 02, 2018	Sheet 1 of 60

LCFC confidential
File Name : TURING 4D&5D
Board Number : NM-B661
PN : DA600013W00



Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date
		2014/01/21

Title		
Block Diagram		
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Voltage Rails (0--> Means ON , X--> Means OFF)

Power Plane / State	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.2V	+5VS +3VS +1.8VS +1.05VS +0.6VS +CPU_CORE +VNN
S0	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0IX(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCIE PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0			
1	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
2			
3			
4	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB3.0
	1	Type C(RSVD)
USB 2.0	0	Type C(USB 2.0)(RSVD)
	1	USB3.0 (2.0)
	2	Touch Screen(RSVD)
	3	USB2.0
	4	Finger Print(RSVD)
	5	CARD READER
	6	CAMERA
7	BT	

DDI PORT LIST

Port	Device
DDI0	HDMI
DDI1	NC
eDP	eDP

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

EC SM Bus0 address

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery	0x16	Thermal Sensor	0x98(reserve)	DDR SO-DIMM	0xA0
		Charger	0x12			Wlan	Rsvd

I2C4/I2C7 Bus address (Touch Pad)

Device	Address
Slave	0x15
Descriptor	0x0001

RCOMP RESISTOR REQUIREMENT

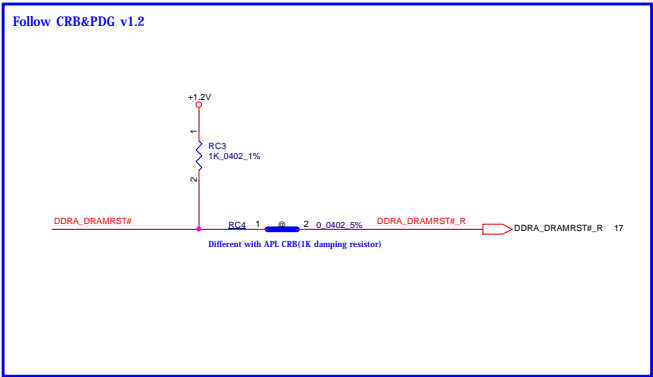
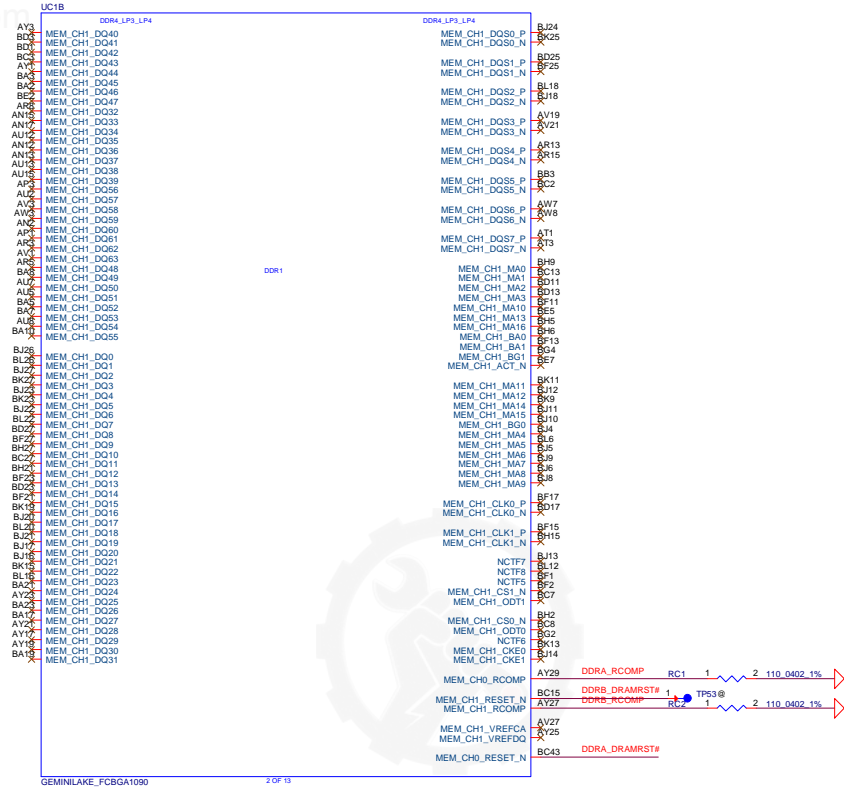
INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
Memory	MEM_CH0_RCOMP	RC1	110 +/-1%
	MEM_CH1_RCOMP	RC2	110 +/-1%
USB2	USB2_RCOMP	RC64	113 +/-1%
USB3/PCIe/SATA	PCIe2_USB3_SATA3_RCOMP_P/N	RC63	100 +/-1%
PCIe Refclk	PCIe_REF_CLK_RCOMP	RC62	56 +/-1%
DP/eDP*/HDMI*	EDP_RCOMP_P/N	RC79	100 +/-1%
MDS1	MDS1_RCOMP	RC78	150 +/-1%
CNV1	CNV_WT_RCOMP	RC48	150 +/-1%
SMBUS/GPIO/EMMC for all 1.8V only and 1.8V mode operation of 1.8/3.3V CFIO interfaces	EMMC_RCOMP	RC20	200 +/-1%

BOM Structure Table


BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
EMC_14@	EMC 14" part
EMC_USB@	EMC USB TVS part
1284_EMC@	1284 LAN Transformer EMC part
CD@	Cost Down part
RF@	For RF part
RF_NS@	For RF un-stuff part
RF_PXNS@	For RF GPU un-stuff part
14@	For 14" part
15@	For 15" part
8106E@	8106E LAN SKU part@
8107E@	8107E LAN SKU part@
1284@	1284 LAN Transformer part
8400M@	8400M LAN Transformer part
PX@	Discrete GPU SKU part
TOPAZ@	TOPAZ dGPU SKU part
EXO@	R16M-MI-30 dGPU SKU part
UMA@	UMA SKU ID part
TMSEN@	Thermal Sensor part
TMSEN_PX@	dGPU Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
NUVOTON@	NOVOTON TPM part
NATIONZ@	NATIONZ TPM part
TS@	Touch Screen part
FP@	Finger Print part
KBL@	KB Backlight part
UART@	UART debug part
RTCST@	Clear RTCST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N4100@	GLK N4100 CPU part
N4000@	GLK N4000 CPU part
N5000@	GLK N5000 CPU part
M8GX2@	Micron 8GbX2 VRAM X76 SKU
S8GX2@	Samsung 8GbX2 VRAM X76 SKU
H8GX2@	Hynix 8GbX2 VRAM X76 SKU
M8G@	Micron 8GbX2 VRAM
S8G@	Samsung 8GbX2 VRAM
H8G@	Hynix 8GbX2 VRAM
PCB@	MB PCB part
ODD@	ODD PCB part

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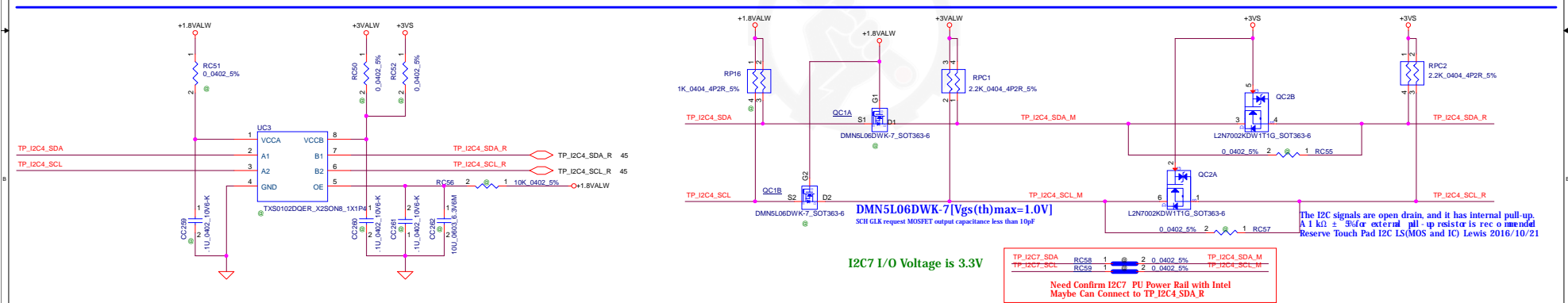
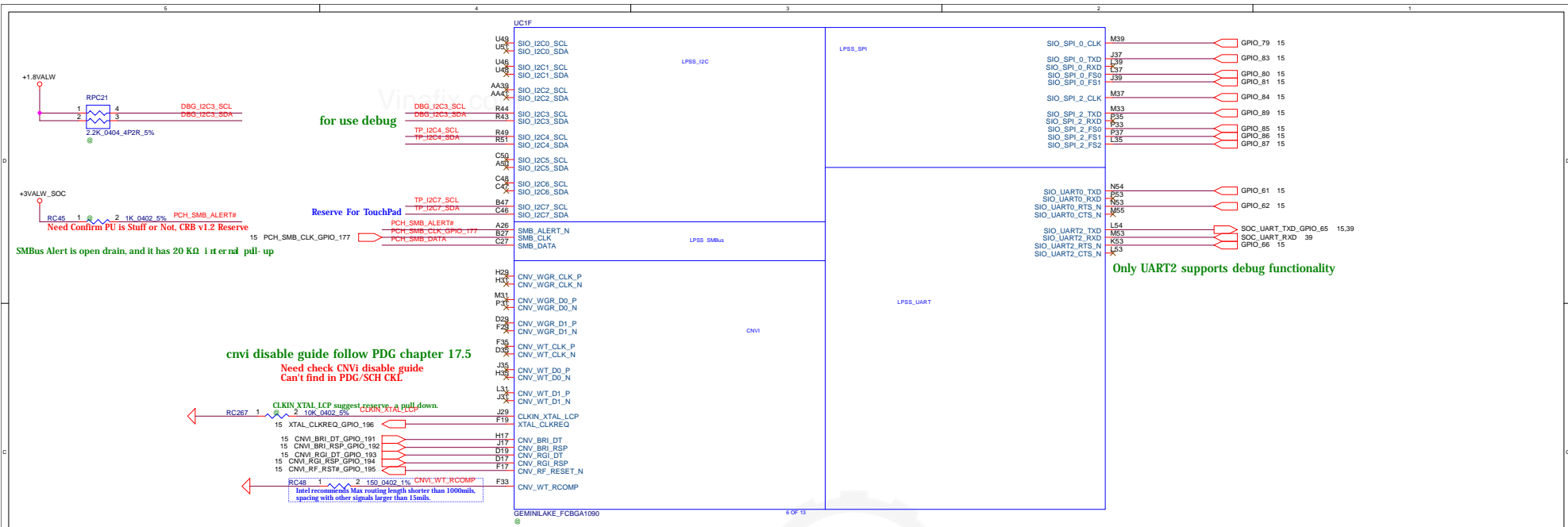


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EG431/EG532

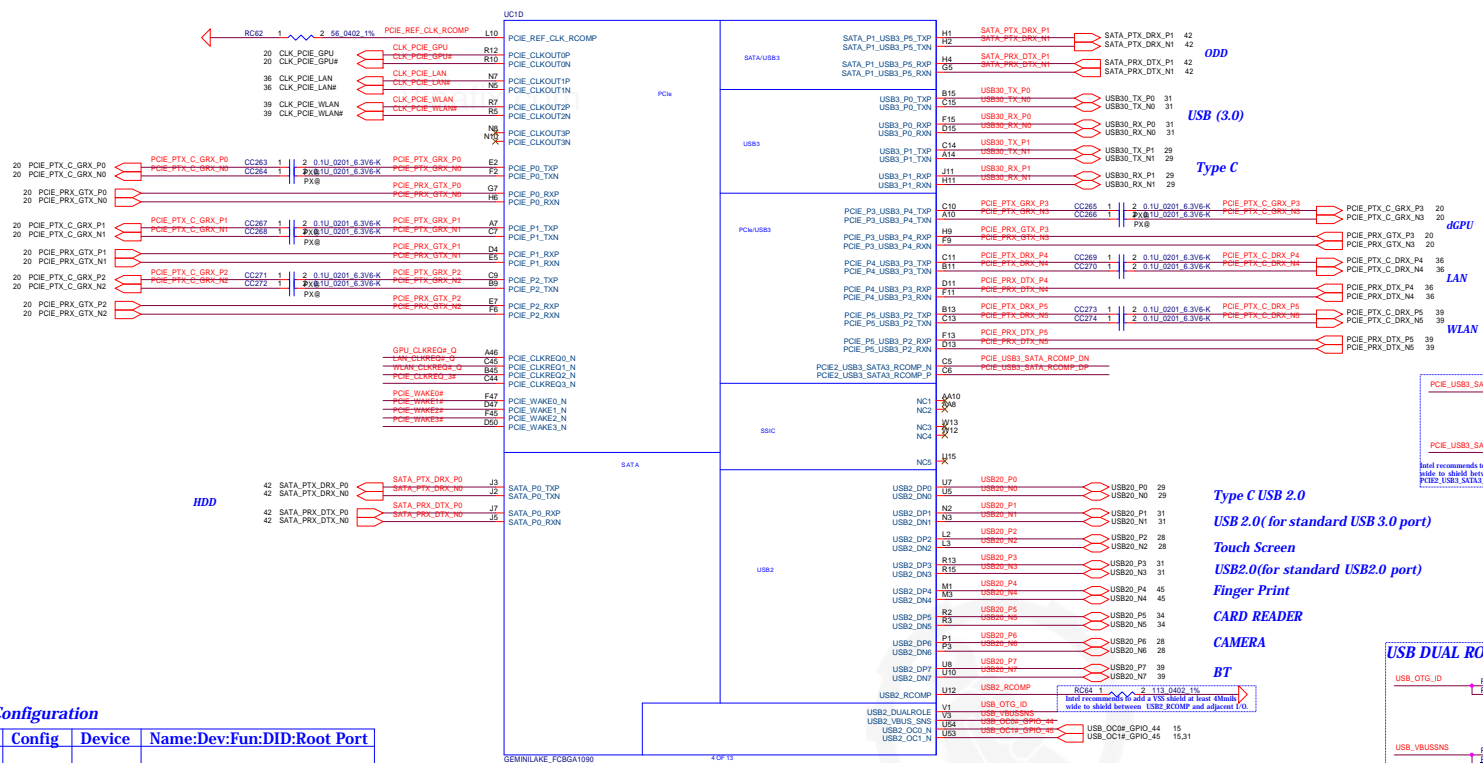
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SMB_CLK&SMB_DATA is OD(PDG v1.2 P309). Reserve MOS LS, Keep +3VS PU, CRB w/o PU, need BIOS check if have internal PU I/O Voltage is controlled by Hardware Strap(GPIO_163: PD) & Soft Strap 3.3(default)(SMP v0.82 P84)

SMBUS I/O Voltage is controlled by Hardware Strap(GPIO_163)

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Issued Date	2013/03/26	Deciphered Date	2014/01/21	SOC (I2C,SMBus,CNVI,UART)	
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dGPU

LAN

WLAN

HDD

Type C USB 2.0

USB 2.0 (for standard USB 3.0 port)

Touch Screen

USB2.0 (for standard USB2.0 port)

Finger Print

CARD READER

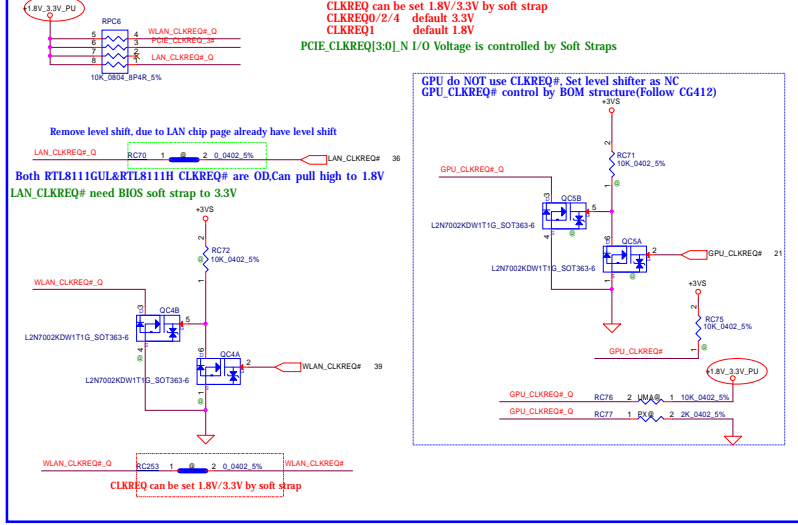
CAMERA

BT

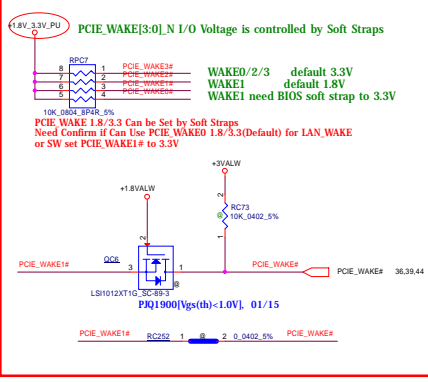
PCIe Configuration

Port	Config	Device	Name:Dev:Fun:DID:Root Port
P0			
P1	X4	dGPU	PCIe1(Func0):19:0:0x31D8:2
P2			
P3			
P4	X1	LAN	PCIe0(Func0):20:0:0x31D6:0
P5	X1	WLAN	PCIe0(Func1):20:1:0x31D7:1

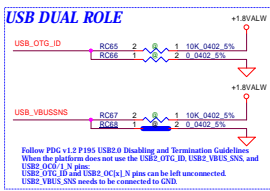
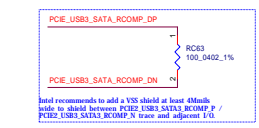
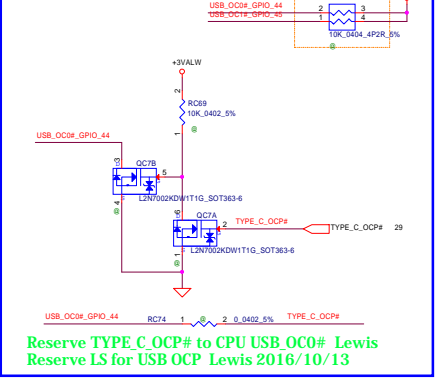
CLOCK REQUEST



LAN WAKE

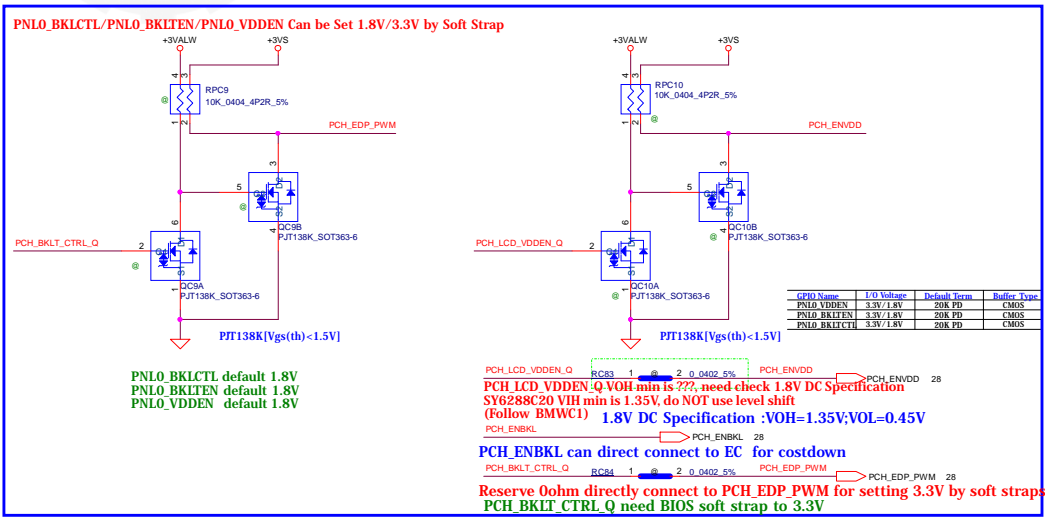
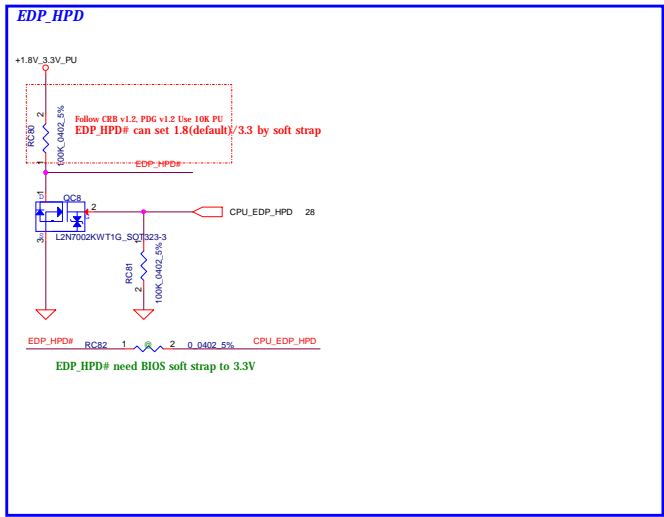
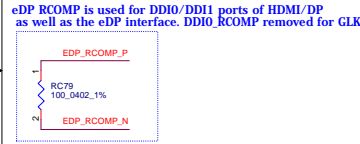
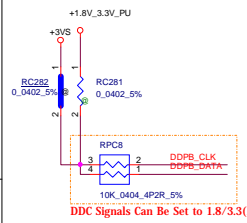
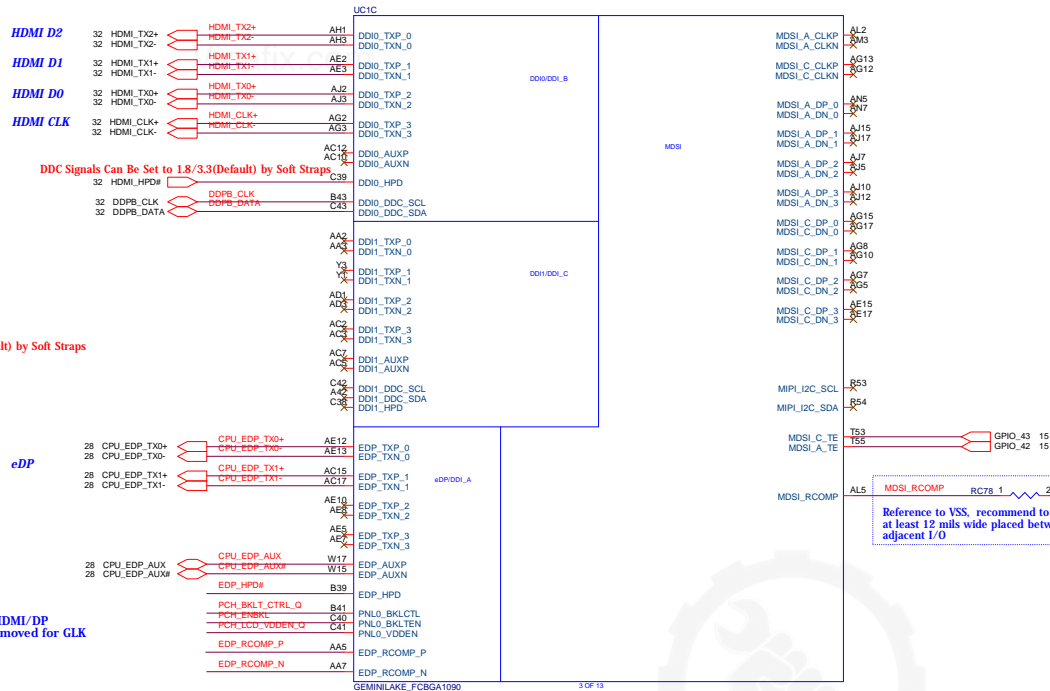


USB OCP



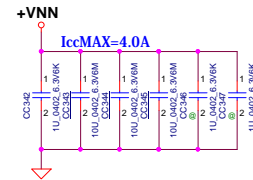
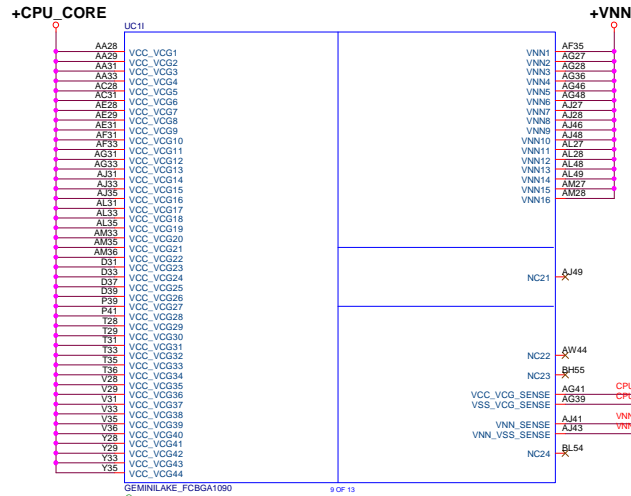
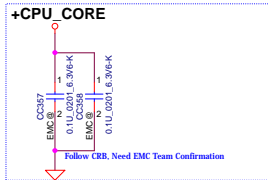
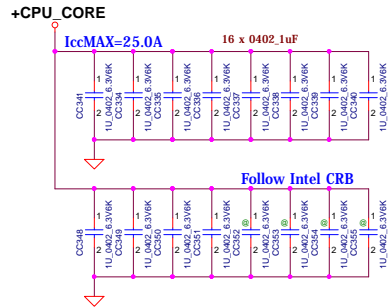
DDI PORT LIST

Port	Device	HPD Net	HPD Pin
DDIO	HDMI	HDMI_HPD#	C39
DDI1	N/A	N/A	C38
EDP	eDP	EDP_HPD#	B39



GPIO Name	I/O Voltage	Default Term	Buffer Type
PNL0_VDDEN	3.3V/1.8V	20K PD	CMOS
PNL0_BKLTEN	3.3V/1.8V	20K PD	CMOS
PNL0_BKLTCT	3.3V/1.8V	20K PD	CMOS

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Title	SOC (Power2)	
LCFC		

UC1K

A3	VSS_6	AF44	VSS_53
A6	VSS_13	AF45	VSS_54
A12	VSS_1	AF47	VSS_56
A16	VSS_11	AF48	VSS_57
A20	VSS_2	AF50	VSS_58
A24	VSS_3	AF52	VSS_59
A28	VSS_4	AF53	VSS_60
A32	VSS_5	AF55	VSS_61
A36	VSS_7	AC20	VSS_64
A40	VSS_8	AL21	VSS_67
A44	VSS_9	AG25	VSS_81
A48	VSS_10	AG29	VSS_82
A51	VSS_11	AG35	VSS_86
AA12	VSS_12	AG38	VSS_89
AA13	VSS_14	AJ9	VSS_69
AA15	VSS_15	AJ13	VSS_77
AA17	VSS_16	AJ18	VSS_80
AA21	VSS_17	AK25	VSS_70
AA23	VSS_18	AJ29	VSS_71
AA25	VSS_19	AK38	VSS_72
AA27	VSS_20	AJ38	VSS_73
AA35	VSS_21	AJ39	VSS_74
AA43	VSS_22	AK44	VSS_75
AA48	VSS_23	AK1	VSS_76
AB1	VSS_24	AK3	VSS_78
AB3	VSS_25	AK55	VSS_79
AB5	VSS_26	AL3	VSS_80
AB55	VSS_27	AL7	VSS_86
AC9	VSS_33	AL7	VSS_86
AC13	VSS_33	AL8	VSS_97
AC23	VSS_28	AL10	VSS_98
AC25	VSS_29	AL12	VSS_81
AC27	VSS_30	AL13	VSS_82
AC29	VSS_31	AL15	VSS_83
AE18	VSS_32	AL16	VSS_84
AE23	VSS_35	AL20	VSS_88
AE25	VSS_36	AL25	VSS_89
AE27	VSS_36	AL29	VSS_88
AE3	VSS_37	AL39	VSS_89
AE36	VSS_38	AL41	VSS_91
AF1	VSS_39	AL43	VSS_92
AF3	VSS_40	AL44	VSS_93
AF4	VSS_49	AL46	VSS_94
AF5	VSS_50	AL51	VSS_97
AF6	VSS_61	AM1	VSS_96
AF9	VSS_62	AM21	VSS_99
AF11	VSS_63	AM23	VSS_101
AF12	VSS_41	AM25	VSS_101
AF14	VSS_42	AM29	VSS_102
AF16	VSS_43	AM31	VSS_102
AF18	VSS_44	B5	VSS_104
AF23	VSS_45	AM38	VSS_104
AF25	VSS_46	AM5	VSS_106
AF29	VSS_47	B1	VSS_106
AF40	VSS_48	AN8	VSS_110
AF42	VSS_51	AN9	VSS_107
	VSS_52	AN10	VSS_108
		AN46	VSS_109

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UC1L

AN48	VSS_111	BC11	VSS_165
AN49	VSS_112	BC17	VSS_166
AN51	VSS_113	BC19	VSS_166
AN53	VSS_114	BC21	VSS_168
AP23	VSS_114	BC22	VSS_168
AP27	VSS_115	BC25	VSS_169
AP28	VSS_116	BC31	VSS_170
AP29	VSS_117	BC33	VSS_171
AP33	VSS_118	BC35	VSS_172
AP35	VSS_119	BC37	VSS_173
AR2	VSS_120	BC39	VSS_174
AR7	VSS_124	BC41	VSS_176
AR10	VSS_130	BC45	VSS_177
AR12	VSS_121	BC51	VSS_177
AR17	VSS_122	BD9	VSS_170
AR39	VSS_123	BD15	VSS_187
AR44	VSS_125	BD19	VSS_180
AR46	VSS_126	BD21	VSS_181
AR49	VSS_127	BD28	VSS_182
AR54	VSS_128	BD36	VSS_183
AT23	VSS_129	BD37	VSS_184
AT33	VSS_131	BD47	VSS_185
AL5	VSS_131	BE3	VSS_186
AU10	VSS_135	BE28	VSS_189
AU28	VSS_133	BE53	VSS_188
AU48	VSS_134	BF5	VSS_190
AL3	VSS_136	BF19	VSS_194
AL7	VSS_137	BF27	VSS_191
AL7	VSS_138	BF47	VSS_192
AL10	VSS_139	BG1	VSS_193
AL12	VSS_140	BG6	VSS_195
AL13	VSS_141	BG28	VSS_199
AL15	VSS_142	BG50	VSS_198
AL17	VSS_143	BG59	VSS_197
AL20	VSS_144	BH1	VSS_200
AL25	VSS_145	BH13	VSS_201
AW5	VSS_147	BH17	VSS_201
AW10	VSS_150	BH18	VSS_202
AW18	VSS_146	BH25	VSS_203
AW46	VSS_148	BH25	VSS_204
AW51	VSS_149	BH28	VSS_205
AW54	VSS_151	BH31	VSS_206
AV13	VSS_152	BH33	VSS_207
AV15	VSS_153	BH37	VSS_208
AV28	VSS_154	BH39	VSS_209
AV41	VSS_155	BH41	VSS_210
AV43	VSS_156	BH45	VSS_211
B2	VSS_157	BJ2	VSS_212
B5	VSS_158	BJ2	VSS_215
B5	VSS_159	BJ15	VSS_213
BA27	VSS_160	BJ19	VSS_214
BA29	VSS_161	BJ25	VSS_216
B81	VSS_162	BJ29	VSS_217
BB28	VSS_163	BJ37	VSS_218
BB55	VSS_163	BJ37	VSS_219
BC5	VSS_164	BJ41	VSS_219
BC5	VSS_178	BJ41	VSS_220

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UC1M

AL23	VSS_221	J51	VSS_272
BK4	VSS_222	K3	VSS_273
BK1	VSS_223	K28	VSS_274
BK17	VSS_223	K28	VSS_275
BK21	VSS_224	L5	VSS_276
BK35	VSS_225	L7	VSS_277
BK39	VSS_226	L8	VSS_278
BK55	VSS_227	L19	VSS_279
BL5	VSS_228	L31	VSS_280
BL8	VSS_230	M15	VSS_281
BL10	VSS_231	M25	VSS_282
BL14	VSS_232	M28	VSS_283
BL24	VSS_232	M28	VSS_284
BL28	VSS_233	M41	VSS_285
BL32	VSS_234	N12	VSS_286
BL42	VSS_235	N28	VSS_287
BL46	VSS_236	N46	VSS_288
BL48	VSS_237	N51	VSS_289
BL51	VSS_238	P21	VSS_290
C1	VSS_239	P55	VSS_291
C12	VSS_240	R8	VSS_292
C28	VSS_243	R28	VSS_293
C36	VSS_244	R28	VSS_294
D6	VSS_245	R38	VSS_295
D9	VSS_246	U13	VSS_296
D21	VSS_246	V27	VSS_297
D41	VSS_248	V39	VSS_298
D45	VSS_249	V55	VSS_299
D55	VSS_250	W2	VSS_300
E28	VSS_251	W3	VSS_301
E50	VSS_252	W5	VSS_302
E55	VSS_253	W7	VSS_303
F1	VSS_254	W8	VSS_304
F4	VSS_256	W10	VSS_305
F21	VSS_257	W38	VSS_306
F31	VSS_257	W41	VSS_307
G28	VSS_258	W43	VSS_308
H15	VSS_259	W43	VSS_309
H15	VSS_260	W46	VSS_310
H21	VSS_261	W48	VSS_311
H23	VSS_262	W49	VSS_312
H28	VSS_263	W51	VSS_313
H33	VSS_264	Y1	VSS_314
H39	VSS_265	Y23	VSS_315
J8	VSS_266	Y25	VSS_316
J27	VSS_267	Y27	VSS_317
J33	VSS_268	Y31	VSS_318
J41	VSS_269	Y3	VSS_319
J45	VSS_270	U3	VSS_320
	VSS_271	VSS_321	VSS_321

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			Rev
			Date

SOC (VSS)

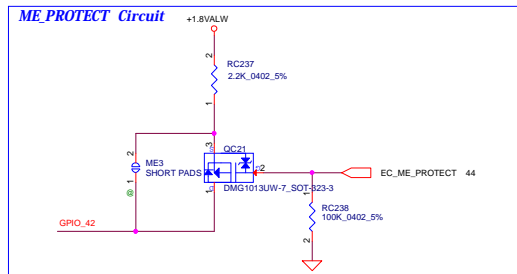
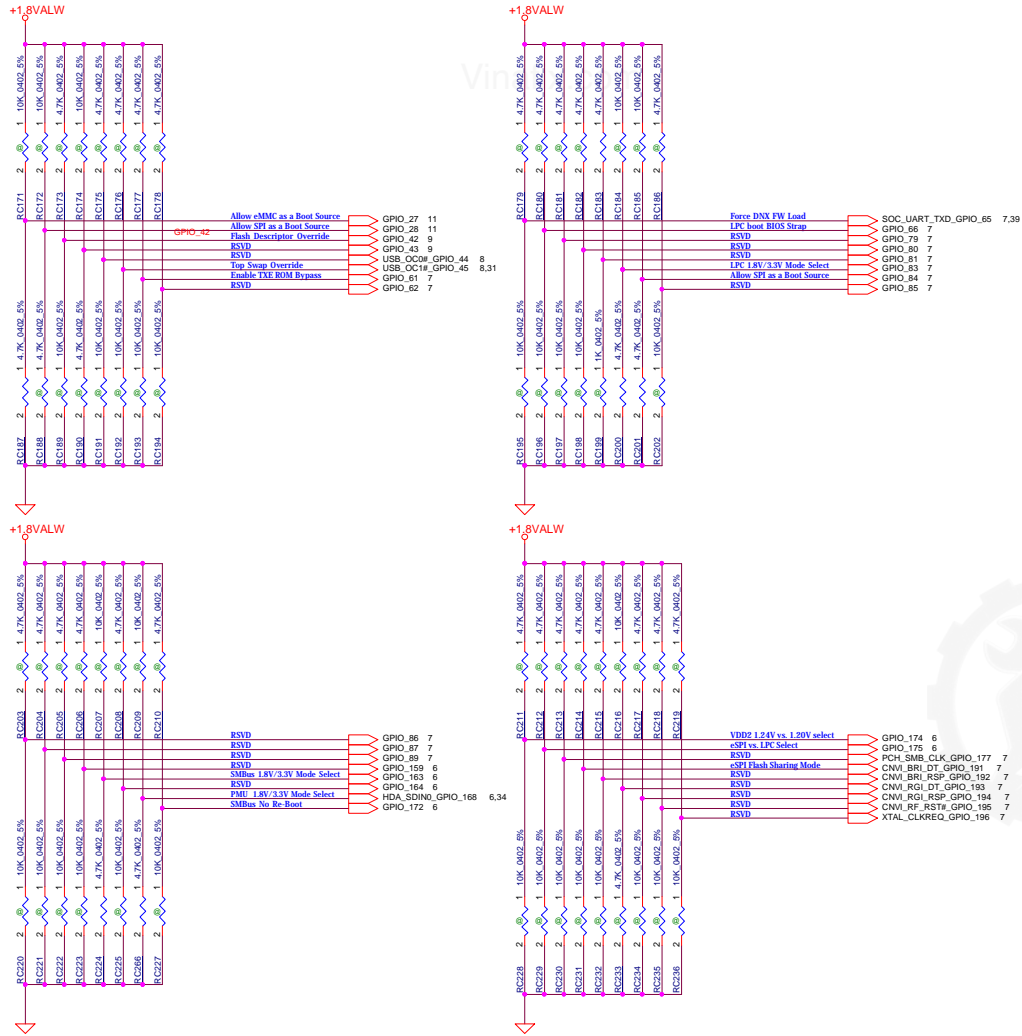


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Hardware STRAPS(Follow up CRB)



EC_ME_PROTECT	GPIO_42	TXE Flash Descriptor Override
Low	High	Override
High	Low	No Override (Normal Operation)


GPIO#	Purpose	Internal Termination	Schematics Setting	Pin Usage	Remark
GPIO_27	Allow eMMC as a Boot Source	20K PU	4.7K PD	1 = Enable(Default); 0 = Disable[✓] If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_28	Allow SPI as a Boot Source	20K PU	Floating	1 = Enable(Default)[✓]; 0 = Disable If platform is using eMMC as boot device, then provide a pull-down for this strap to disable SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_42	Flash Descriptor Override	20K PD	Floating	1 = Override; 0 = No Override(Normal Operation)[✓] This strap enables the platform to override security features in the SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_43	RSVD	20K PU	Floating	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_44	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_45	Top swap override	20K PD	Floating	1 = Enable; 0 = Disable(Default)[✓] This strap enables platform to change where the core will look for BIOS code for a SPI boot only	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_61	Enable TXE ROM Bypass	20K PD	Floating	1 = Enable Bypass; 0 = Disable Bypass(Default)[✓] This strap tells TXE SIO to bypass Read-Only Memory (ROM) that it has on SoC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_62	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_65	Force DNX FW Load	20K PD	Floating	1 = Force; 0 = Do Not Force(Default)[✓] This strap is a recovery strap for corrupted FW image, will force TXE3A to execute a link dump	Follow CRB(v1.2 P58); EDS(v1.2 P40); PDG(v1.2 P471)
GPIO_66	LPC boot BIOS strap	20K PD	Floating	1 = Boot From LPC; 0 = Do Not(Default)[✓] The board should strap this low and do not use otherwise	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_79	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_80	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_81	RSVD	20K PU	4.7K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_83	LPC 1.8V/3.3V mode select	20K PD	4.7K PD	1=buffer set to 1.8V mode 0=buffer set to 3.3V mode (default)[✓]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_84	Allow SPI as a boot source	20K PU	4.7K PD	1=disable 0=enable (default)[✓]	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_85	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_86	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_87	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_89	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_159	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_163	SMBus 1.8V/3.3V mode select	20K PD	4.7K PD	1=buffer set to 1.8V mode 0=buffer set to 3.3V mode (default)[✓]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_164	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_168	PMU 1.8V/3.3V mode select	20K PD	4.7K PD	1=buffer set to 1.8V mode 0=buffer set to 3.3V mode (default)[✓]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_172	SMBus No Re-Boot	20K PD	Floating	1 = Enable; 0 = Disable (default)[✓] Note: Platforms should strap this LOW. Functionality is handled by the FMS	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_174	VDD2 1.24V vs. 1.20V select	20K PD	Floating	1=VDD2 is 1.24V. 0=VDD2 is 1.20V (default) Need Check	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_175	eSPI vs LPC	20K PD	Floating	1=eSPI mode; 0=LPC mode (default) Note: The default for AD will be eSPI due to a bug on LPC	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_177	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_191	eSPI Flash Sharing Mode	20K PD	Floating	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS, default)[✓]	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_192	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_193	RSVD	20K PU	Floating	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_194	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_195	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_196	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)

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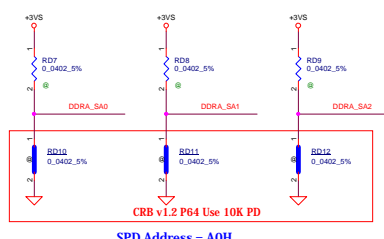
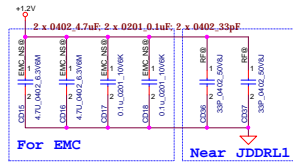
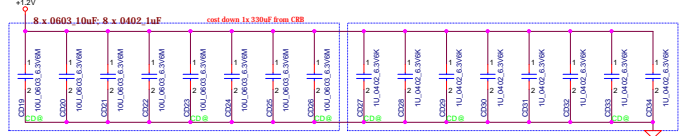
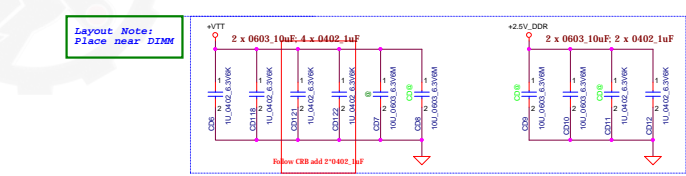
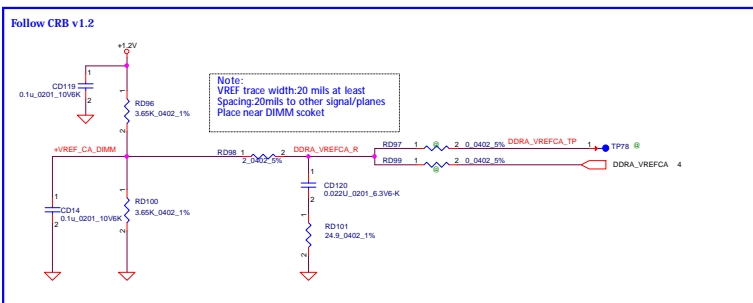
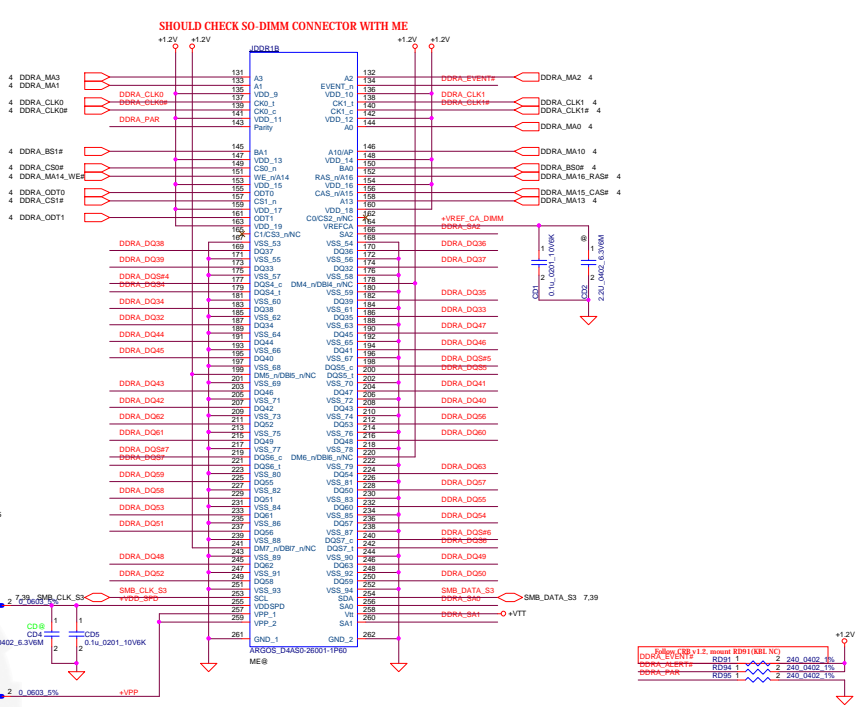
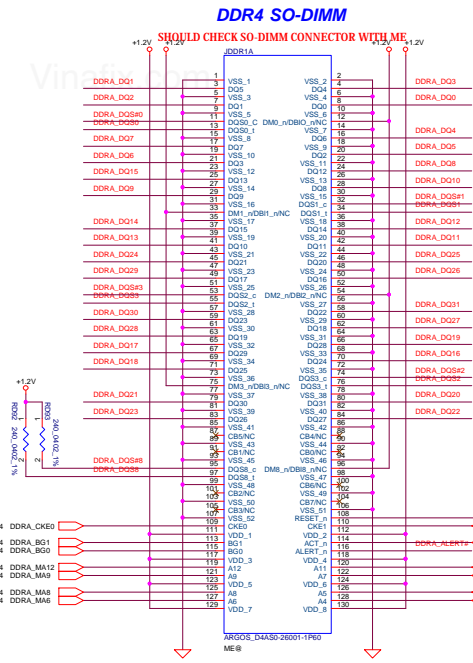
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DDR4 Swap Mapping table

DDR4 NET	DDR4 SO-DIMM	DDR4 NET	DDR4 SO-DIMM
DDR4_DQ0---DQ	DQ0		
DDR4_DQ1---DQ	DQ1		
DDR4_DQ2---DQ	DQ2		
DDR4_DQ3---DQ	DQ3		
DDR4_DQ4---DQ	DQ4		
DDR4_DQ5---DQ	DQ5		
DDR4_DQ6---DQ	DQ6		
DDR4_DQ7---DQ	DQ7		
DDR4_DQ8---DQ	DQ8		
DDR4_DQ9---DQ	DQ9		
DDR4_DQ10---DQ	DQ10		
DDR4_DQ11---DQ	DQ11		
DDR4_DQ12---DQ	DQ12		
DDR4_DQ13---DQ	DQ13		
DDR4_DQ14---DQ	DQ14		
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DDR4_DQ49---DQ	DQ49		
DDR4_DQ50---DQ	DQ50		
DDR4_DQ51---DQ	DQ51		
DDR4_DQ52---DQ	DQ52		
DDR4_DQ53---DQ	DQ53		
DDR4_DQ54---DQ	DQ54		



SPD Address = A0H

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0.62449.757

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

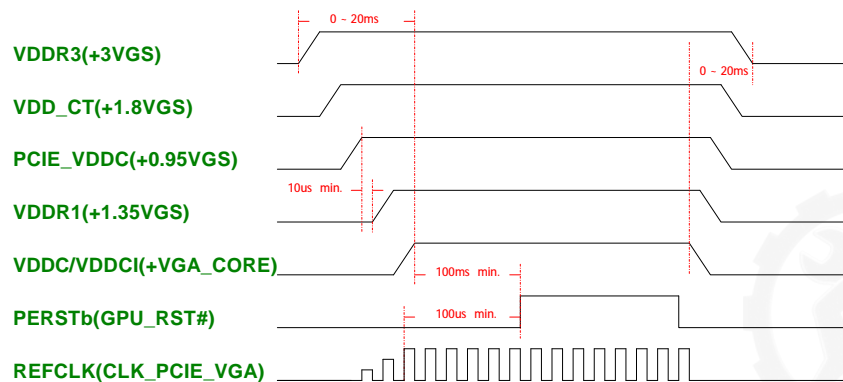
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s).

For power down, reversing the ramp-up sequence is recommended.




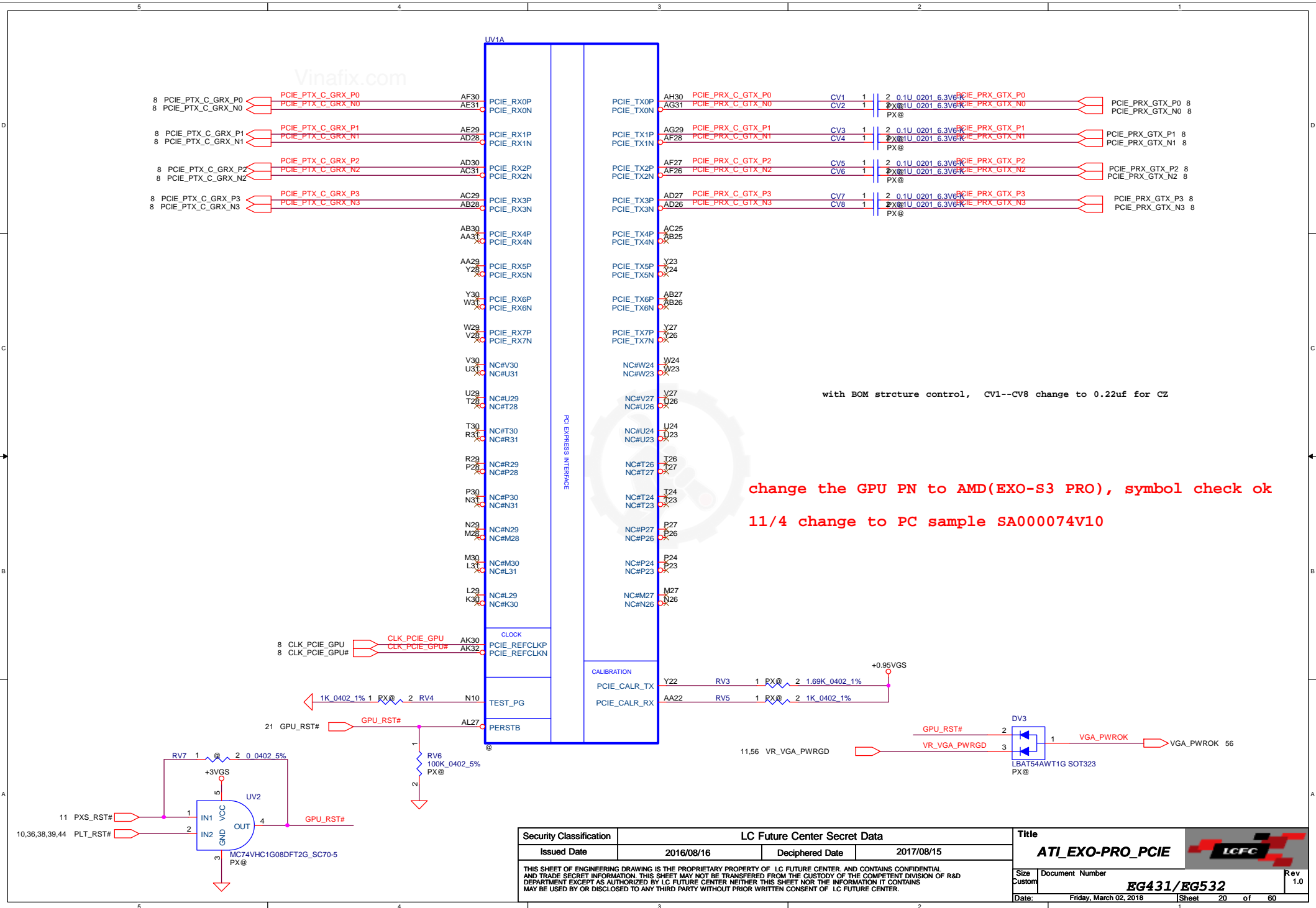
VRAM ID config

Memory Type	VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC8H24MJR-R0C	100	4.53K
	Micron MT51J256M32HF-70:A	111	4.75K
	Samsung K4G80325FB-HC28	110	3.4K
	000	NC	4.75K
	010	4.53K	2K
	001	8.45K	2K

FBGA Code: D9SXD

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with BOM structure control, CV1--CV8 change to 0.22uf for CZ


change the GPU PN to AMD(EXO-S3 PRO), symbol check ok
 11/4 change to PC sample SA000074V10

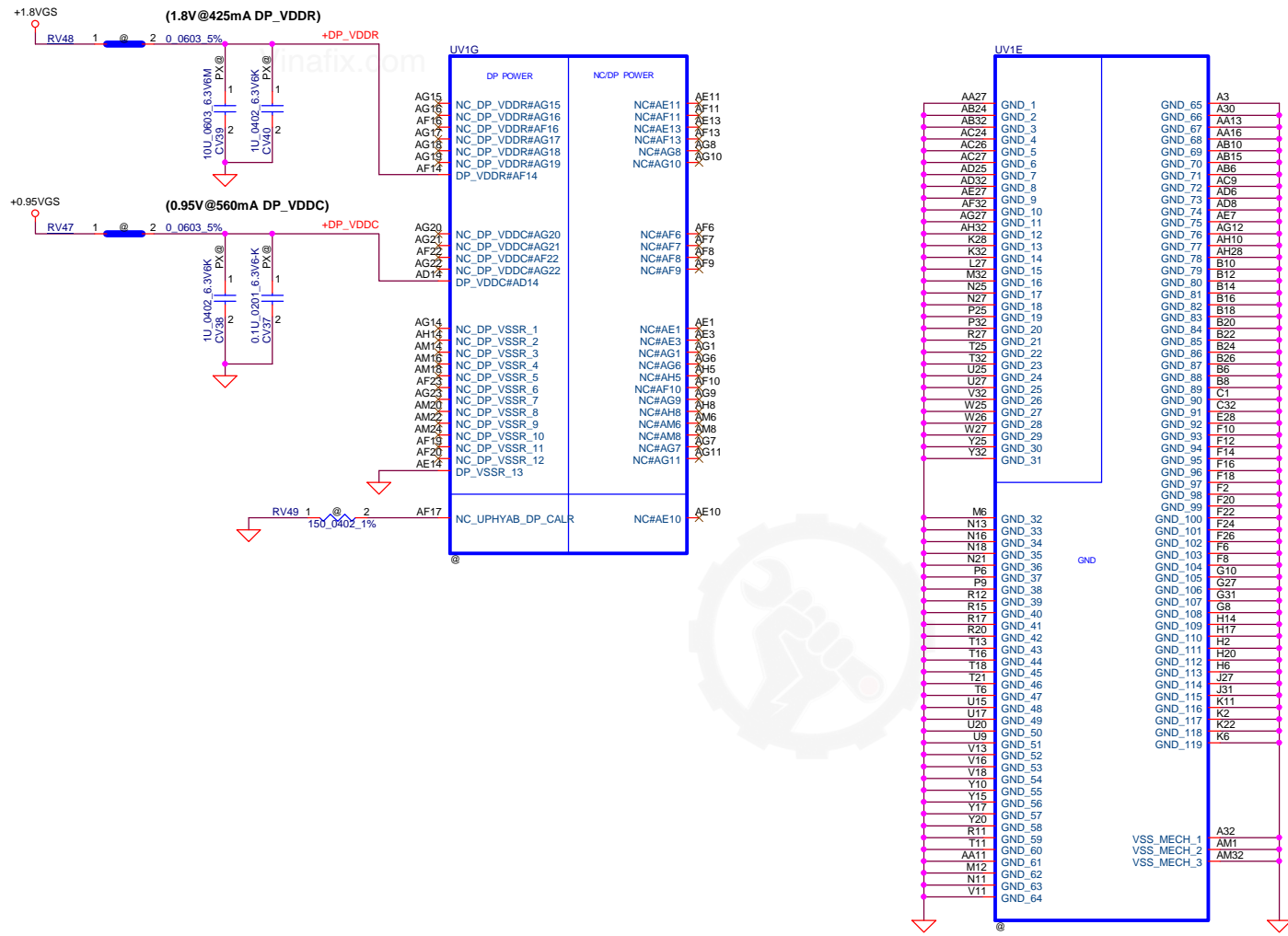
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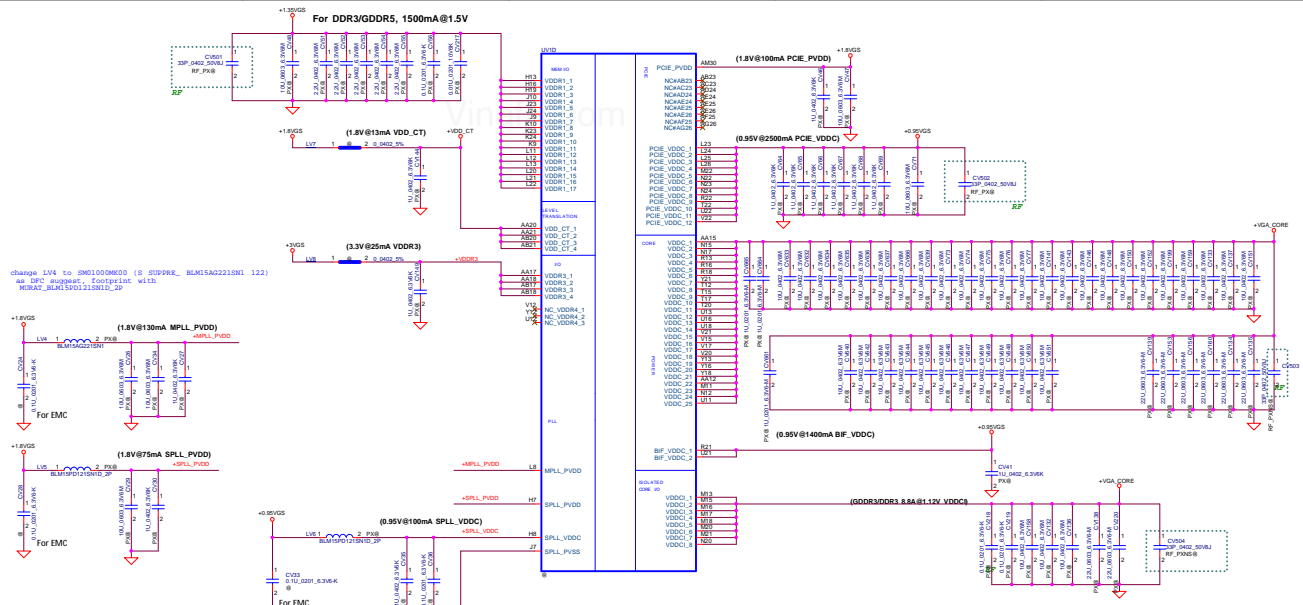
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ATI_EXO-PRO_TMDP		
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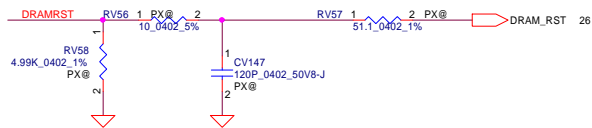
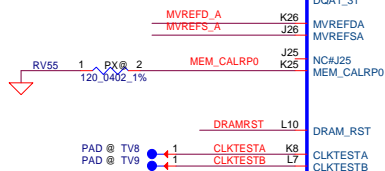
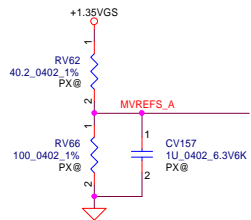
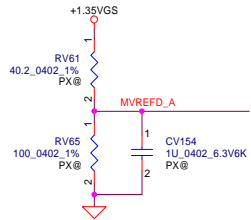
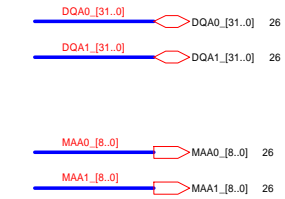


change LV4 to SM1000W600 (S SUPP9K_BLM5A2221SN1 122)
 *in BFLI Supp9K: 600000000 WITH
 MURAV_BLM5A2221SN1D_0



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IV10



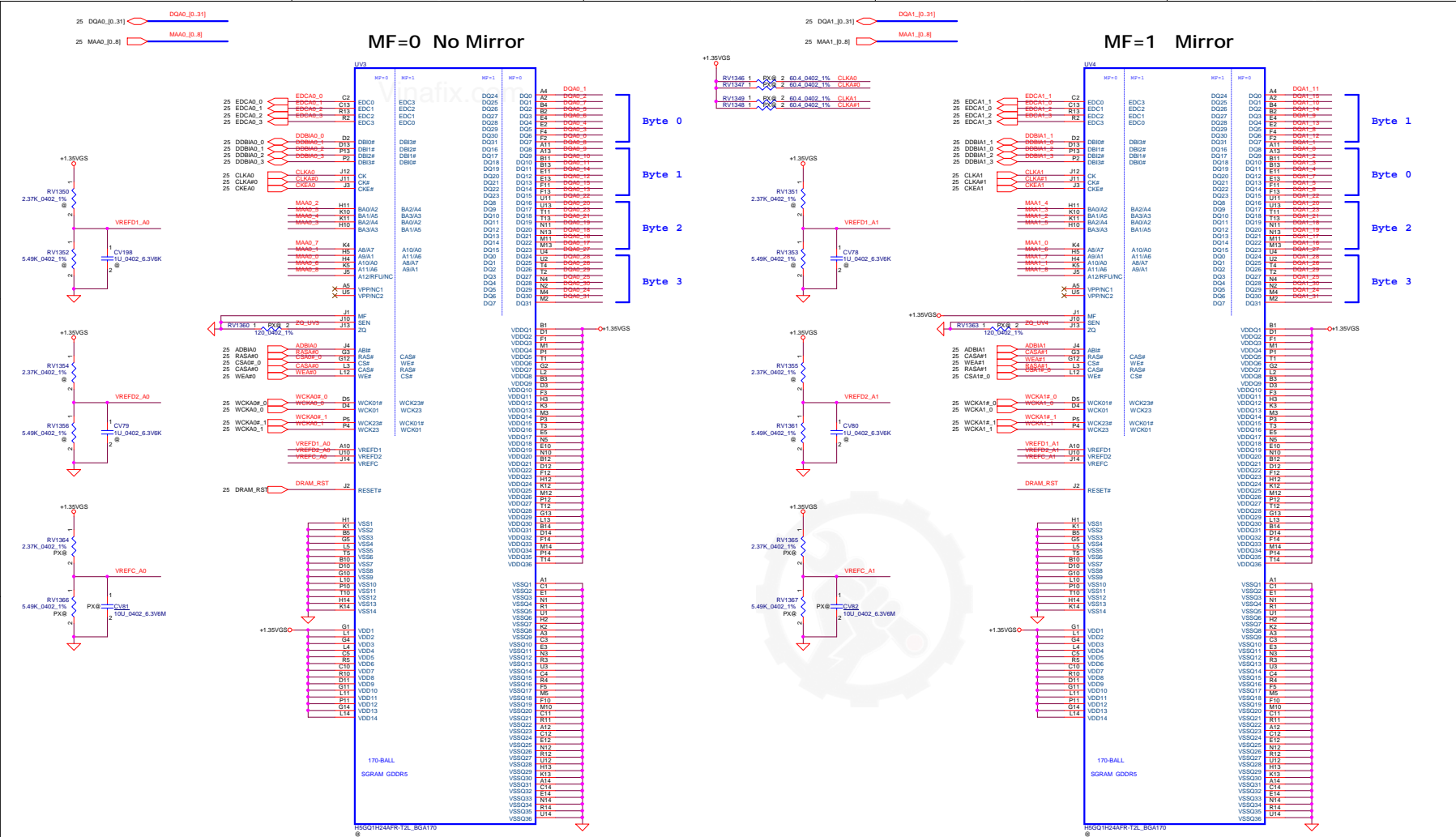
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ATI_EXO-PRO_MEM IF

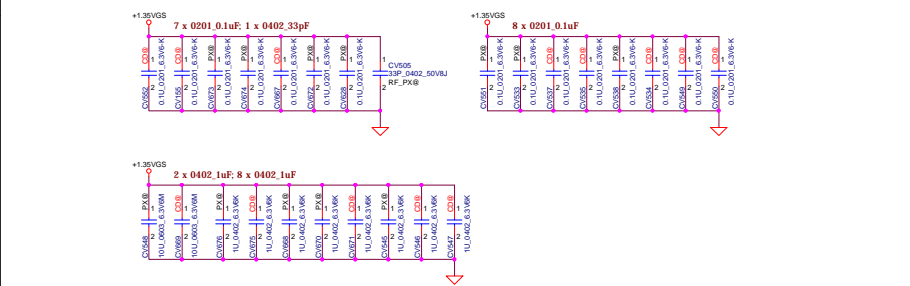

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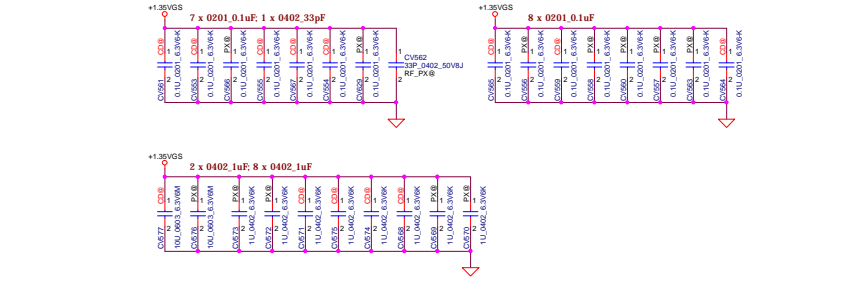
MF=1 Mirror



Place Near at UV3 Side




Place Near at UV4 Side



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Doc No	Document Number	Rev	1.0
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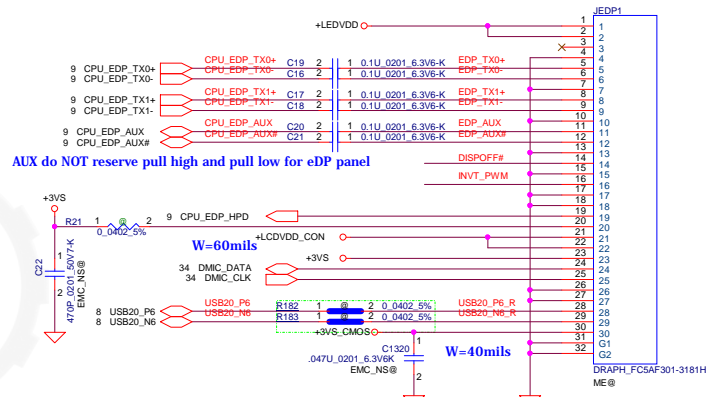
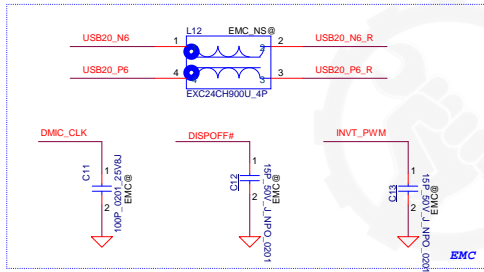
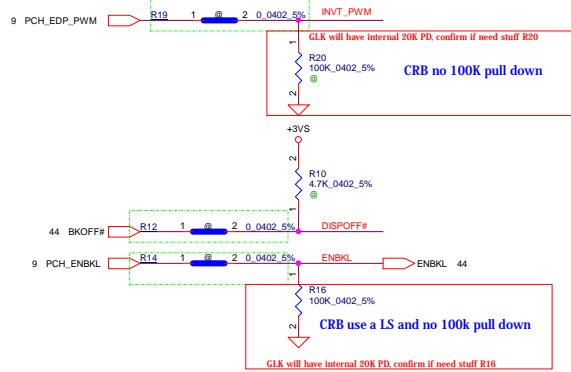
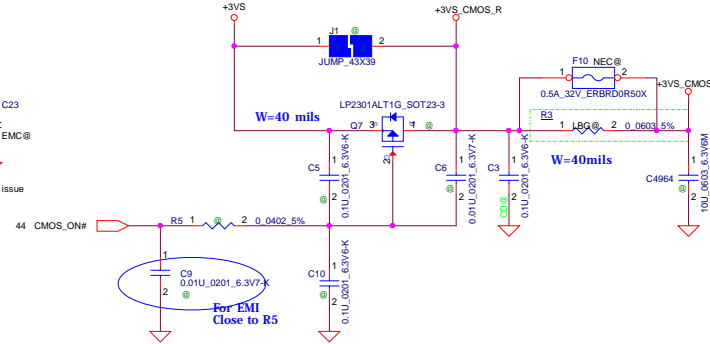
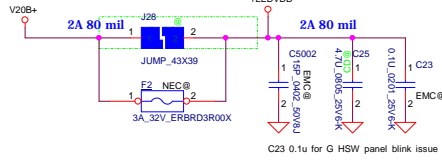
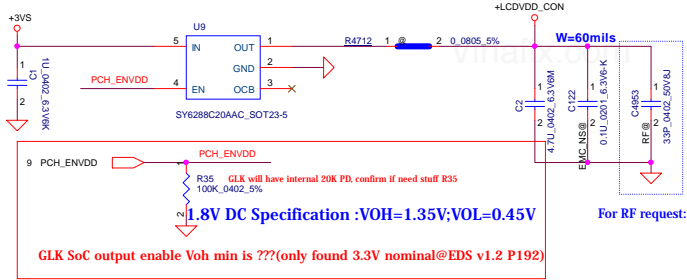


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LCD POWER CIRCUIT

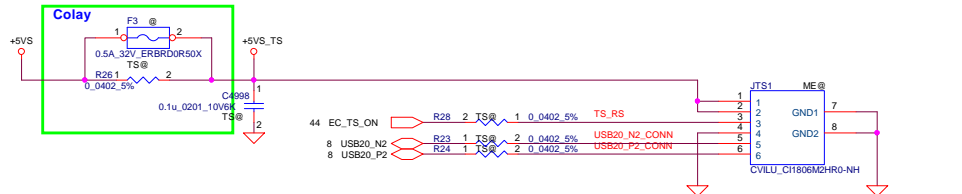
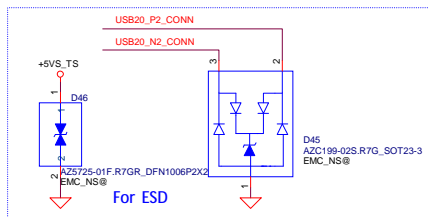
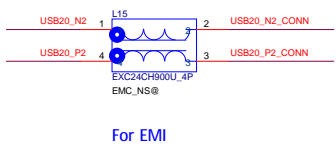
B+ to +LEDVDD POWER

CMOS CAMERA

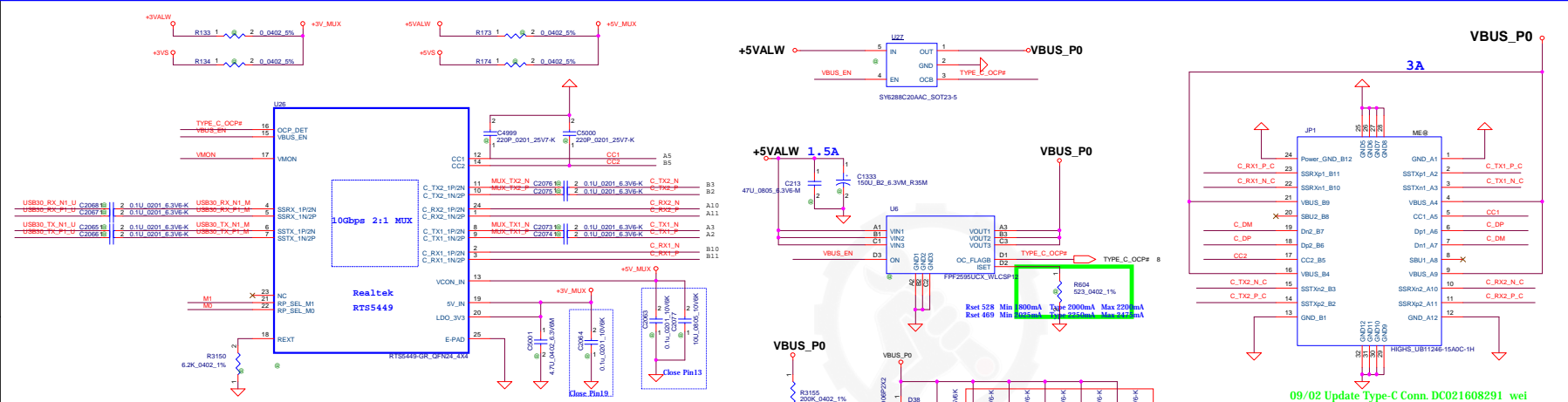
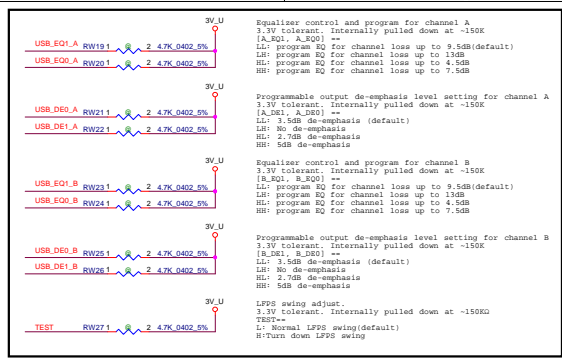
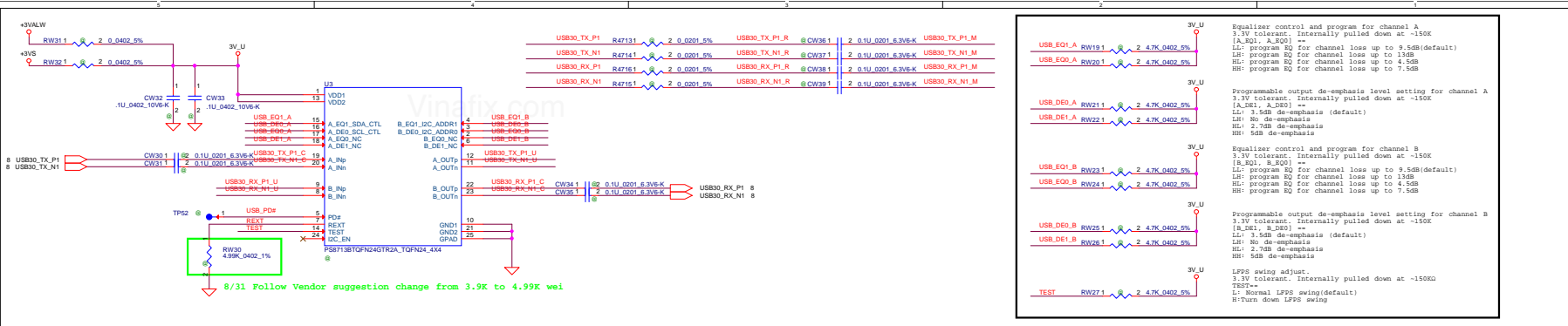


Touch Screen

Touch Screen



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Rp configuration

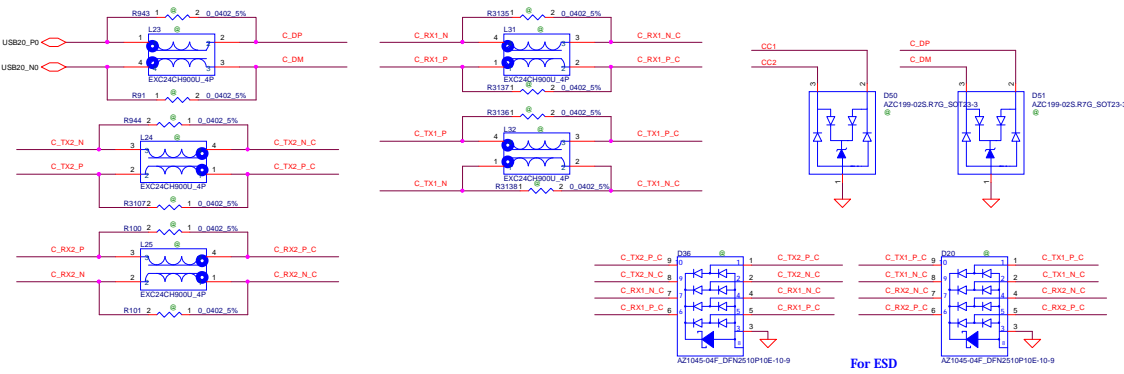
Rp	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

For C.VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount


For C.VBUS power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount



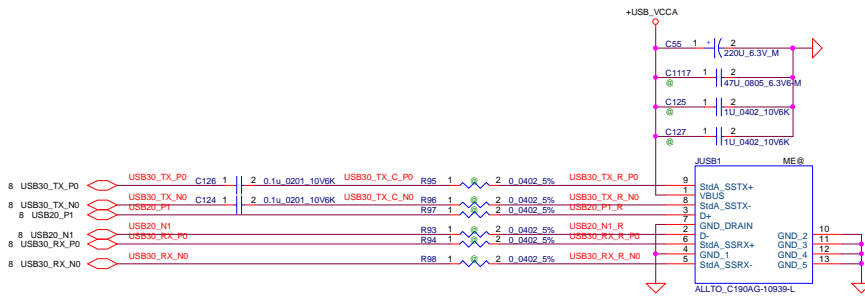
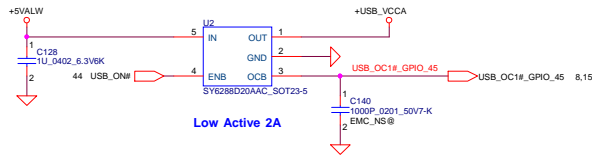
Vinafix.com



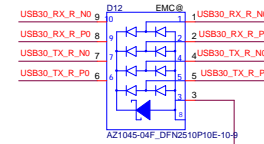
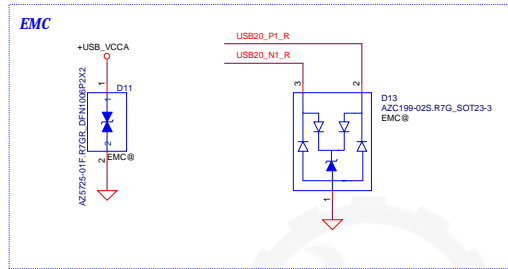
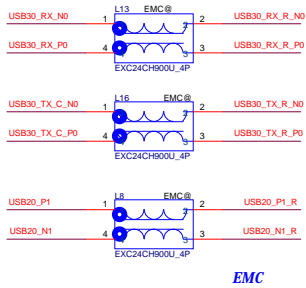
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USB3.0 Port X 1

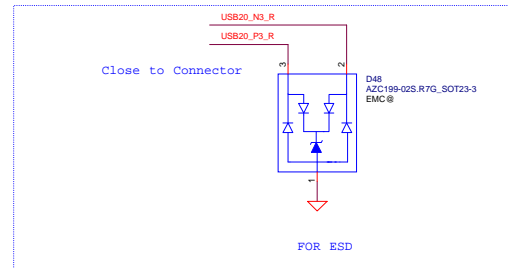
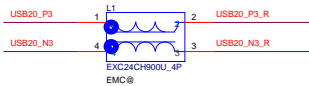
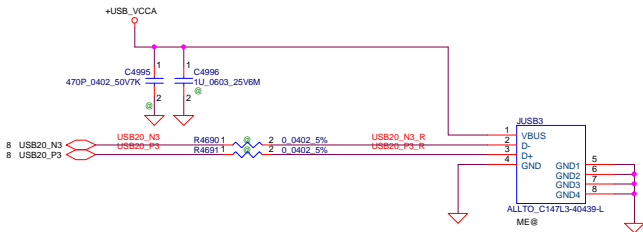
Vinafix.com



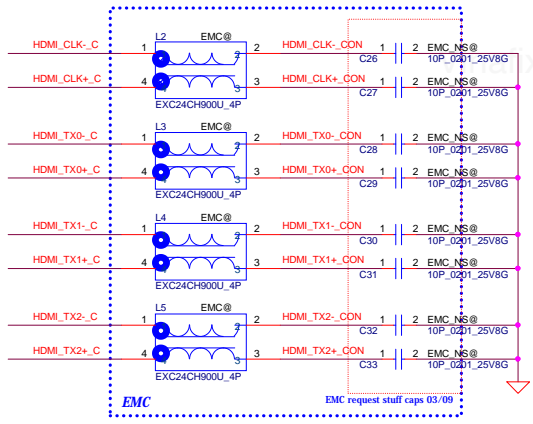
09/05 Update USBConn. P/N DC021609011 wei



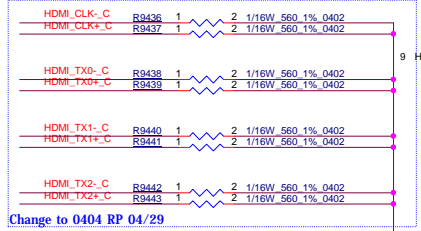
Update footprint symbol lewis



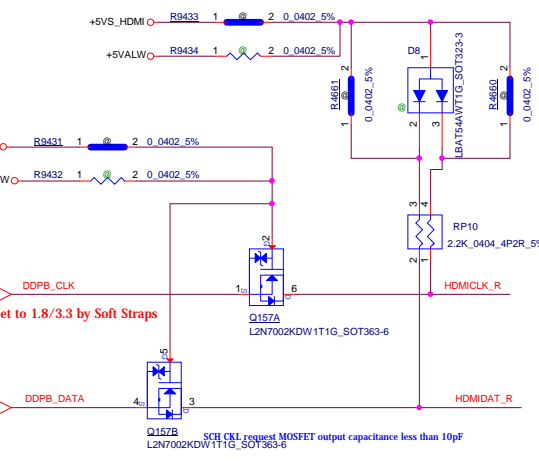
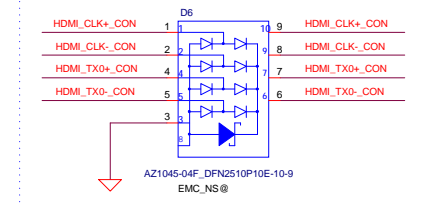
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Follow PDG & CRB use 470ohm.SVT change 470 to 560 for HDMI issue

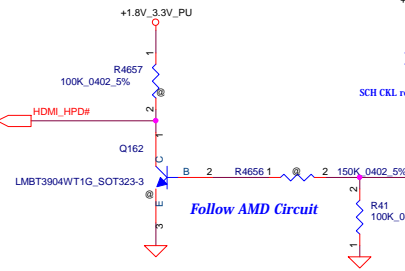


Change to 0404 RP 04/29

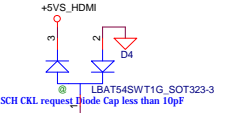


DDC Signals Can Be Set to 1.8/3.3 by Soft Straps

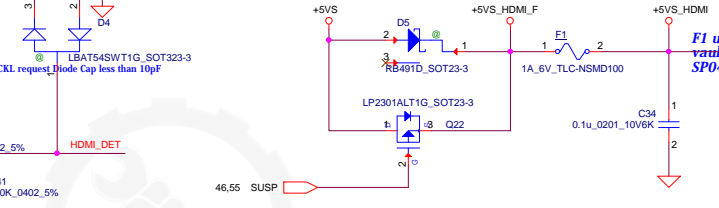
SCH CLK request MOSFET output capacitance less than 10pF



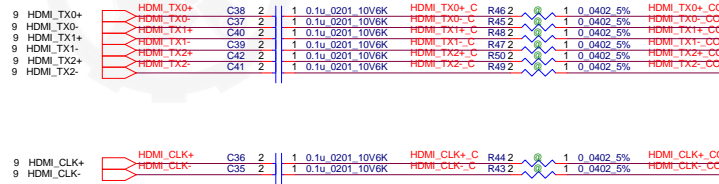
Follow AMD Circuit



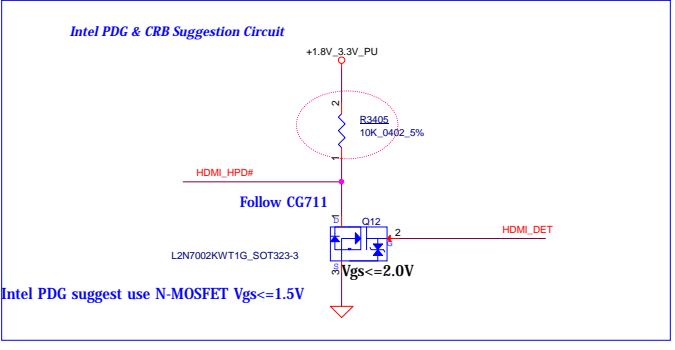
SCH CLK request Diode Cap less than 10pF



F1 use SP040007H00 footprint, only change description, value and part number. SP040007K00 and SP040007H00 is same footprint.



8/16 Update HDMIComm. P/N DC021608081 wei



Intel PDG & CRB Suggestion Circuit


Follow CG711

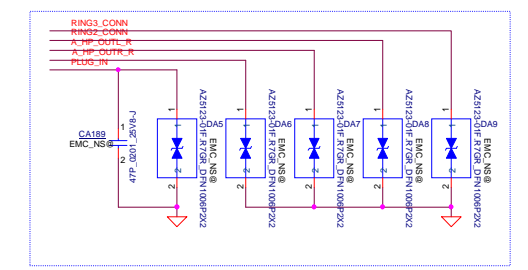
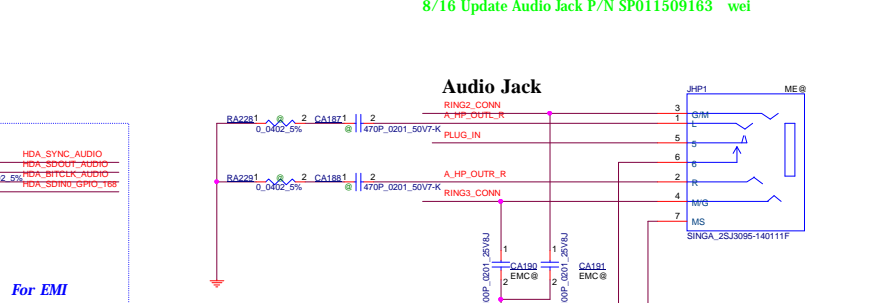
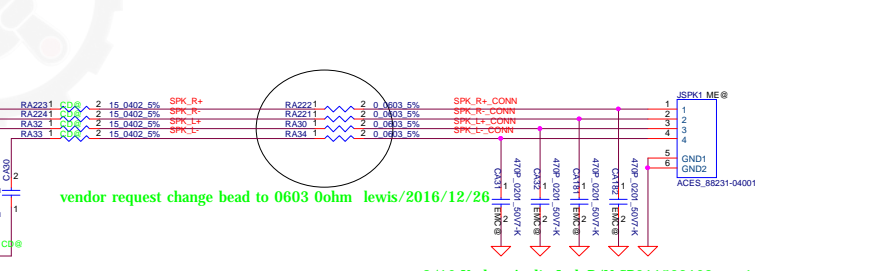
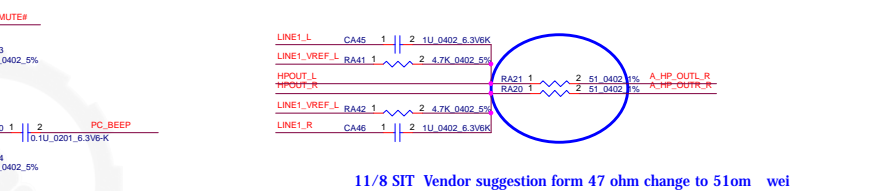
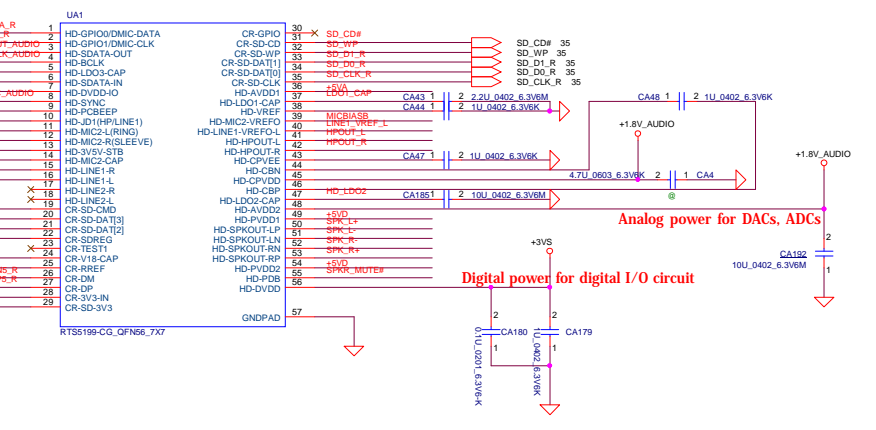
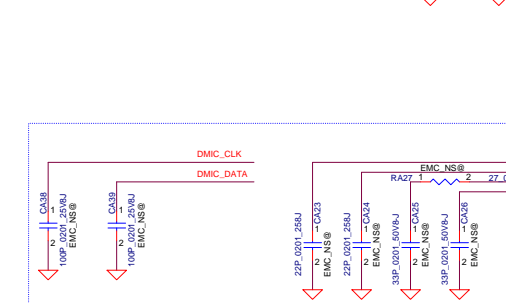
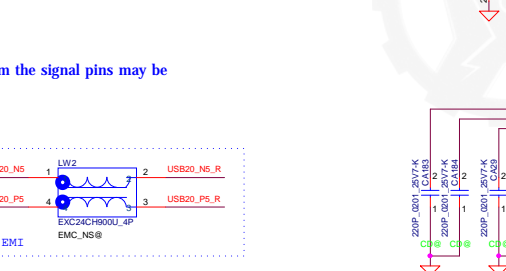
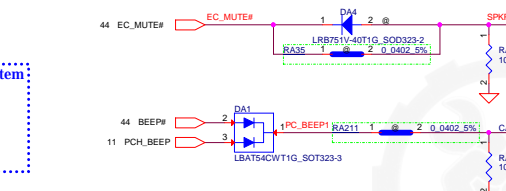
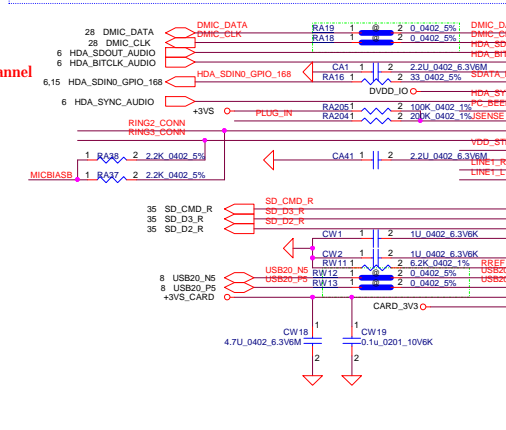
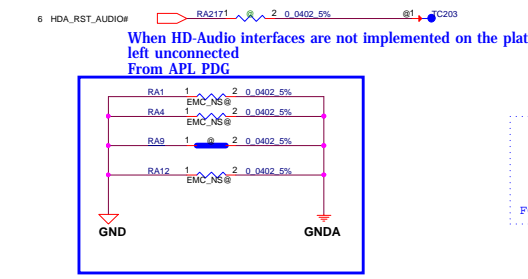
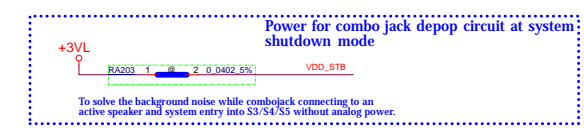
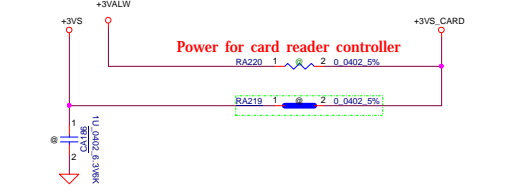
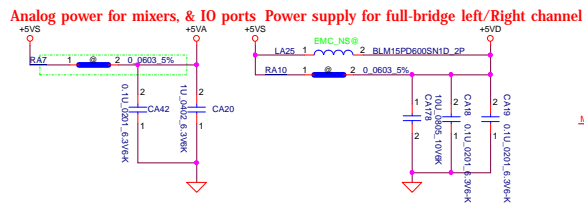
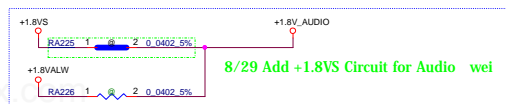
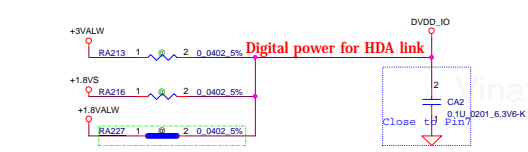
Intel PDG suggest use N-MOSFET Vgs<=2.0V

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11/8 SIT Vendor suggestion form 47 ohm change to 51om wei

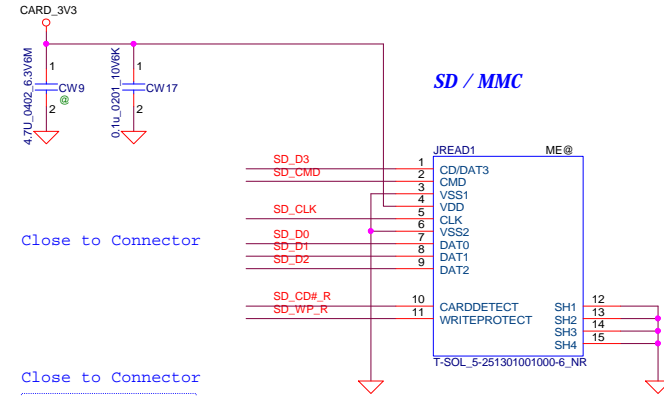
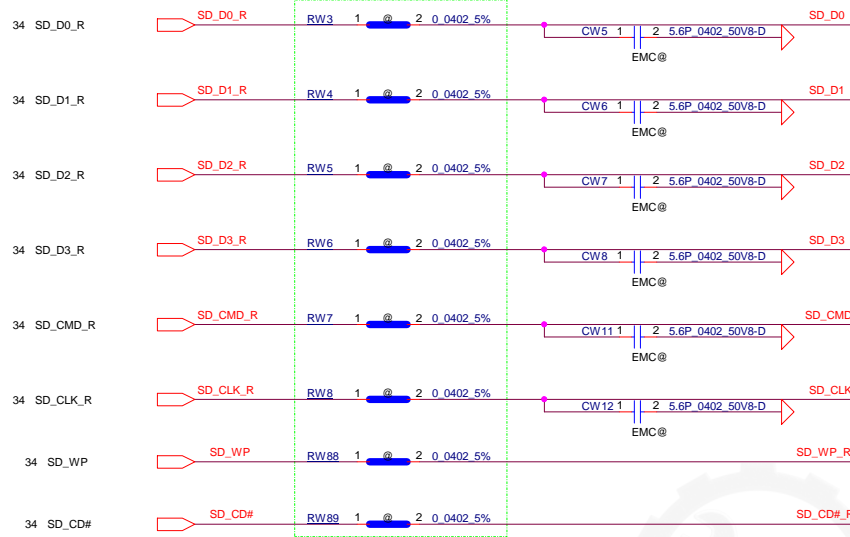
vendor request change bead to 0603 0ohm lewis/2016/12/26

8/16 Update Audio Jack P/N SP011509163 wei

8/16 Update Audio Jack P/N DC021608101 wei

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Date:	Friday, March 02, 2016	ISheet	34	a1	60

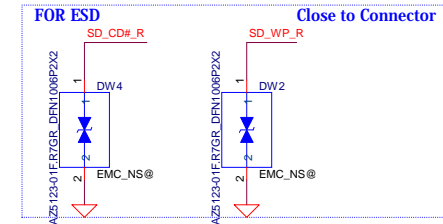
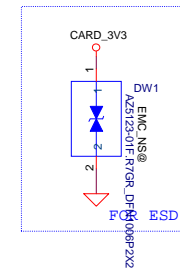
Vinafix.com




Close to Connector

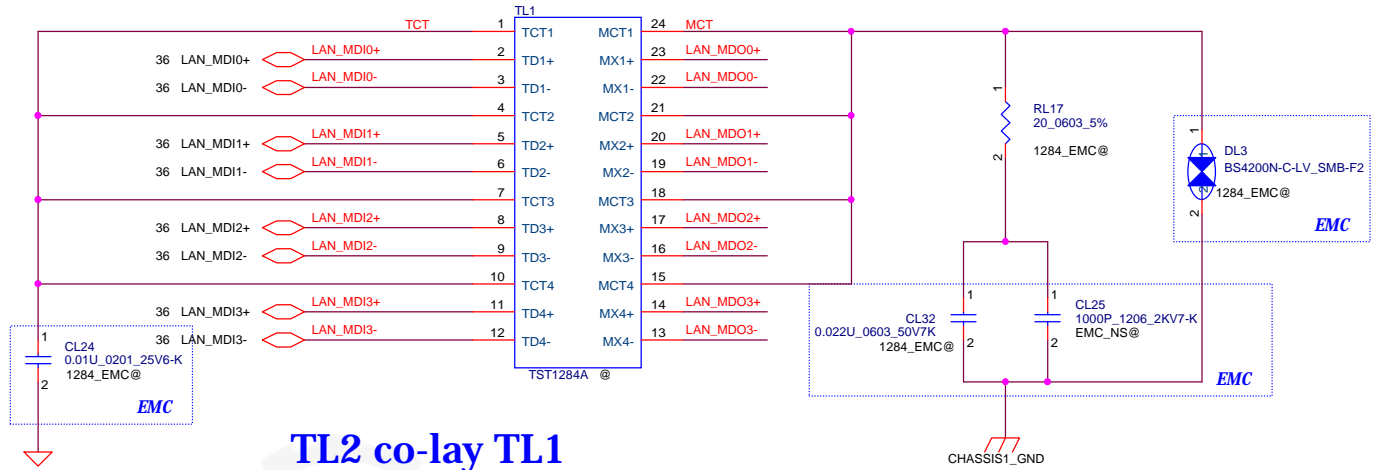
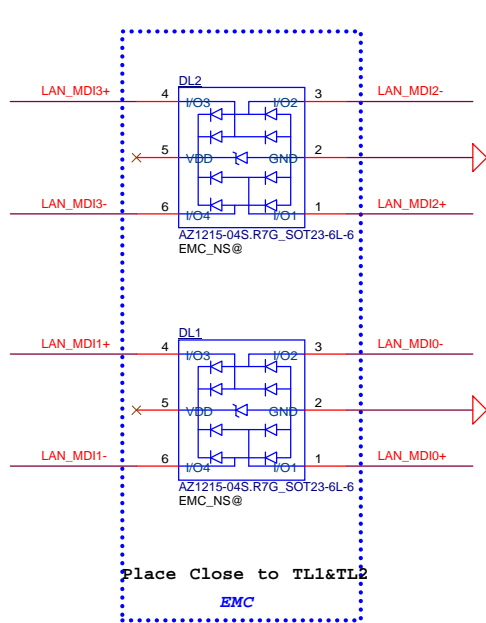
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8/16 Update Conn. P/N SP07000WG00 wei

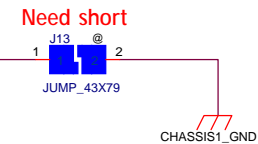
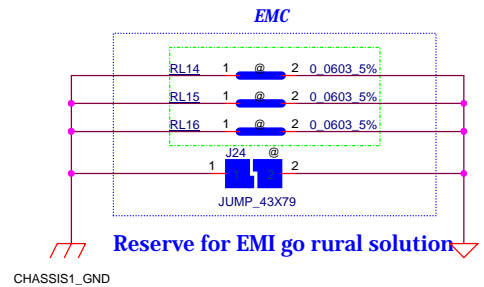
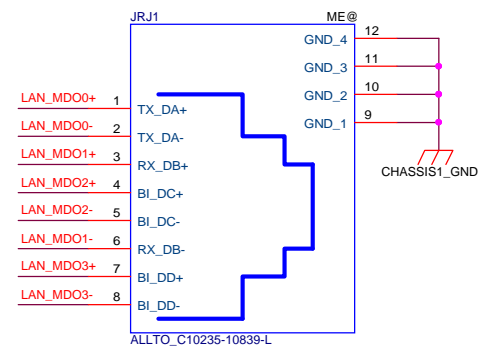
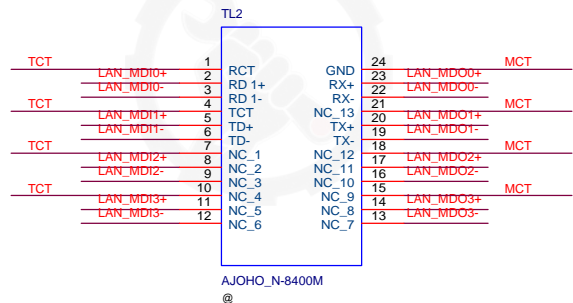


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change TL1 PN SP050008C00 to SP050009G00; TL1 is SP050008C00 footprint



TL2 co-lay TL1

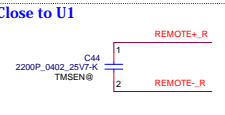


8/16 Update RJ45 P/N DC021608091 wei

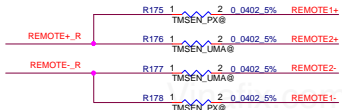
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THERMAL SENSOR

Close to U1

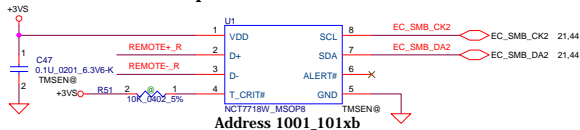


Set Thermal Sensor as a BOM Structure

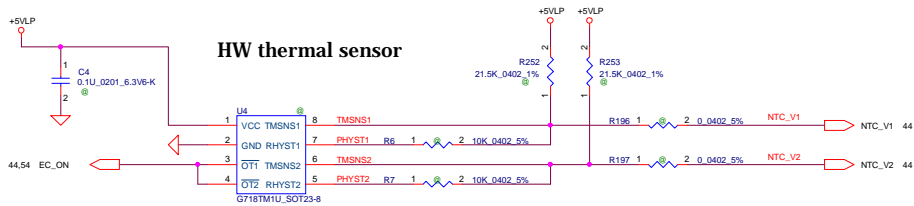


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

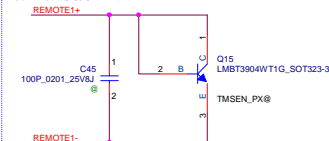


Address 1001_101xb

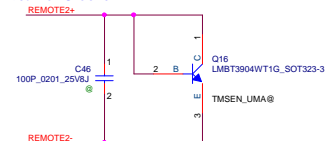


Over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold:
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

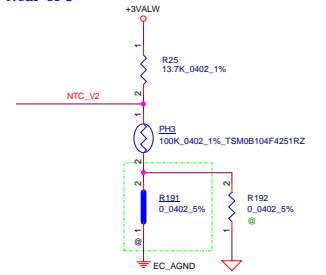
Near GPU&VRAM



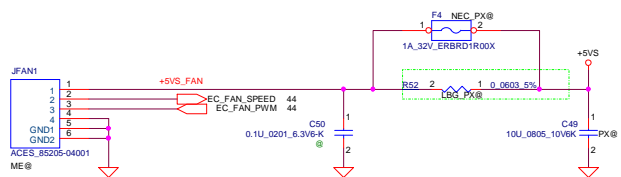
Near CPU Core



Near CPU

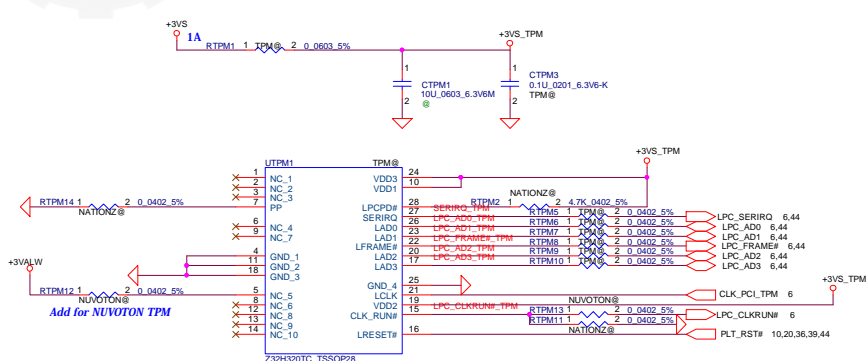


FAN Conn



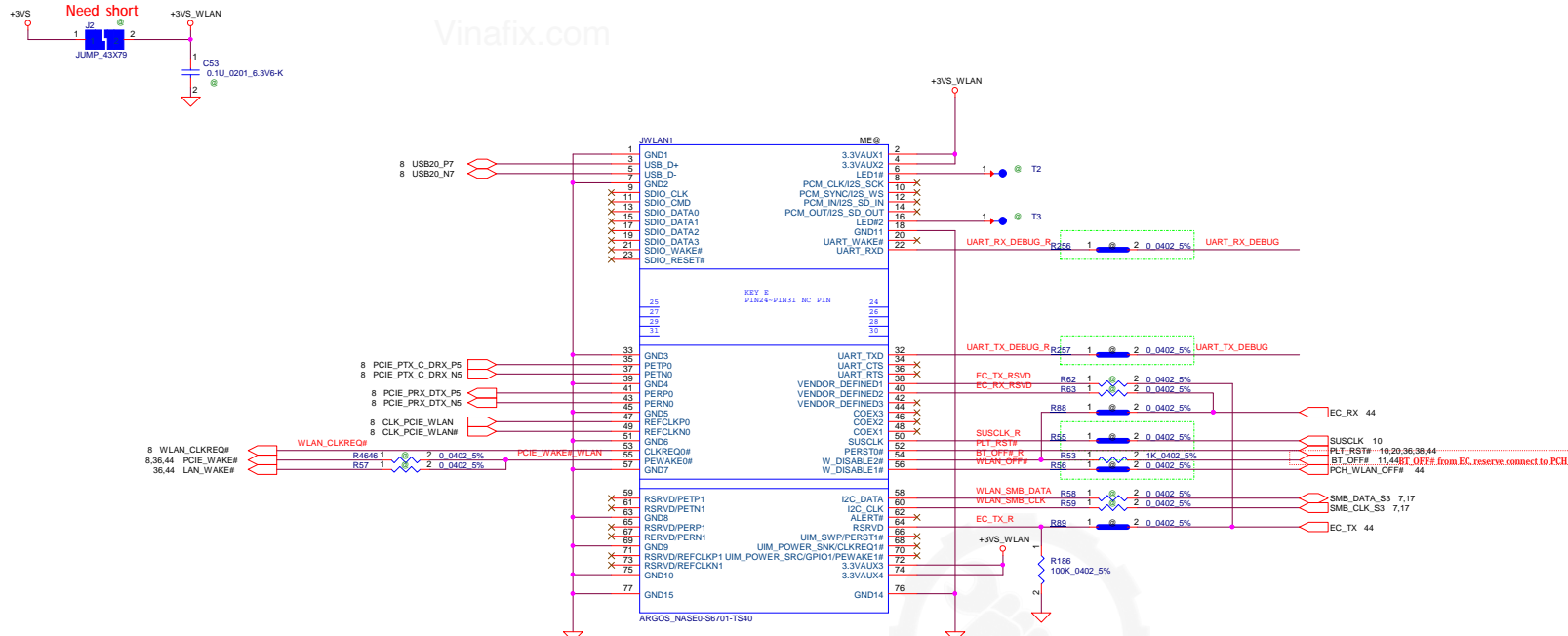
Update FAN conn. footprint to SP020008X0J
SP020012200 main source is SP020008X0J
Lewis 2016/10/14

TPM

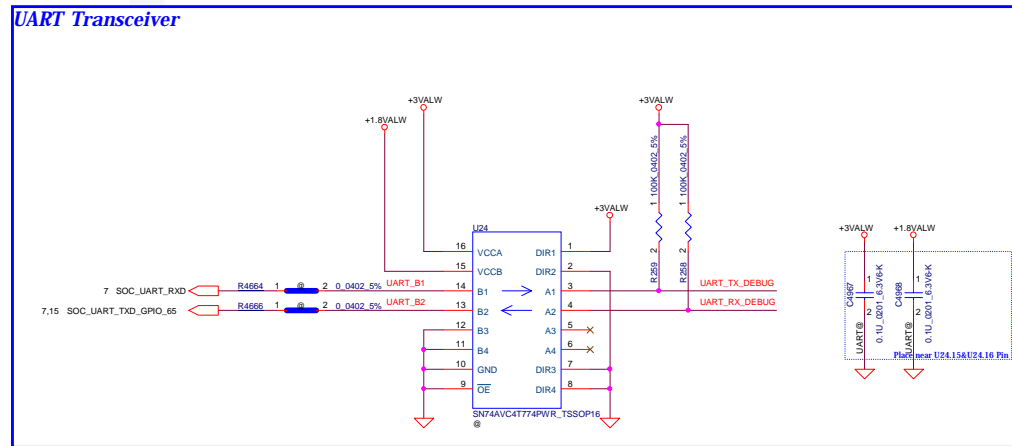


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN/TPM	
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Mini-Express Card(WLAN/WiMAX)



8/16 Update Conn. P/N SP070013200 wei
Copy DG421 symbol




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Vinafix.com



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				Date: Friday, March 02, 2018	Rev 1.0
				Sheet 40 of 60	

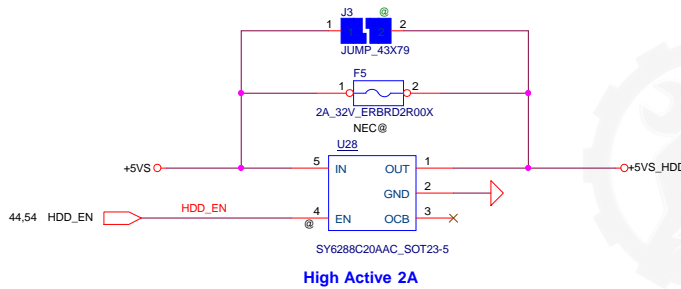
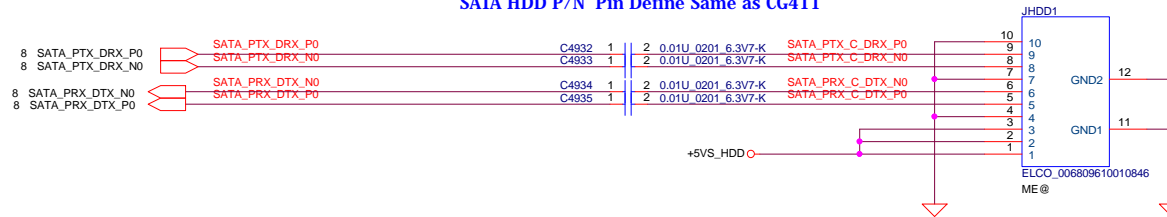
Vinafix.com



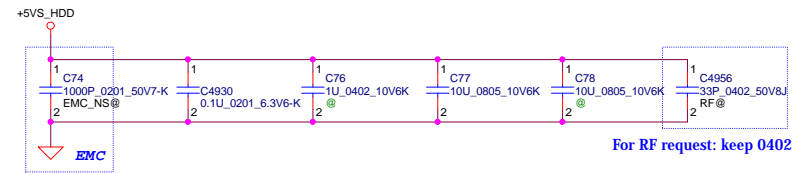
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Issued Date	2014/12/11	Deciphered Date	2015/12/11	Size		
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				Date:	Friday, March 02, 2018	Sheet

SATA HDD Conn.

SATA HDD P/N Pin Define Same as CG411

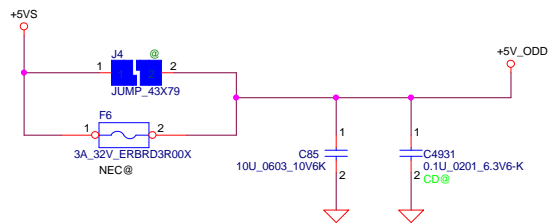


High Active 2A

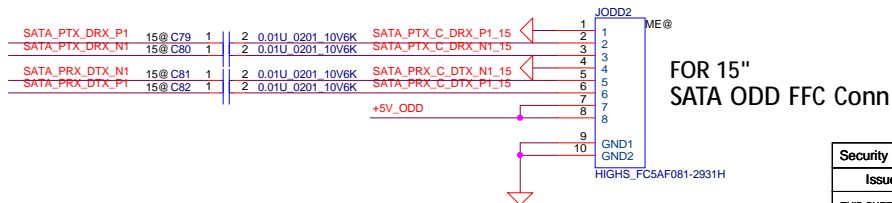
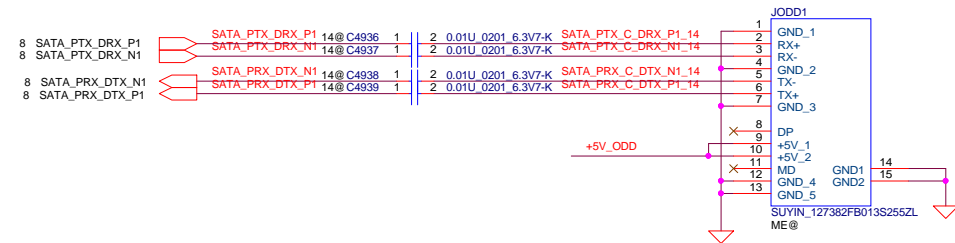


FOR RF request: keep 0402

+5VS to +5V_ODD



FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn


8/16 Update Conn. P/N SP01001YV00 wei

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	HDD/ODD CONN	
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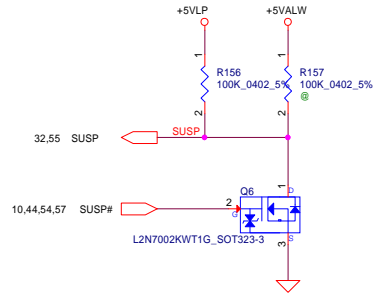
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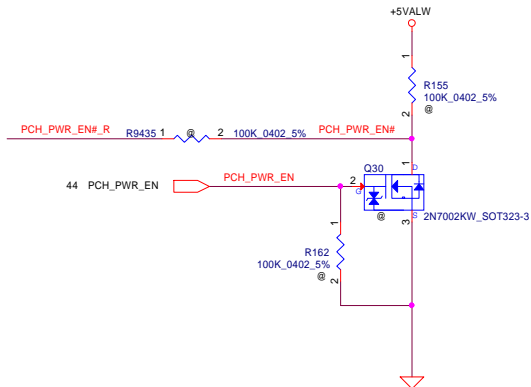
Title		
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Size	Document Number	Rev
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Delete +5VS/+3VS Load Switch

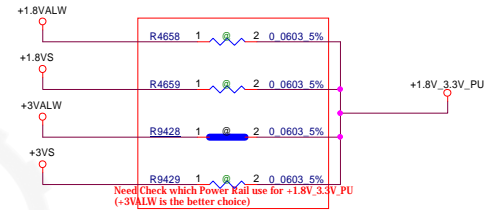


Vinafix.com

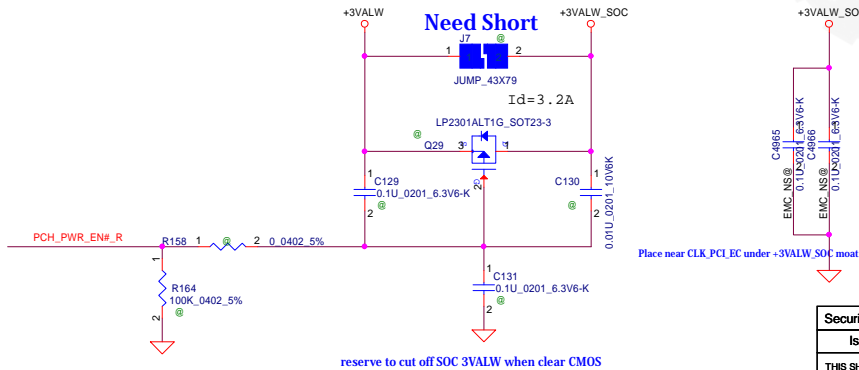
+3VALW to +3VALW_SOC



+1.8V_3.3V_PU Power Rail for 1.8/3.3 Select by Soft Strap



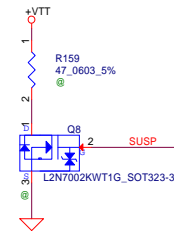
Need Short



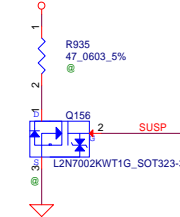
reserve to cut off SOC 3VALW when clear CMOS

For DisCharge

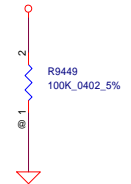
Need Check with power discharge




+1.2V



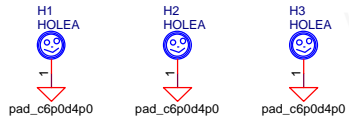
+2.5V_DDR



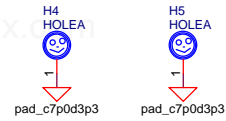
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Title		
DC V TO VS INTERFACE		
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Custom	EG431/EG532	1.0
Date:	Friday, March 02, 2018	Sheet 46 of 80

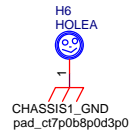
CPU Thermal Holes3



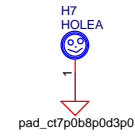
GPU Thermal Holes2



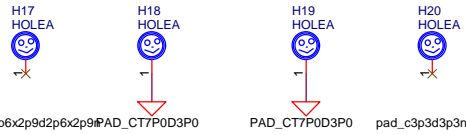
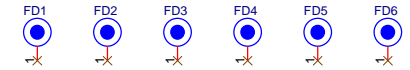
Close to RJ45



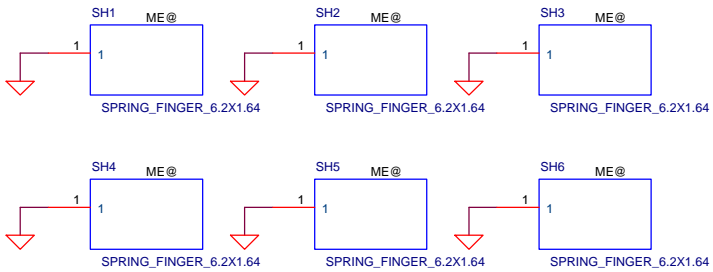
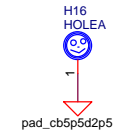
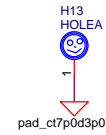
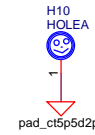
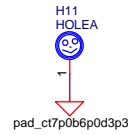
Close to Audio jack



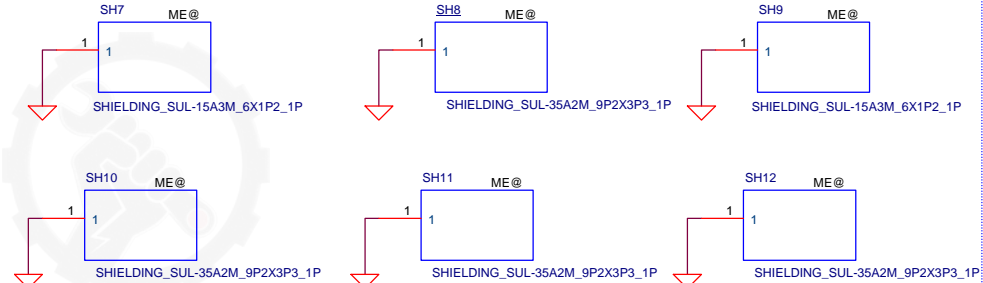
PCB Federal Mark PAD




WLAN Standoff

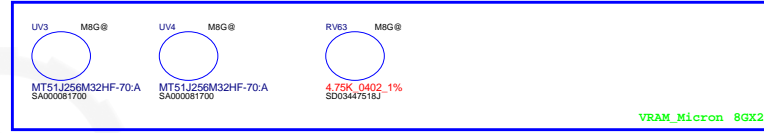
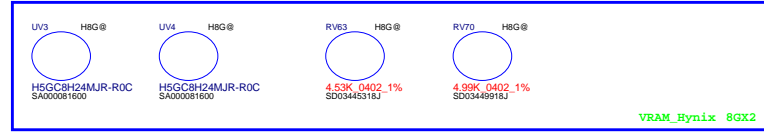
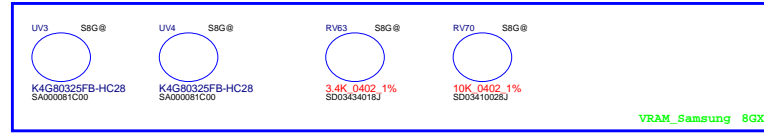
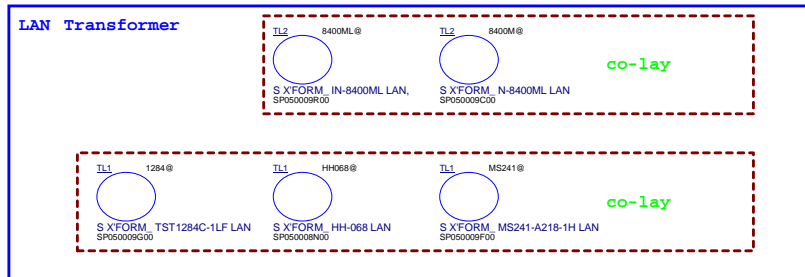
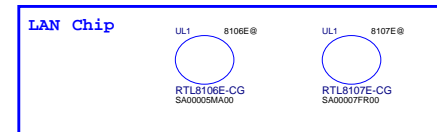
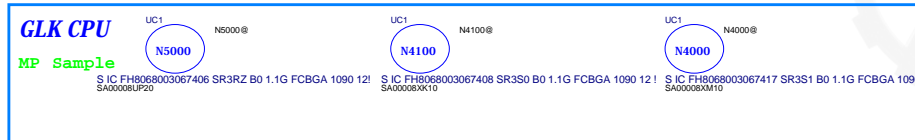
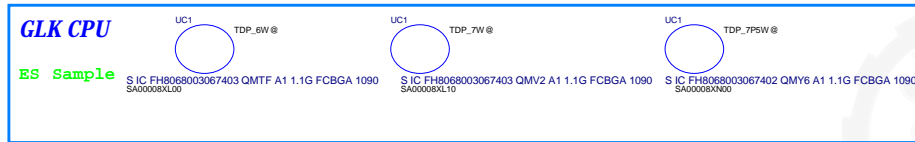
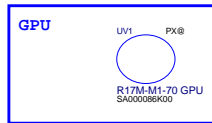
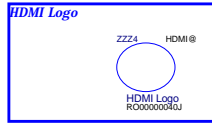
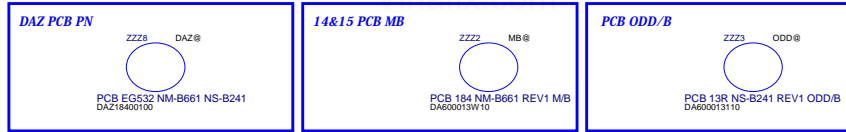


USB3.0 Shielding



DDR4 Shielding

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				Date:	Friday, March 02, 2018	Sheet 47 of 60




VRAM ID config

Memory Type	VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC8H24MJR-R0C	100	4.53K 4.99K
	Micron MT51J256M32HF-70:A	111	4.75K NC
	Samsung K4G80325FB-HC28	110	3.4K 10K
	000	NC	4.75K
	010	4.53K	2K
	001	8.45K	2K

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Size C	Document Number	Rev 1.0	
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Virtual symbol




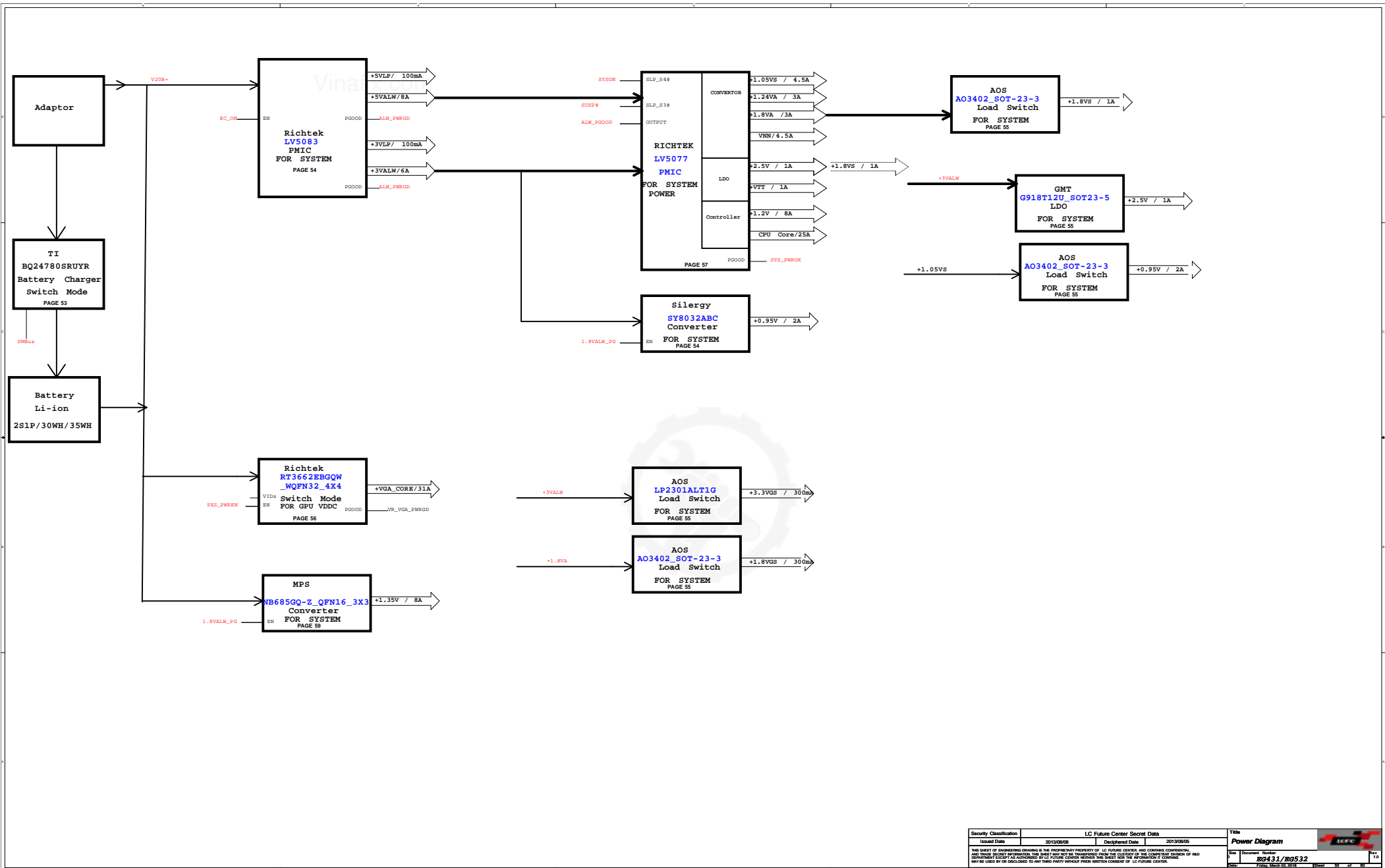
EG431/EG532

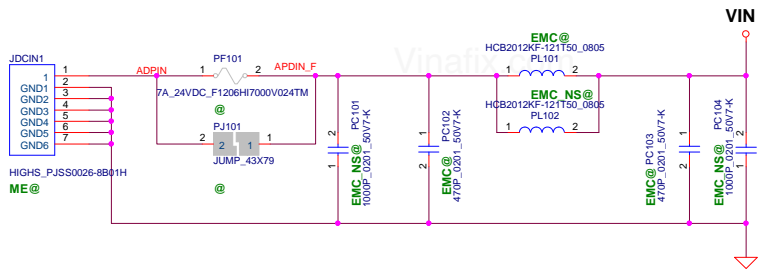
Vinafix.com



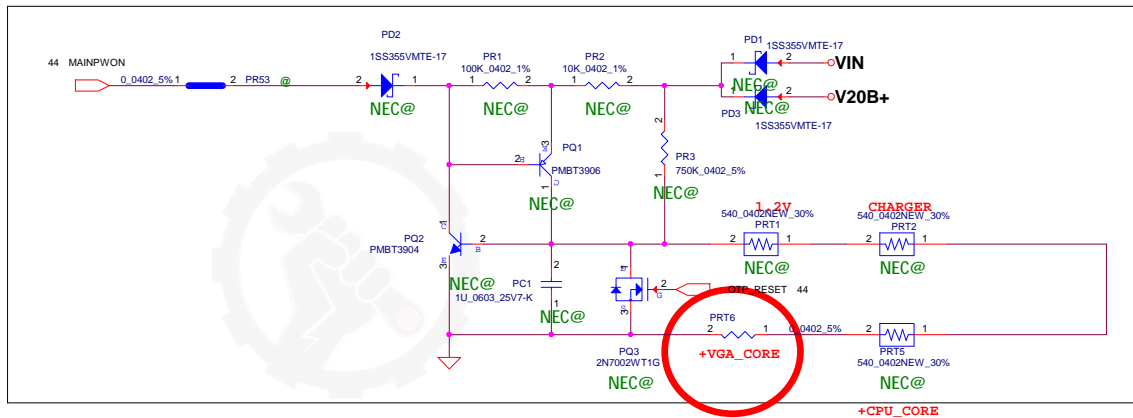
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Size	Document Number	Rev
Custom	EG431/EG532	1.0
Date:	Friday, March 02, 2018	Sheet 49 of 60

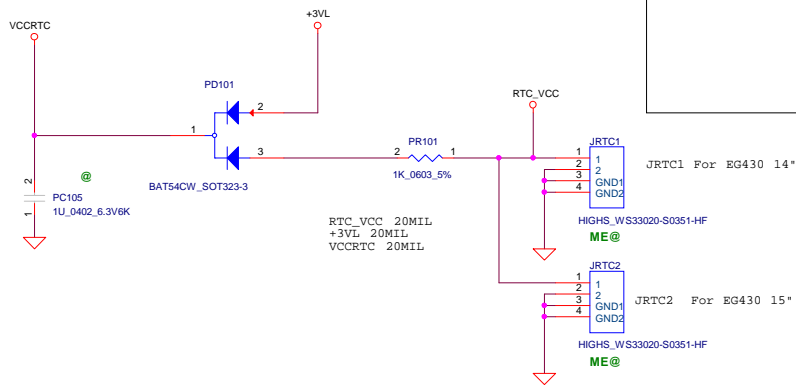




OTP

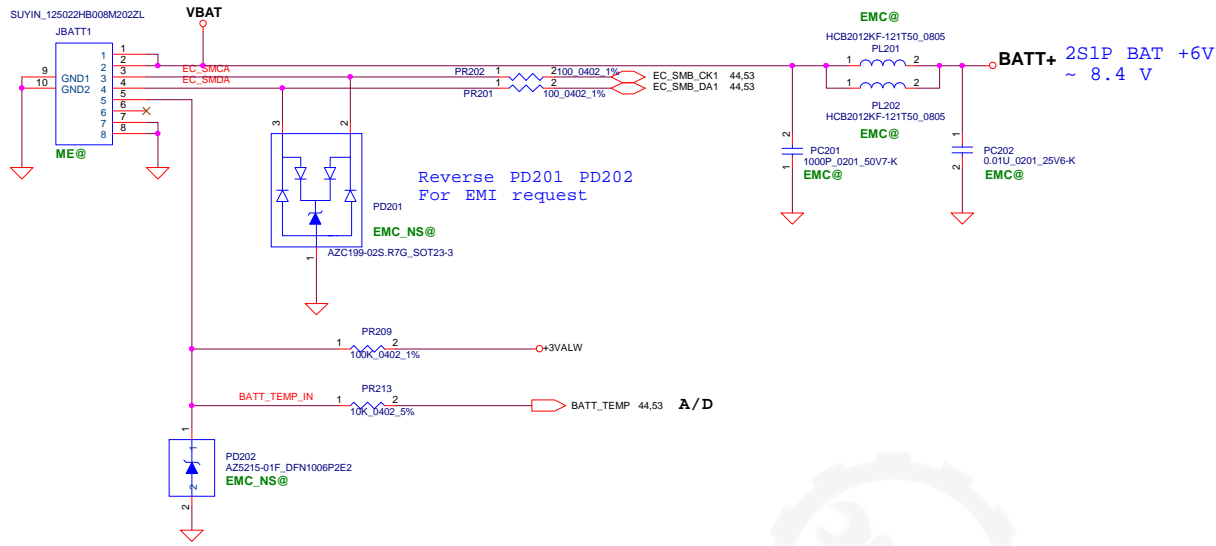


NEC NO DIS SKU change this NTC to Resistor.

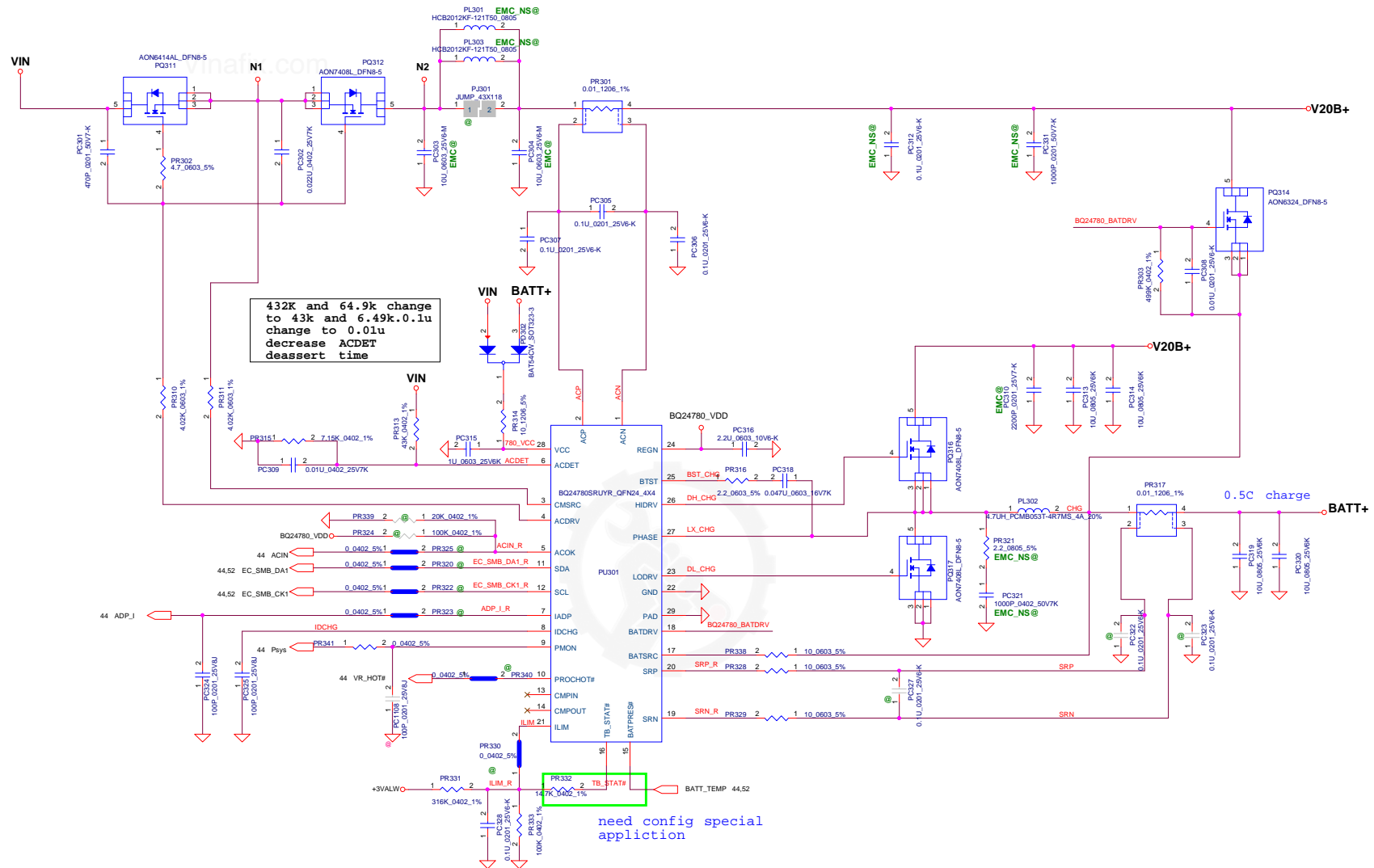


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Issued Date	2015/08/20	Deciphered Date 2016/08/20
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Title		
PWR-DCIN / RTC charger		
Size	Document Number	Rev
Custom	EG431/BG532	1.0
Date:	Friday, March 02, 2018	Sheet 51 of 60



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-BATTERY CONN/OTF LCFC	
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Size	Document Number	Rev		1.0	
Custom	EG431/BG532	Date:		Friday, March 02, 2018	
Date:			Sheet	52	of 60



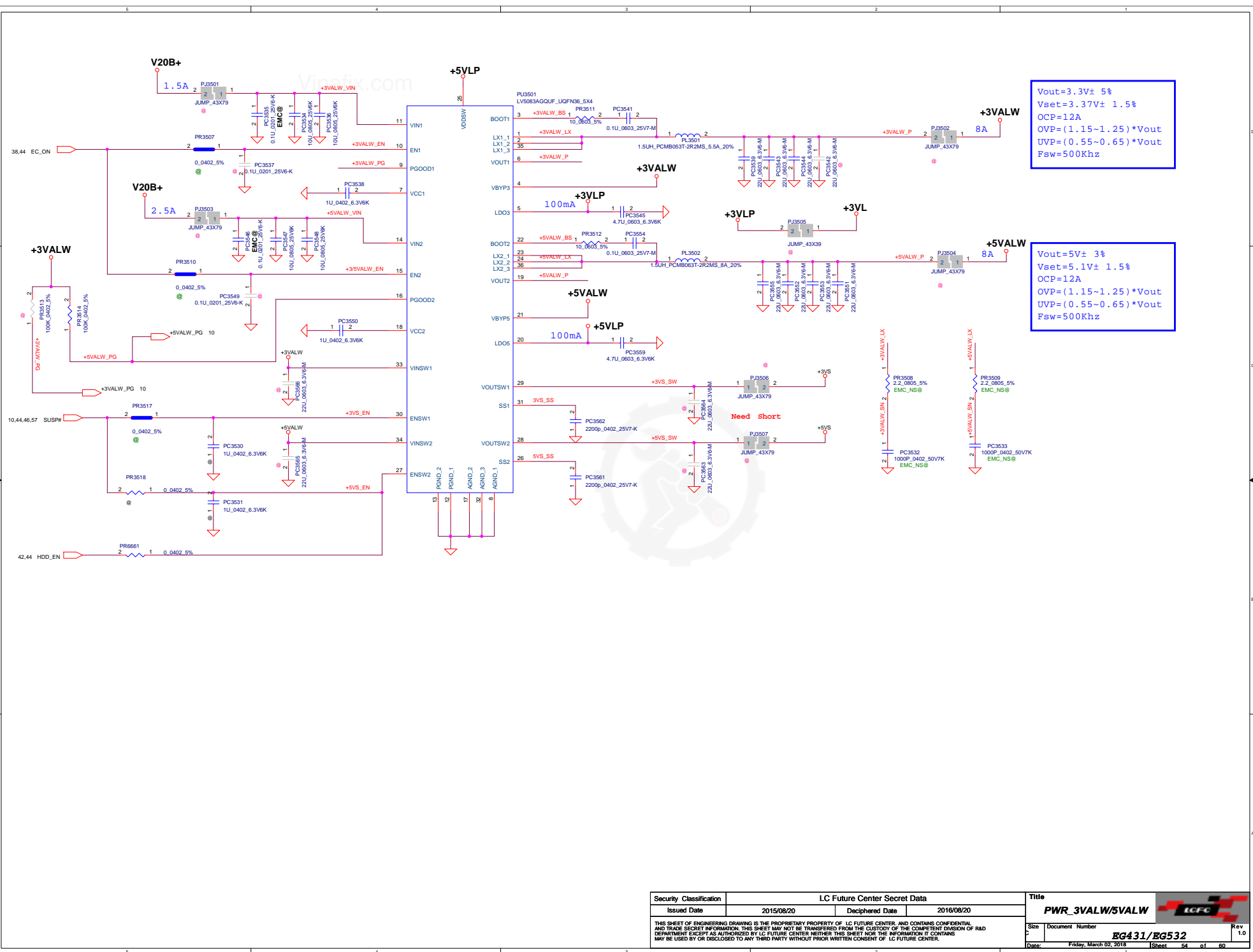
432k and 64.9k change to 43k and 6.49k. 0.1u change to 0.01u decrease ACDET deassert time

need config special application

Security Classification	LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date
2015/08/20		2016/08/20
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Title	PWR-CHARGER	
Size	Document Number	Rev
	EG431/EG532	1.0
Date:	Friday, March 02, 2016	Sheet 55 of 60



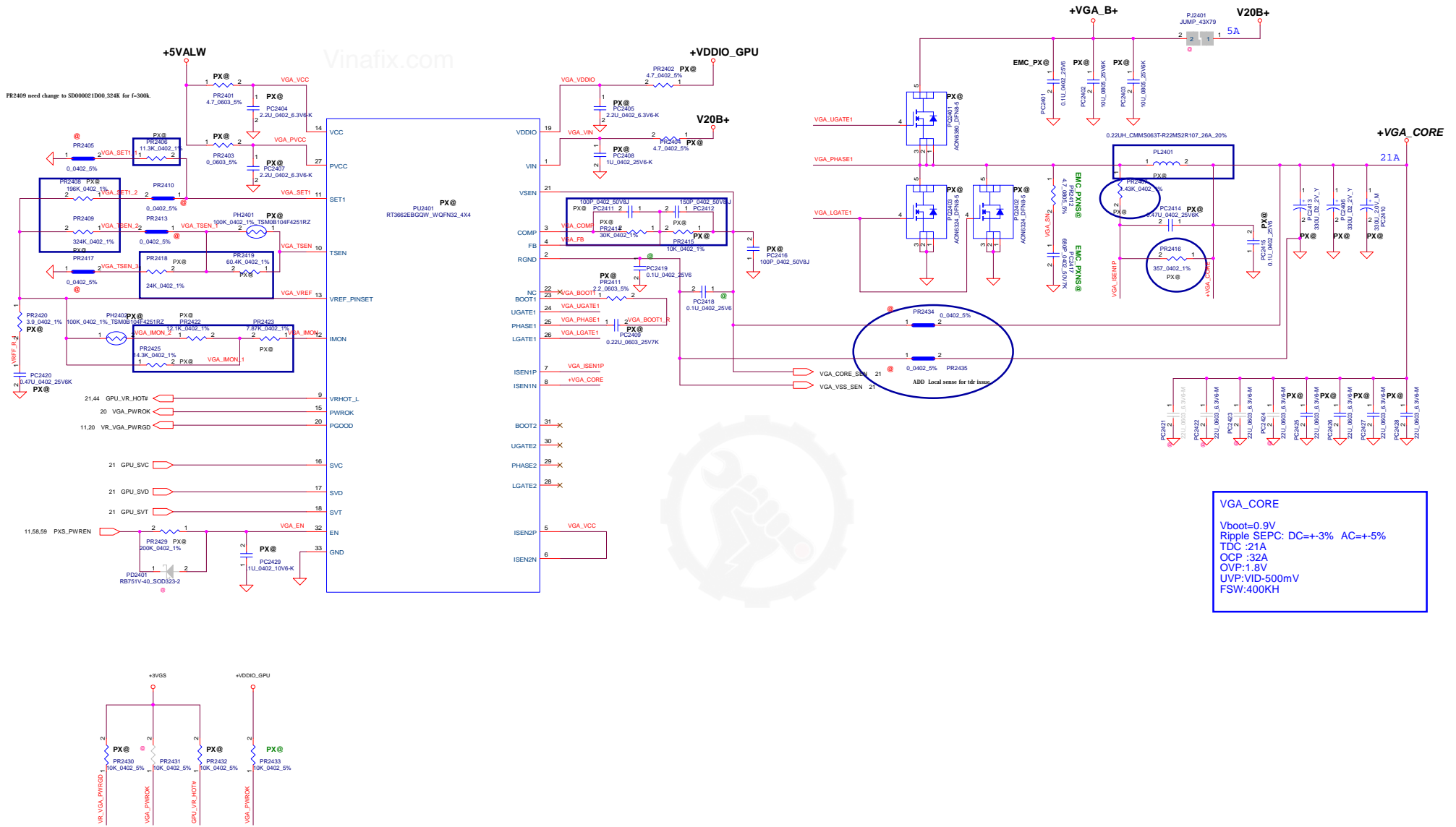


$V_{out} = 3.3V \pm 5\%$
 $V_{set} = 3.37V \pm 1.5\%$
 $OCP = 12A$
 $OVP = (1.15 \sim 1.25) * V_{out}$
 $UVP = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 500Khz$

$V_{out} = 5V \pm 3\%$
 $V_{set} = 5.1V \pm 1.5\%$
 $OCP = 12A$
 $OVP = (1.15 \sim 1.25) * V_{out}$
 $UVP = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 500Khz$

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR_3VALW/5VALW	
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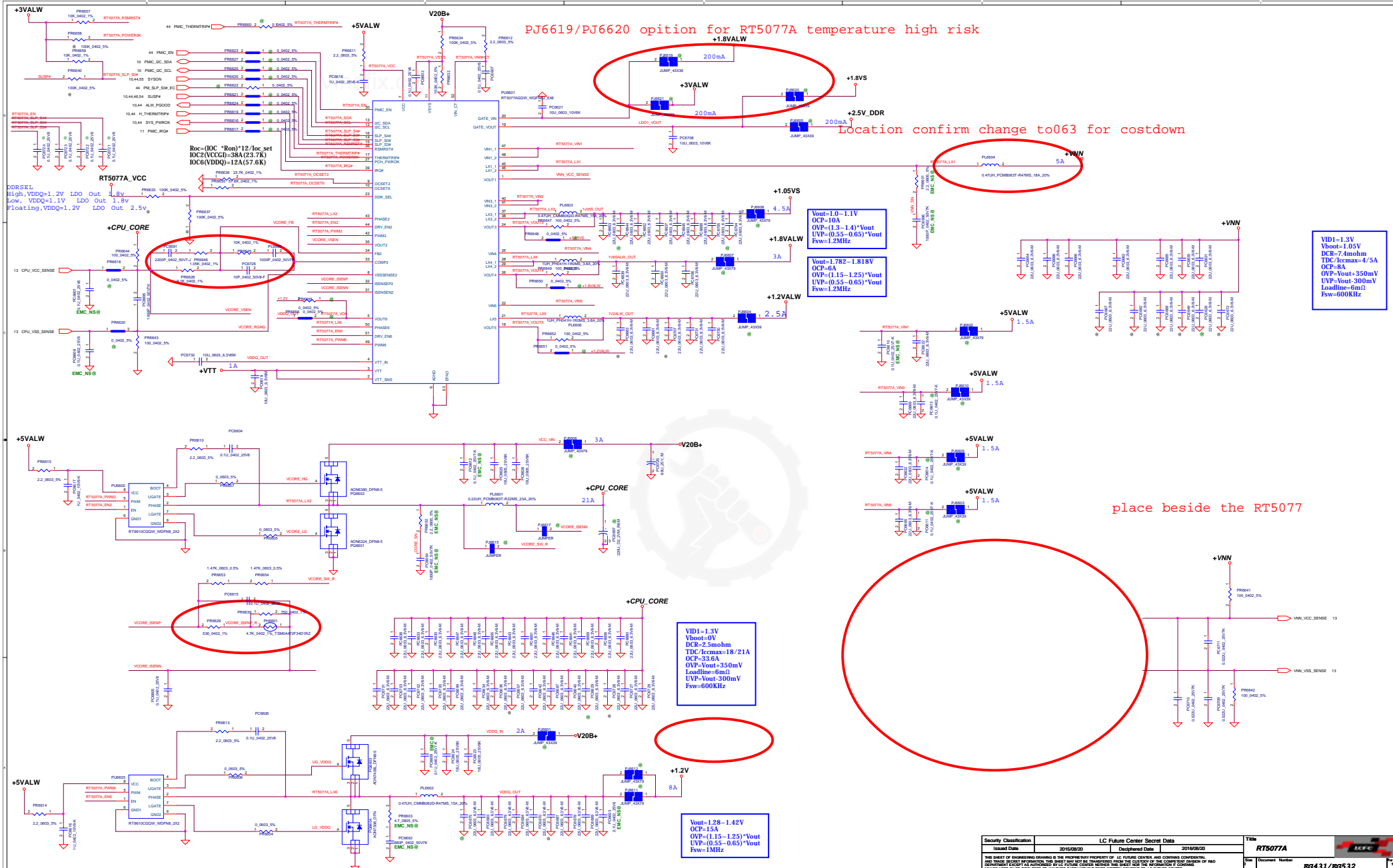
PR2409 need change to SD000021D00.324K for I-300K.



VGA_CORE
 Vboot=0.9V
 Ripple SEPC: DC=+3% AC=+5%
 IDC =21A
 OCP =32A
 OVP=1.8V
 LVP:VID=500mV
 FSW:400KH

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-VGA_CORE_AMD	
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PJ6619/PJ6620 option for RT5077A temperature high risk



Roc=(Ioc * Rth) * 12 / loc set
 Ioc2(VCCG)=38A(23.7K)
 Ioc6(VDDQ)=12A(57.6K)

DDRSEL High, VDDQ=1.2V LDO Out 1.8V
 Low, VDDQ=1.1V LDO Out 1.8V
 Floating, VDDQ=1.2V LDO Out 2.5V

Vout=1.0-1.1V
 OCP=10A
 OVP=(1.3-1.4)*Vout
 UVP=(0.55-0.65)*Vout
 Fsw=1.2MHz

Vout=1.782-1.818V
 OCP=6A
 OVP=(1.15-1.25)*Vout
 UVP=(0.55-0.65)*Vout
 Fsw=1.2MHz

VID1=1.3V
 Vboot=1.05V
 DCR=7.4mohm
 TDC/Icmax=4/5A
 OCP=6A
 OVP=Vout+350mV
 Loadline=6mV
 Fsw=600kHz

VID1=1.3V
 Vboot=0V
 DCR=2.5mohm
 TDC/Icmax=18/21A
 OCP=33.6A
 OVP=Vout+350mV
 Loadline=6mV
 UVP=Vout-300mV
 Fsw=600kHz

Vout=1.28-1.42V
 OCP=1.5A
 OVP=(1.15-1.25)*Vout
 UVP=(0.55-0.65)*Vout
 Fsw=1MHz

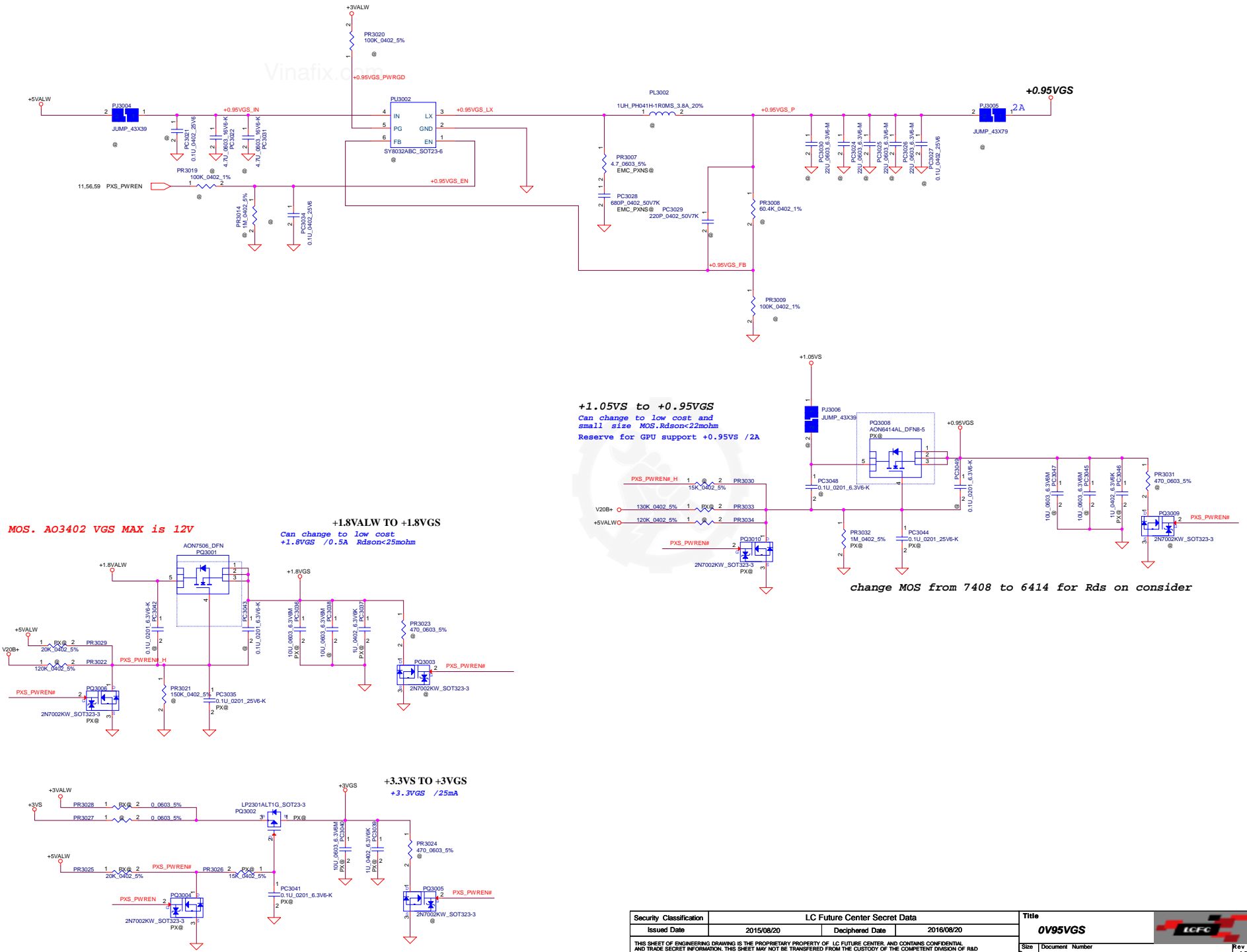


place beside the RT5077

Location confirm change to 063 for costdown

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Issued Date	2015/09/20	Designed Date	2016/09/20
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Vinafix




+1.05VS to +0.95VGS
 Can change to low cost and small size MOS. Rds on < 2mohm
 Reserve for GPU support +0.95VS / 2A

MOS. A03402 VGS MAX is 12V

+1.8VALW TO +1.8VGS
 Can change to low cost
 +1.8VGS / 0.5A Rds on < 25mohm

change MOS from 7408 to 6414 for Rds on consider

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20161216:SDV to SIT
1.p56-p57 add R=100ohm,C=680pF in FB pin;
2.pr3324 change to 55.4kohm,pr3323 change to 24.3k;
3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
5. GPU change 14 items to support AMD request.

20161219:SDV to SIT
1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT
1. PMIC change 1.24V Vin from 3VALW to1.8VALW;
2.change PR2431 from PX@ to @, PR2433 from @ to PX@,
3.change PR734 to @.

20170104:SDV to SIT
1. PMIC change LV5075B TO LV5075A



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