


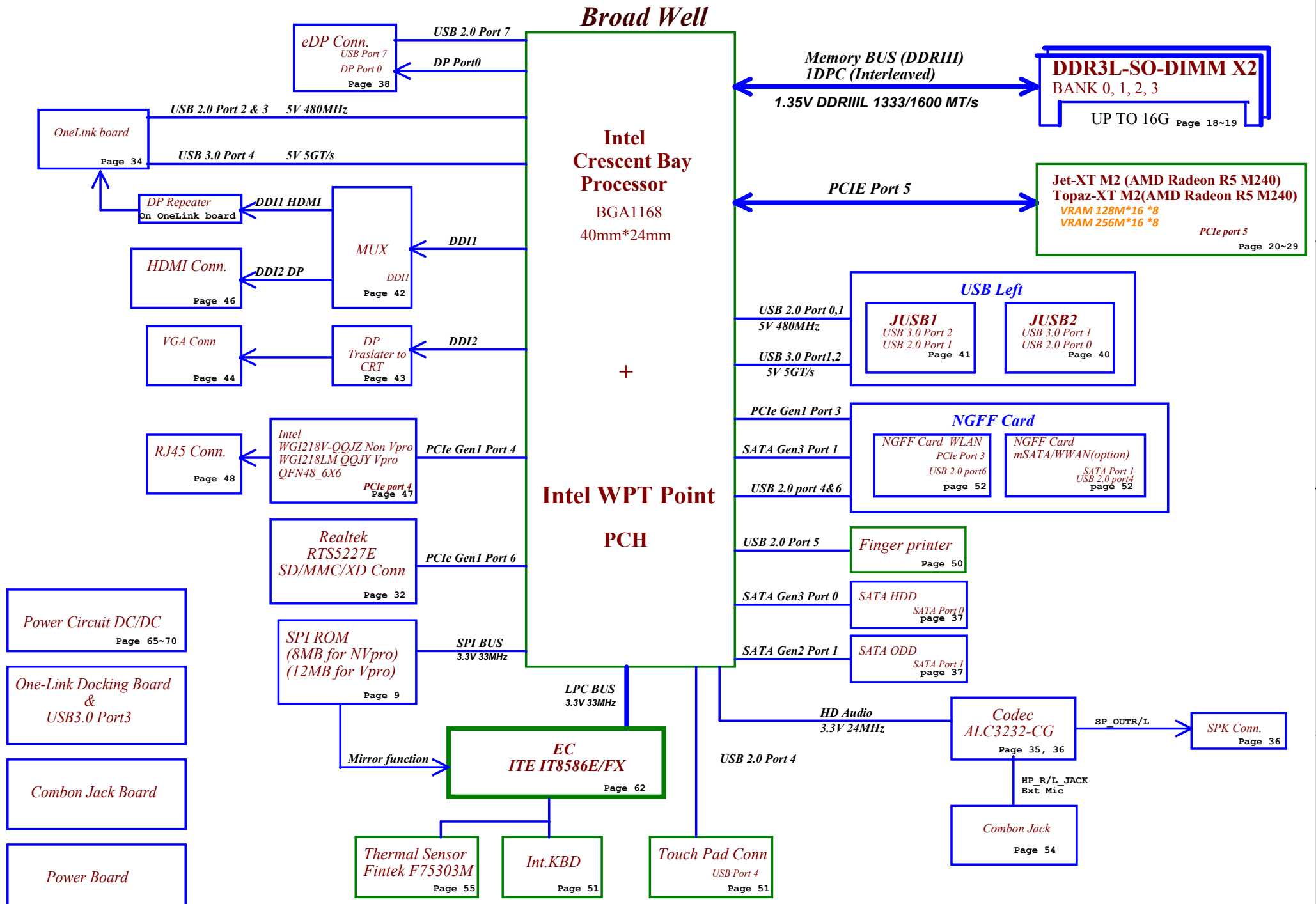
# *LCFC Confidential*

## *NM-A221 Rev1.0 Schematic*

*Intel Crescent Bay Processor with DDRIII + Wild Cat Point PCH  
AMD Opal-XT/ Jet-XT*

*2013-09-07 Rev1.0*

Security Classification	LC Future Center Secret Data		Title			
Issued Date	2013/09/07	Deciphered Date	2014/09/07		<b>COVER PAGE</b>	
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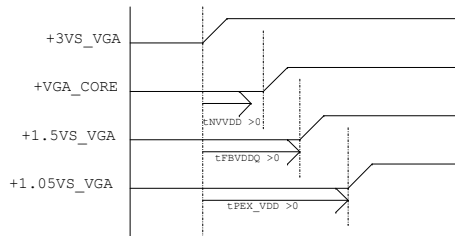
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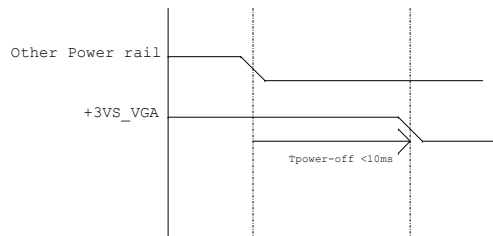


### VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms  
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

### Performance Mode P0 TDP at Tj = 102 C\* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID	setting	I2C Slave address ID
N13P-GT (28nm)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU	N13P-GT		
FB Memory (GDDR5)			
Samsung 2500MHz	K4G10325FG-HC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24MFR-T2C		
	64Mx32	PD 25K	

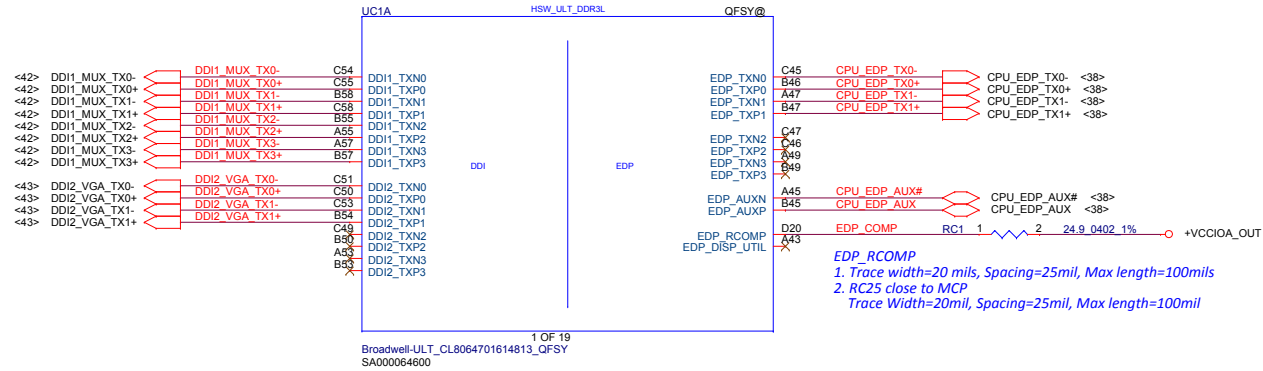
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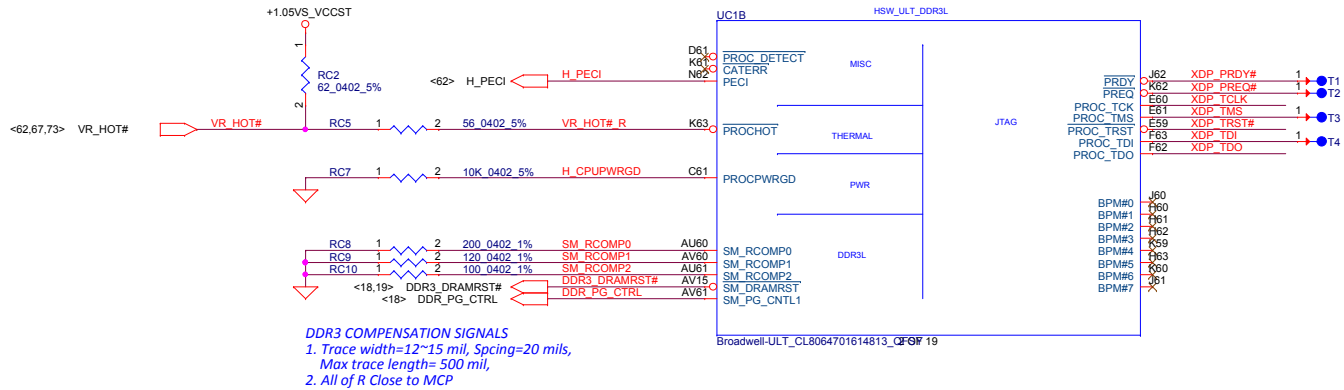
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For 14" : DOCKING  
For 15" : HDMI & DOCKING

For 14" : HDMI  
For 15" : VGA

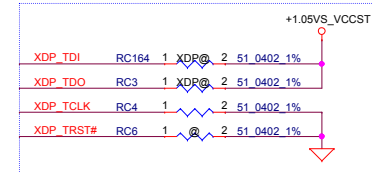


**EDP\_RCOMP**  
1. Trace width=20 mils, Spacing=25mil, Max length=100mils  
2. RC25 close to MCP  
Trace Width=20mil, Spacing=25mil, Max length=100mil



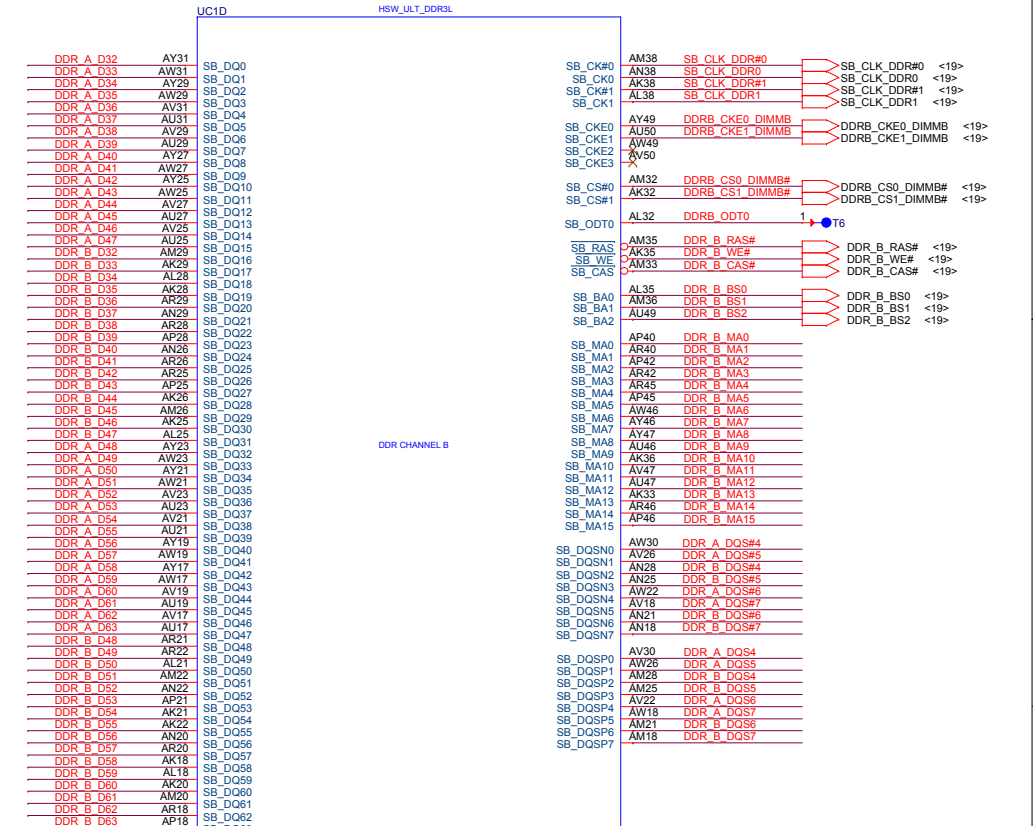
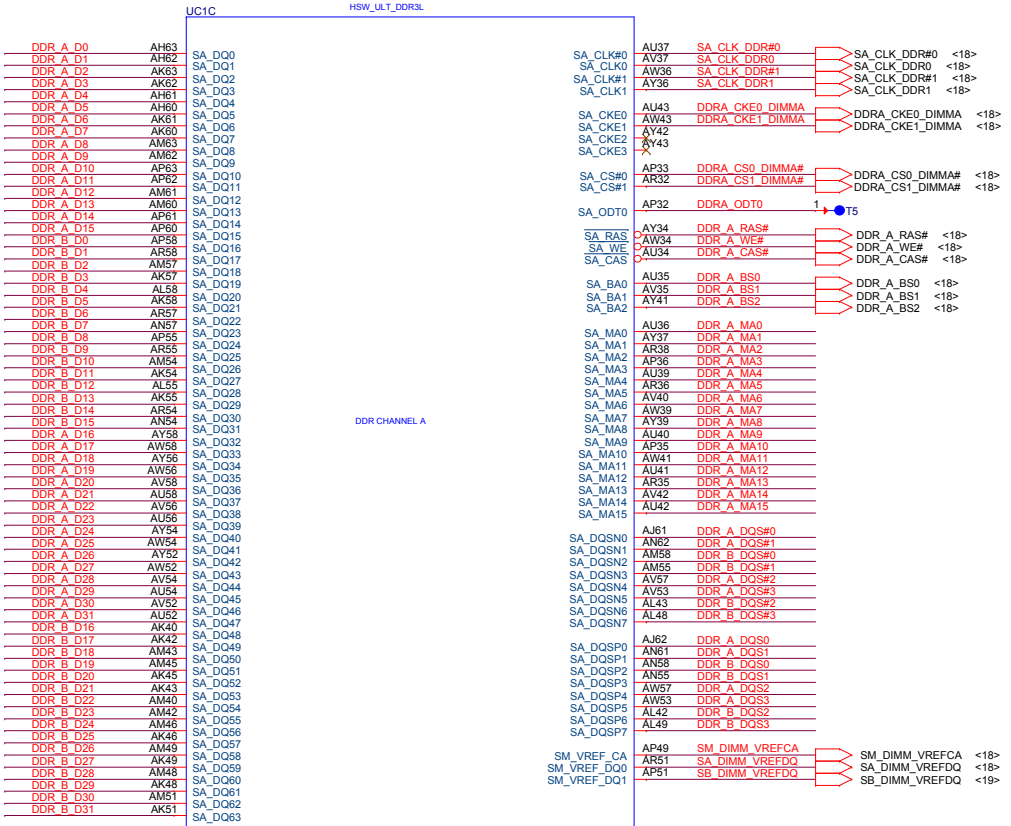
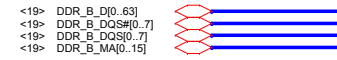
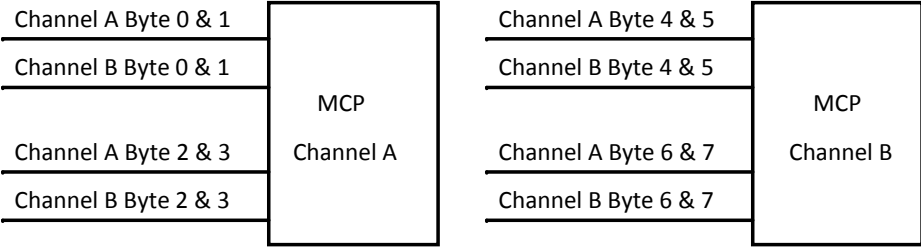
**DDR3 COMPENSATION SIGNALS**  
1. Trace width=12~15 mil, Spacing=20 mils,  
Max trace length= 500 mil,  
2. All of R Close to MCP

PU/PD Res. For CPU-XDP SIGNAL, Place R Closer to CPU



XDP PU/PD portion need to check again.

# Interleaved (Butterfly Topology) Broadwell Platform System Memory Interface Document Number: 528378 BDW U DDR3L/DDR3L-RS SO-DIMM Interleaved Recommendations

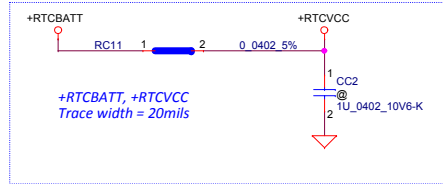


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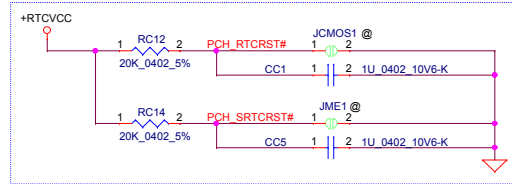
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Issued Date	2013/09/07	Deciphered Date		2014/09/07	BDW_DDR3L INT		
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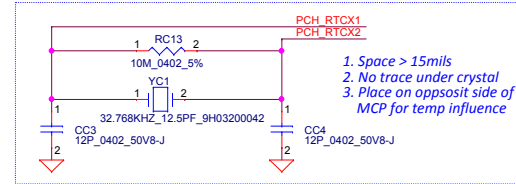
**RTC External Circuit**



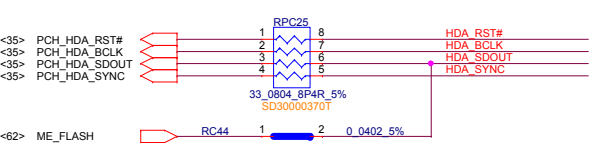
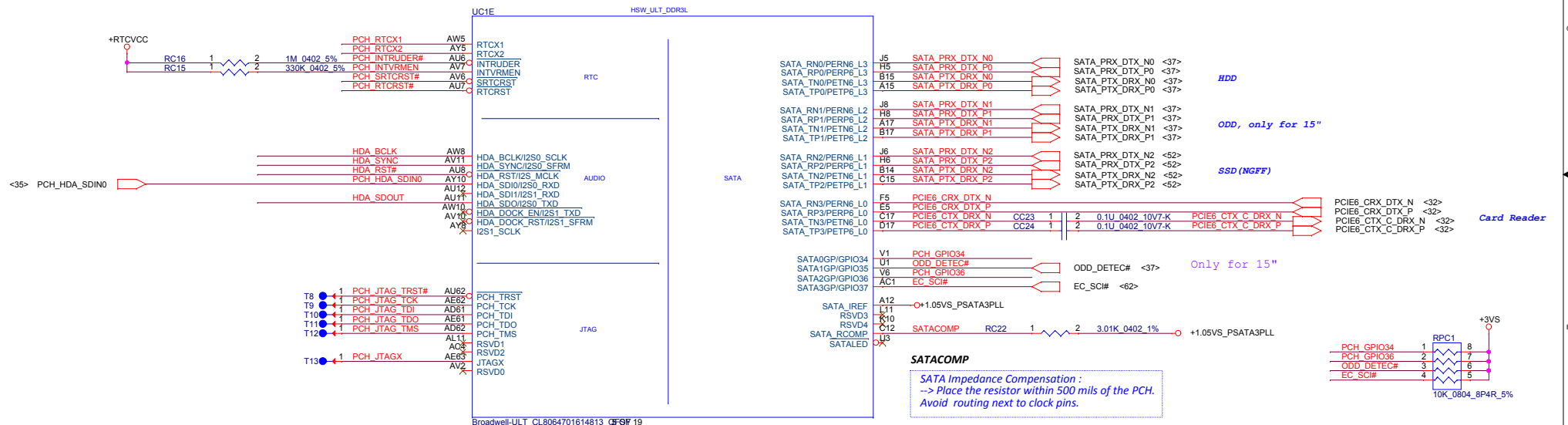
**JCMOS, JME Setting, Need Under DDR Door**



**RTC Crystal**



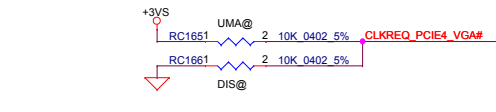
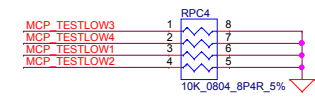
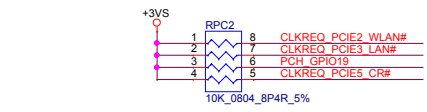
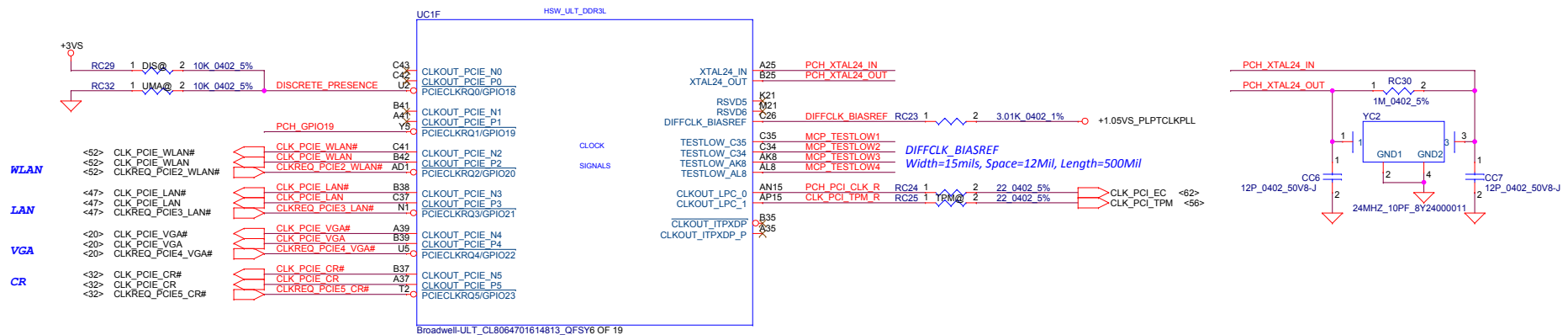
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**INTVRMEN**

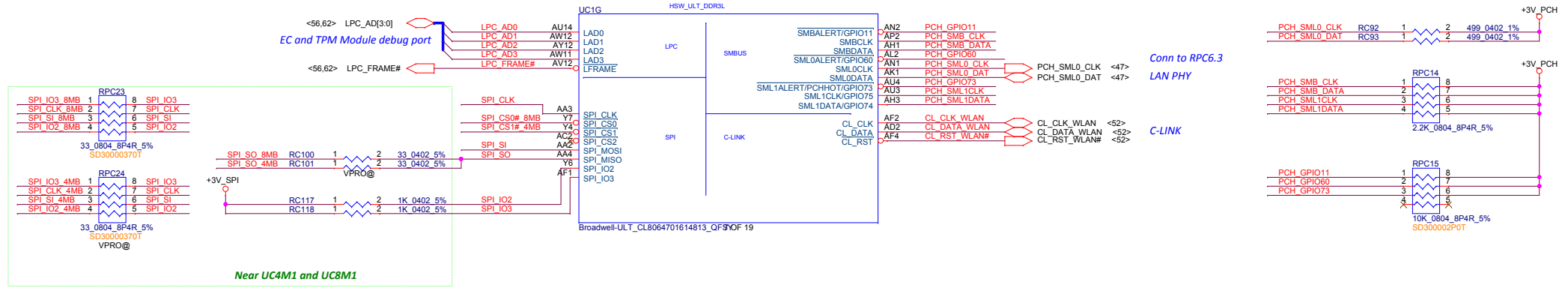
1. INTVRMEN, should always be pull high
  - \* H Integrated VRM enable (Default)
  - L Integrated VRM disable
2. Internal Voltage Regulator Enable:  
This signal enables the internal 1.05 V regulators.

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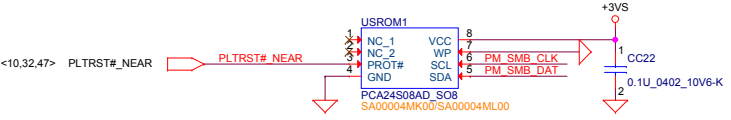


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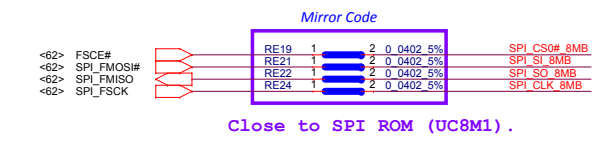
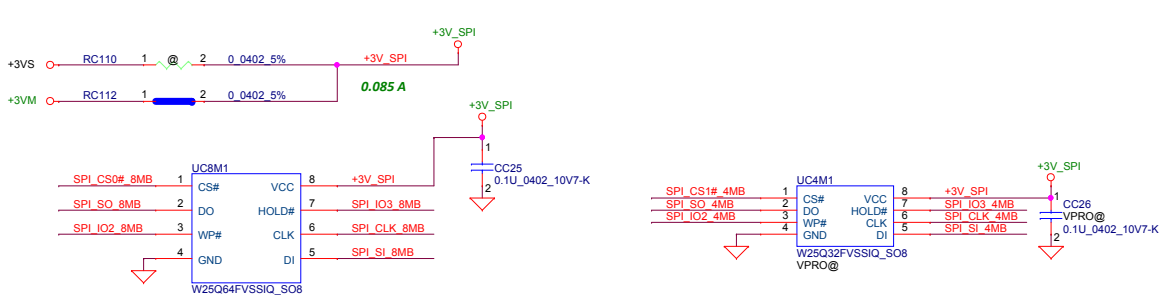




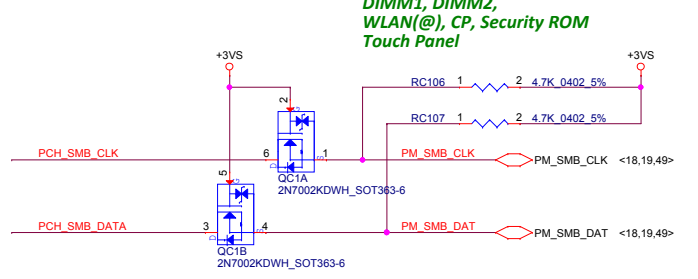
**Security ROM**



**M3 Support + Intel LAN PHY / Wireless LAN Solution**

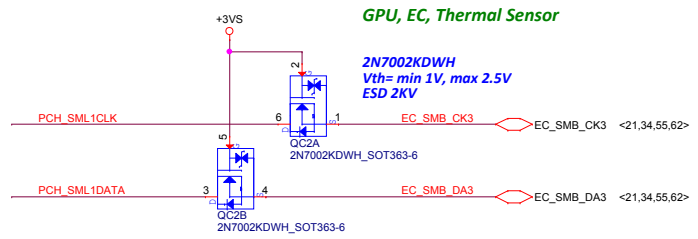


**SM Bus**

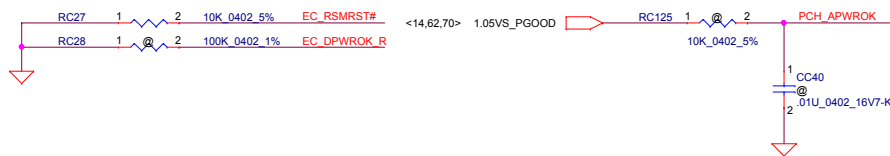
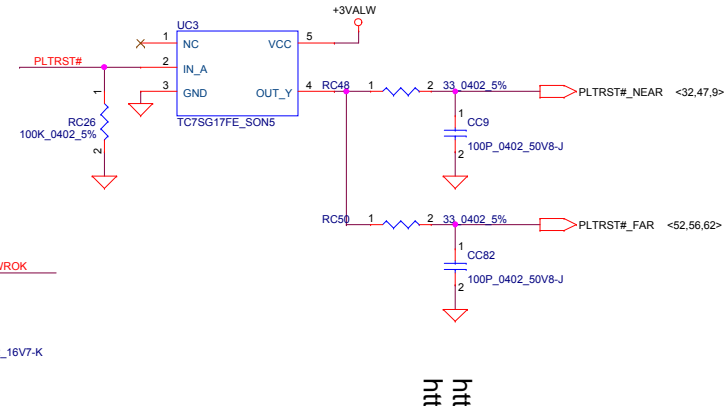
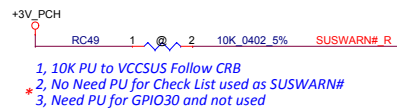
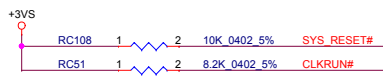
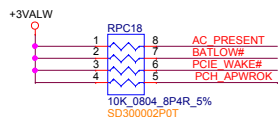
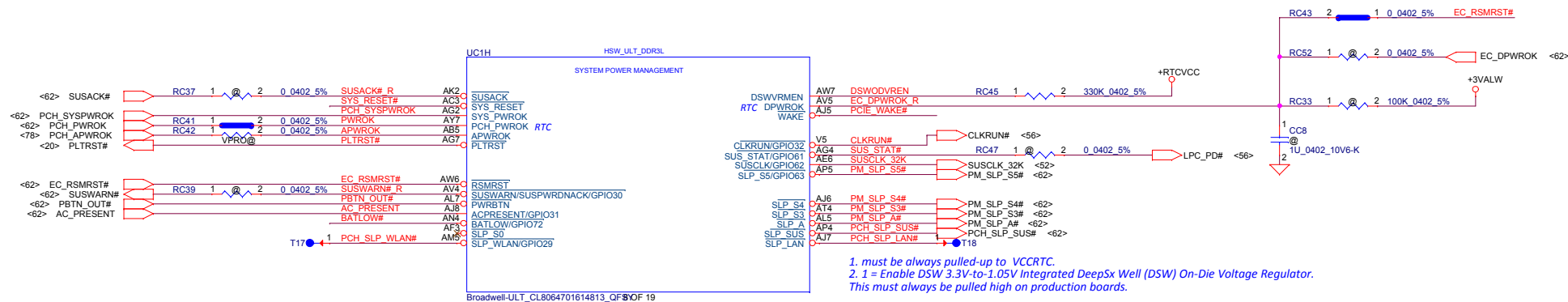


**DIMM1, DIMM2, WLAN(@), CP, Security ROM Touch Panel**

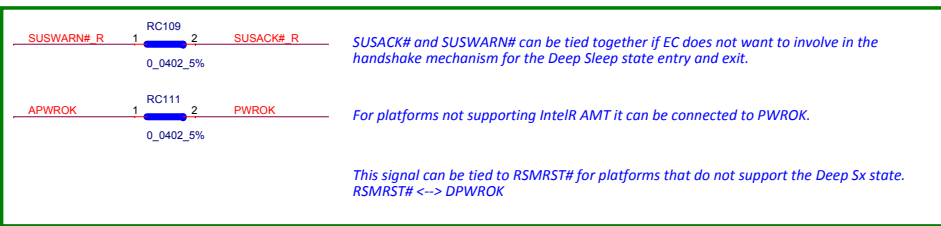
**GPU, EC, Thermal Sensor**



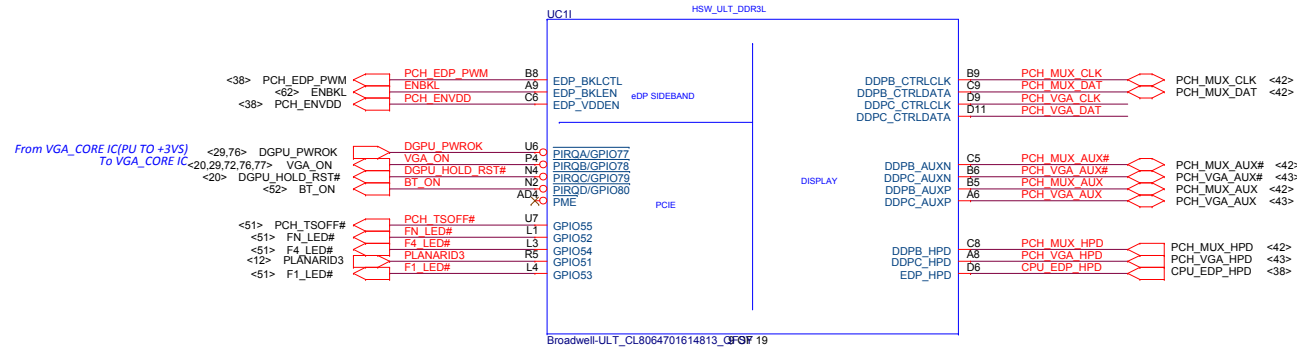
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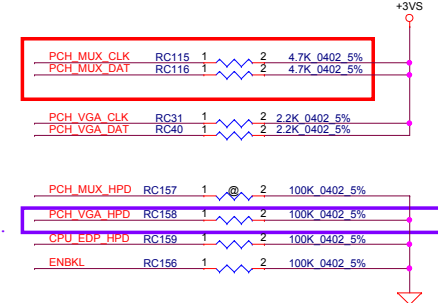
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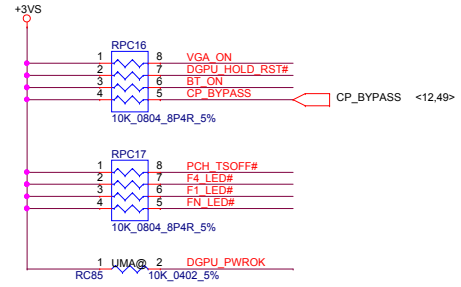
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1. 鐵VENDOR 鐵板PU , 鐵板Vih anf Vil Tmeet SPEC value.
2. Vender fine tune recommend value.(Pass Through Mode)
3. Vendor recommend use PU 4.7K ohm. (10/1) Intel Spec is PU 2.2K ohm



After testing, check if can un-stuff.

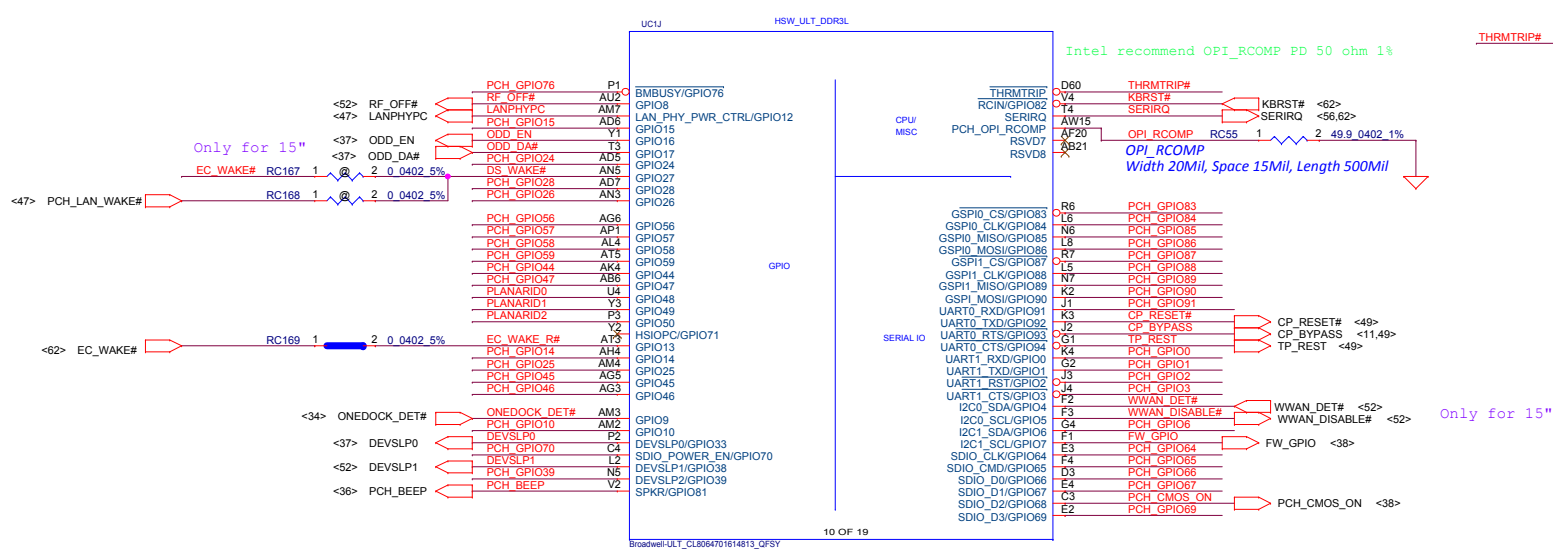


DDPB\_CTRLDATA: Port B Detected  
 DDPC\_CTRLDATA: Port C Detected

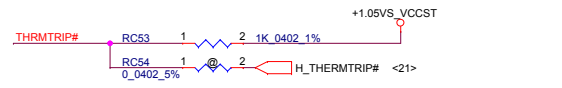
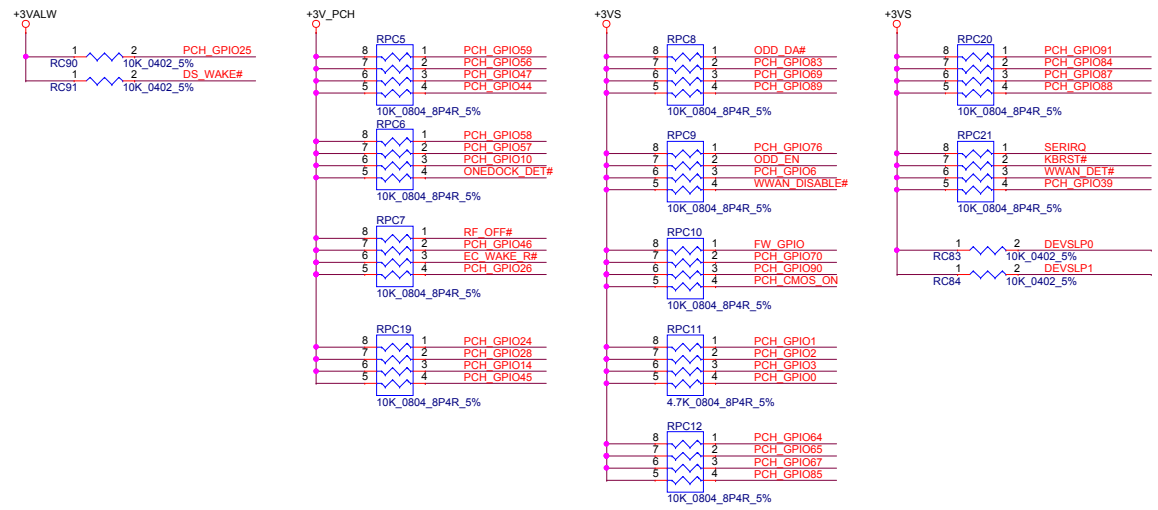
\* 1: Port B or C is detected  
 0: Port B or C is not detected

Internal PD 15K~40K, nominal 20K

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	SATA Port
DEVSLP0	SATA Port 0
DEVSLP1	SATA Port 1

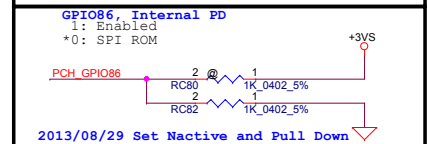
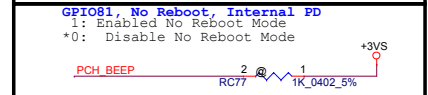
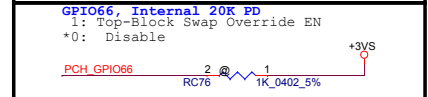
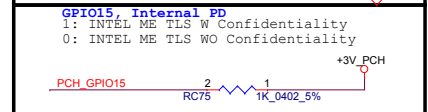
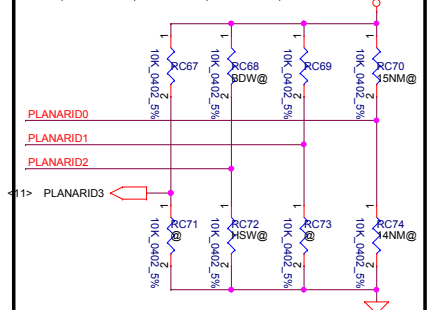


Intel recommend OPI\_RCOMP PD 50 ohm 1%

OPI\_RCOMP  
Width 20Mil, Space 15Mil, Length 500Mil

Only for 15"

Planar ID			
PLANARID0 (GPIO48)	GPIO18	PLANARID2 (GPIO50)	PLANARID3 (GPIO51)
0	14"	UMA	HSW
1	15"	OPT	BDW



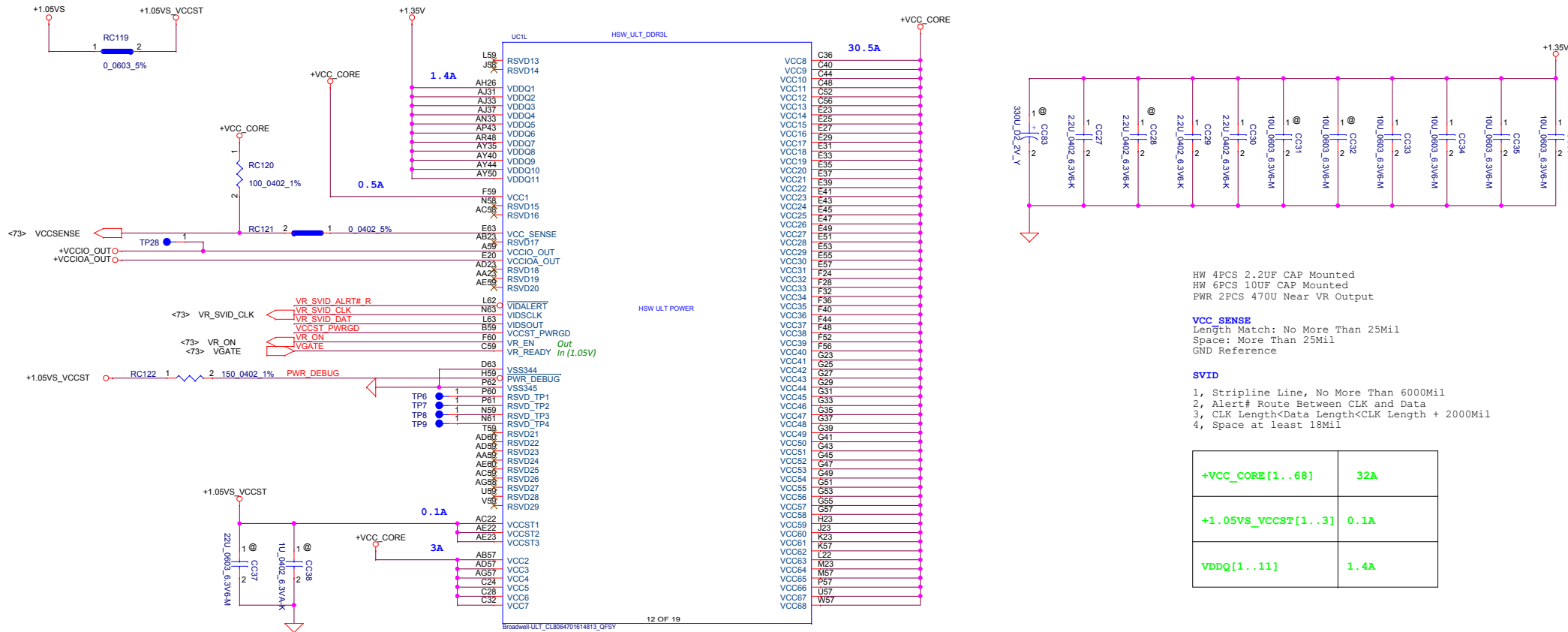
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Title	<b>BDW_GPIO/SIO</b>
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# Haswell MCP (Power)



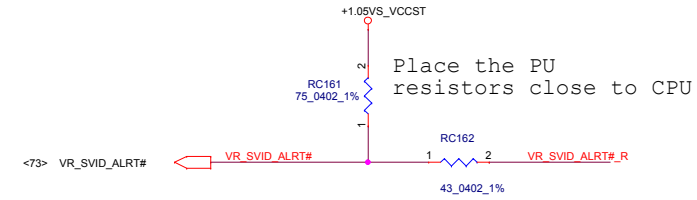
HW 4PCS 2.2UF CAP Mounted  
 HW 6PCS 10UF CAP Mounted  
 PWR 2PCS 470U Near VR Output

**VCC SENSE**  
 Length Match: No More Than 25Mil  
 Space: More Than 25Mil  
 GND Reference

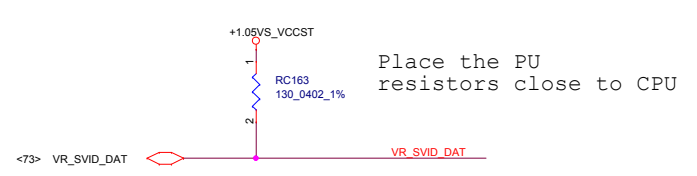
**SVID**  
 1, Stripline Line, No More Than 6000Mil  
 2, Alert# Route Between CLK and Data  
 3, CLK Length<Data Length<CLK Length + 2000Mil  
 4, Space at least 18Mil

+VCC_CORE[1..68]	32A
+1.05VS_VCCST[1..3]	0.1A
VDDQ[1..11]	1.4A

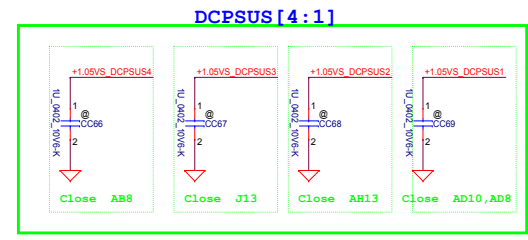
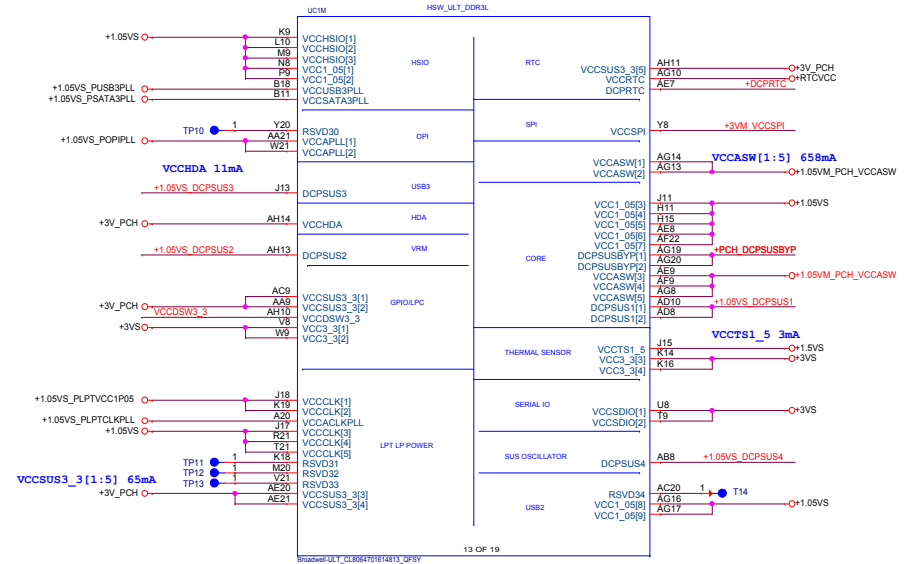
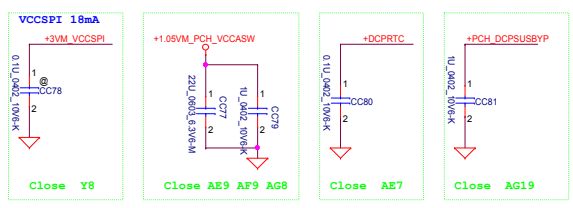
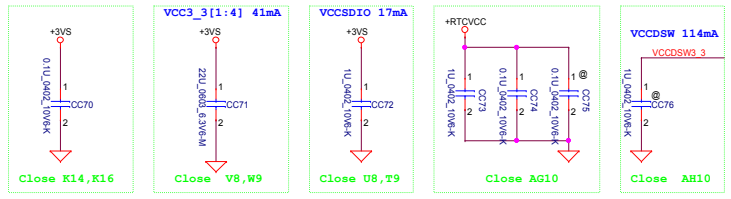
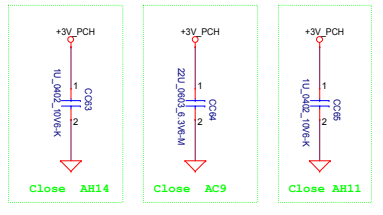
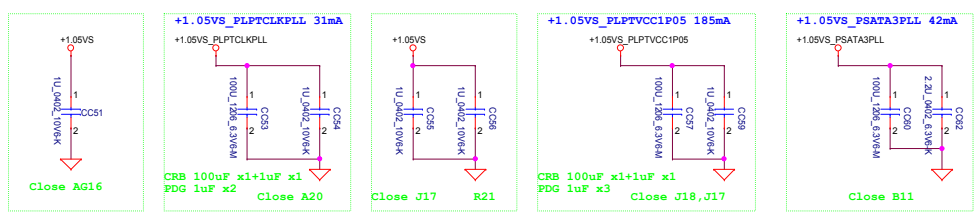
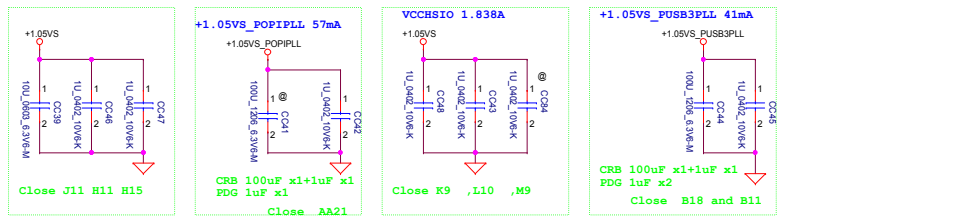
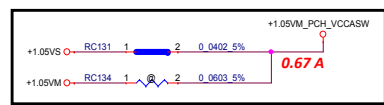
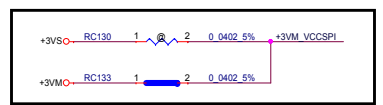
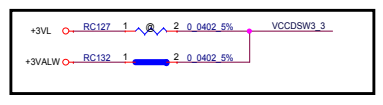
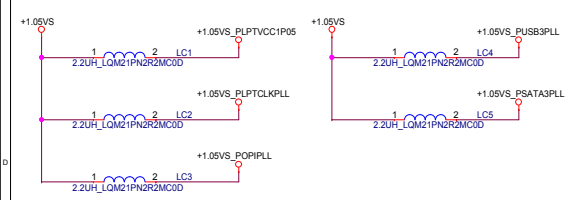
## SVID ALERT



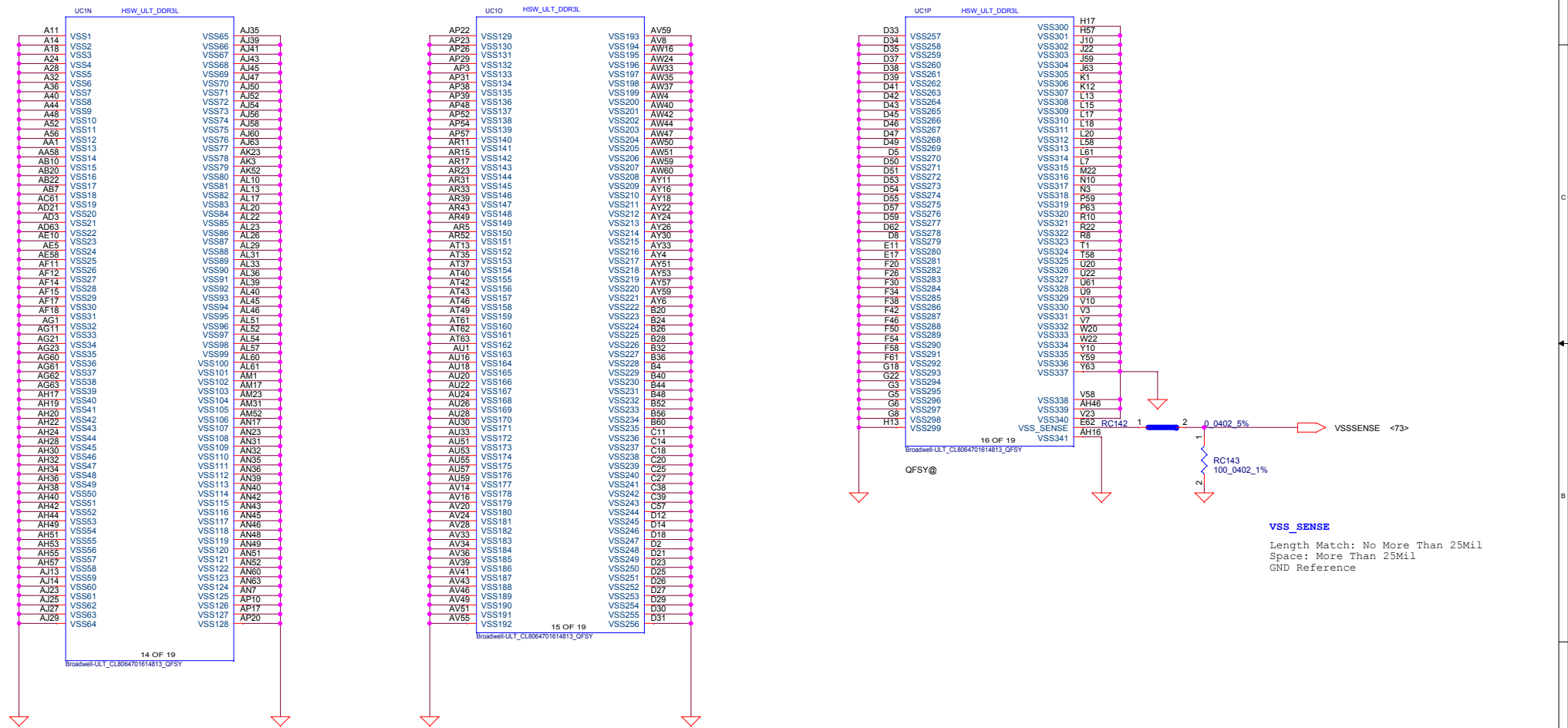
## SVID DATA



**Haswell MCP (Power2)**

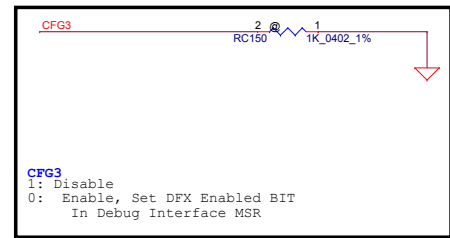
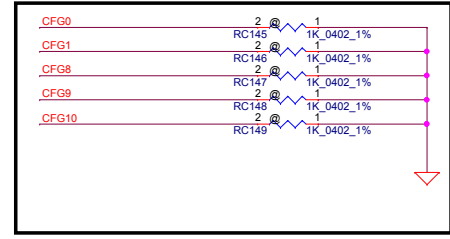
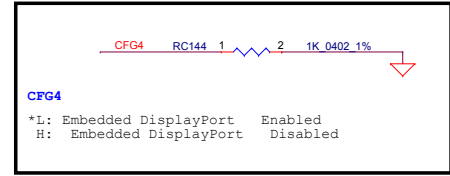
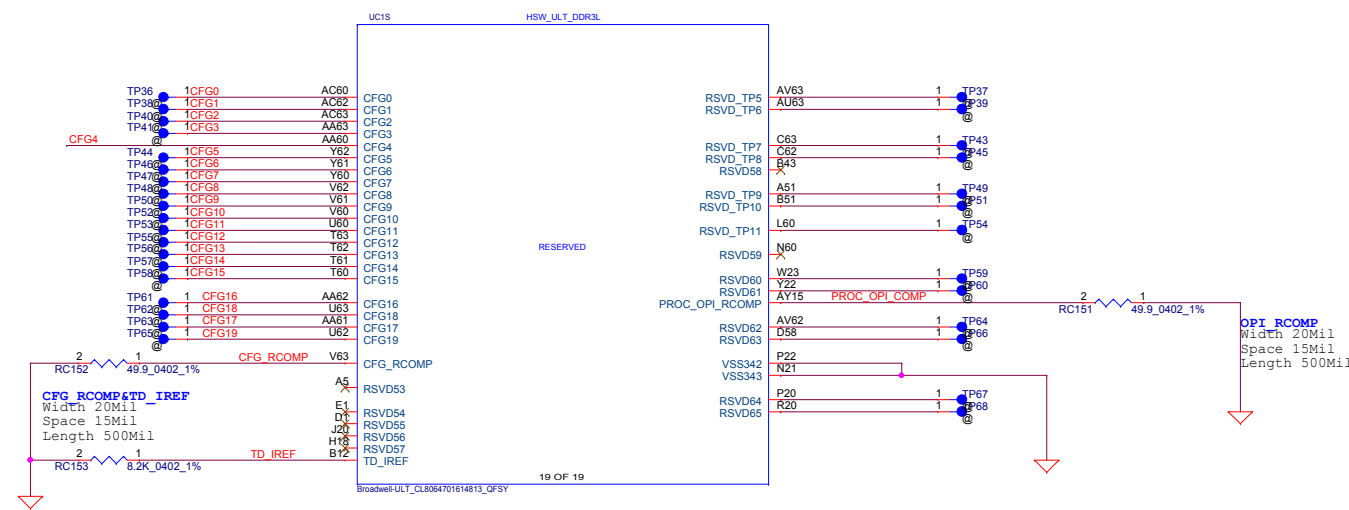
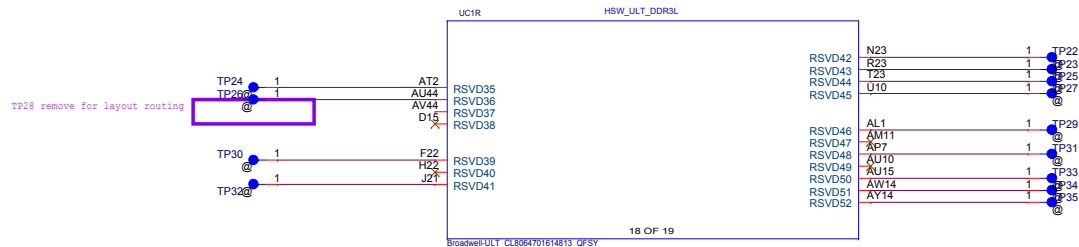
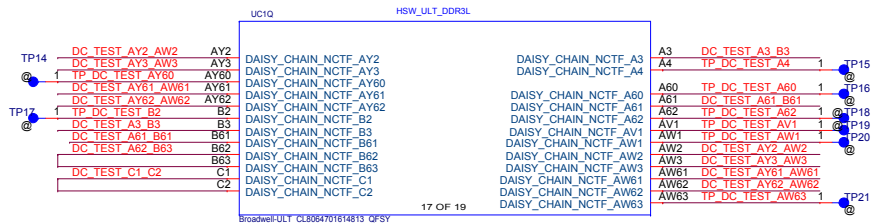


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Date:	Thursday, November 08, 2014			Sheet	16 of 81		

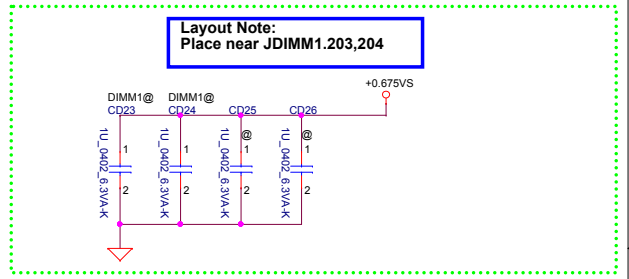
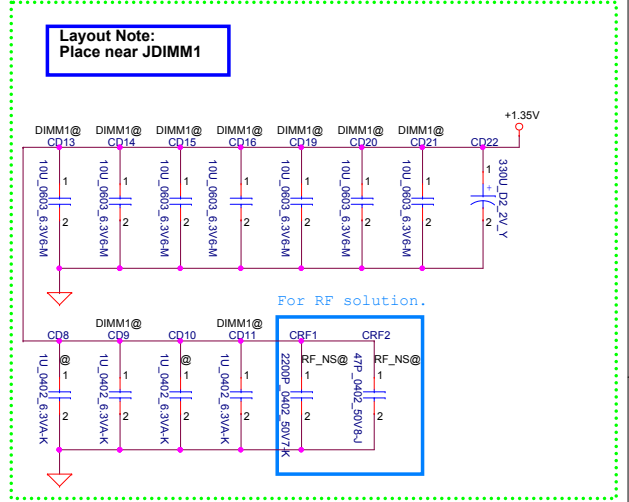
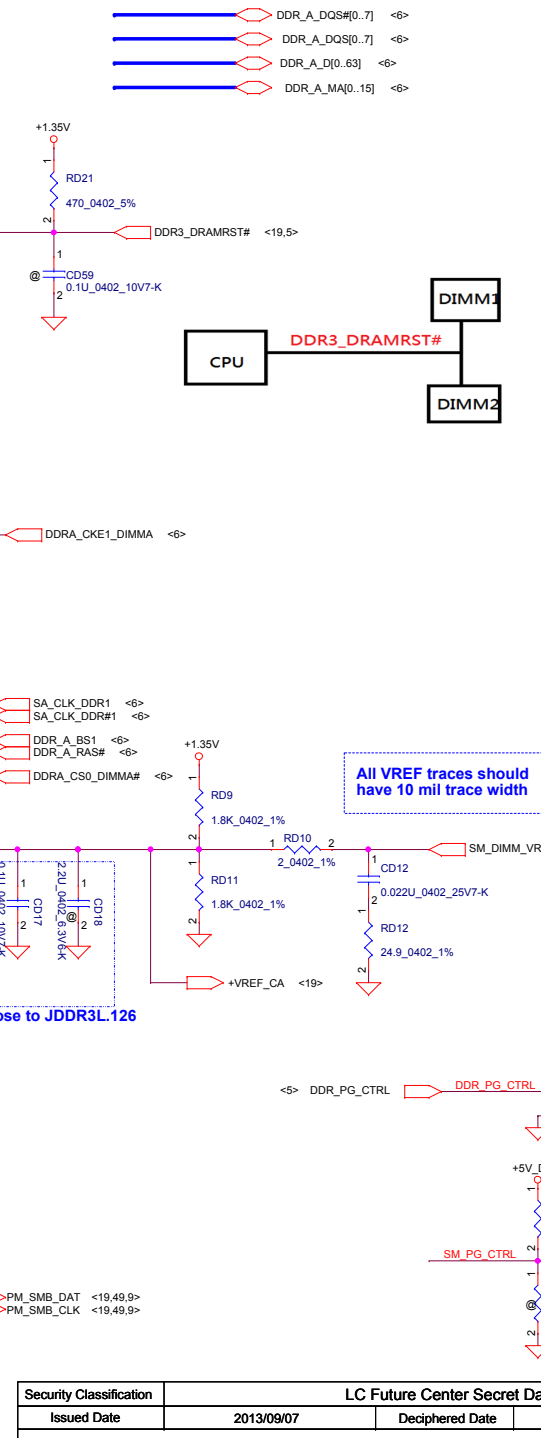
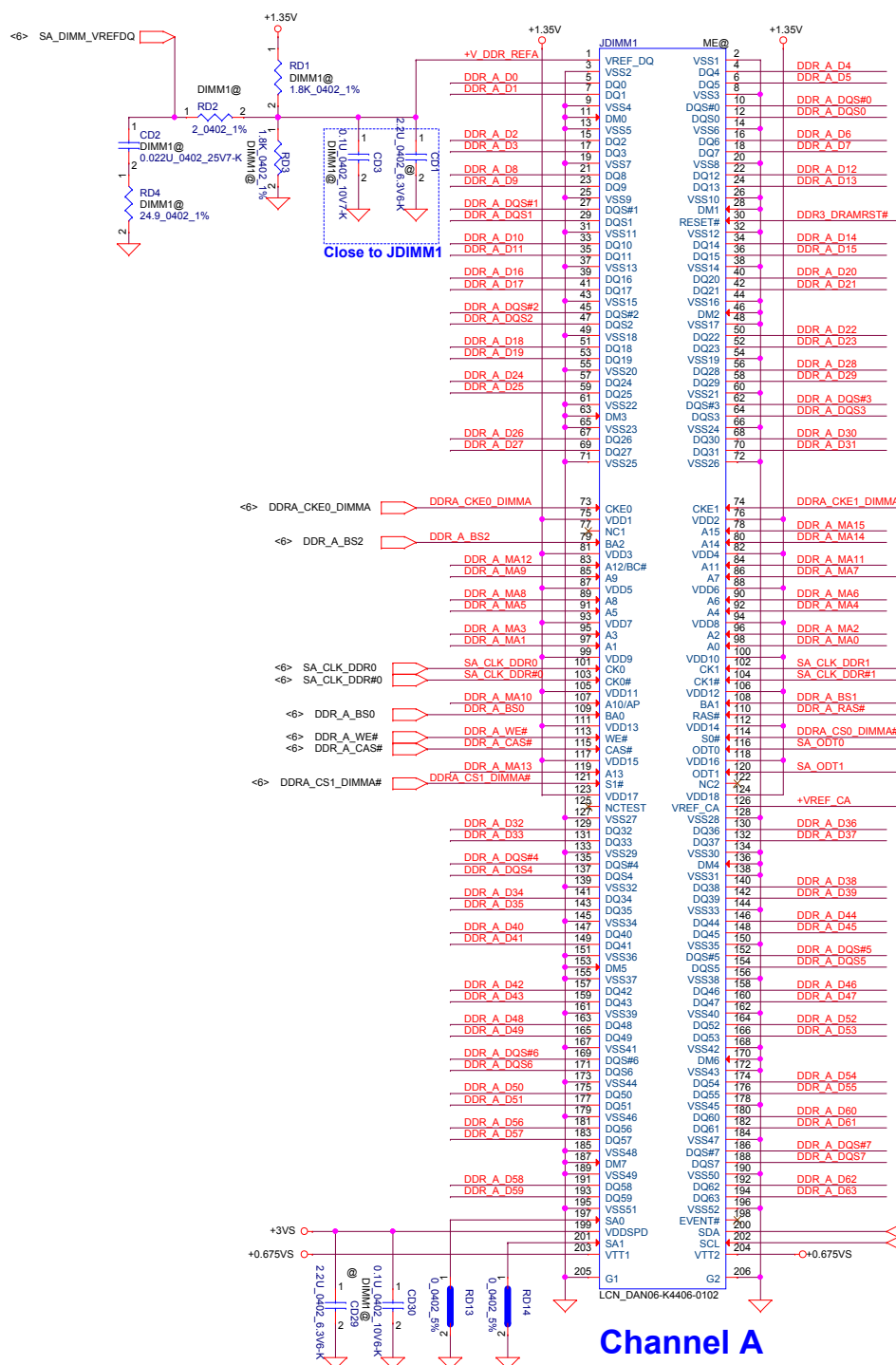




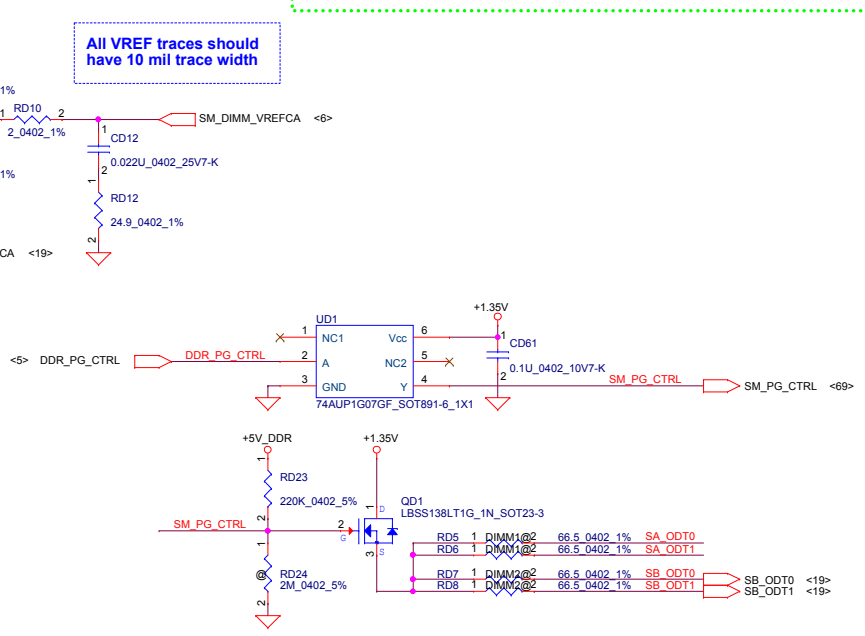
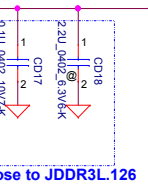
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				Date: Thursday, November 08, 2014 1 Sheet 17 of 81	



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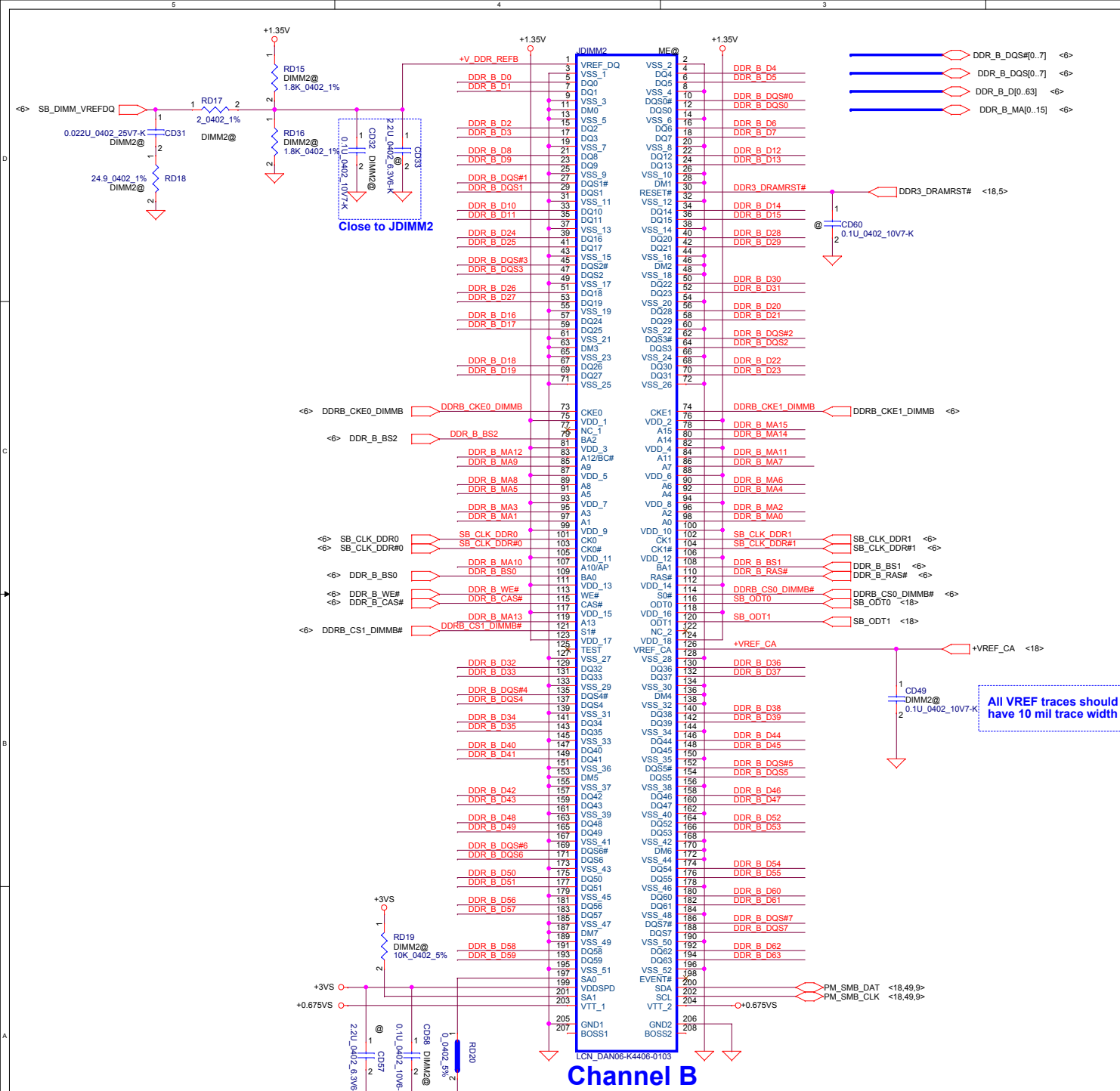


All VREF traces should have 10 mil trace width



# Channel A

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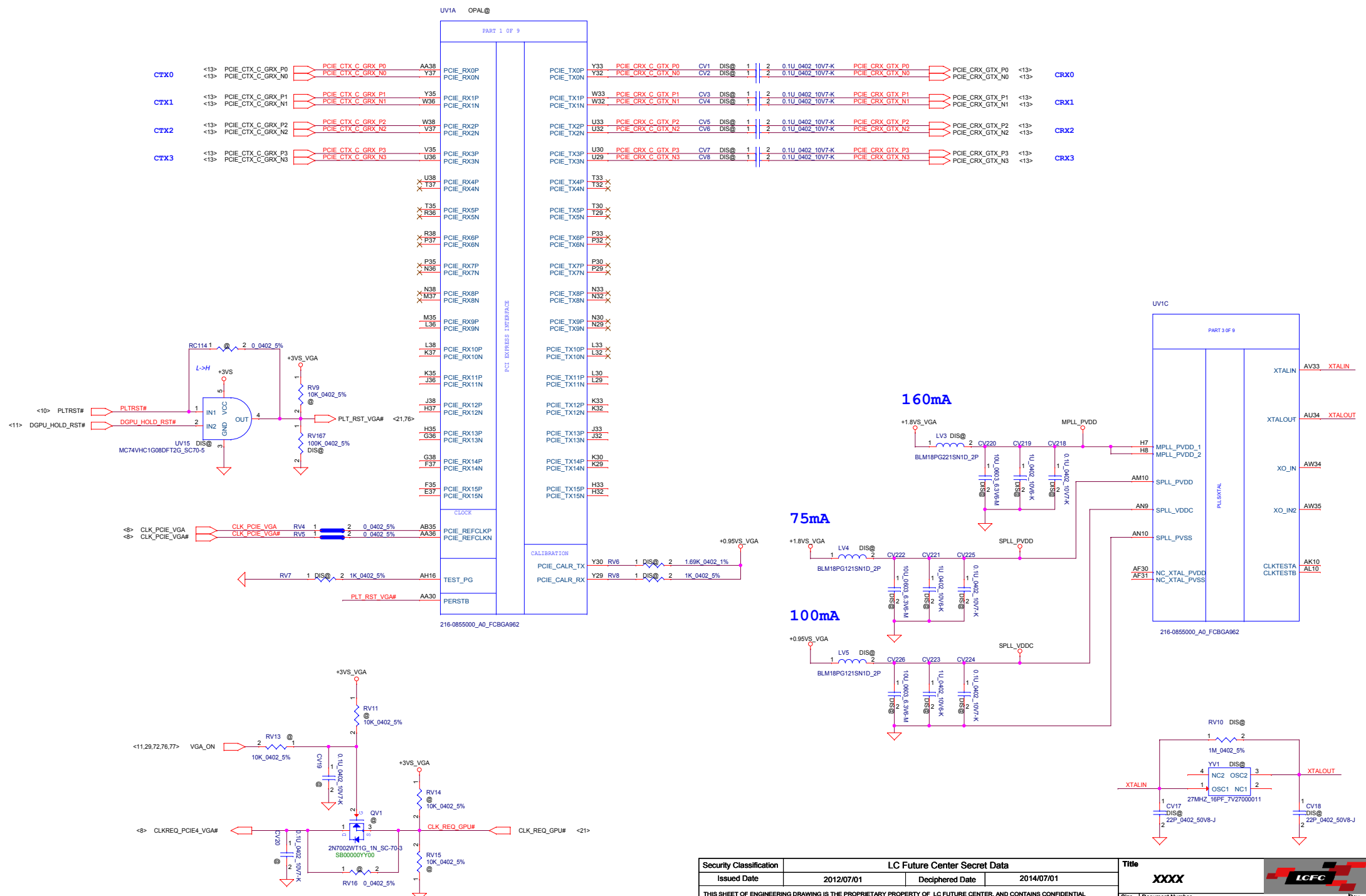
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DIMM\_2 STD H:4mm


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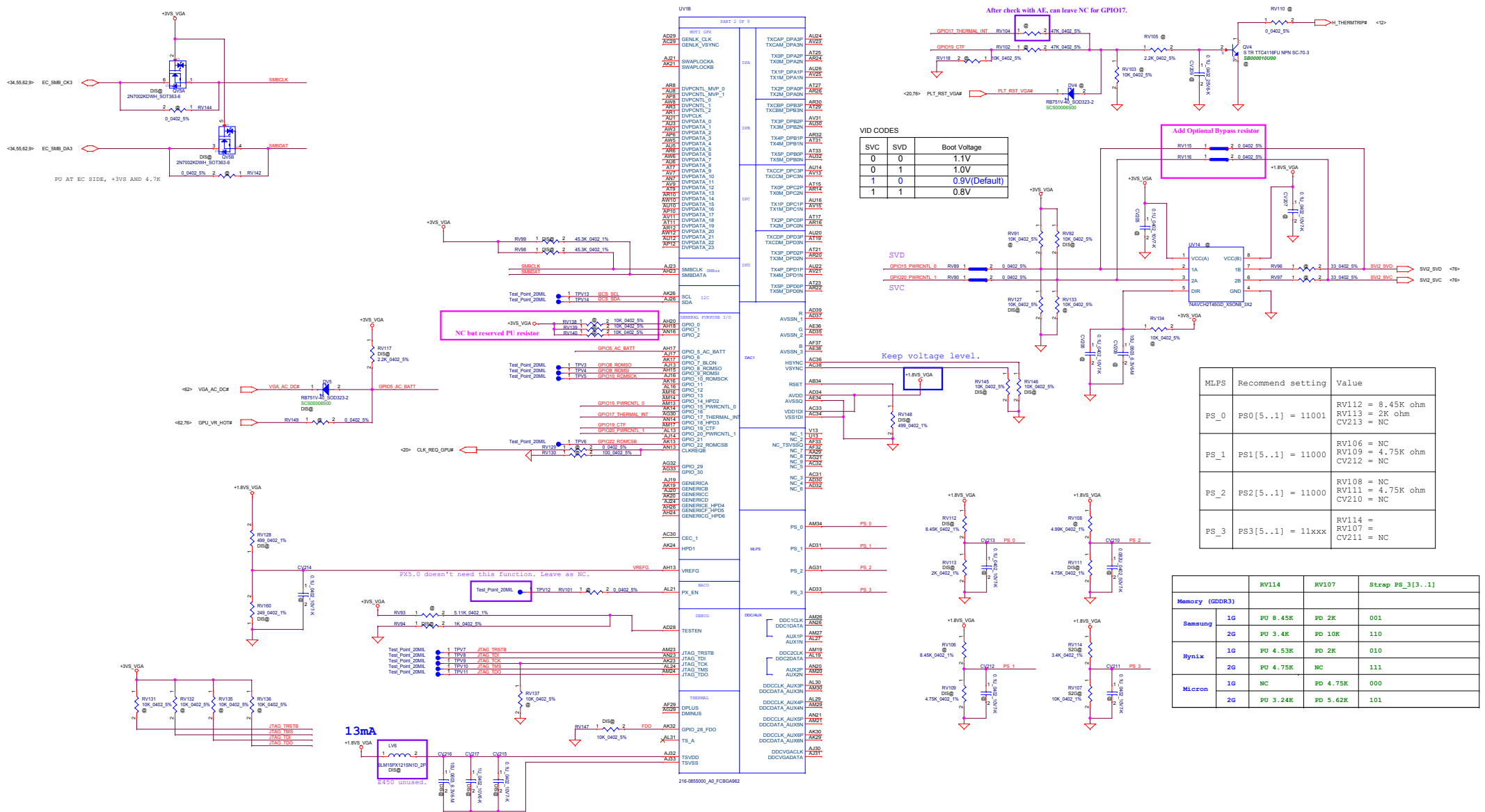
**ICFC**

**AITE1 NM-A221**

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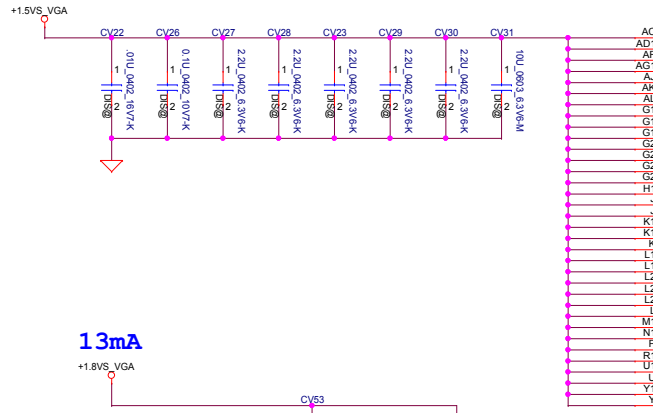
VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

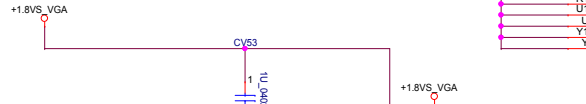
MLPS	Recommend setting	Value
PS_0	FS0[5..1] = 11001	RV112 = 8.45k ohm RV113 = 2K ohm CV213 = NC
PS_1	FS1[5..1] = 11000	RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2	FS2[5..1] = 11000	RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3	FS3[5..1] = 11xxx	RV114 = RV107 = CV211 = NC

	RV114	RV107	Strap_PS_3[3..1]
Memory (GDDR3)			
Samsung	1G	PU 8.45K PD 2K	001
	2G	PU 3.4K PD 10K	110
Hynix	1G	PU 4.53K PD 2K	010
	2G	PU 4.75K NC	111
Micron	1G	NC PD 4.75K	000
	2G	PU 3.24K PD 5.62K	101

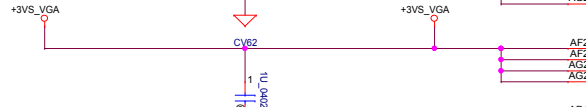
1.5A



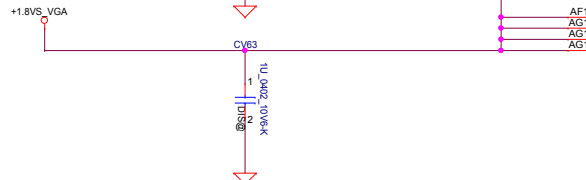
13mA



25mA



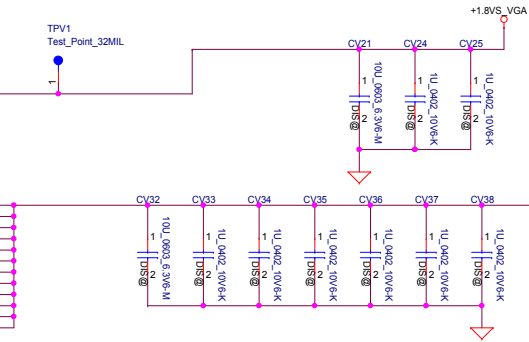
30mA



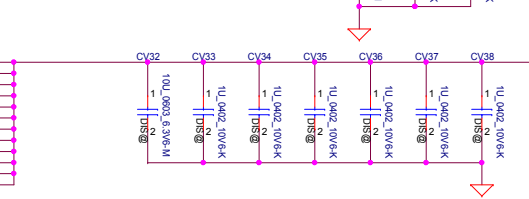
MEM I/O	MEM I/O	PCIE	BACO	CORE	I/O	DVP	VOLTAGE SENSE	ISOLATED CORE I/O
AC7	VDDR1_1	AA31	VDDC_1	AA15	VDDR3_1	AD12	AF28	AA13
AD11	VDDR1_2	AA32	VDDC_2	AA17	VDDR3_2	AF11	AG28	AB13
AF7	VDDR1_3	AA33	VDDC_3	AA20	VDDR3_3	AF12		AC12
AG10	VDDR1_4	AA34	VDDC_4	AA22	VDDR3_4	AG24		AC15
AJ7	VDDR1_5	W30	VDDC_5	AA24	VDDR3_4			AD16
AK1	VDDR1_6	T31	VDDC_6	AA27	VDDR3_4			AD16
AL9	VDDR1_7	V28	VDDC_7	AB18	VDDR3_4			M15
GI1	VDDR1_8	W29	VDDC_8	AB18	VDDR3_4			M16
GI4	VDDR1_9	AB37	VDDC_9	AB21	VDDR3_4			M18
GI7	VDDR1_10		VDDC_10	AB23	VDDR3_4			M23
G20	VDDR1_11		VDDC_11	AB28	VDDR3_4			N13
G23	VDDR1_12		VDDC_12	AC17	VDDR3_4			N15
G26	VDDR1_13		VDDC_14	AC20	VDDR3_4			N17
G29	VDDR1_14		VDDC_15	AC22	VDDR3_4			N20
H10	VDDR1_15		VDDC_16	AC24	VDDR3_4			N22
J7	VDDR1_16		VDDC_17	AD16	VDDR3_4			R12
J9	VDDR1_17		VDDC_18	AD21	VDDR3_4			R13
K11	VDDR1_18		VDDC_19	AD21	VDDR3_4			R16
K13	VDDR1_19		VDDC_20	AD23	VDDR3_4			R21
K6	VDDR1_20		VDDC_21	AF17	VDDR3_4			R23
L12	VDDR1_21		VDDC_22	AF20	VDDR3_4			R26
L21	VDDR1_22		VDDC_23	AF22	VDDR3_4			T20
L23	VDDR1_23		VDDC_24	AG16	VDDR3_4			T22
L26	VDDR1_24		VDDC_25	AG18	VDDR3_4			T24
L7	VDDR1_25		VDDC_26	AH22	VDDR3_4			U18
M11	VDDR1_26		VDDC_28	AH27	VDDR3_4			U21
N11	VDDR1_27		VDDC_29	AH28	VDDR3_4			U23
P7	VDDR1_28		VDDC_30	M26	VDDR3_4			U26
R11	VDDR1_29		VDDC_31	N24	VDDR3_4			V17
U11	VDDR1_30		VDDC_32	R18	VDDR3_4			V20
U7	VDDR1_31		VDDC_33	R21	VDDR3_4			V22
Y11	VDDR1_32		VDDC_34	R23	VDDR3_4			V24
Y7	VDDR1_33		VDDC_35	R26	VDDR3_4			V27
	VDDR1_34		VDDC_36	T17	VDDR3_4			Y16
			VDDC_37	T20	VDDR3_4			Y18
			VDDC_38	T22	VDDR3_4			Y21
			VDDC_39	T24	VDDR3_4			Y23
			VDDC_40	U18	VDDR3_4			Y26
			VDDC_41	U21	VDDR3_4			Y28
			VDDC_42	U23	VDDR3_4			Y28
			VDDC_44	U26	VDDR3_4			Y28
			VDDC_45	V17	VDDR3_4			Y28
			VDDC_46	V20	VDDR3_4			Y28
			VDDC_47	V22	VDDR3_4			Y28
			VDDC_48	V24	VDDR3_4			Y28
			VDDC_49	V27	VDDR3_4			Y28
			VDDC_50	Y16	VDDR3_4			Y28
			VDDC_51	Y18	VDDR3_4			Y28
			VDDC_52	Y21	VDDR3_4			Y28
			VDDC_53	Y23	VDDR3_4			Y28
			VDDC_54	Y26	VDDR3_4			Y28
			VDDC_55	Y28	VDDR3_4			Y28
			VDDC_56	Y28	VDDR3_4			Y28
			VDDC_1	AA13	VDDR3_4			Y28
			VDDC_2	AB13	VDDR3_4			Y28
			VDDC_3	AC12	VDDR3_4			Y28
			VDDC_4	AC15	VDDR3_4			Y28
			VDDC_5	AD16	VDDR3_4			Y28
			VDDC_6	AD16	VDDR3_4			Y28
			VDDC_7	M15	VDDR3_4			Y28
			VDDC_8	M16	VDDR3_4			Y28
			VDDC_9	M18	VDDR3_4			Y28
			VDDC_10	M23	VDDR3_4			Y28
			VDDC_11	N13	VDDR3_4			Y28
			VDDC_12	N15	VDDR3_4			Y28
			VDDC_13	N17	VDDR3_4			Y28
			VDDC_14	N20	VDDR3_4			Y28
			VDDC_15	N22	VDDR3_4			Y28
			VDDC_16	R12	VDDR3_4			Y28
			VDDC_17	R13	VDDR3_4			Y28
			VDDC_18	R16	VDDR3_4			Y28
			VDDC_19	R21	VDDR3_4			Y28
			VDDC_20	R23	VDDR3_4			Y28
			VDDC_21	T12	VDDR3_4			Y28
			VDDC_22	T15	VDDR3_4			Y28
			VDDC_23	T16	VDDR3_4			Y28
			VDDC_24	T18	VDDR3_4			Y28
			VDDC_25	T19	VDDR3_4			Y28

216-0855000\_A0\_FCBGA962

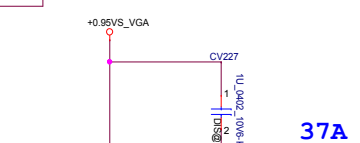
100mA



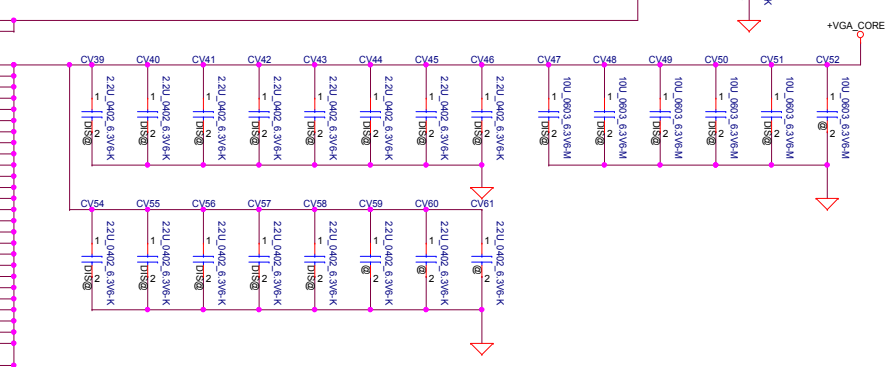
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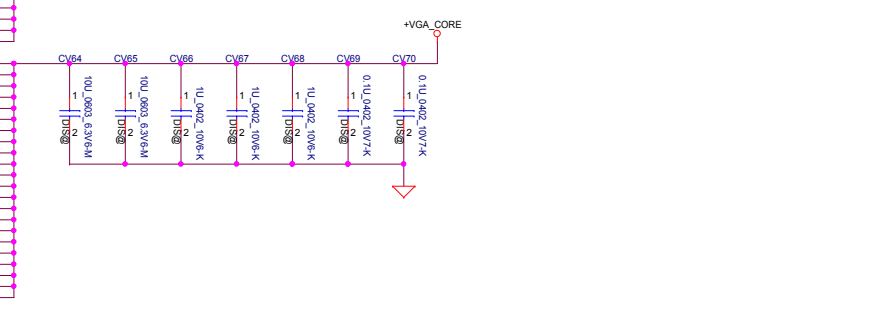
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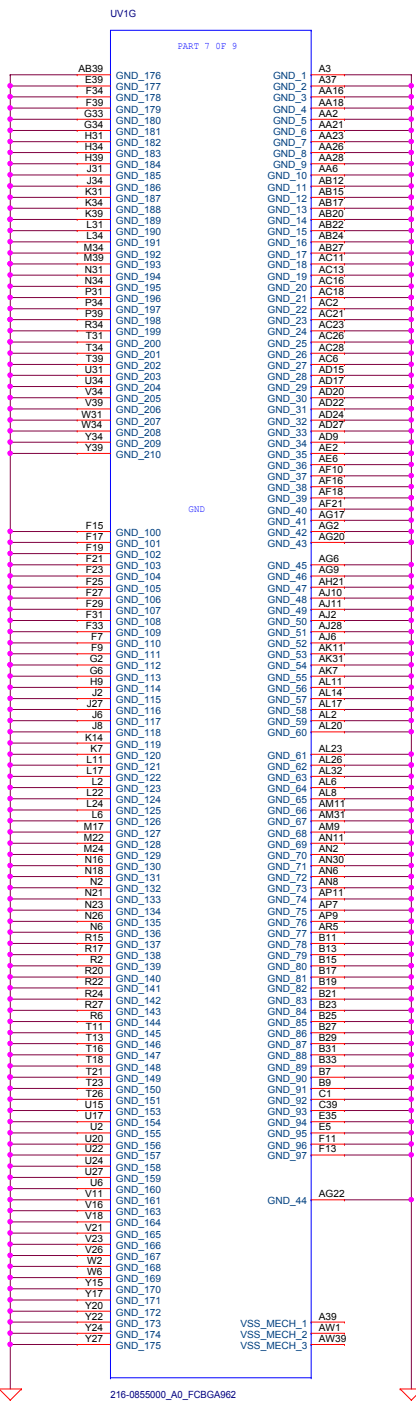
37A



37A



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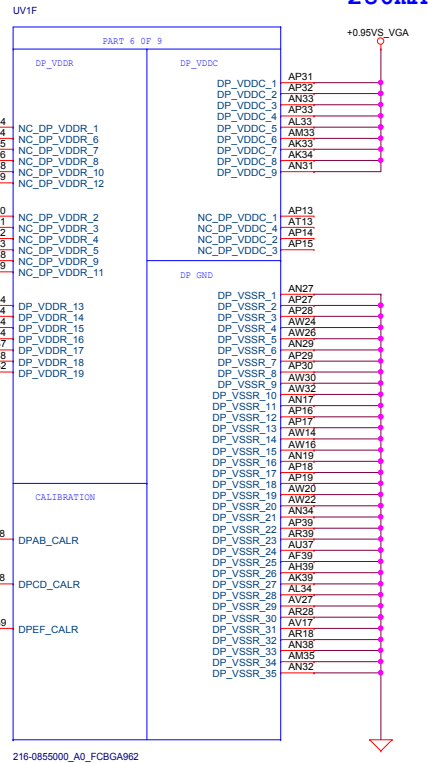
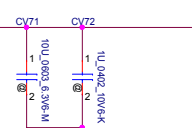
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VSS\_MECH\_1  
VSS\_MECH\_2  
VSS\_MECH\_3

A39  
AW1  
AW39

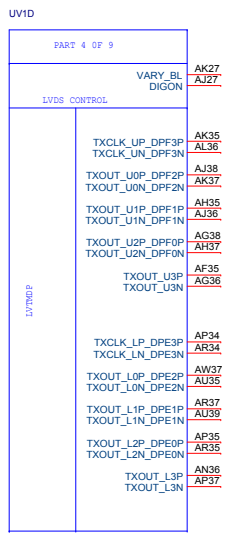
237mA

+1.8VS\_VGA



280mA

+0.85VS\_VGA

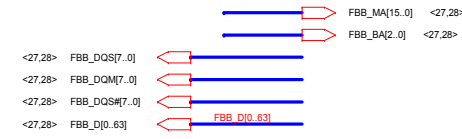
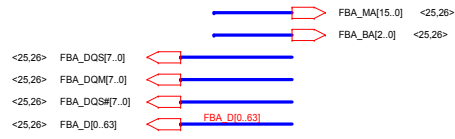


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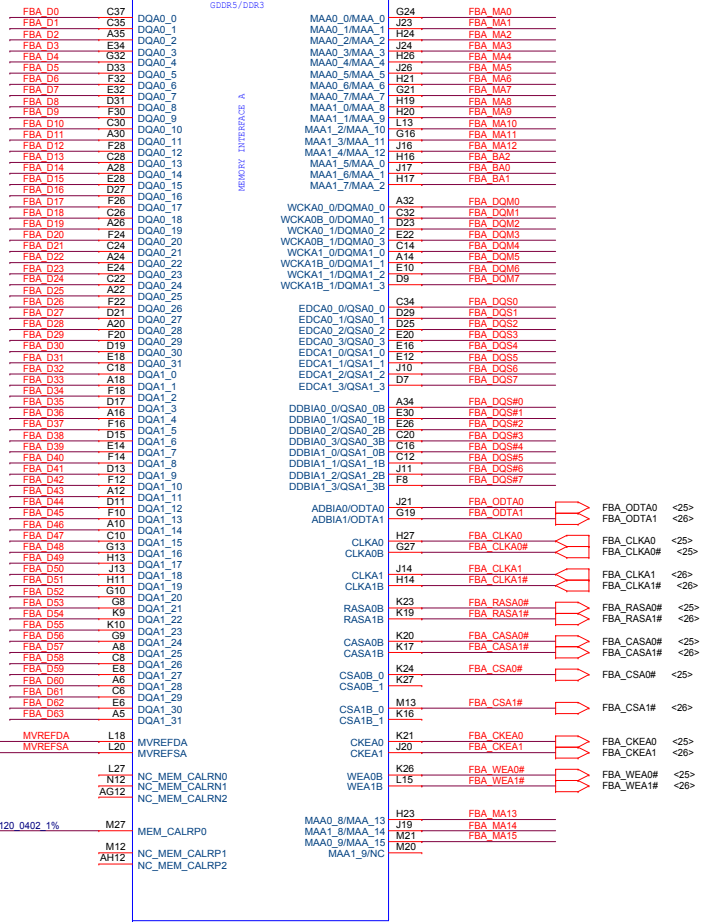


ATE1 NM-A221



UV1H

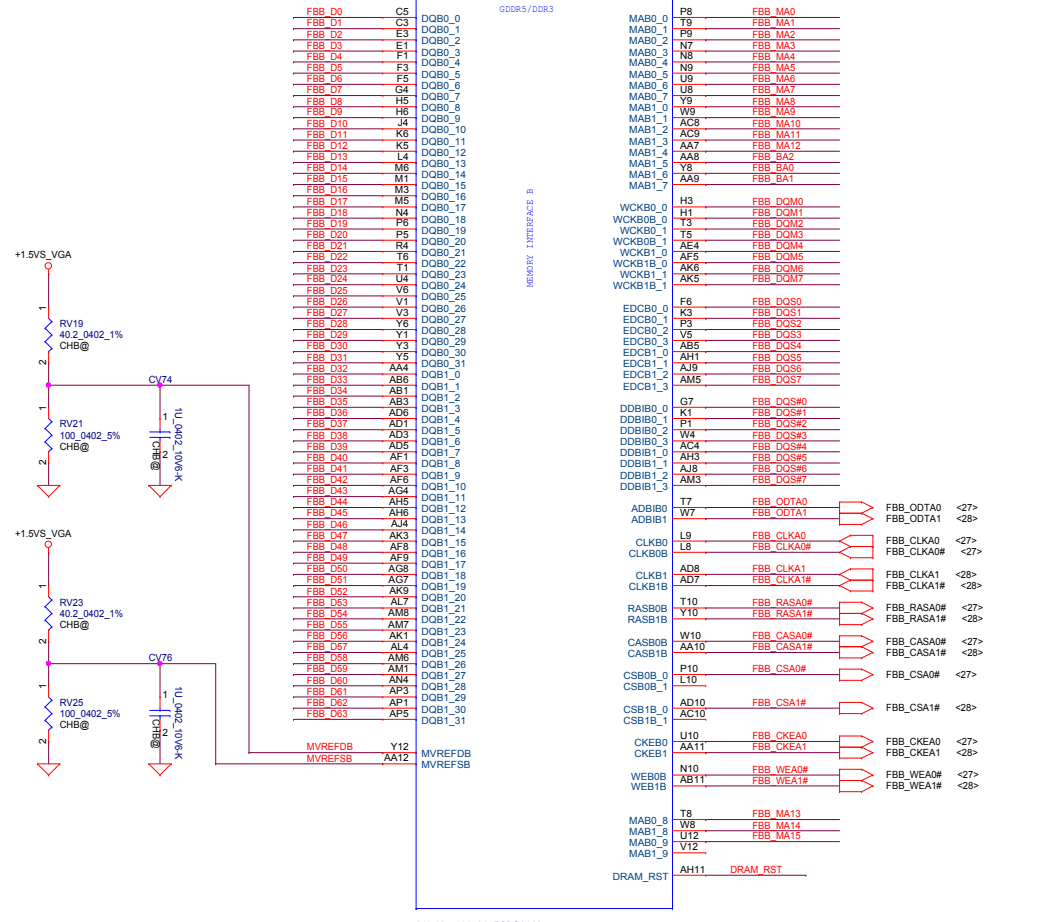
PART 8 OF 9  
GDDR3/DDR3



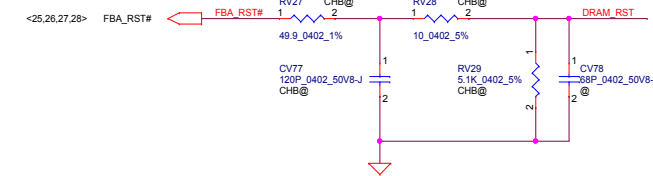
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UV1I

PART 9 OF 9  
GDDR3/DDR3



216-0855000\_A0\_FCBGA962

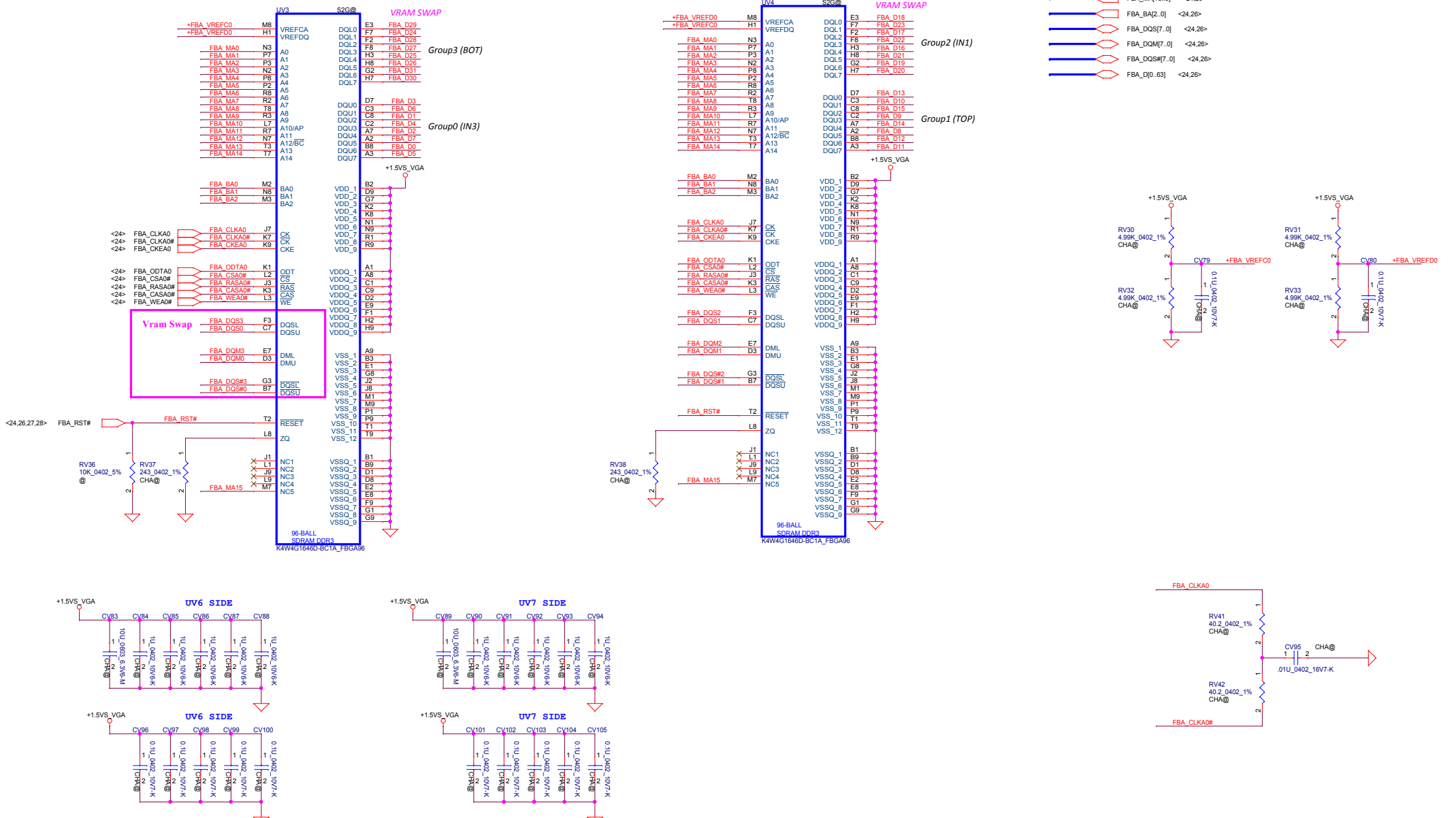


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Date:	Thursday, November 08, 2014 1 Sheet 24 of 81								

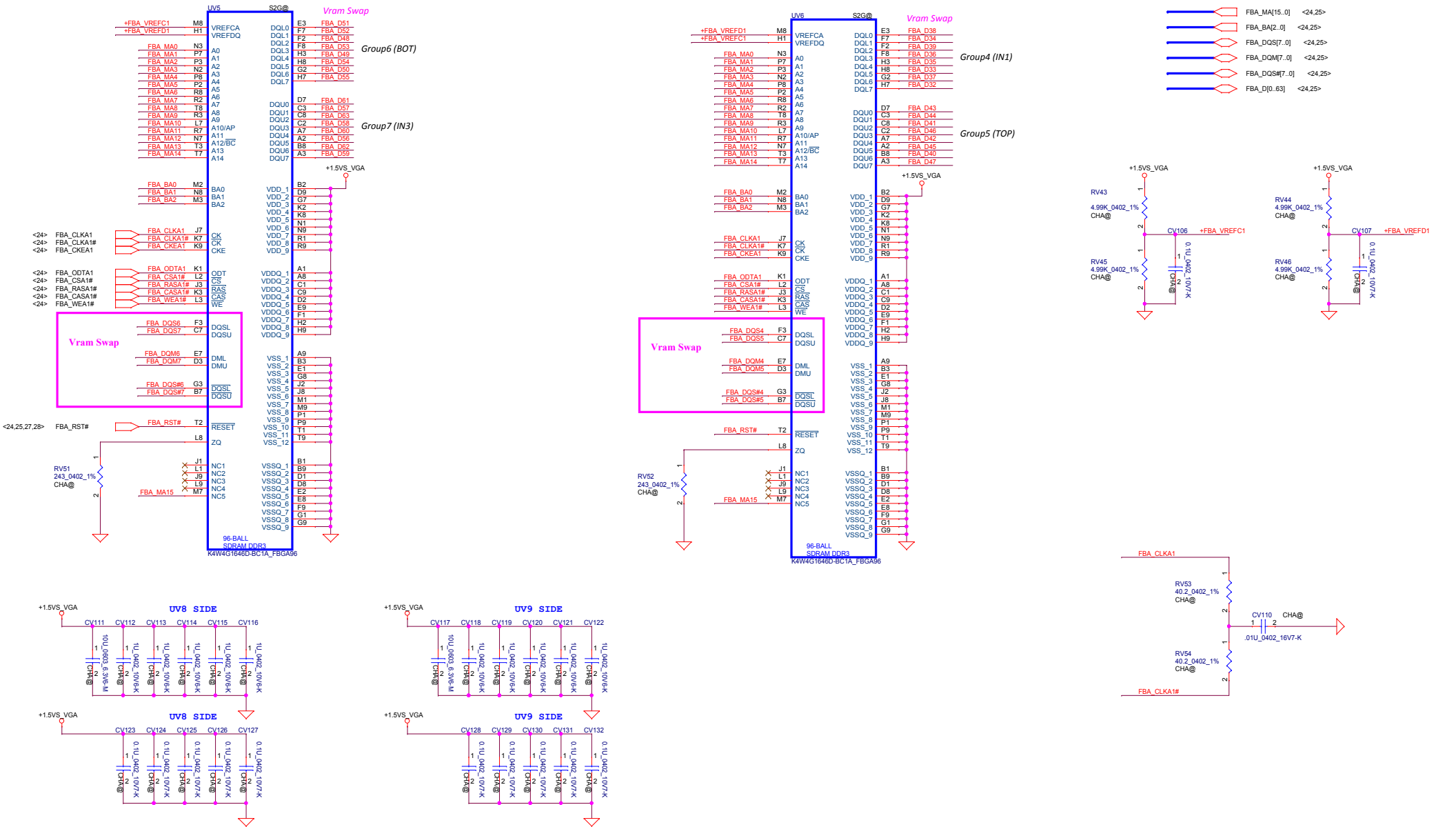


# Memory Partition A - Lower 32 bits

Change all VRAM footprint to MT41K256M16HA107\_FBGA96P-A39P

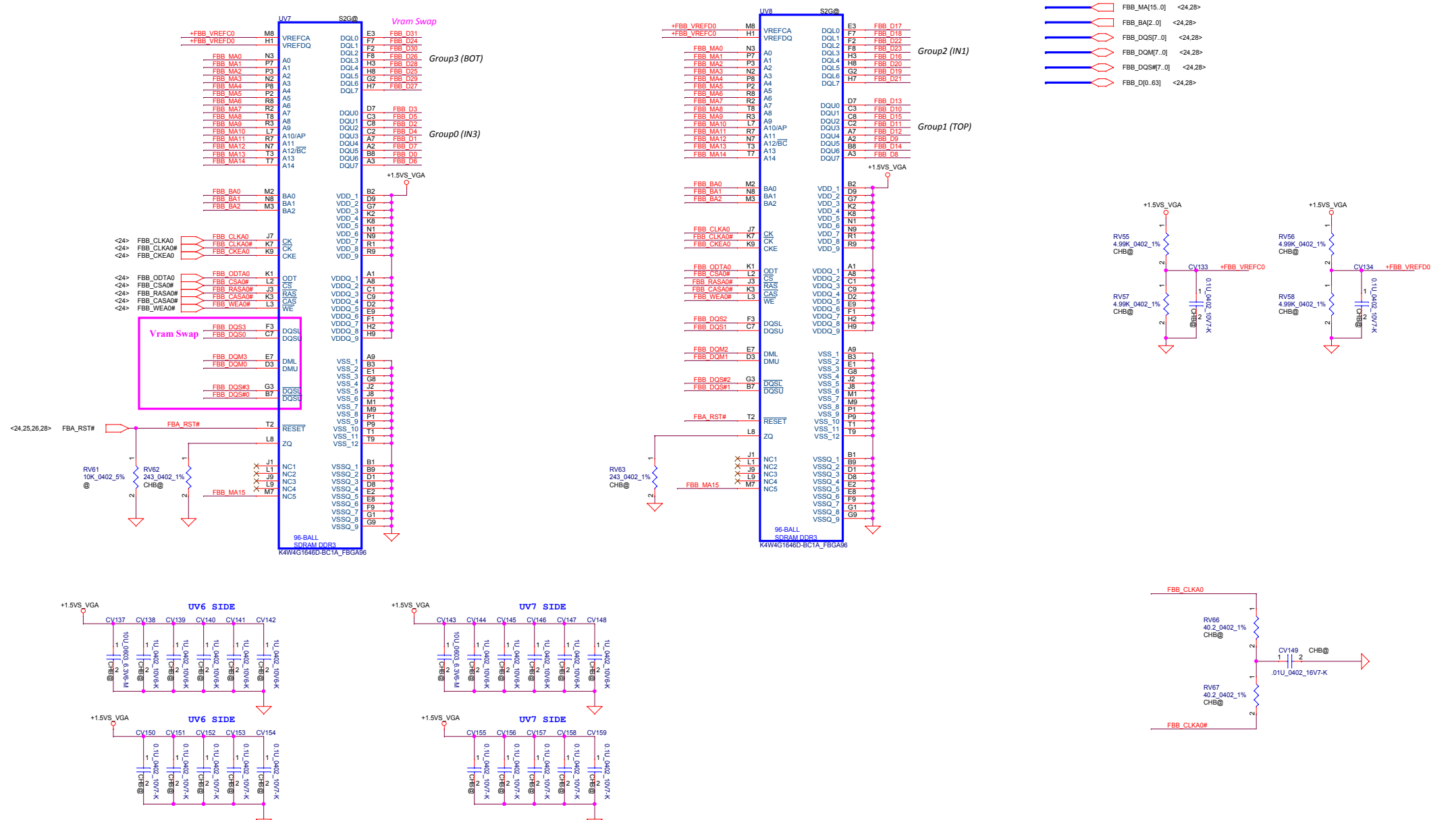


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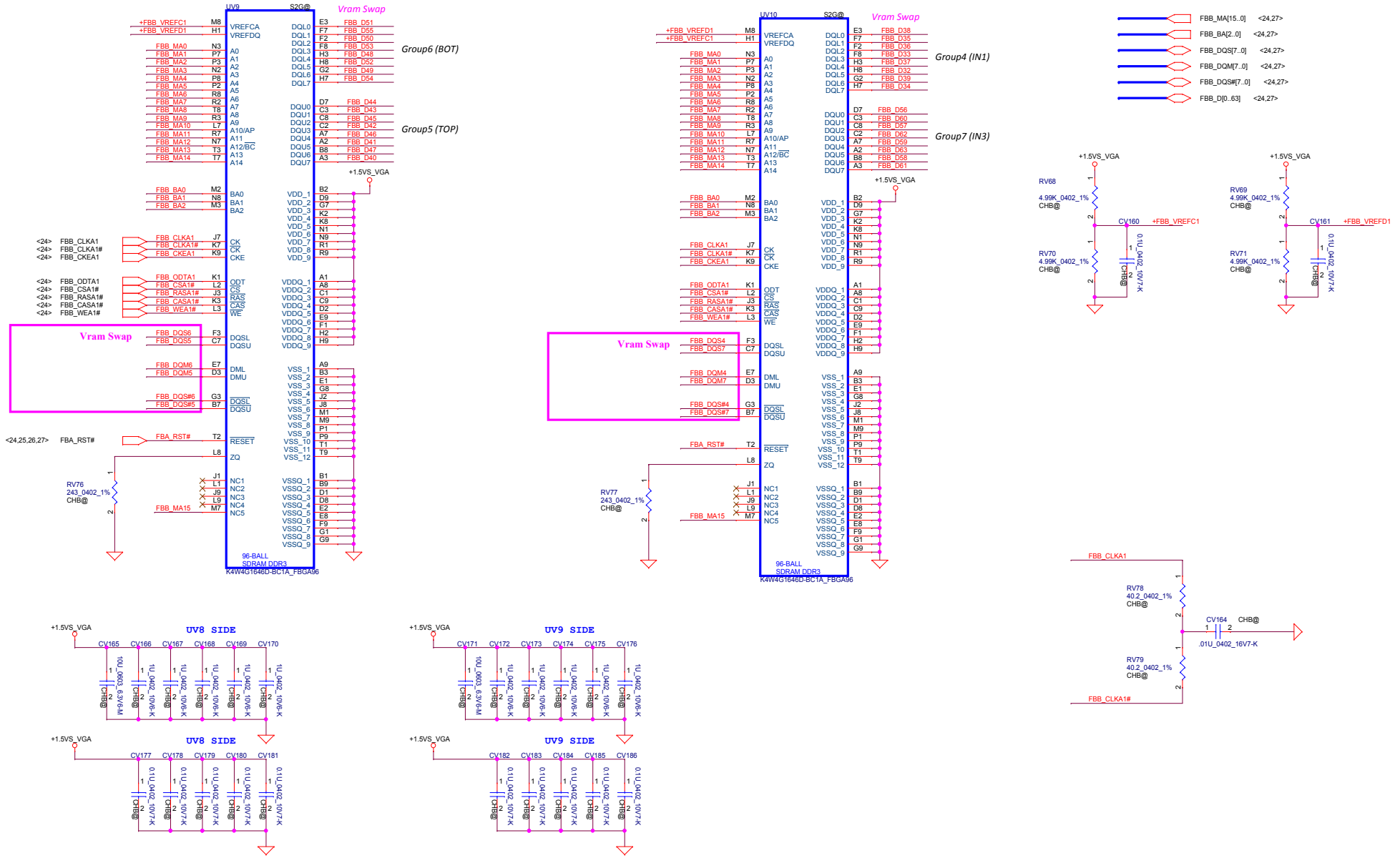


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# Memory Partition A - Lower 32 bits




# Memory Partition A - Upper 32 bits




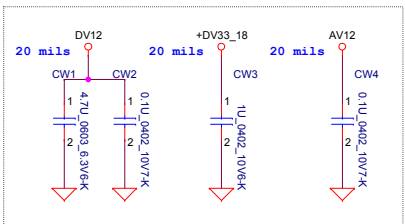


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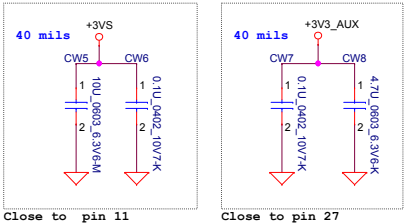
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Rev					1.0	<b>AITE1 NM-A221</b>

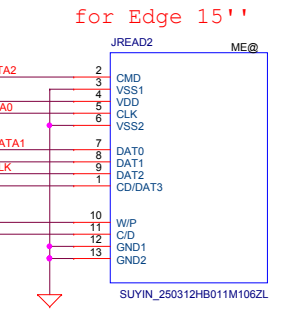
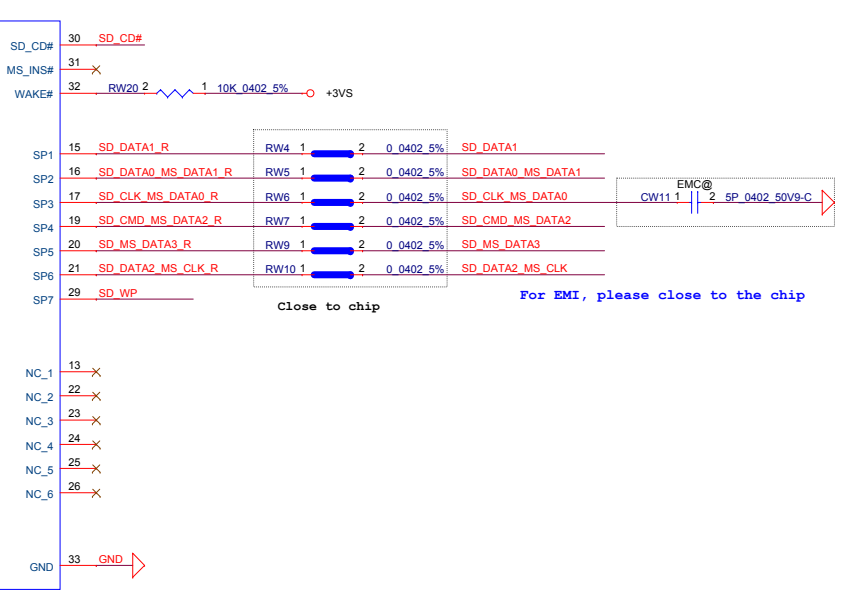
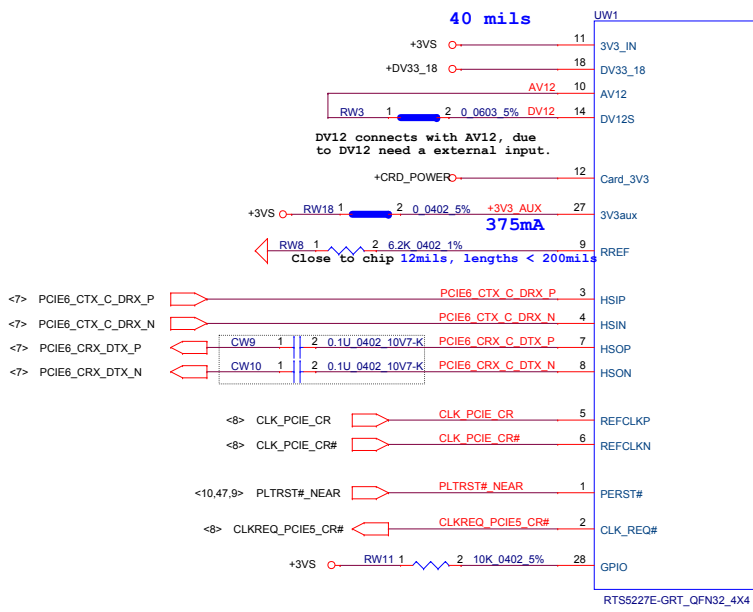


All of cap. close to chip

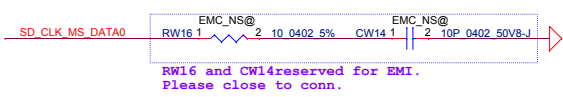
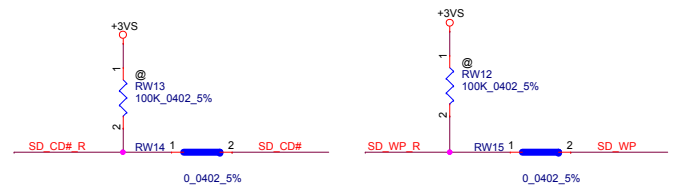


Close to pin 11

Close to pin 27




Close to JREAD1.

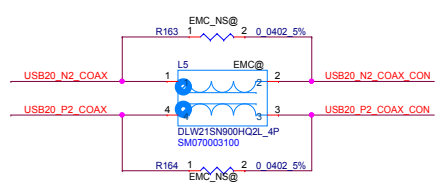


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**(Move to sub board)**

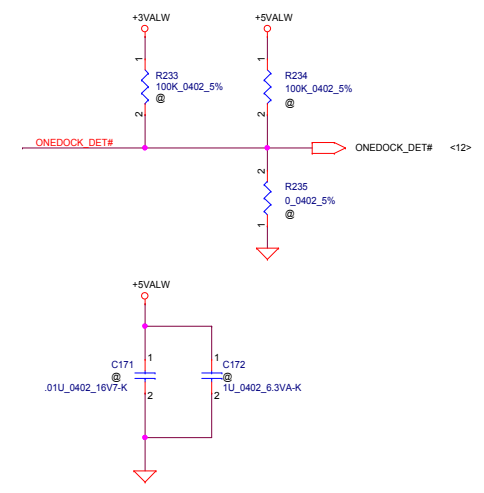
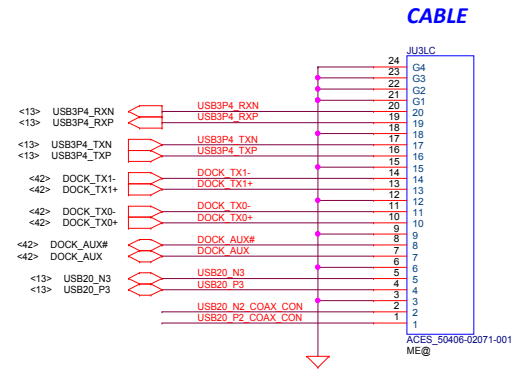
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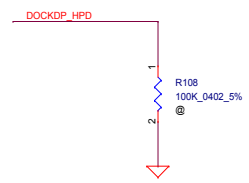
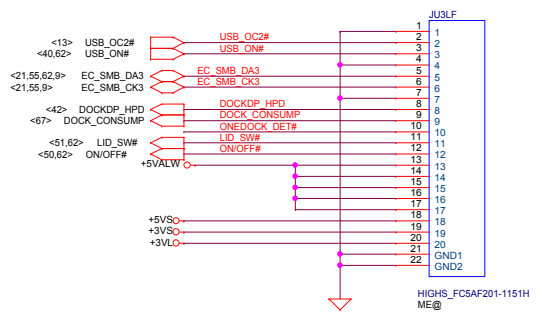
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DOCKNG

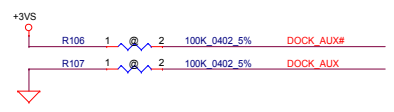
SUB/B



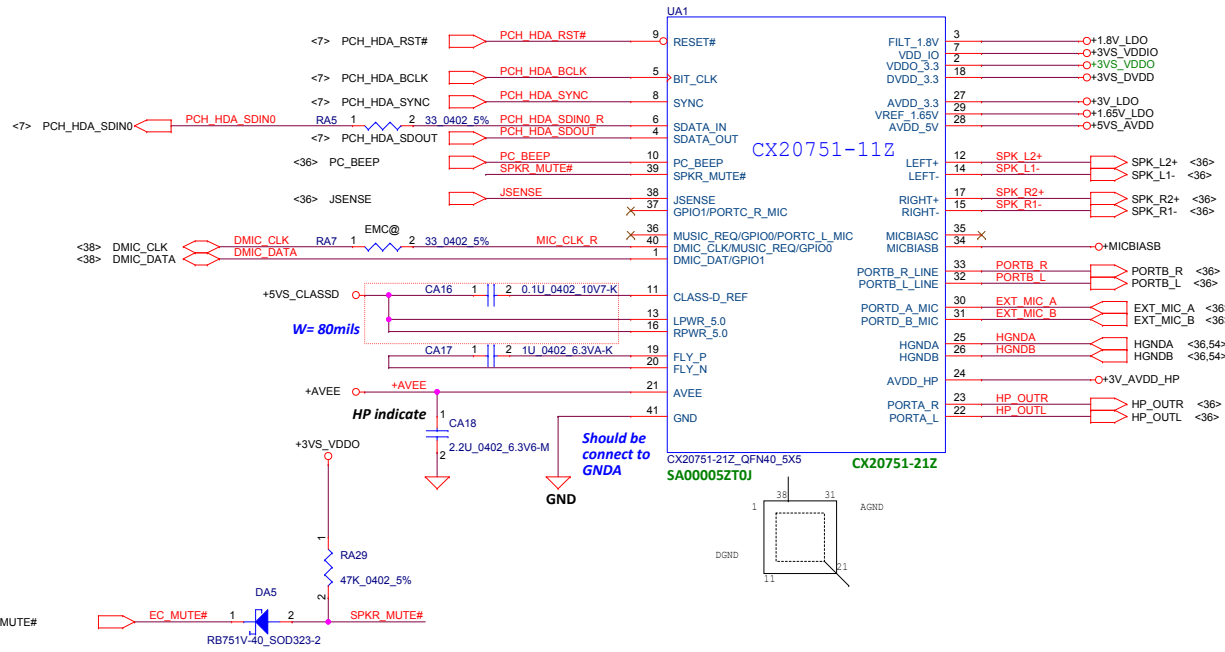
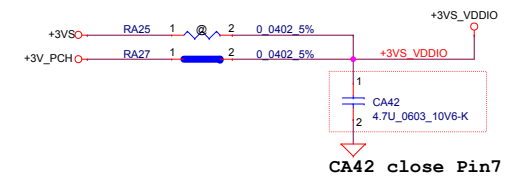
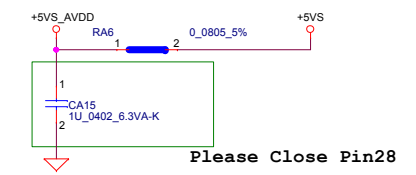
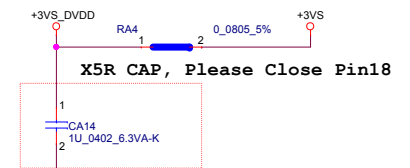
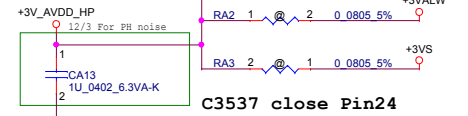
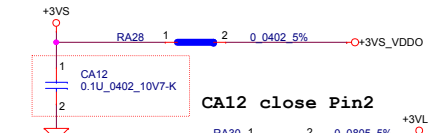
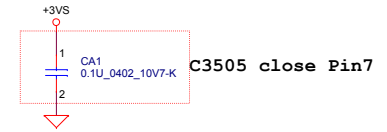
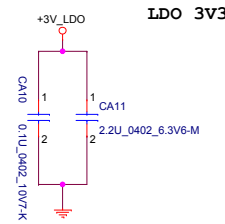
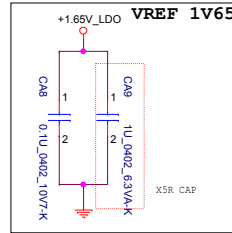
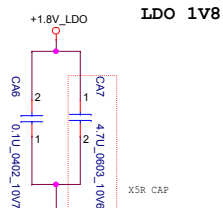
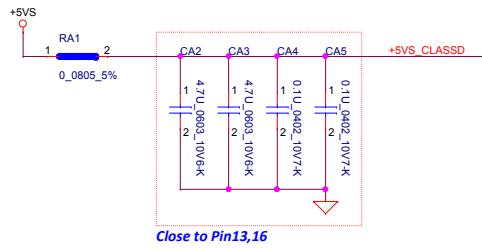
FFC



1. AC Capacitor place on Sub/B  
2. Need to check with MUX IC vendor whether still need AC cap between MUX IC and device.



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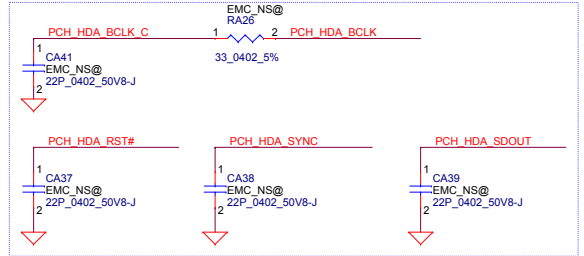


Apple --> EXT\_MIC\_A, HGND  
 Nokia --> EXT\_MIC\_B, HGND

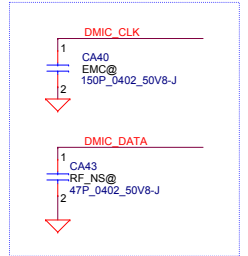
W= 80mils

Should be connect to GND

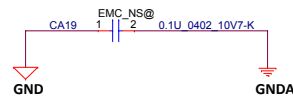
**EMI, close to UA1**



**RF, close to RA7**



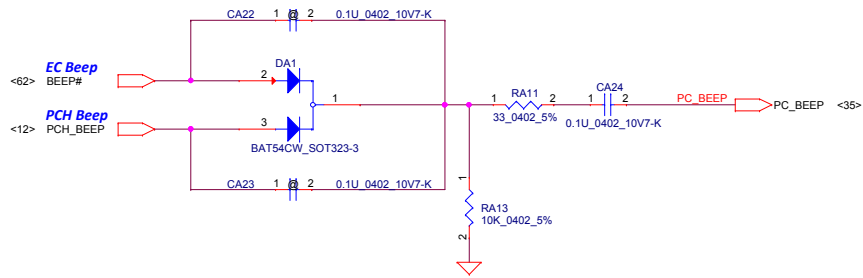
W= 300mils



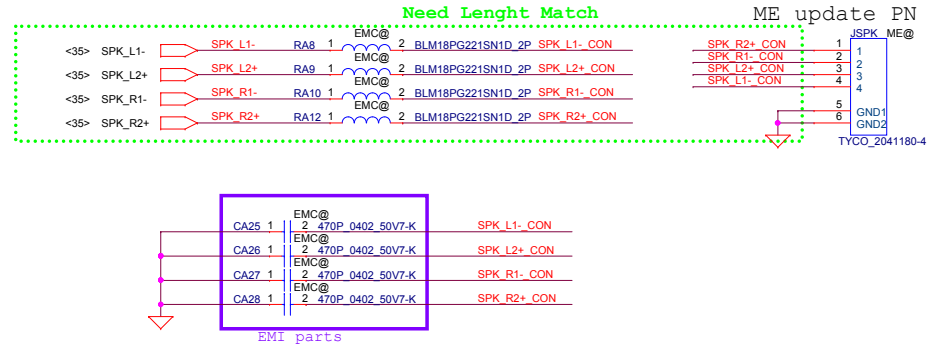
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### PC BEEP

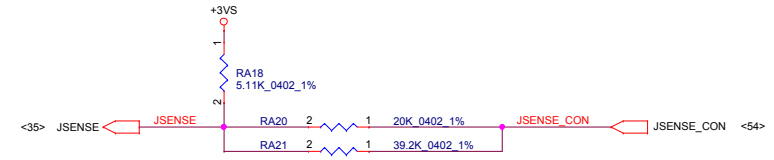
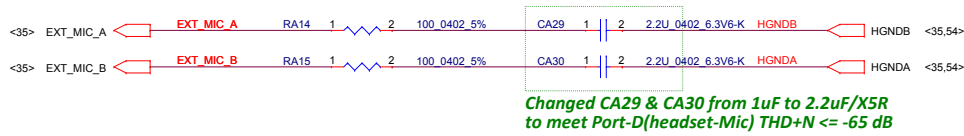


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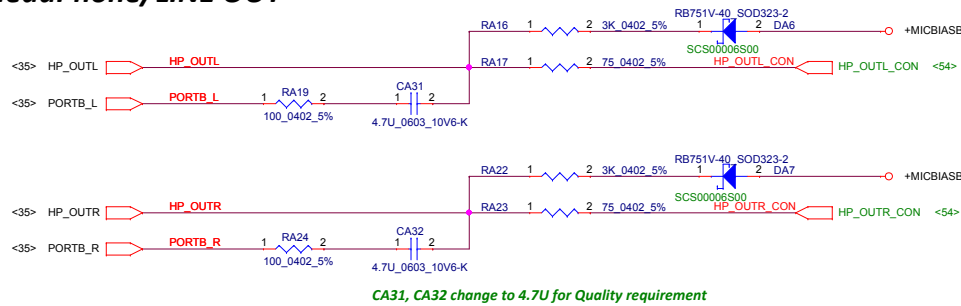


### EXT. MIC/LINE IN

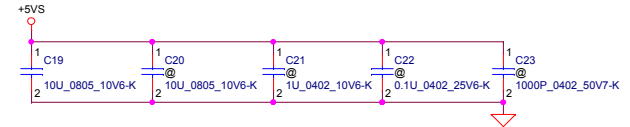
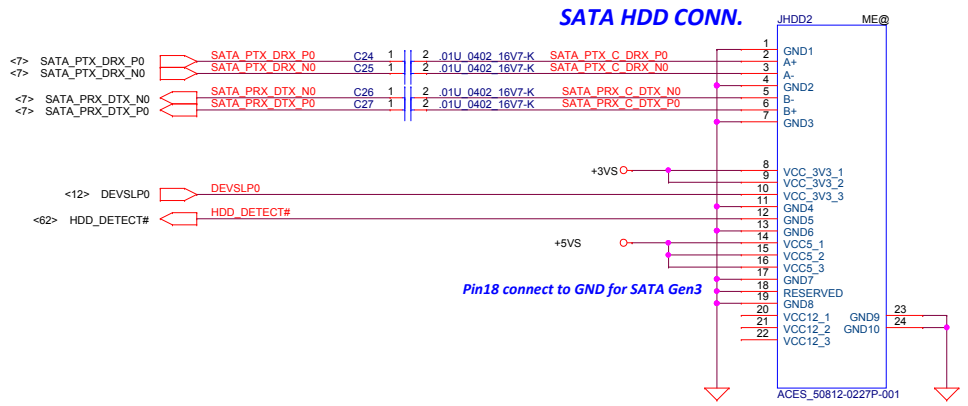
Apple --> EXT\_MIC\_A, HGND B  
 Nokia --> EXT\_MIC\_B, HGND A



### HeadPhone/LINE OUT

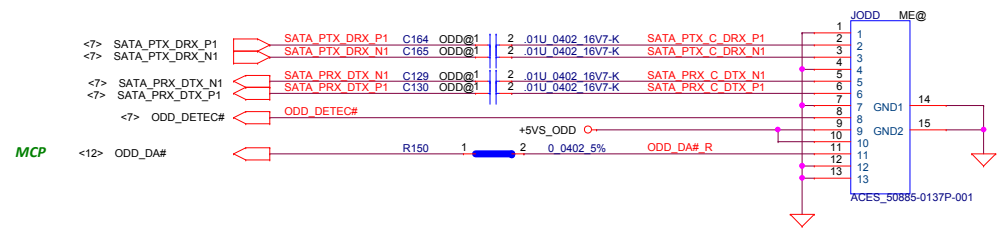


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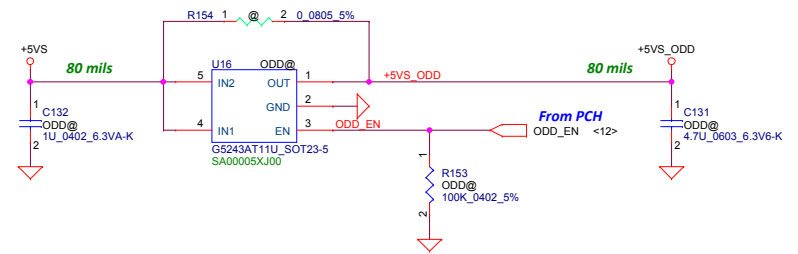


Pin18 connect to GND for SATA Gen3

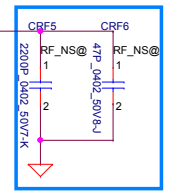
### SATA ODD CONN



### +5VS TO +5VS\_ODD

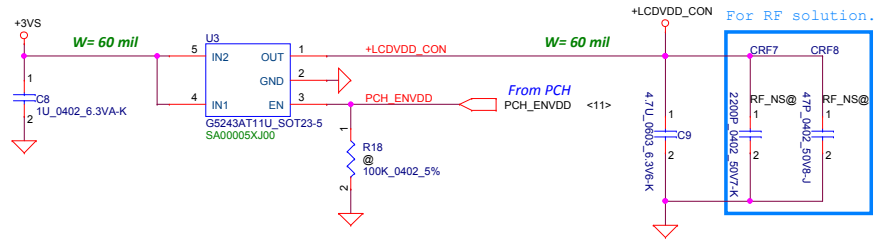


For RF solution. Close to JODD connector.

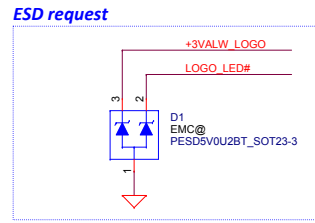
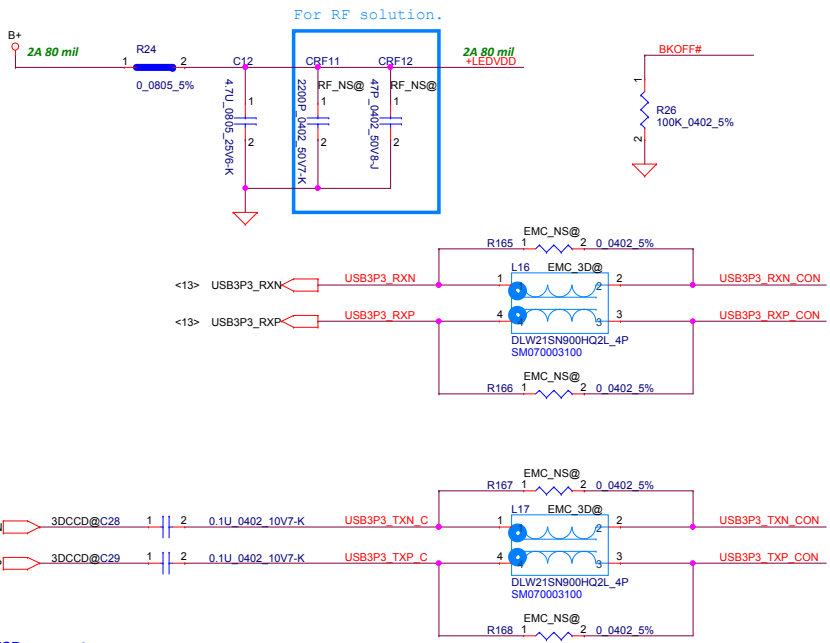
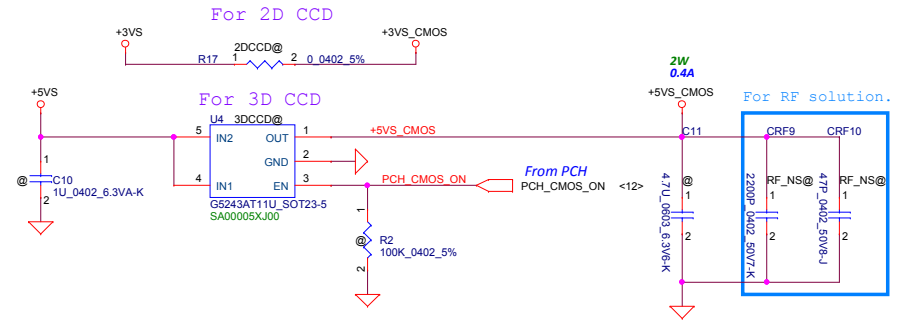


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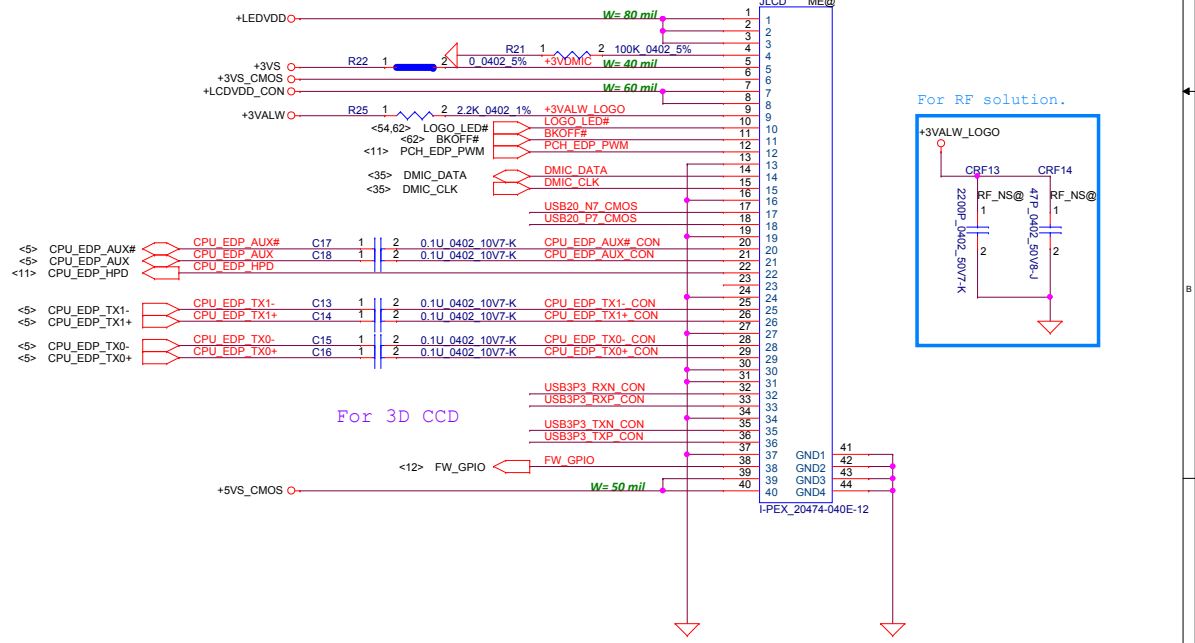
**LCDVDD Circuit**



**CMOS Camera**




**eDP CONN.**

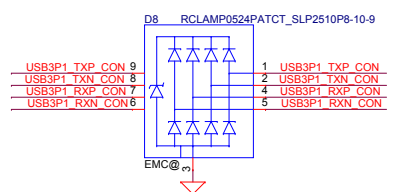
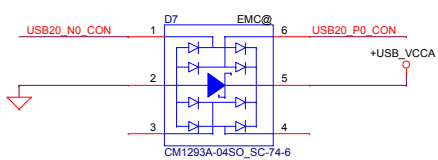
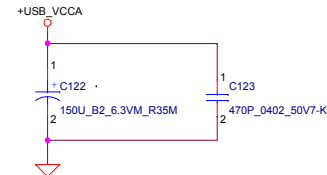
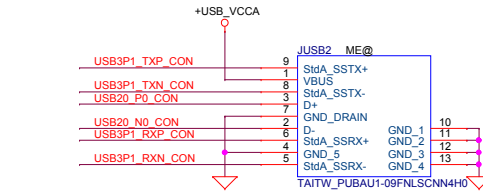
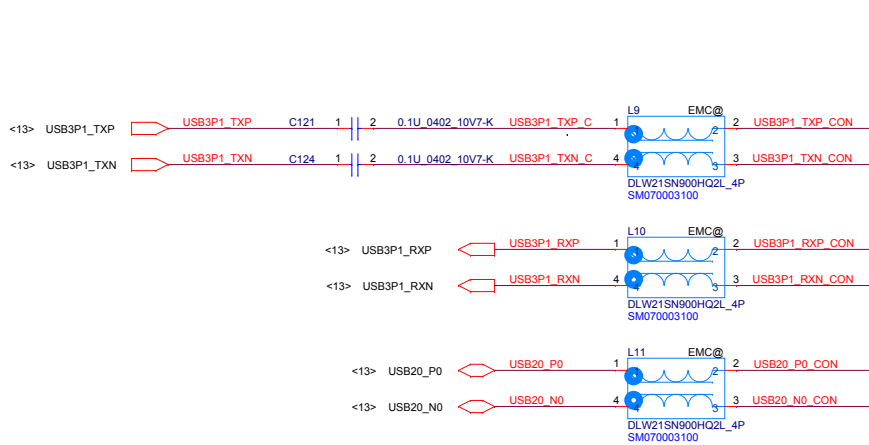
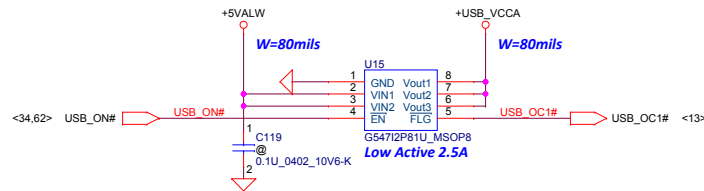



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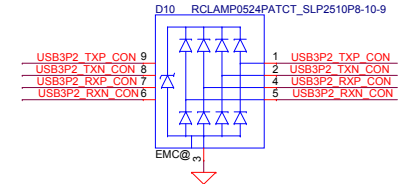
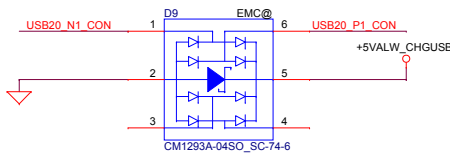
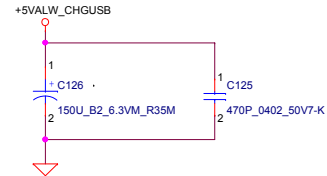
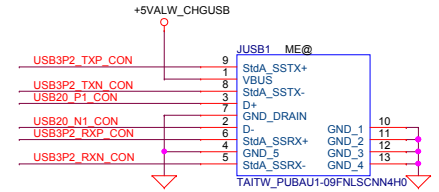
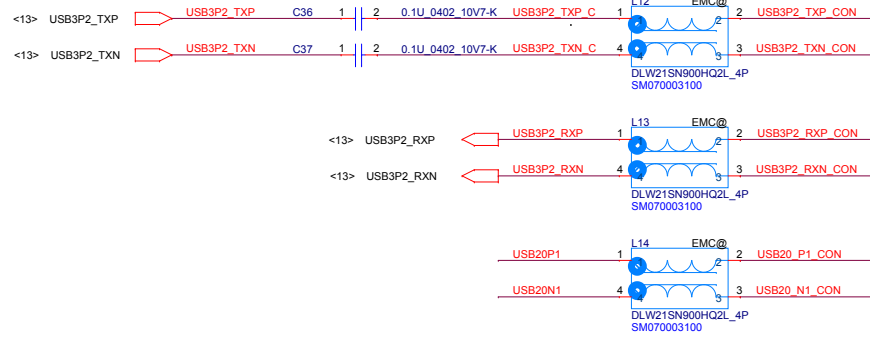
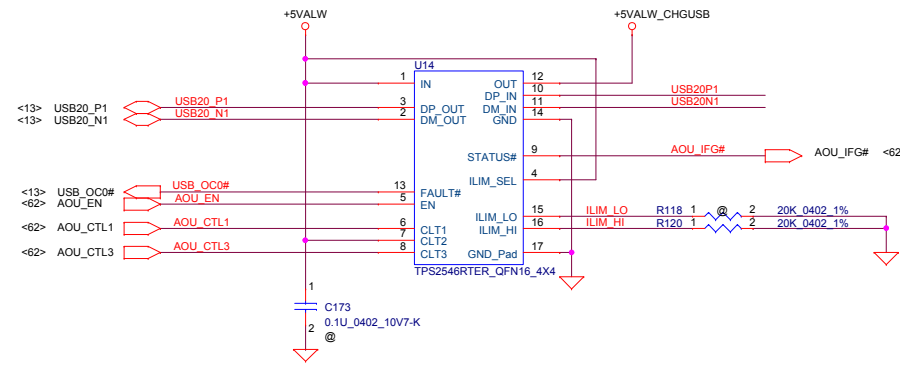
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				Document Number	<b>AITE1 NM-A221</b>	
				Date:	Thursday, November 06, 2014	
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### POWER SWITCH



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				Date:	Thursday, November 06, 2014   Sheet 40 of 81

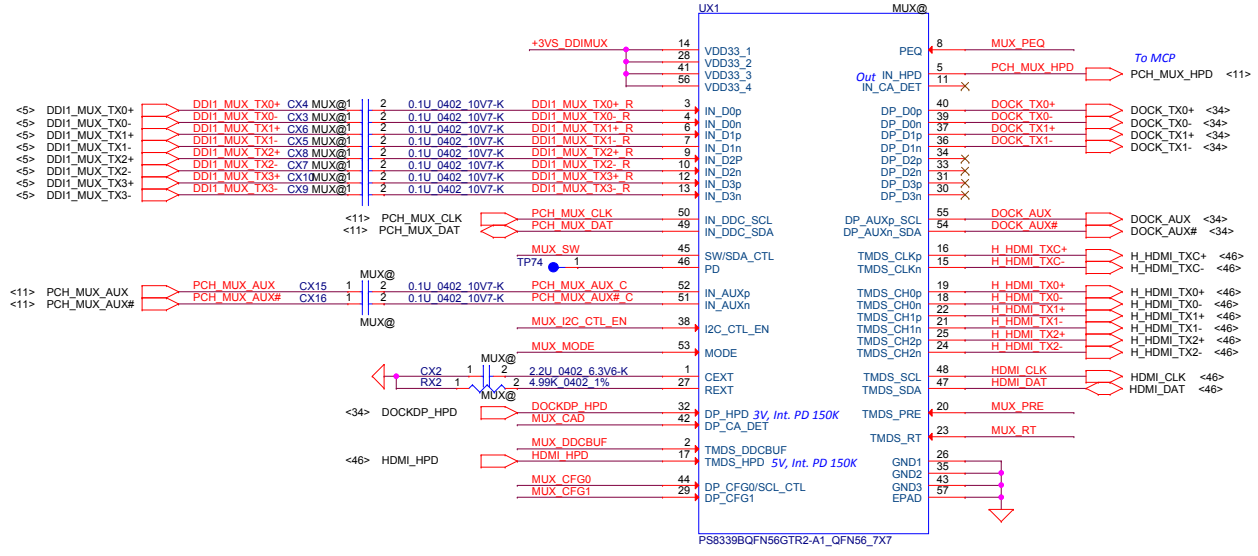
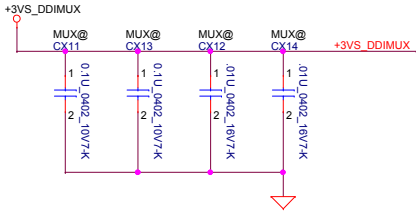
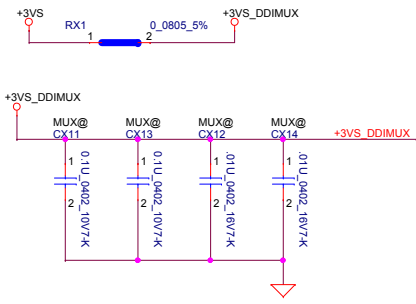




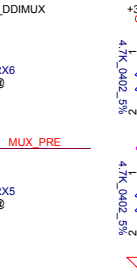
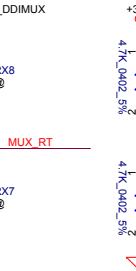
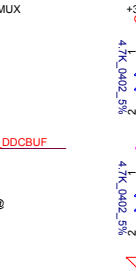
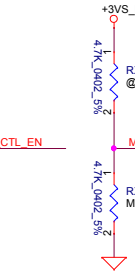
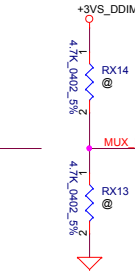
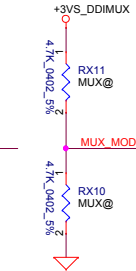
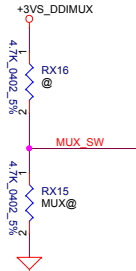
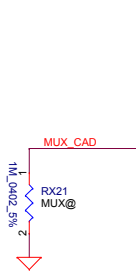
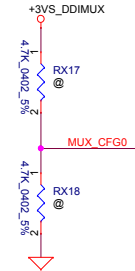
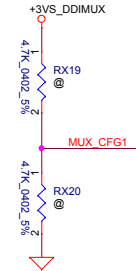
TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
* 1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
* 1	1	1	0	SDP2	Data Connected
* 1	1	0	X	SDP1	Data Connected
* 0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
* 0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

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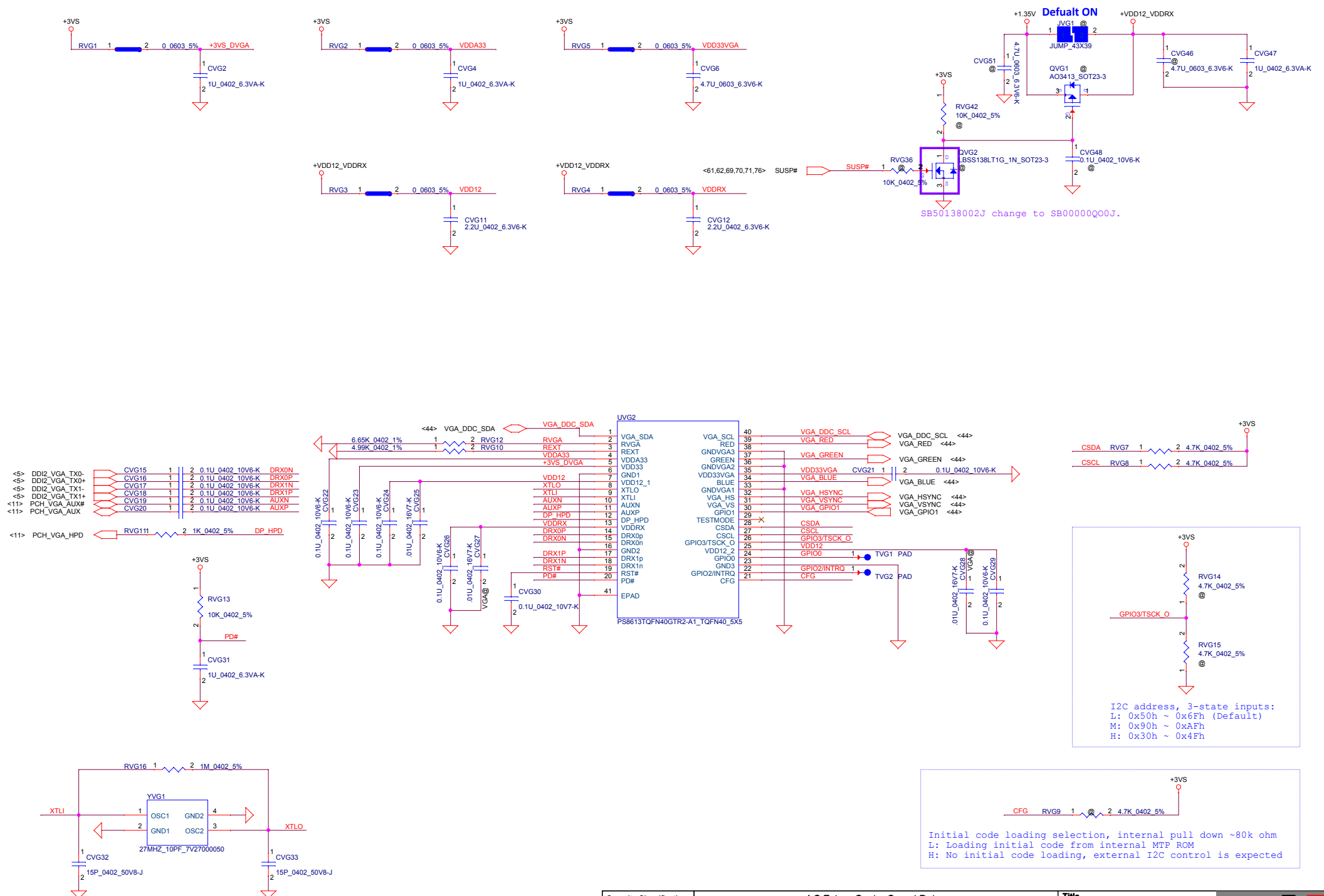
**Auto Mode  
DP Higher Priority**



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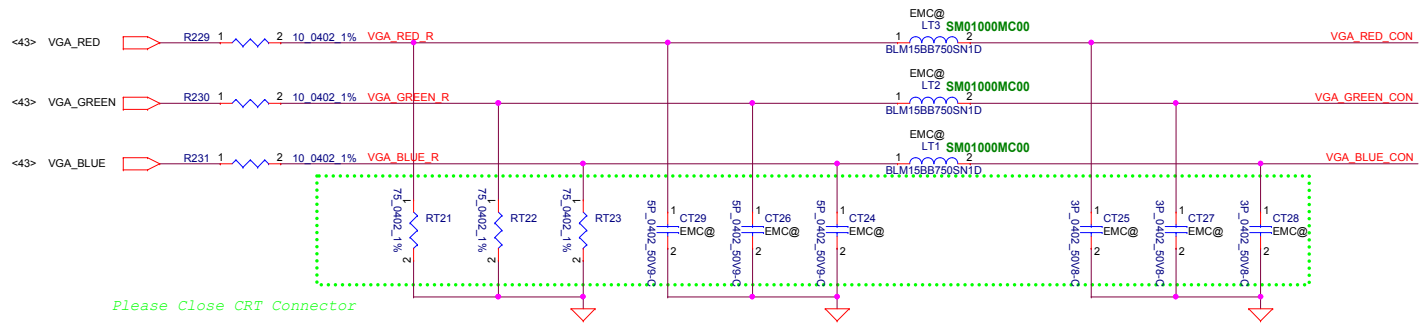
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**LCFC**  
**AITE1 NM-A221**

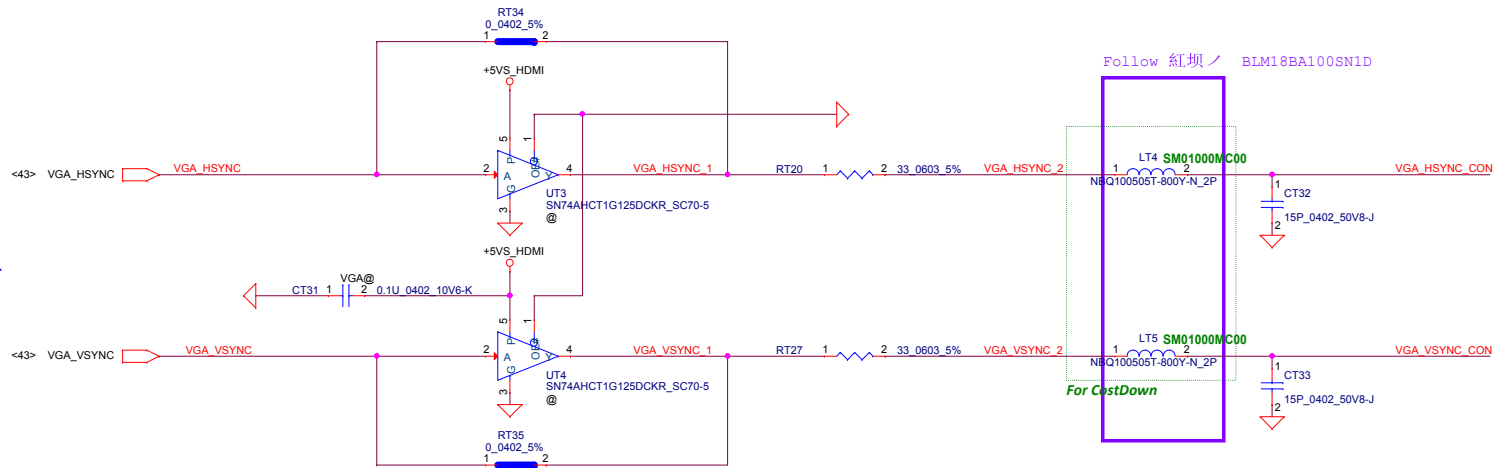


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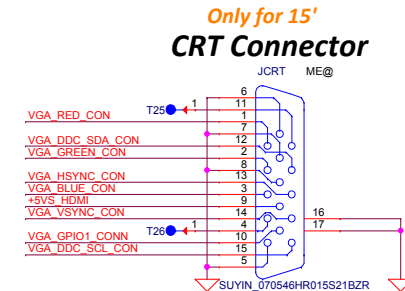


Please Close CRT Connector

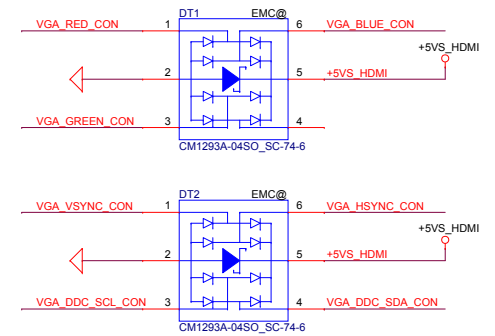
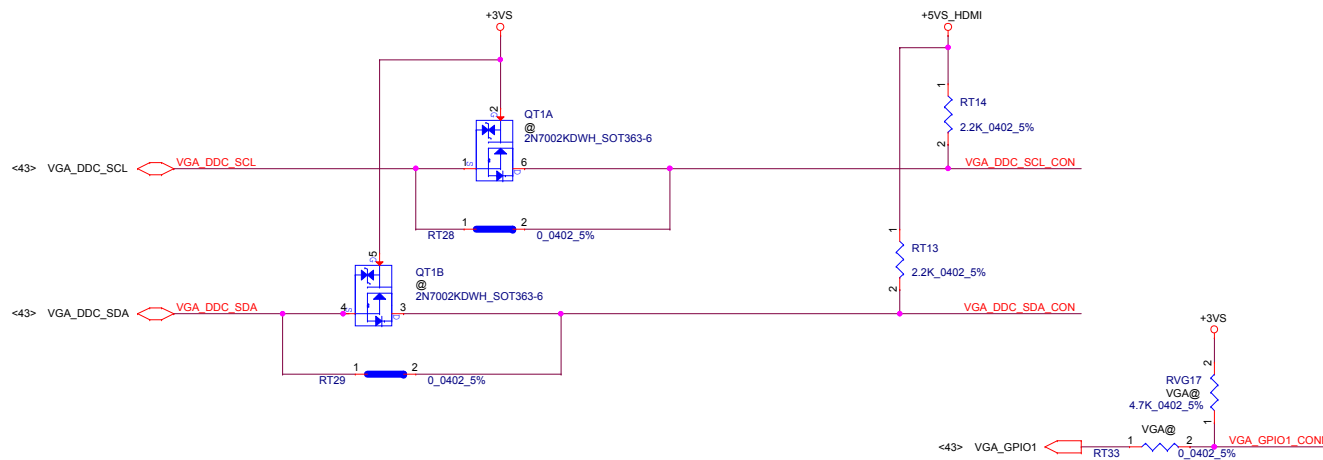


Follow 紅坝 / BLM18BA100SN1D


For CostDown




Traslater

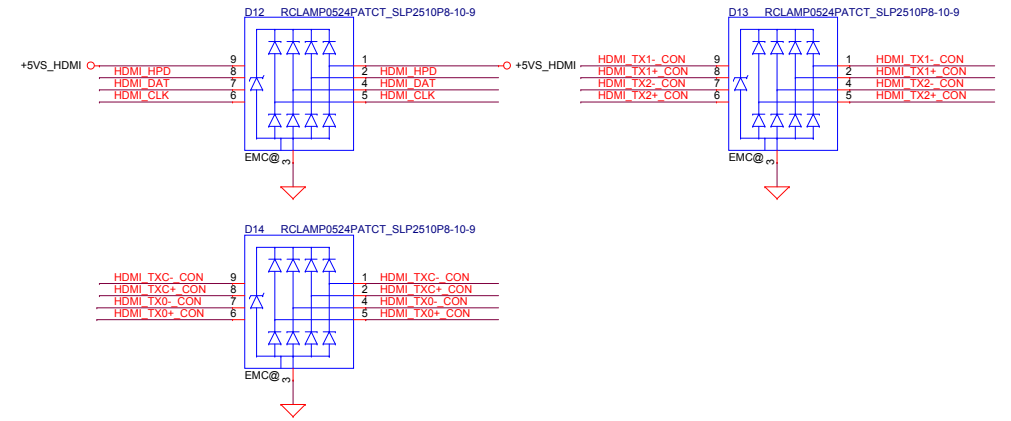
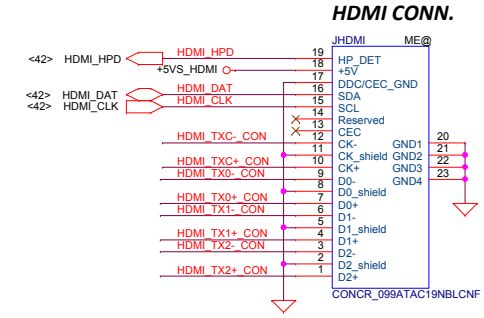
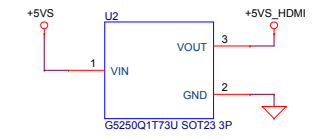
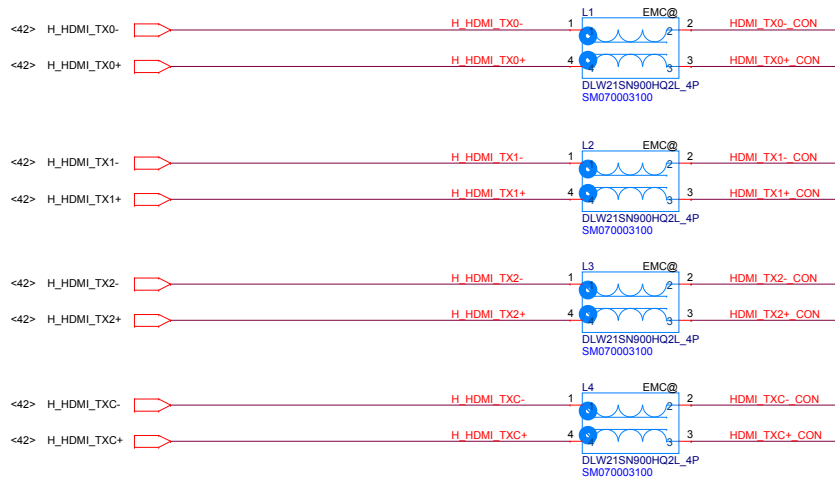


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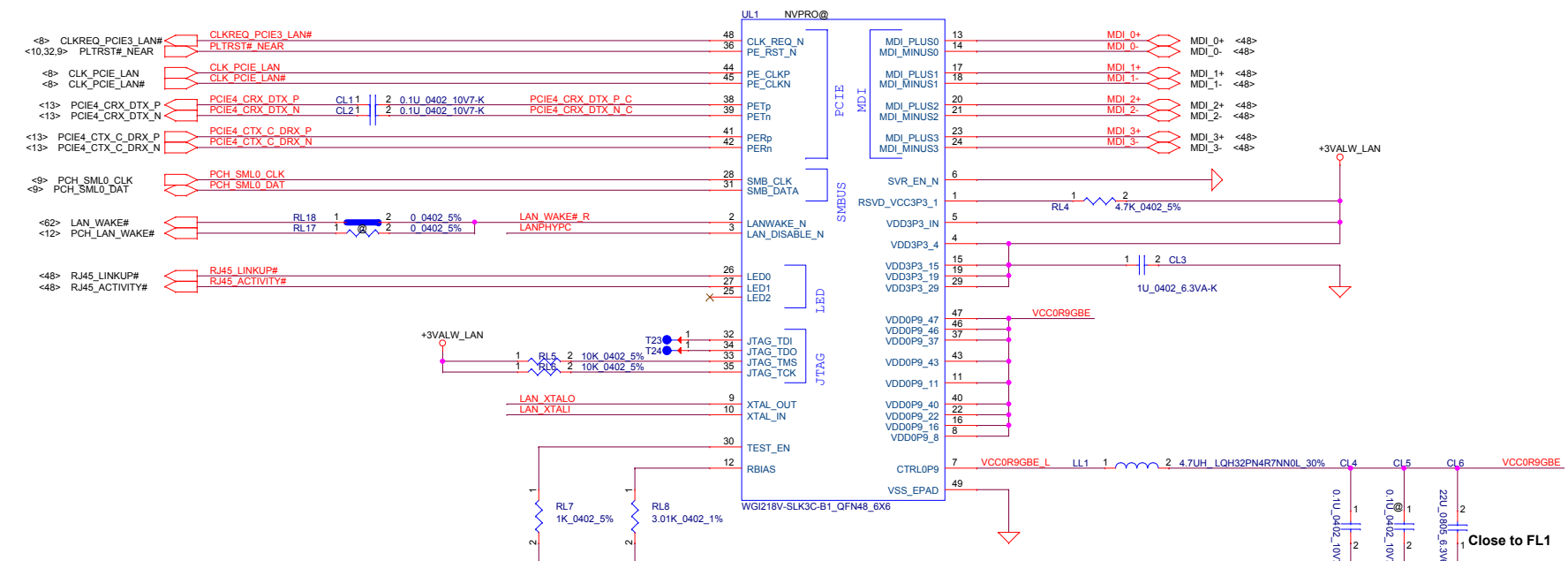
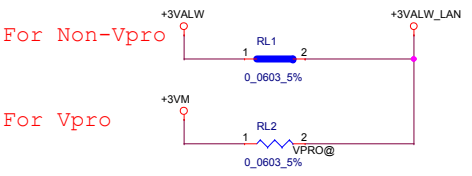

  
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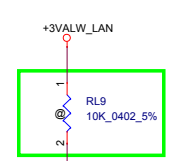
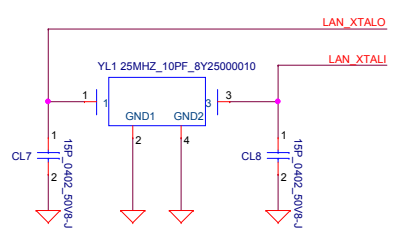
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**UL1 GBE PHY**

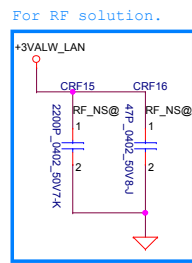
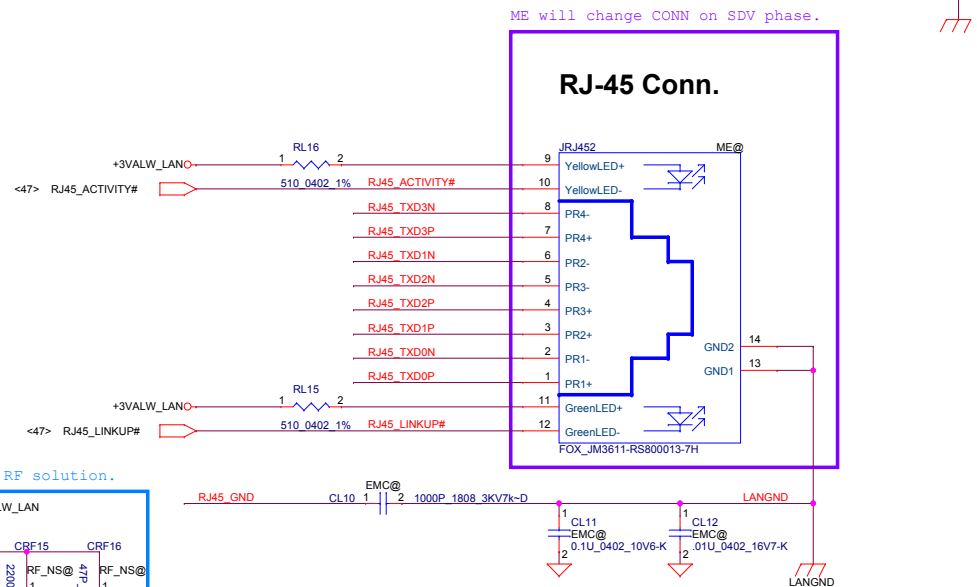
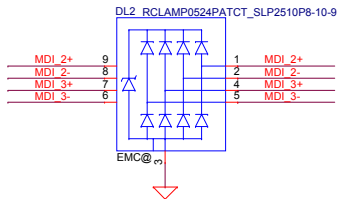
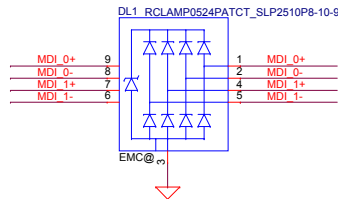
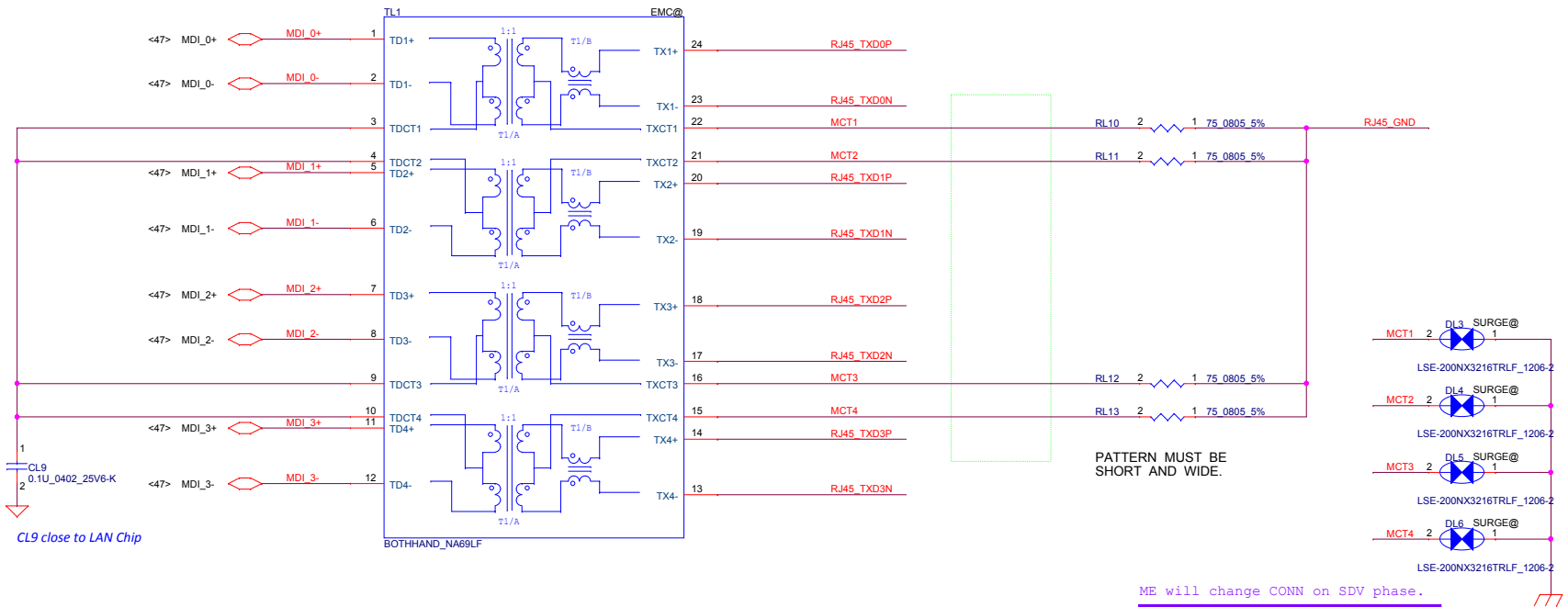
vPro Model	Non-vPro Model
I218LM	I218V

ST-1\_SWG\_SDV-SWG\_EC062  
Add vPro/Non-vPro table.



<12> LANPHYC

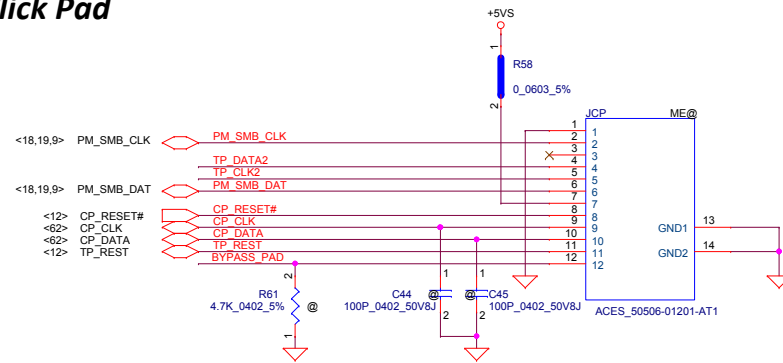
When use Native function, intel recommend pull high 10K ohm  
This part is un-mount in Sting.



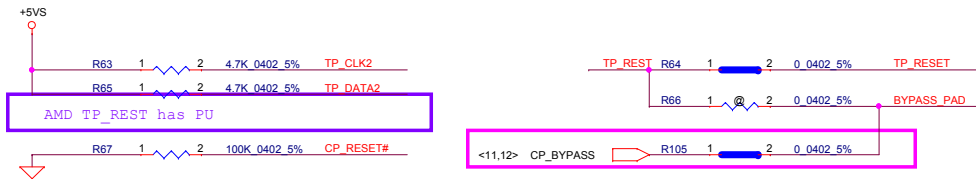
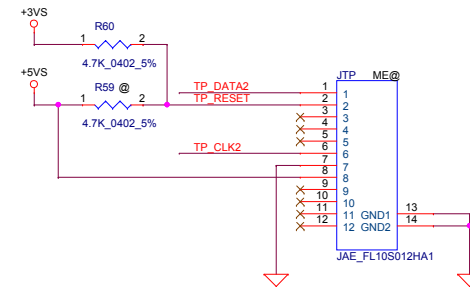
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### Click Pad



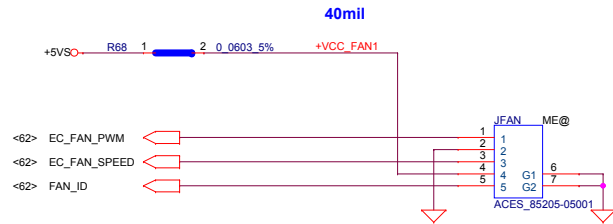
### Track point



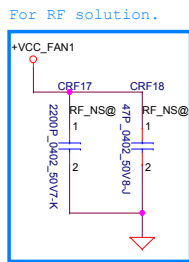
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				Rev	1.0
				Part Number	ATE1 NM-A221



**FAN CONN.**



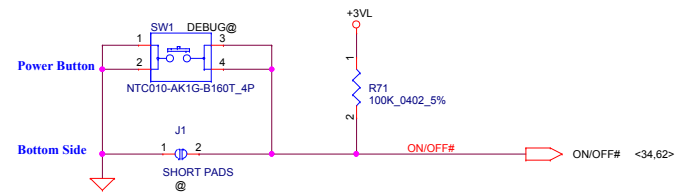
惠璣鐵AMD鐵THERMAL絨板PIN define



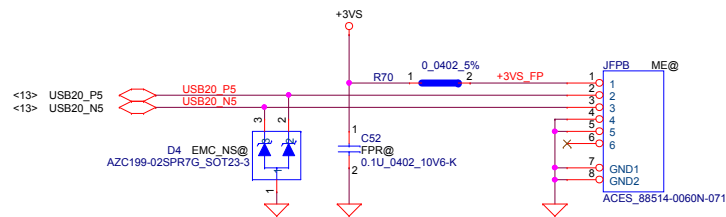
**PWR BTN/LID SW CONN.**

For 14" on board  
For 15" on Sub/B

ON/OFF Switch --> 簿 'Sub/B

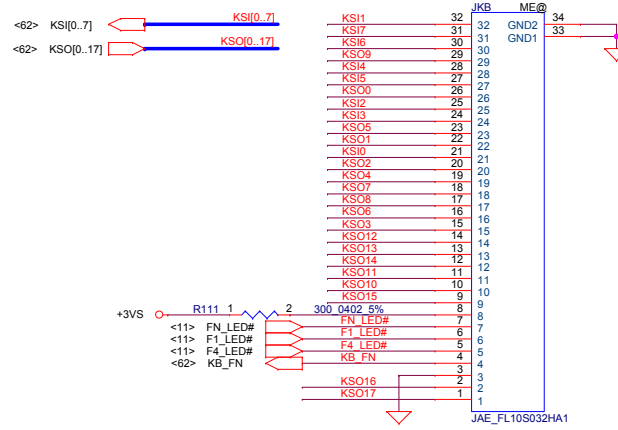


**FingerPrint CONN.**

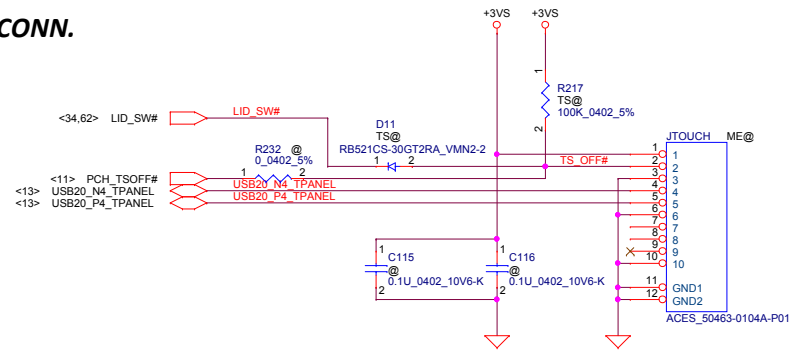


Lid Switch --> 簿 'Sub/B

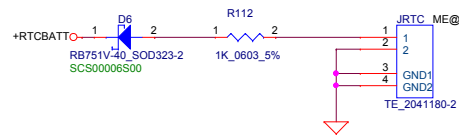
### KB CONN



### TOUCH PANEL CONN.




### RTC CONN.



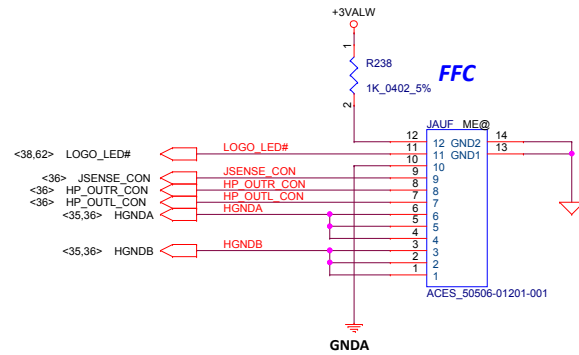
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2013/09/07	Deciphered Date	2014/09/07	
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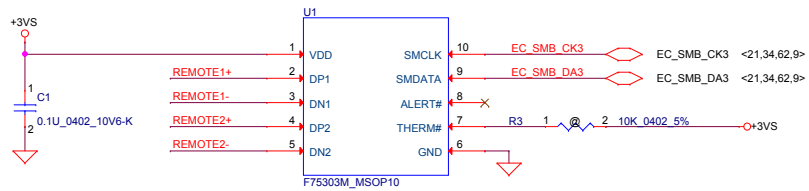
### For Edge 15" Audio board CONNECTOR



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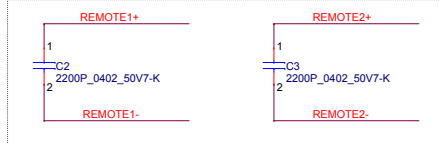
# Thermal Sensor

**Thermal Sensor  
placed near by VRAM**

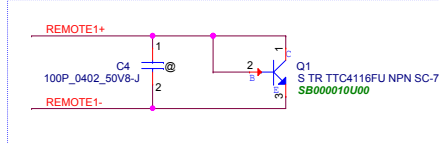


**Address 1001\_101xb**  
*Internal pull up 1.2K to 1.5V*  
*R for initial thermal shutdown temp*

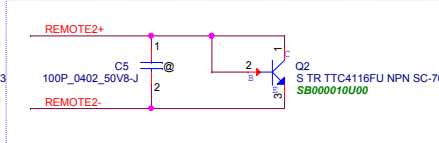
**Close to U1**



**Close to +VCC\_CORE**



**Close JDIMM1&JDIMM2**



**REMOTE2+/-:**  
*Trace width/space:10/10 mil*  
*Trace length:<8"*

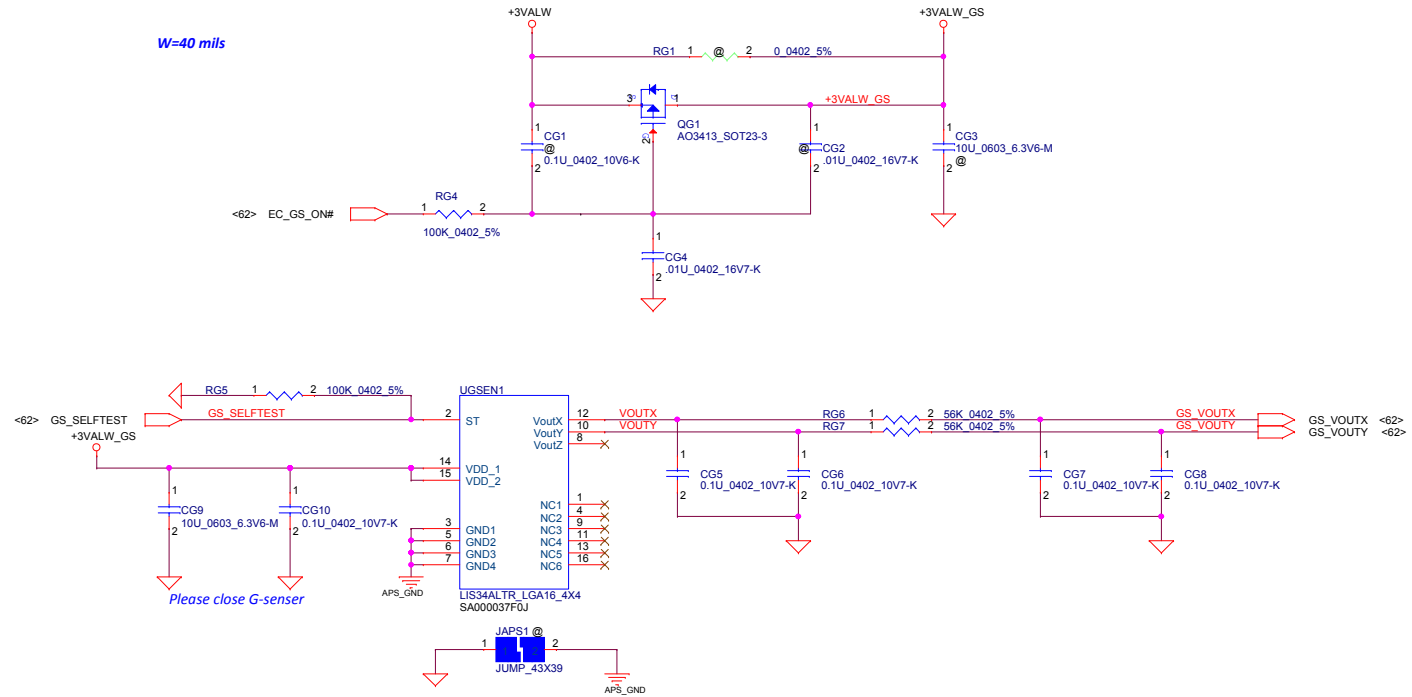
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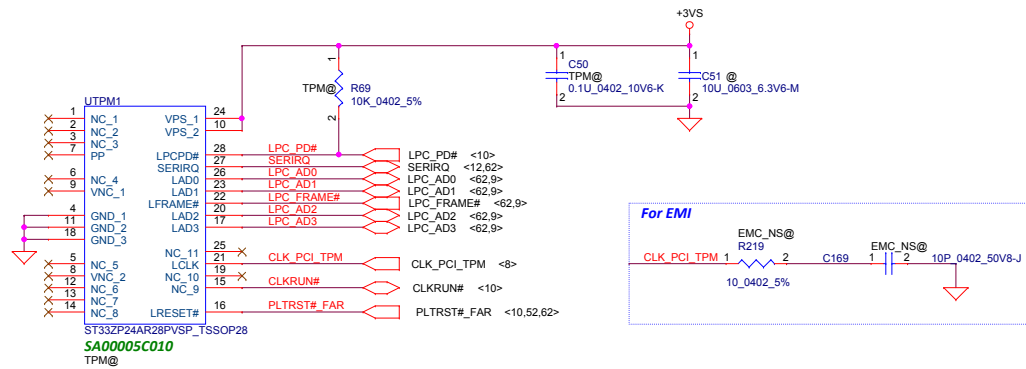
**AITE1 NM-A221**

# APS G-Sensor

W=40 mils



## TPM IC




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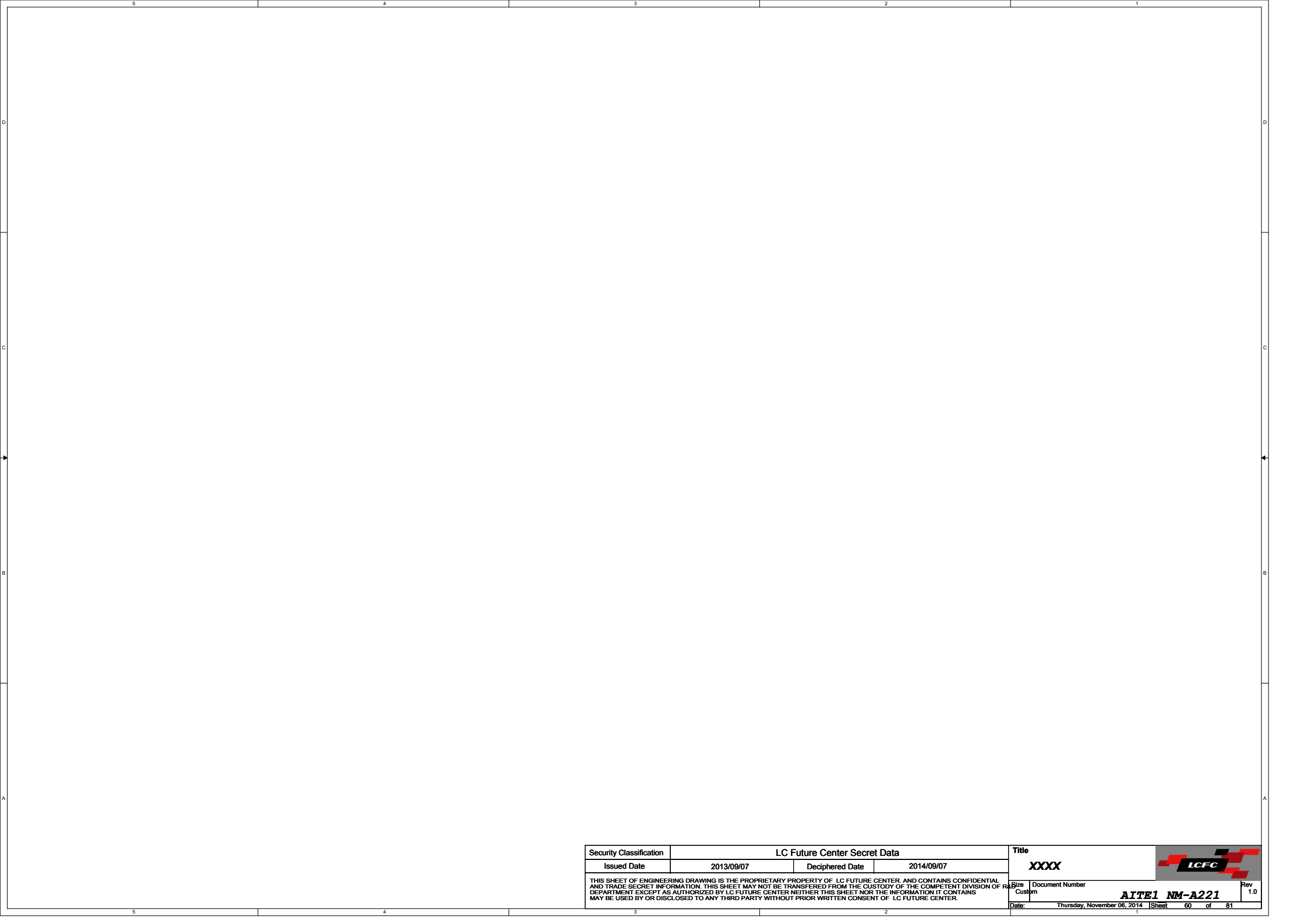
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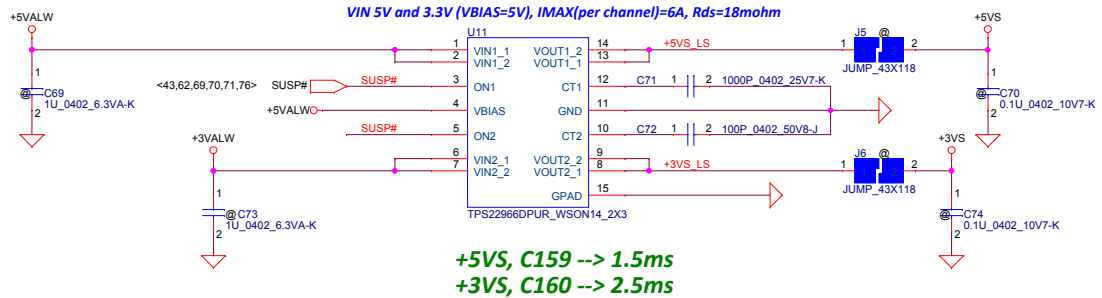
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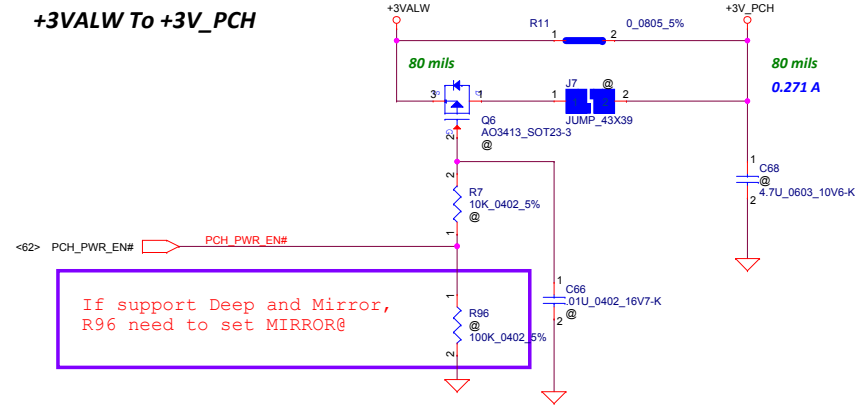


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				<small>Date:</small> Thursday, November 08, 2014	<small>Rev</small> <b>AITE1 NM-A221</b> 1.0
					<small>Sheet</small> 60 <small>of</small> 81

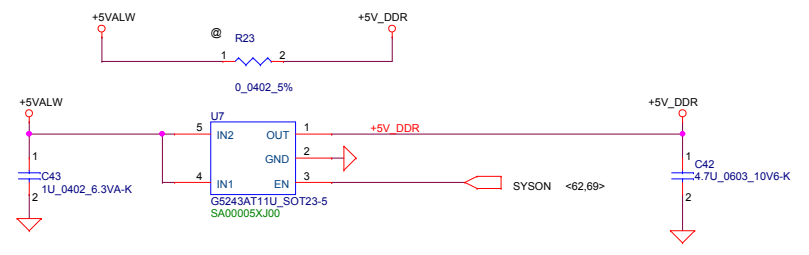
**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**



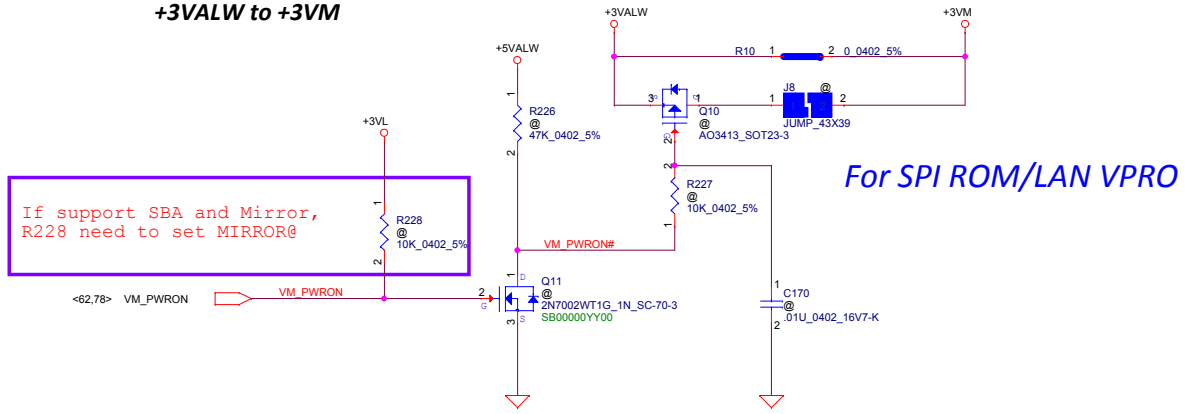
**+3VALW To +3V\_PCH**



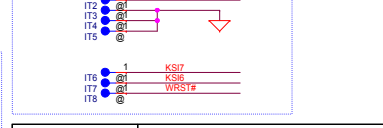
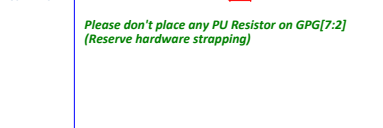
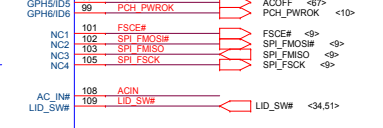
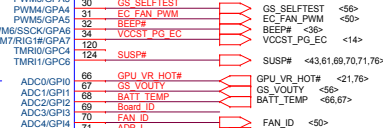
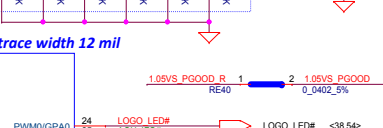
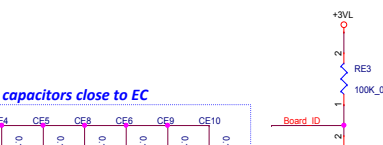
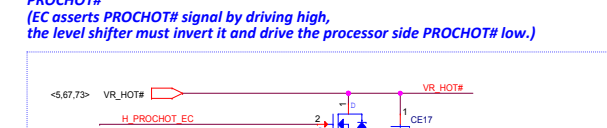
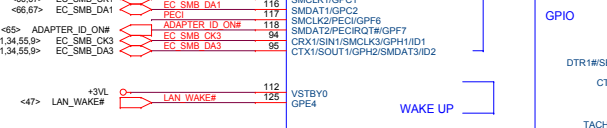
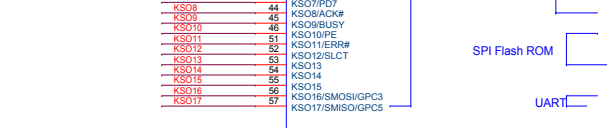
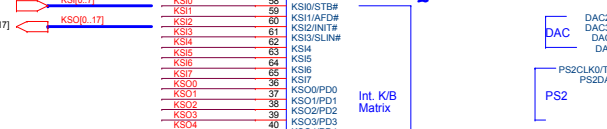
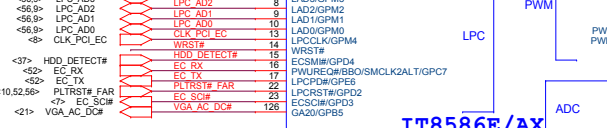
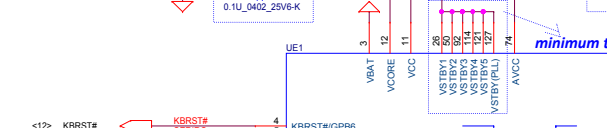
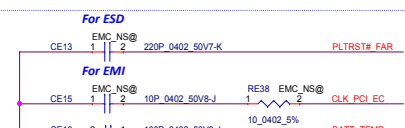
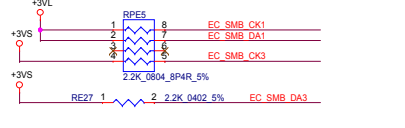
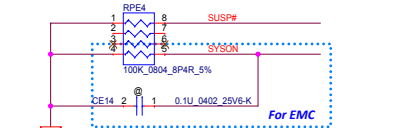
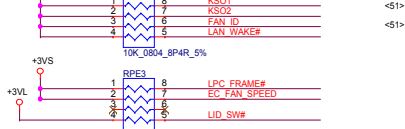
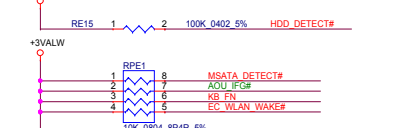
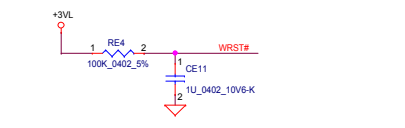
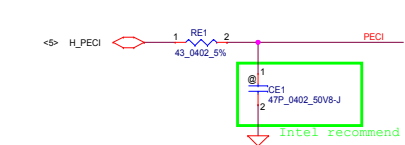
**+5VALW To +5V\_DDR**



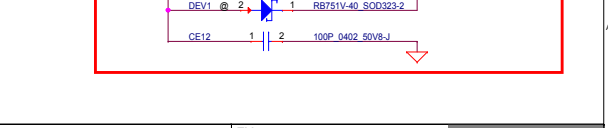
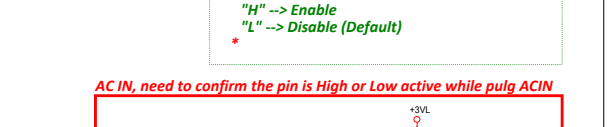
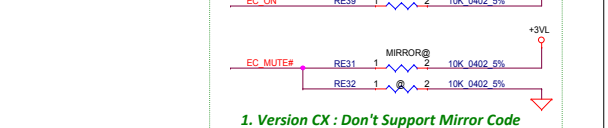
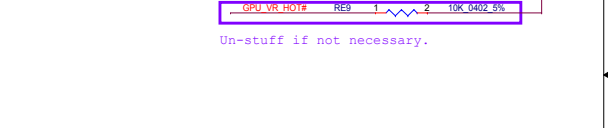
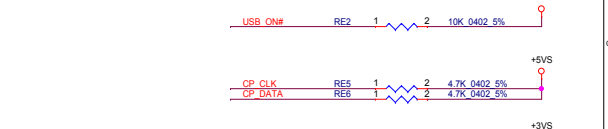
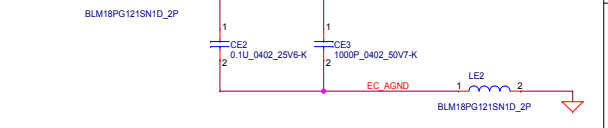
**+3VALW to +3VM**



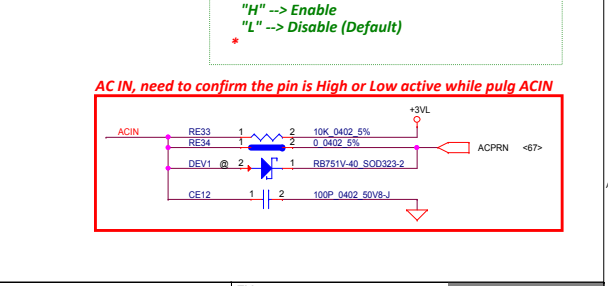
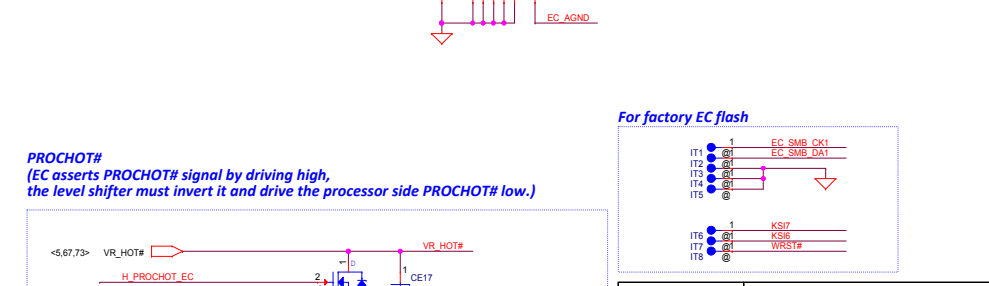
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Board ID	RE7	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



Pin	Signal	Component	Value
1	KBRST#	RE1	43.0402_5%
2	WRST#	RE4	100K_0402_5%
3	HDD_DETECT#	RE15	100K_0402_5%
4	MSATA_DETECT#	RPE1	10K_0804_8P4R_5%
5	LAN_WAKE#	RPE2	10K_0804_8P4R_5%
6	LPC_FRAME#	RPE3	10K_0804_8P4R_5%
7	EC_FAN_SPEED	RPE4	10K_0804_8P4R_5%
8	LID_SW#	RPE5	10K_0804_8P4R_5%
9	EC_SMB_CK1	RPE6	10K_0804_8P4R_5%
10	EC_SMB_DAT1	RPE6	10K_0804_8P4R_5%
11	EC_SMB_CK3	RPE6	10K_0804_8P4R_5%
12	EC_SMB_DAT3	RPE6	10K_0804_8P4R_5%
13	LAN_WAKE#	RE27	2.2K_0402_5%
14	USB_ON#	RE28	10K_0402_5%
15	MSATA_DETECT#	RE29	10K_0402_5%
16	EC_WAKE#	RE30	10K_0402_5%
17	AC_PRESENT	RE31	10K_0402_5%
18	VBAT	RE11	100K_0402_1%
19	VCORE	RE12	100K_0402_1%
20	VCC	RE13	100K_0402_1%
21	V <sub>AD_BID</sub>	RE7	4.7K_0402_1%
22	CE1	CE1	47PF_0402_50V8-J
23	CE11	CE11	1U_0402_10V6-K
24	CE14	CE14	0.1U_0402_25V6-K
25	CE15	CE15	0.1U_0402_25V6-K
26	CE16	CE16	100PF_0402_50V8-J
27	CE17	CE17	100PF_0402_50V8-J
28	CE18	CE18	0.1U_0402_25V6-K
29	CE19	CE19	0.1U_0402_25V6-K
30	CE20	CE20	0.1U_0402_25V6-K
31	CE21	CE21	0.1U_0402_25V6-K
32	CE22	CE22	0.1U_0402_25V6-K
33	RE40	RE40	1.05VS_PG00D_R
34	RE41	RE41	1.05VS_PG00D
35	RE2	RE2	10K_0402_5%
36	RE8	RE8	10K_0402_5%
37	RE9	RE9	10K_0402_5%
38	RE39	RE39	10K_0402_5%
39	RE31	RE31	10K_0402_5%
40	RE33	RE33	10K_0402_5%



**PROCHOT#**  
 (EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)

**For factory EC flash**

**For ESD**

**For EMI**

**BATT\_TEMP 續續 EC ADC pin**

**ACIN, need to confirm the pin is High or Low active while pulg ACIN**

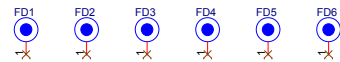
**1. Version CX : Don't Support Mirror Code**  
**Version DX/EX/FX : Support Mirror Code**  
**"H" --> Enable**  
**"L" --> Disable (Default)**


## Screw Hole




Center Zero

## PCB Fedcal Mark PAD

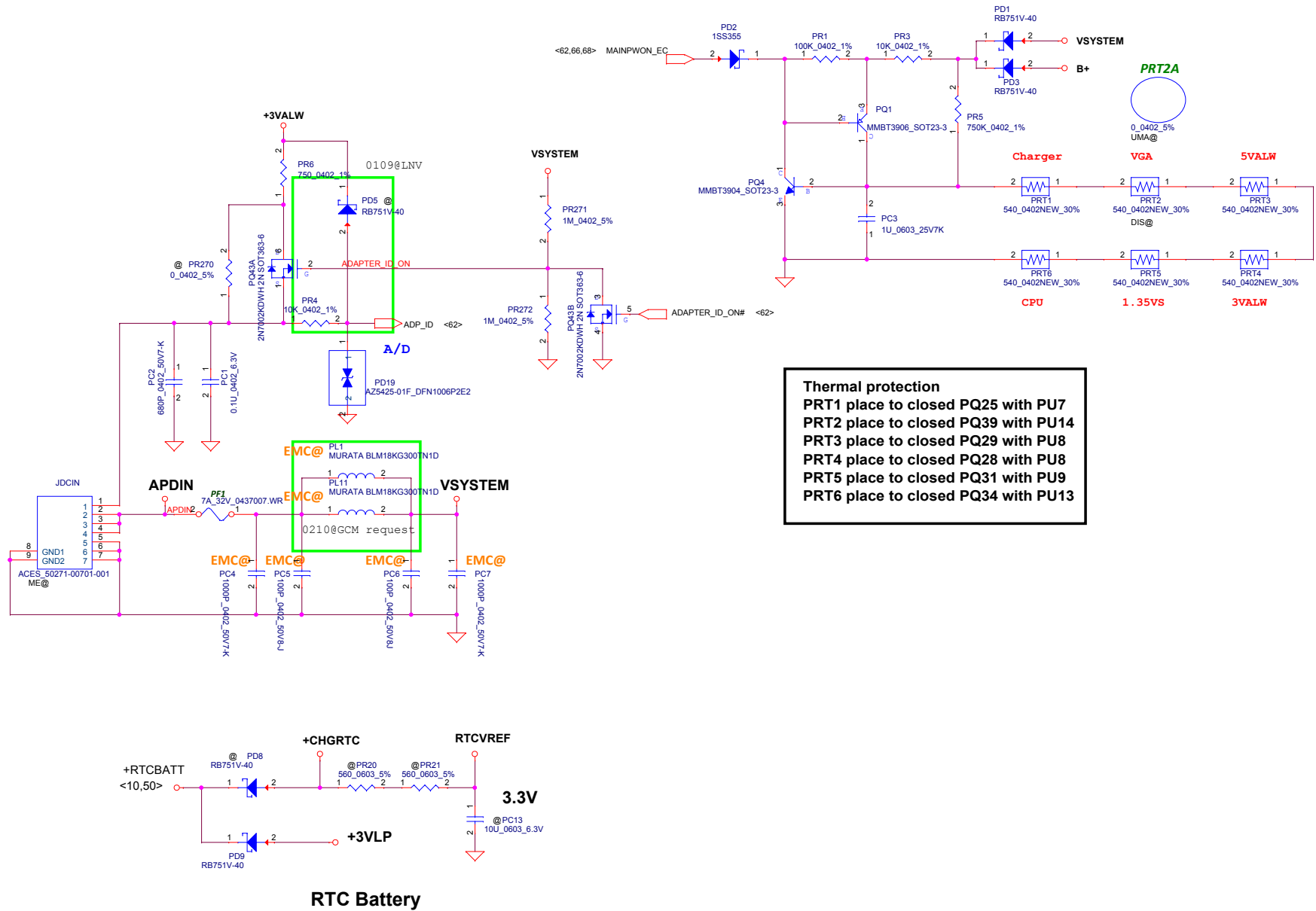


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**Thermal protection**  
 PRT1 place to closed PQ25 with PU7  
 PRT2 place to closed PQ39 with PU14  
 PRT3 place to closed PQ29 with PU8  
 PRT4 place to closed PQ28 with PU8  
 PRT5 place to closed PQ31 with PU9  
 PRT6 place to closed PQ34 with PU13

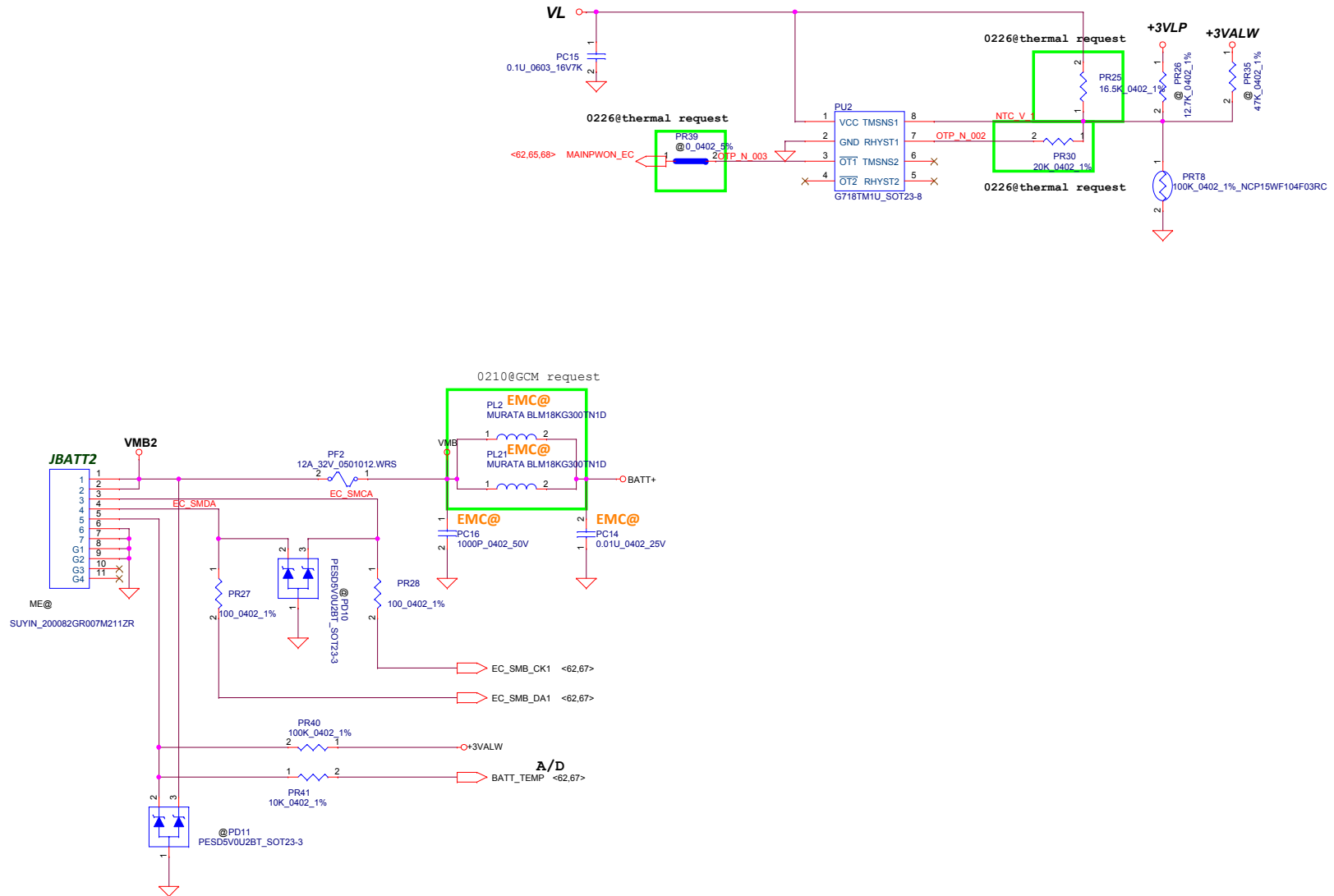
**RTC Battery**

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**PRT8 under CPU bottom side :**  
**CPU thermal protection at 93 +/-3 degree C**  
**Recovery at 56 +/-3 degree C**

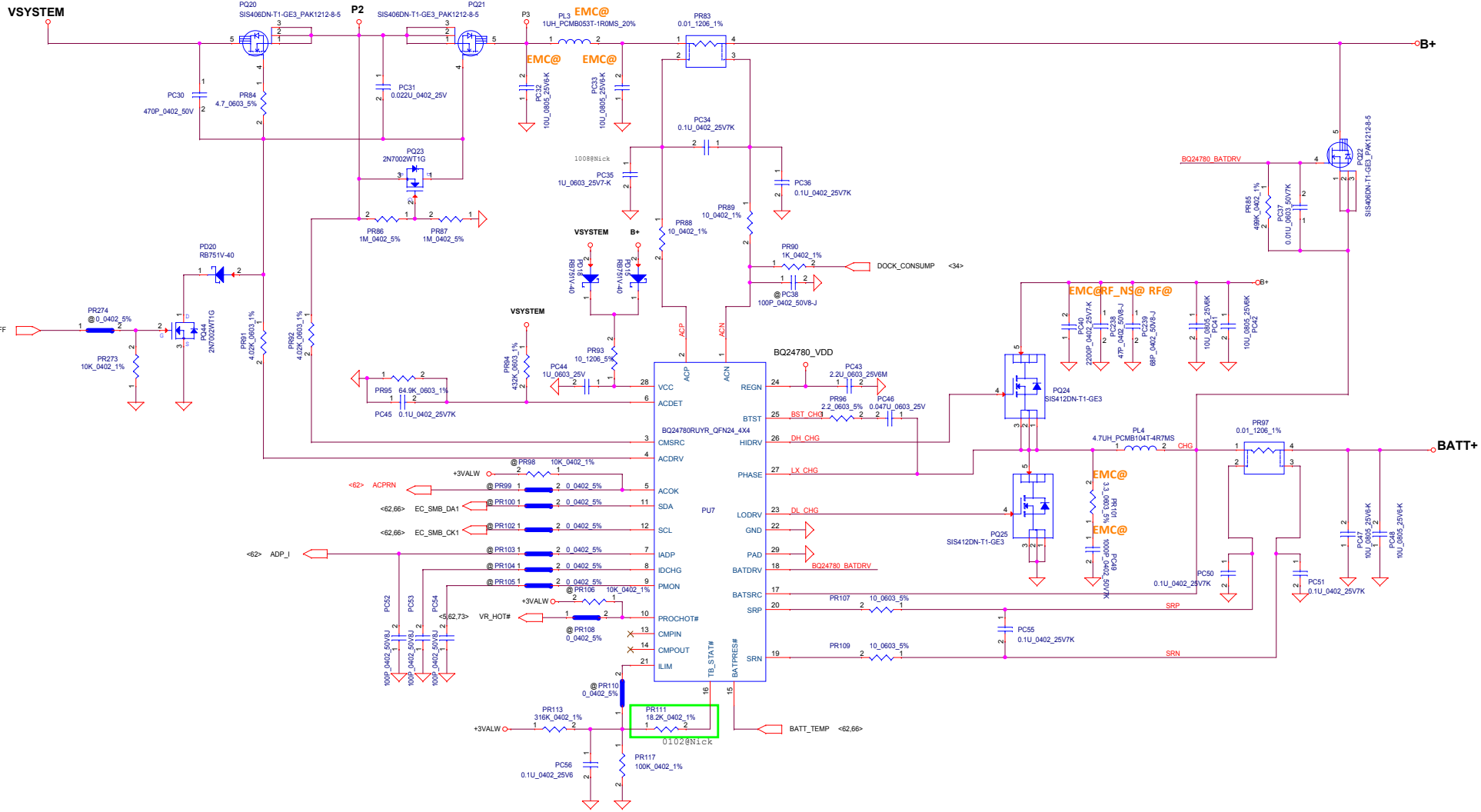



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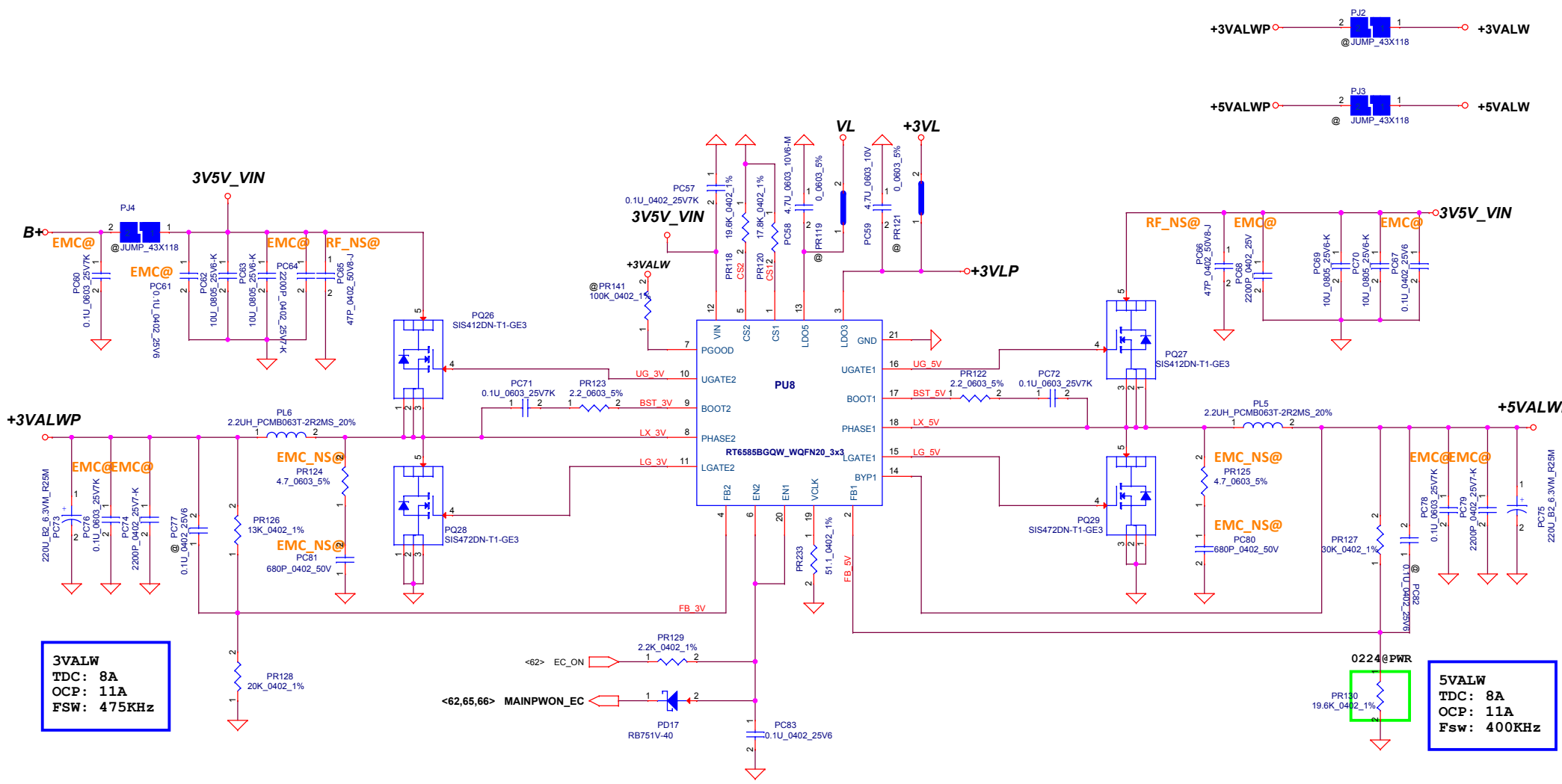
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Document Number	AITE1 NM-A221	
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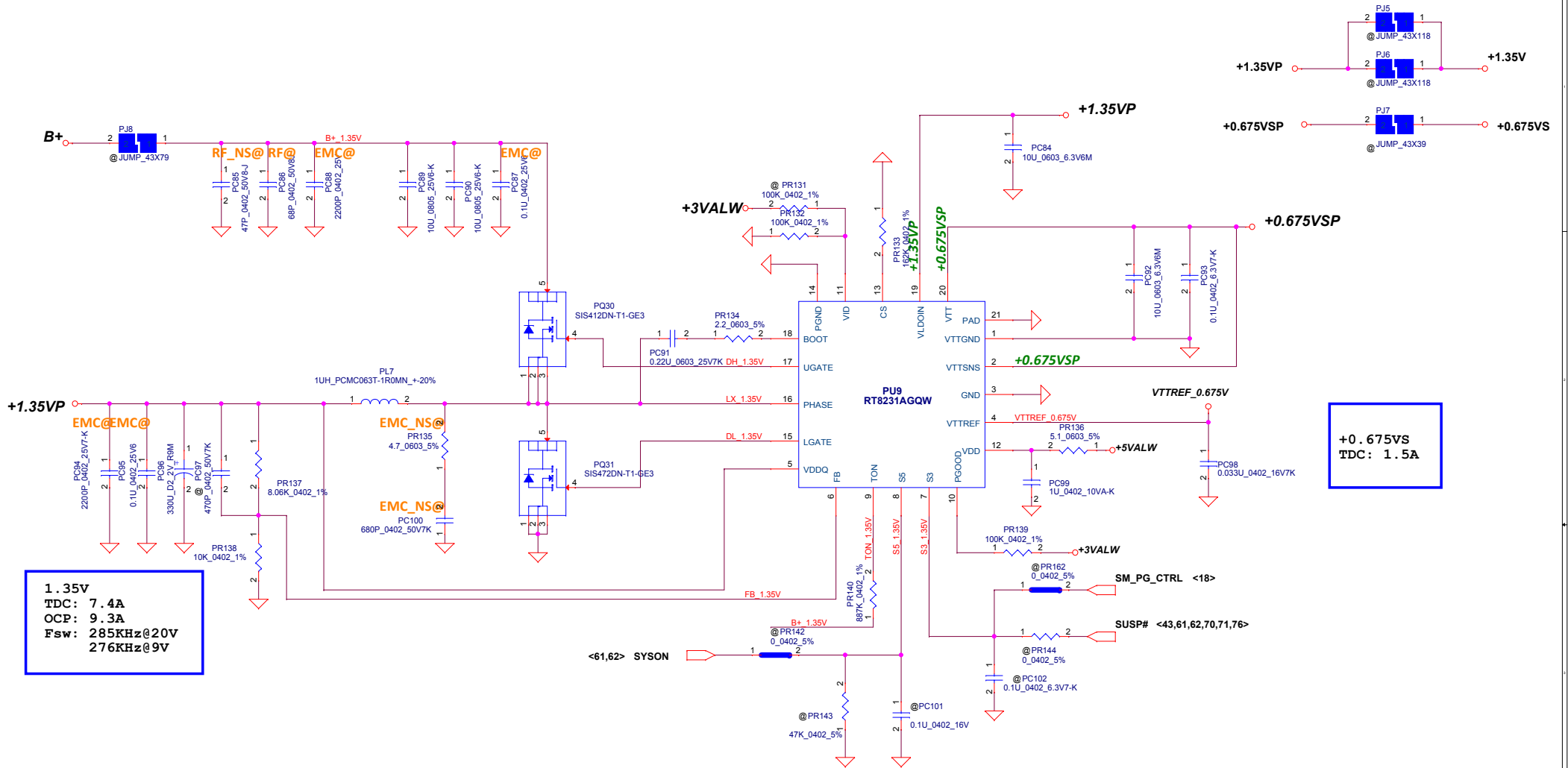
**3VALW**  
 TDC: 8A  
 OCP: 11A  
 FSW: 475KHz

**5VALW**  
 TDC: 8A  
 OCP: 11A  
 Fsw: 400KHz

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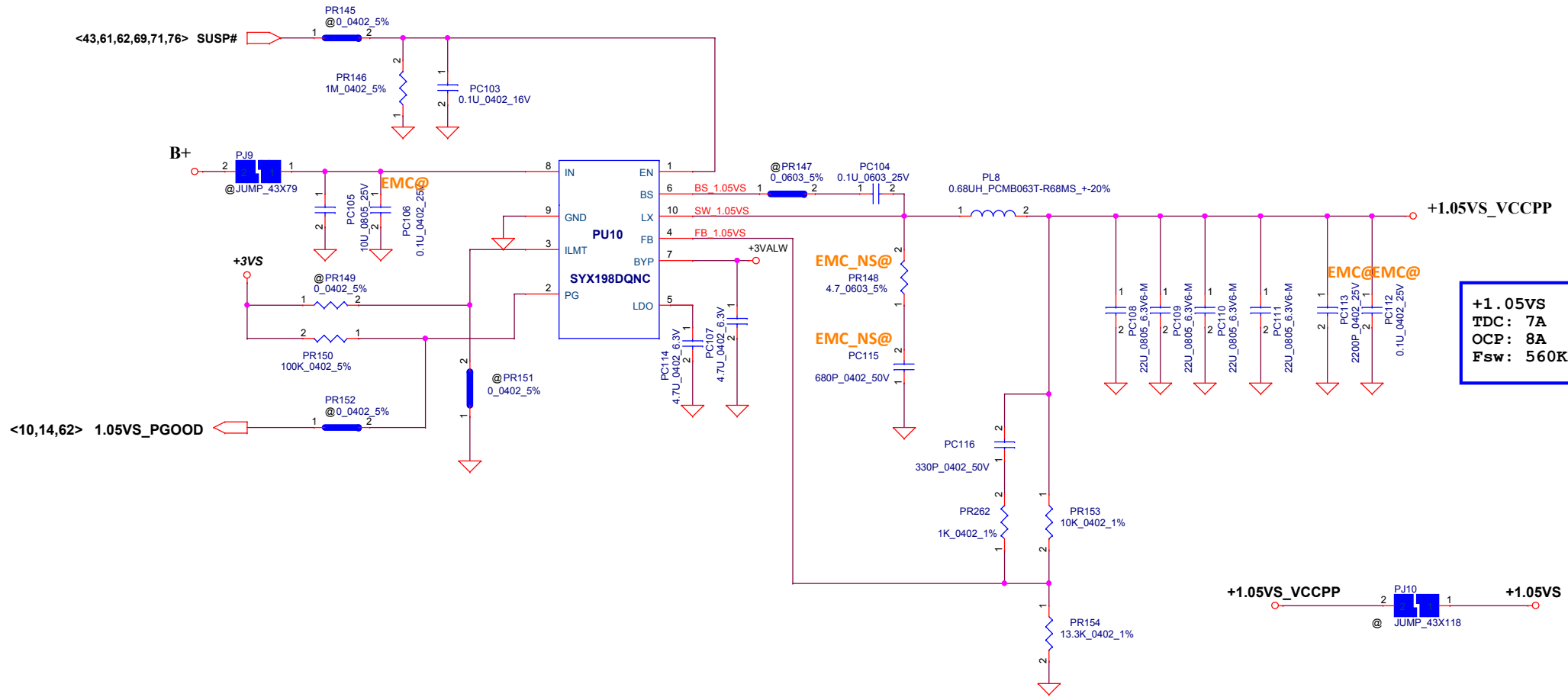
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Size	Document Number	Rev
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Title		LCFC	
<b>+1.35V/+0.675VS</b>		Size Custom	Document Number
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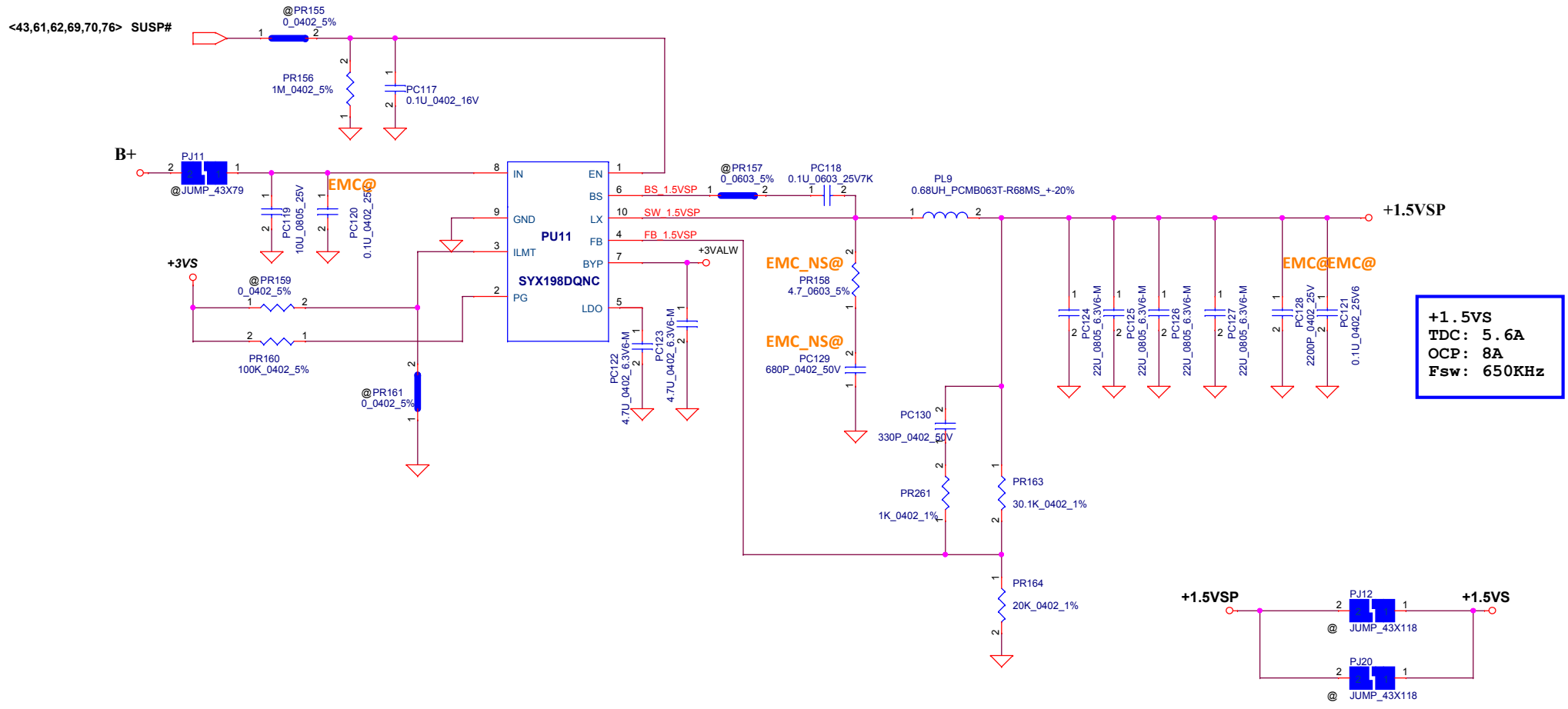


**+1.05VS**  
**TDC: 7A**  
**OCP: 8A**  
**Fsw: 560KHz**

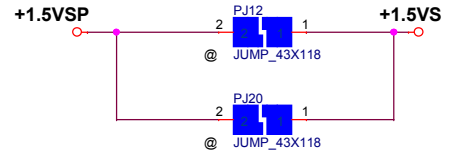
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Issued Date	2013/08/05	Deciphered Date	2014/12/31
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Title	<b>+1.05VS</b>		
Document Number	<b>AITE1 NM-A221</b>		
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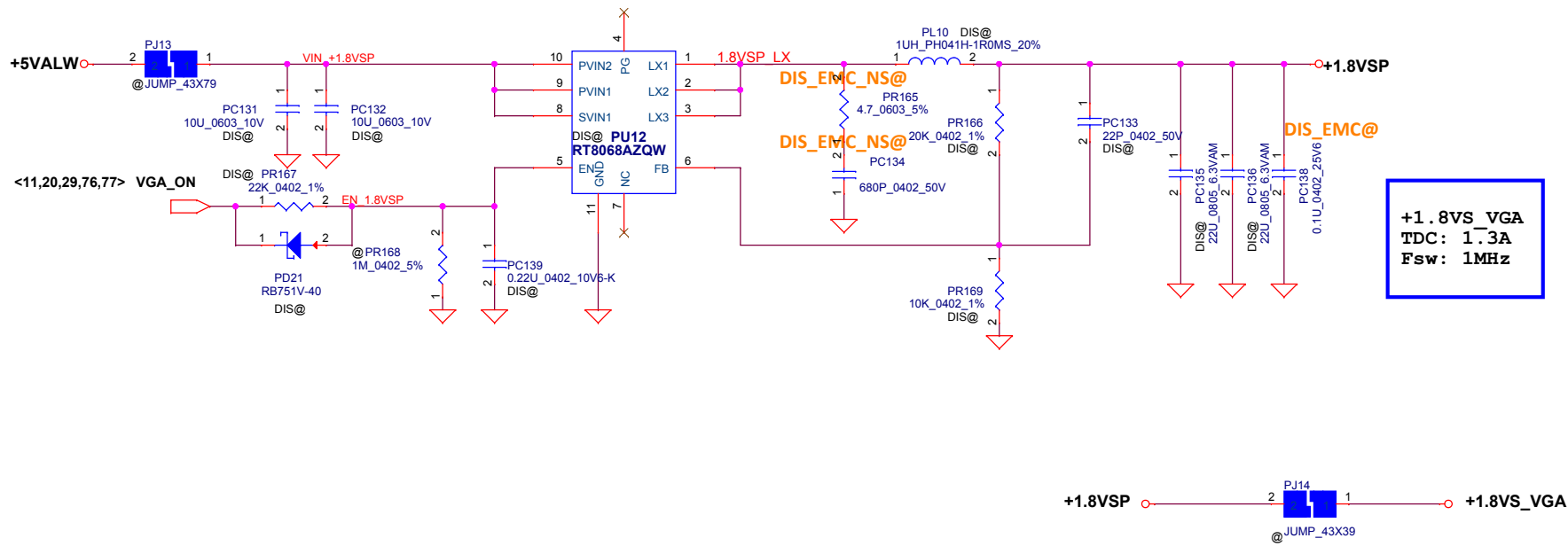





**+1.5VS**  
**TDC: 5.6A**  
**OCP: 8A**  
**Fsw: 650KHz**

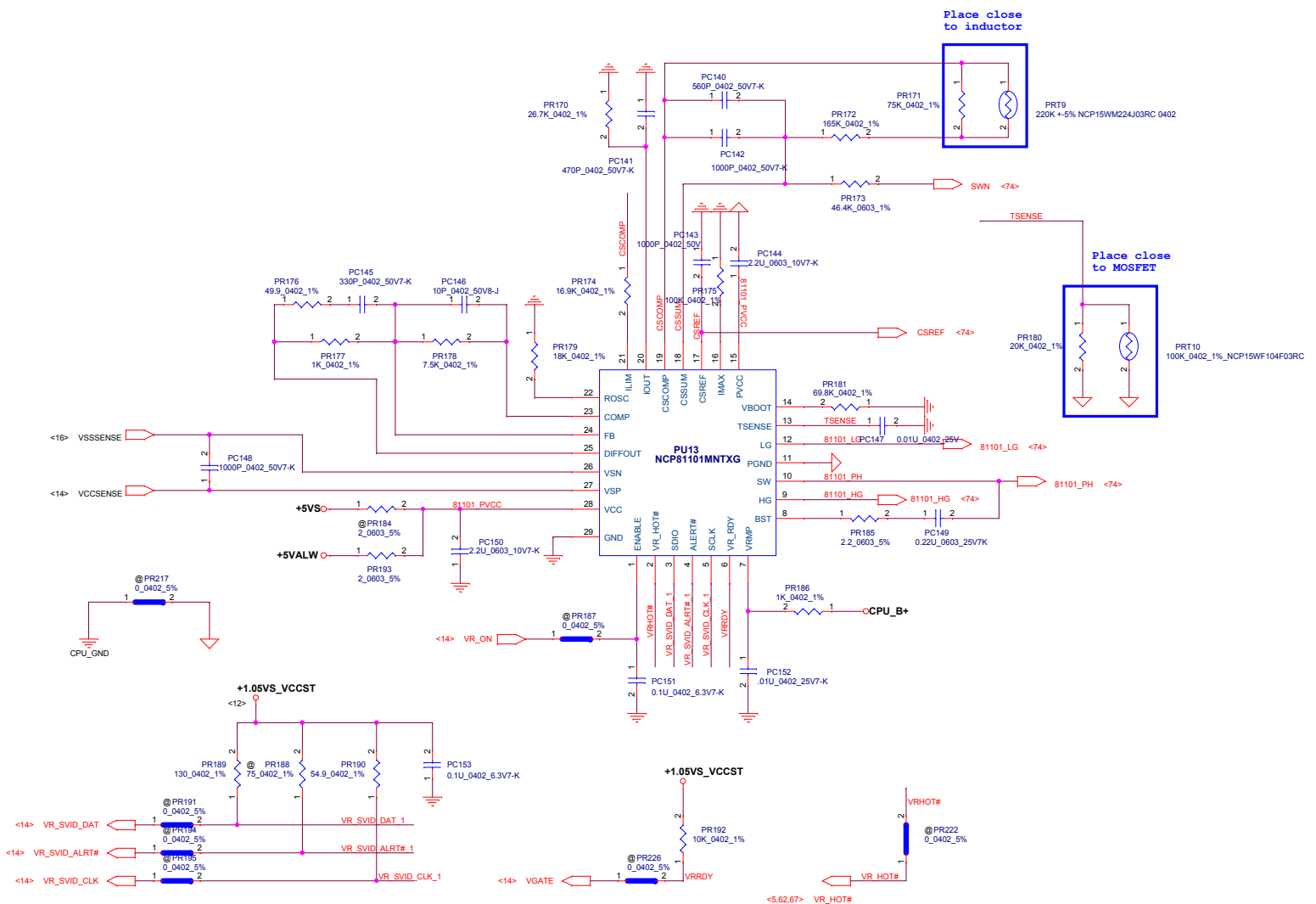


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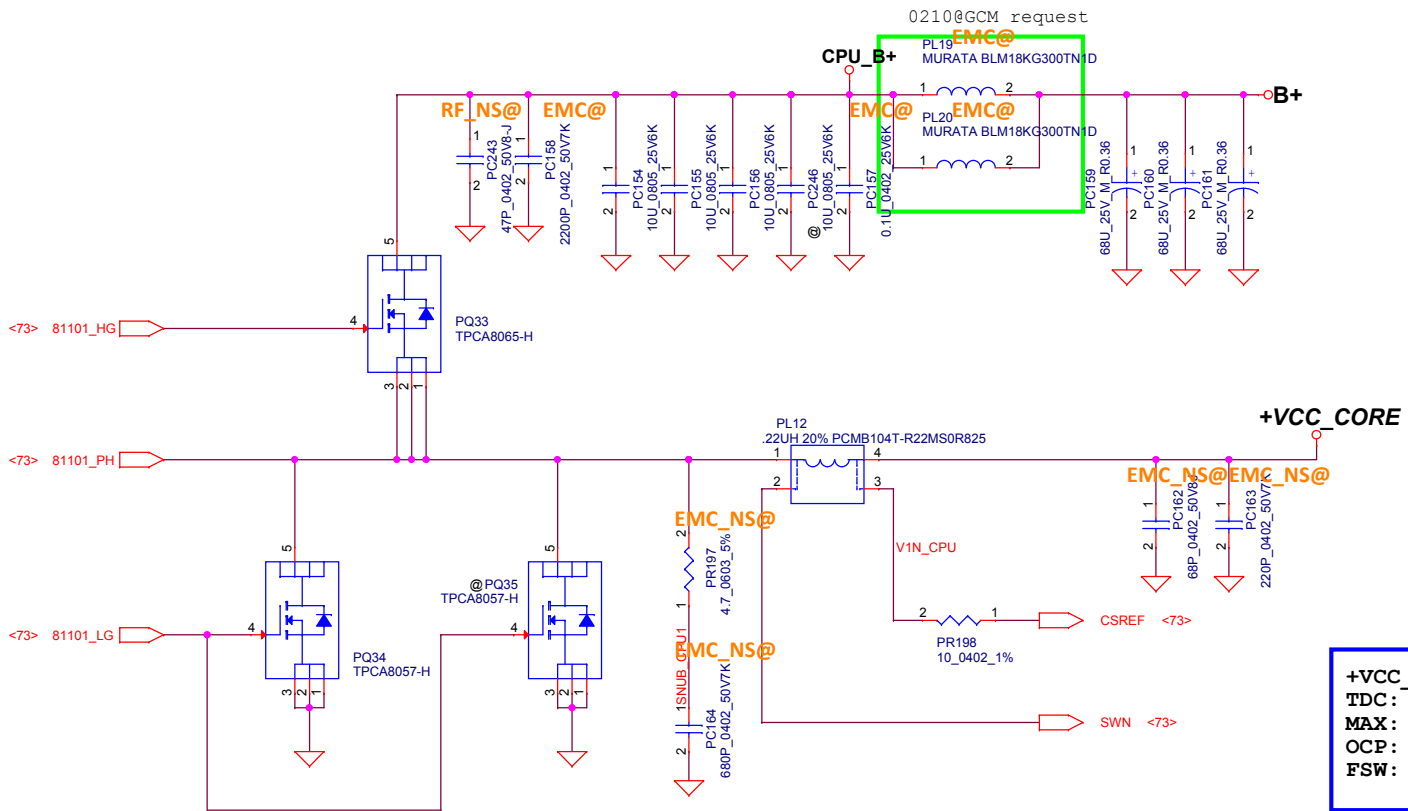


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<b>+VCC_CORE</b>
TDC: 10A
MAX: 32A
OCP: 42A
FSW: 560KHz@20V
670KHz@9V

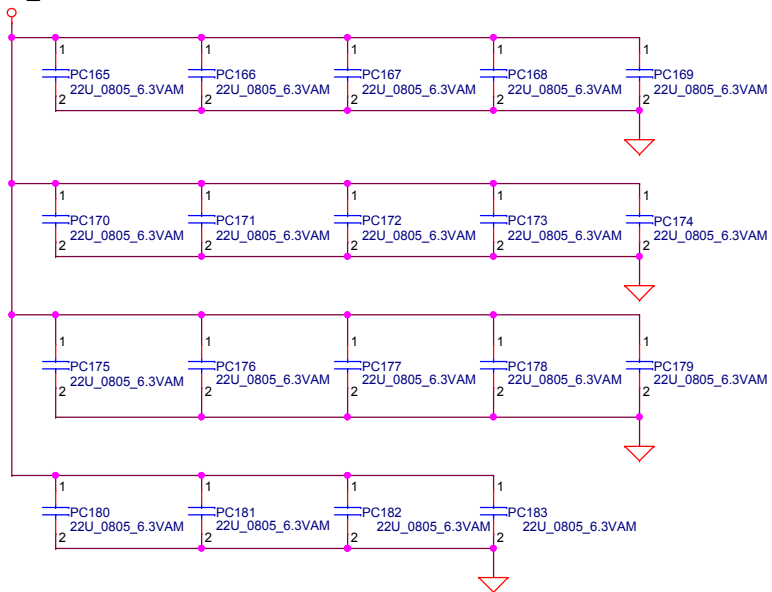
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Title	<b>+CPU_CORE2</b>	
Document Number	AITE1 NM-A221	
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Based on PDDG rev 0.7 Table 5-1.

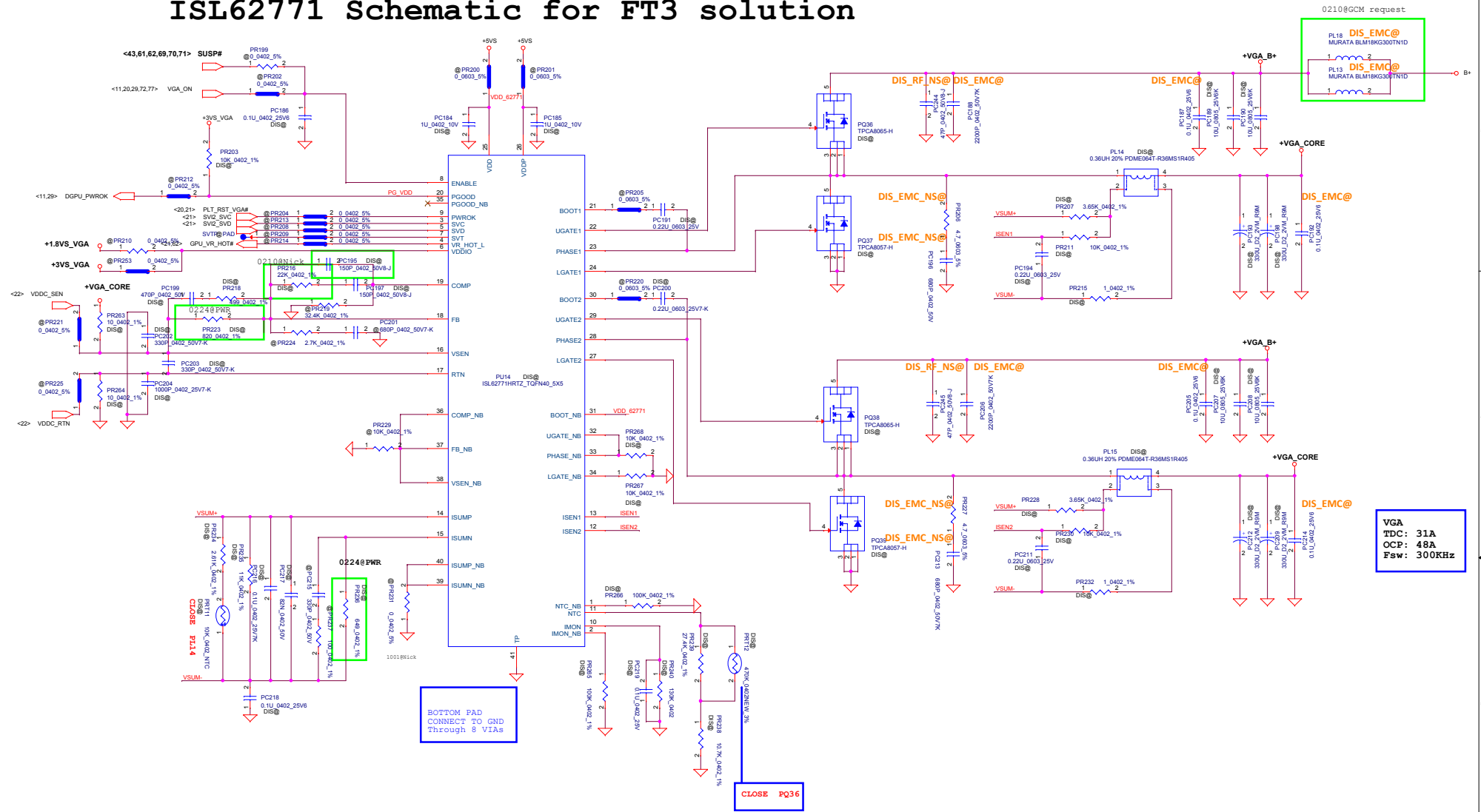
**+VCC\_CORE**



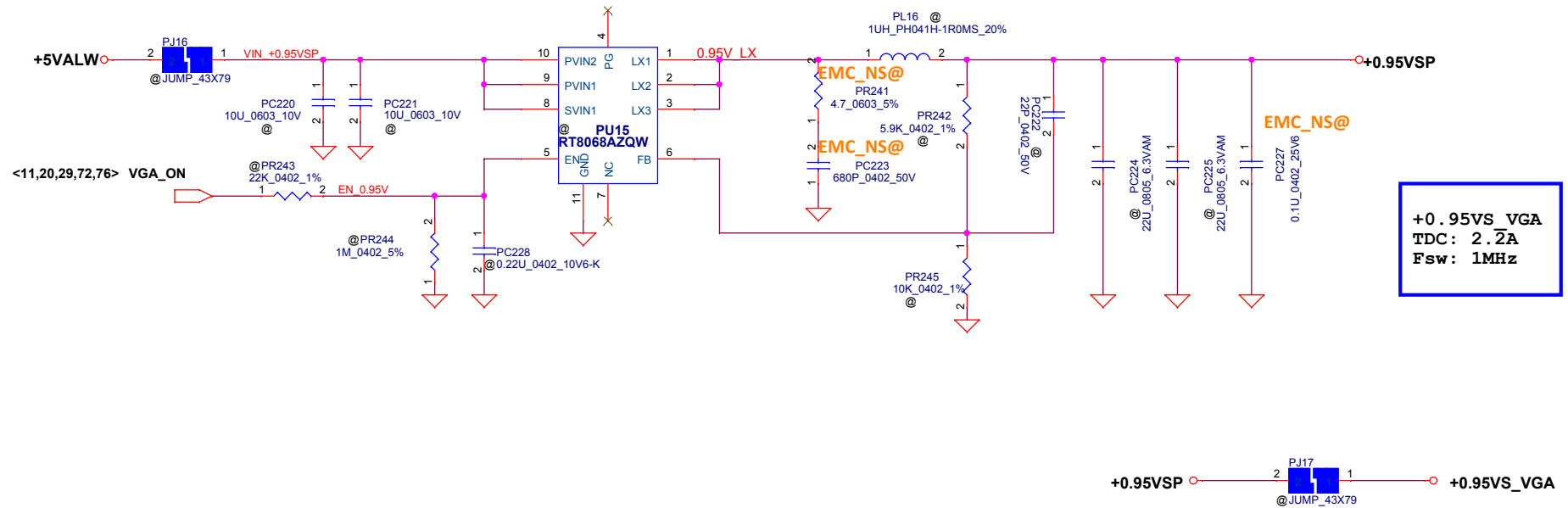
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# ISL62771 Schematic for FT3 solution

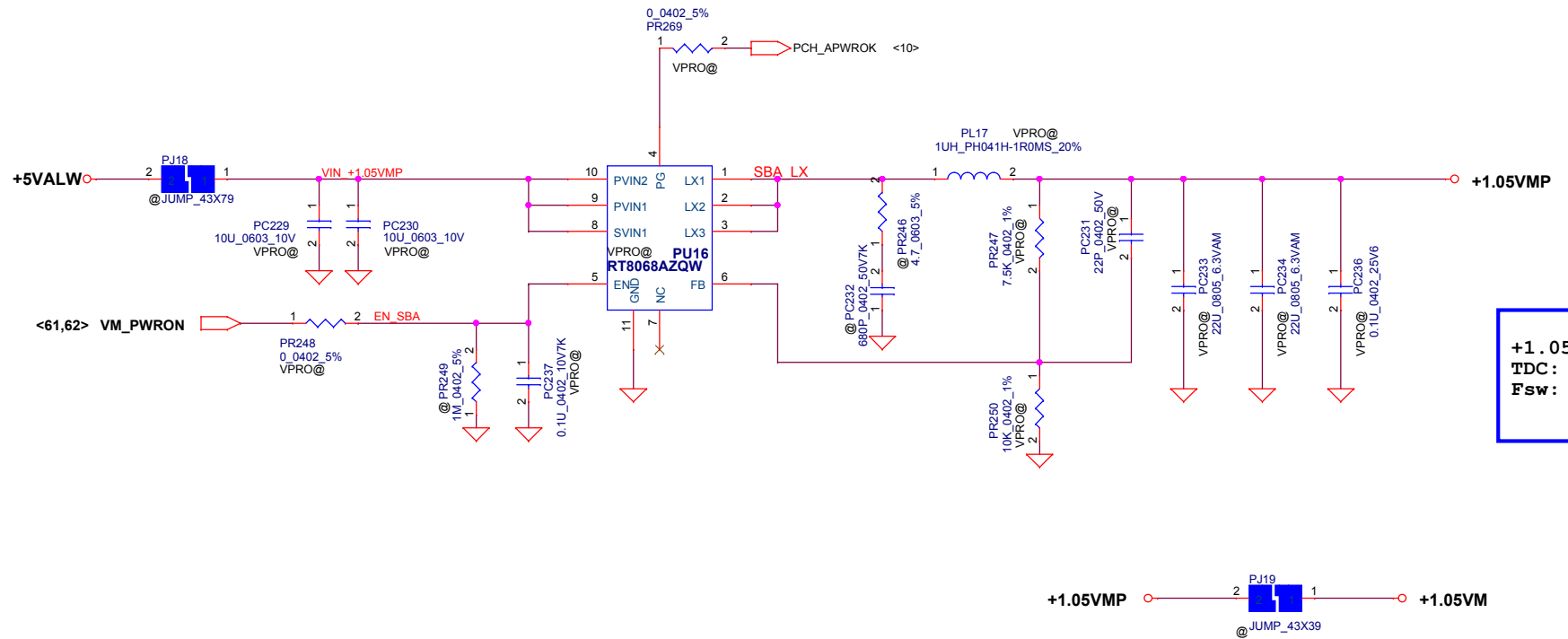


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**+0.95VS\_VGA**  
**TDC: 2.2A**  
**Fsw: 1MHz**

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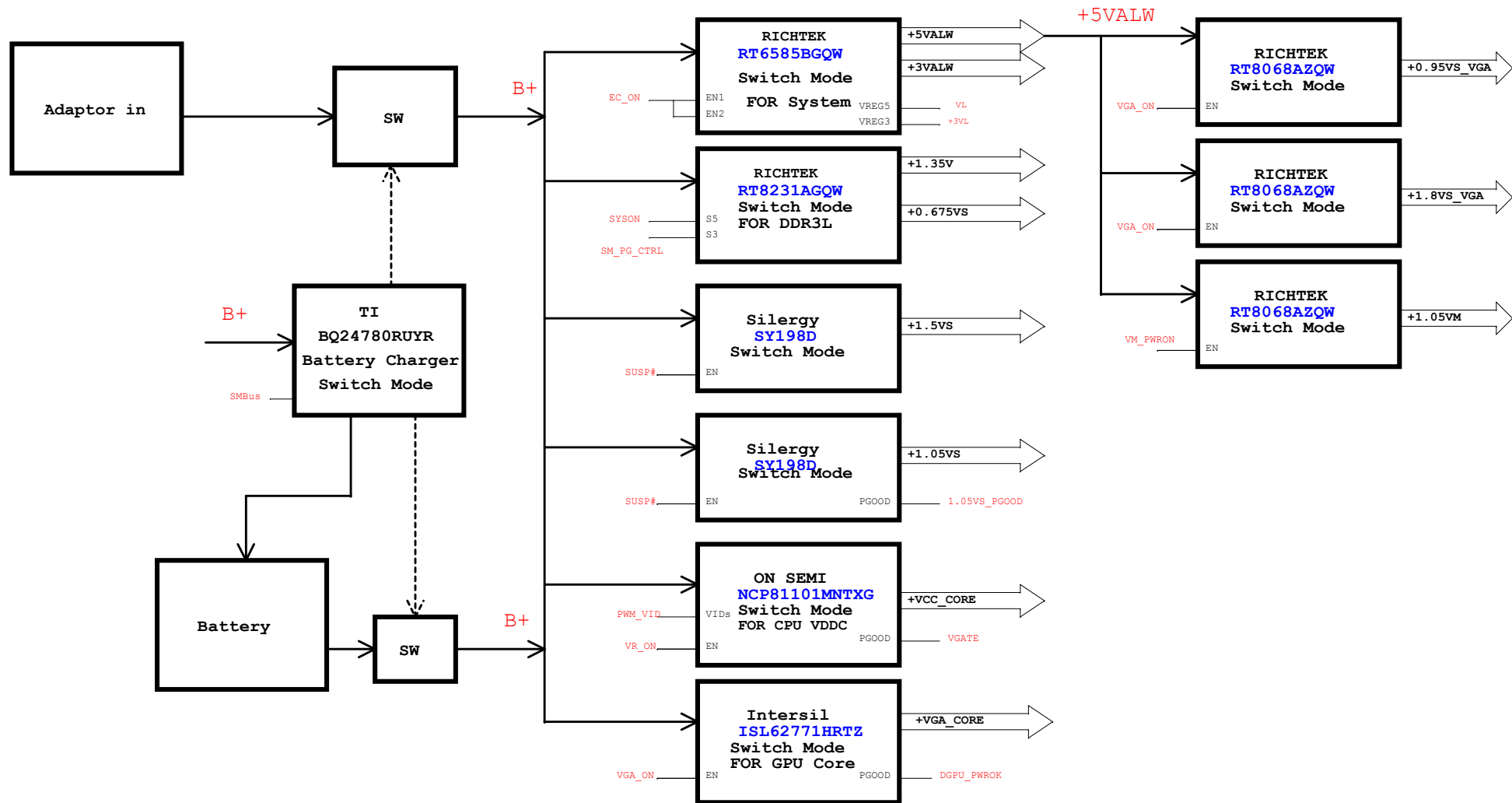
**+1.05VMP**  
**TDC: 1A**  
**Fsw: 1MHz**


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				<b>AITE1 NM-A221</b>	1.0
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# POWER PIR (Product Improve Record)

AIIE1 NM-A151 SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE




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# HW PIR (Product Improve Record)

AIVE1 NM-XXXX SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/10/15

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# Gordon SDV LOGIC SCHEMATICS

NMA-221  
VER 0.1  
Nov/13/2013

1.COVER PAGE  
2.BLOCK DIAGRAM  
3.NOTE LIST  
4.VGA NOTE  
5.BDW\_DDI/EDP/XDP  
6.BDW\_DDR3L INT  
7.BDW\_RTC/HDA/SATA/PCIe/JTAG  
8.BDW\_CLOCK/PM  
9.BDW\_LPC/SPI/SM BUS  
10.BDW\_SYS PM  
11.BDW\_eDP SBAND/DDPx  
12.BDW\_GPIO/SIO  
13.BDW\_PCIE/USB BUS  
14.BDW (Power)  
15.BDW (Power2)  
16.BDW (VSS)  
17.BDW (OTHER)  
18.DDR3L DIMM1  
19.DDR3L DIMM2  
20.Opal & Jet PCIE  
21.Opal & Jet GPIO  
22.Opal & Jet Core Power  
23.Opal & Jet DP Power/GND  
24.Opal & Jet MEM Interface  
25.Opal & Jet DDR3 VRAM U  
26.Opal & Jet DDR3 VRAM L  
27.Opal 22 TO 24 VRAM U2  
28.Opal 23 TO 25 VRAM L2  
29.Opal & Jet swich power  
30.BLANK  
31.BLANK  
32.CARDREADER IC/CONN.  
33.DP RP --> BLANK  
34.DOCKING/ DCIN CONN  
35.CX20751

36.HP/MIC JACK/Speaker  
37.SATA HDD/ODD CONN.  
38.eDP/CMOS CONN.  
39.USB30 RP --> BLANK  
40.USB3 PORT1-BACK  
41.USB3 PORT2-FRONT(AOU)  
42.MUX IC  
43.DP TO VGA  
44.VGA CONN.  
45.HDMI RP --> BLANK  
46.HDMI CONN.  
47.GBE LAN PHY  
48.RJ45 CONN.  
49.CP/TPOINTCONN.  
50.PBTN/LID/FP/FAN CONN.  
51.KB/RTC/TOUCH PAN CONN.  
52.WWAN/WLAN NGFF CONN.  
53.SUB CONN. --> BLANK  
54.SUB-AUDIO JACK CONN.  
55.THERMAL SENSOR  
56.G SENSOR/TPM  
57.BLANK  
58.BLANK  
59.BLANK  
60.BLANK  
61.DC V TO VS/ V-PCH/VM  
62.EC\_IT8586E/FX  
63.PLM/SCREW HOLE  
64.BLANK  
65.DCIN / Vin Detector  
66.BATTERY CONN/OTP  
67.CHARGER(BQ24780)  
68.3V/5VALW(RT6585B)  
69.+1.35V/+0.675V(RT8231A)  
70.+1.05VS(SYX198DQNC)

71.+1.5VS(SYX198DQNC)  
72.+1.8VS\_VGA(RT8068A)  
73.+VCC\_CORE(NCP81101MNTXG)  
74.+VCC\_CORE2  
75.PROCESSOR DECOUPLING  
76.+VGA\_CORE(ISL62771)  
77.+0.95VS\_VGA(RT8068A)  
78.+1.05VM(RT8068A)  
79.PWR-PIR  
80.HW PIR

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				Date:	Thursday, November 06, 2014	Sheet 01 of 01