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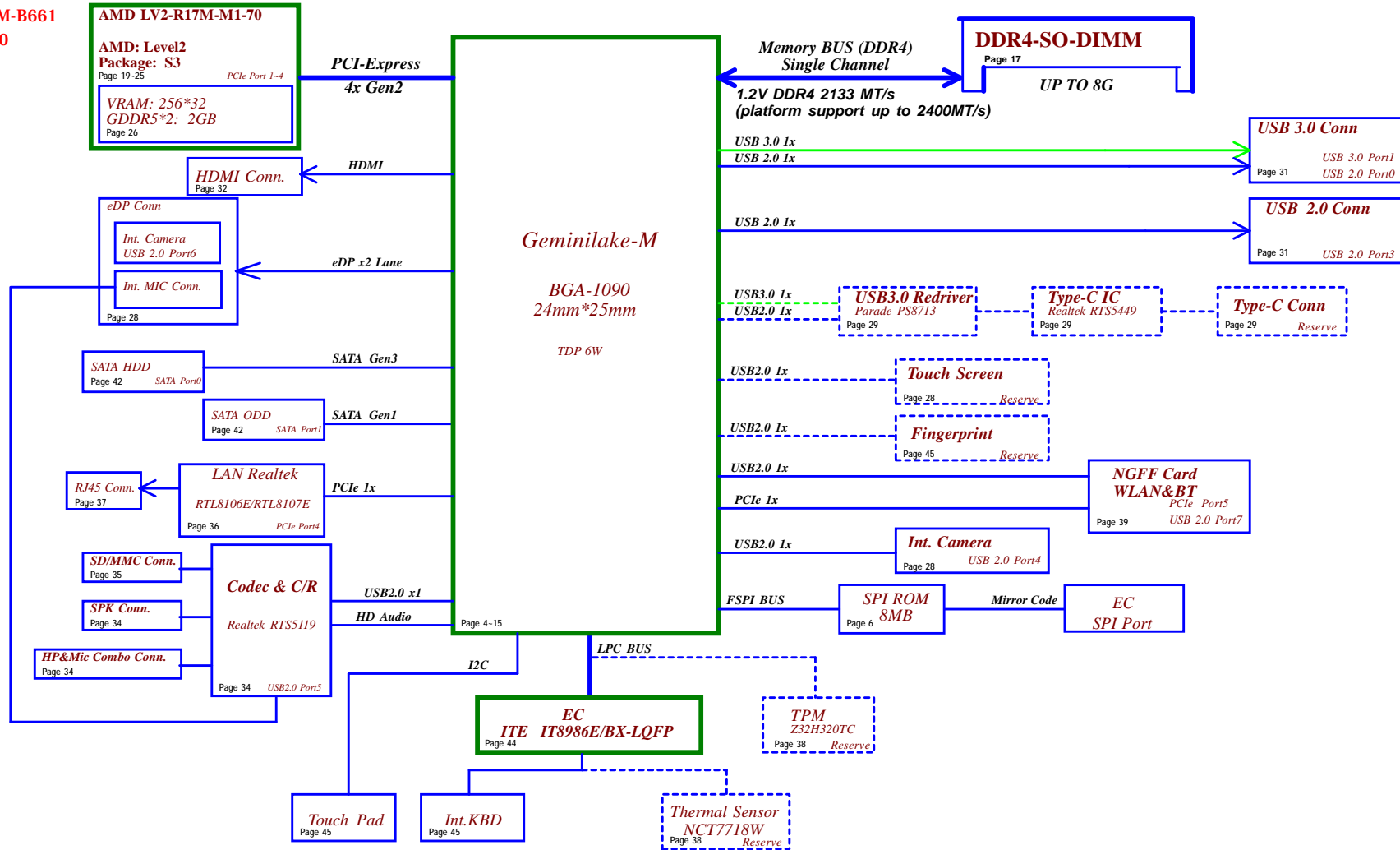
330-IGM M/B EG431/EG532 Schematics Document Intel Geminilake M-Processor with DDR4 + AMD LV2-R17M-M1-70 GPU

2018-03-02

REV:1.0

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2013/08/08	Deciphered Date	2014/01/21	Cover Page			
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LCFC confidential
File Name : TURING 4D&5D
Board Number : NM-B661
PN : DA600013W00



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Issued Date	2013/08/08	Deciphered Date	2014/01/21	Block Diagram	
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Voltage Rails (0--> Means ON , X--> Means OFF)

Power Plane / State	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.2V	+5VS +3VS +1.8VS +1.05VS +0.6VS +CPU_CORE +VNN
S0	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0IX(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB3.0
	1	Type C(RSVD)
USB 2.0	0	Type C (USB 2.0) (RSVD)
	1	USB3.0 (2.0)
	2	Touch Screen(RSVD)
	3	USB2.0
	4	Finger Print(RSVD)
	5	CARD READER
	6	CAMERA
7	BT	

DDI PORT LIST

Port	Device
DDI0	HDMI
DDI1	NC
eDP	eDP

PCIE PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0			
1	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
2			
3			
4	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
EMC_14@	EMC 14" part
EMC_USB@	EMC USB TVS part
1284_EMC@	1284 LAN Transformer EMC part
CD@	Cost Down part
RF@	For RF part
RF_NS@	For RF un-stuff part
RF_PXNS@	For RF GPU un-stuff part
14@	For 14" part
15@	For 15" part
8106E@	8106E LAN SKU part@
8107E@	8107E LAN SKU part@
1284@	1284 LAN Transformer part
8400M@	8400M LAN Transformer part
PX@	Discrete CPU SKU part
TOPAZ@	TOPAZ dGPU SKU part
EXO@	R16M-M1-30 dGPU SKU part
UMA@	UMA SKU ID part
TMSEN@	Thermal Sensor part
TMSEN_PX@	dGPU Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
NOVOTON@	NOVOTON TPM part
NATIONZ@	NATIONZ TPM part
TS@	Touch Screen part
FP@	Finger Print part
KBL@	KB Backlight part
UART@	UART debug part
RTCRST@	Clear RTCRST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N4100@	GLK N4100 CPU part
N4000@	GLK N4000 CPU part
N5000@	GLK N5000 CPU part
M8GX2@	Micron 8GbX2 VRAM X76 SKU
S8GX2@	Samsung 8GbX2 VRAM X76 SKU
H8GX2@	Hynix 8GbX2 VRAM X76 SKU
M8G@	Micron 8GbX2 VRAM
S8G@	Samsung 8GbX2 VRAM
H8G@	Hynix 8GbX2 VRAM
PCB@	MB PCB part
ODD@	ODD PCB part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

EC SM Bus0 address		EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery	0x16	Thermal Sensor	0x98(reserve)	DDR SO-DIMM	0xA0
		Charger	0x12			Wlan	Rsvd

I2C4/I2C7 Bus address (Touch Pad)




Device	Address
Slave	0x15
Descriptor	0x0001

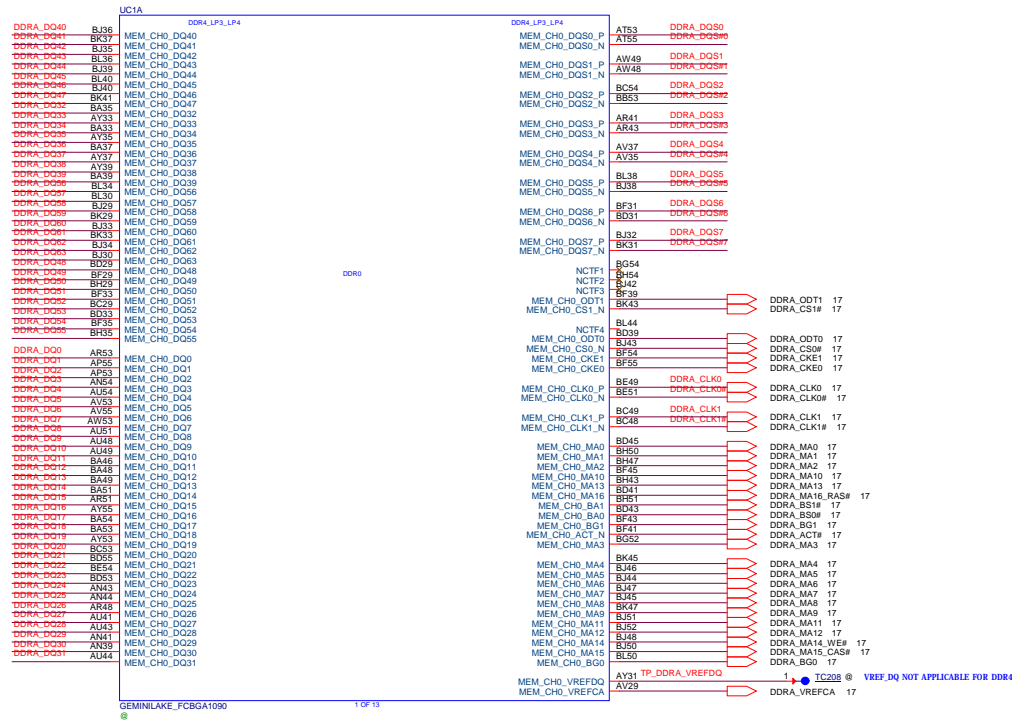
RCOMP RESISTOR REQUIREMENT

INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
Memory	MEM_CH0_RCOMP	RC1	110 +/-1%
	MEM_CH1_RCOMP	RC2	110 +/-1%
USB2	USB2_RCOMP	RC64	113 +/-1%
USB3/PCIe/SATA	PCIe2_USB3_SATA3_RCOMP_P/N	RC63	100 +/-1%
PCIe Refclk	PCIe_REF_CLK_RCOMP	RC62	56 +/-1%
DP/eDP*/HDMI*	EDP_RCOMP_P/N	RC79	100 +/-1%
MDSI	MDSI_RCOMP	RC78	150 +/-1%
CNVi	CNV_WT_RCOMP	RC48	150 +/-1%
SMBUS/GPIO/EMMC for all 1.8V only and 1.8V mode operation of 1.8/3.3V CFIO interfaces	EMMC_RCOMP	RC20	200 +/-1%

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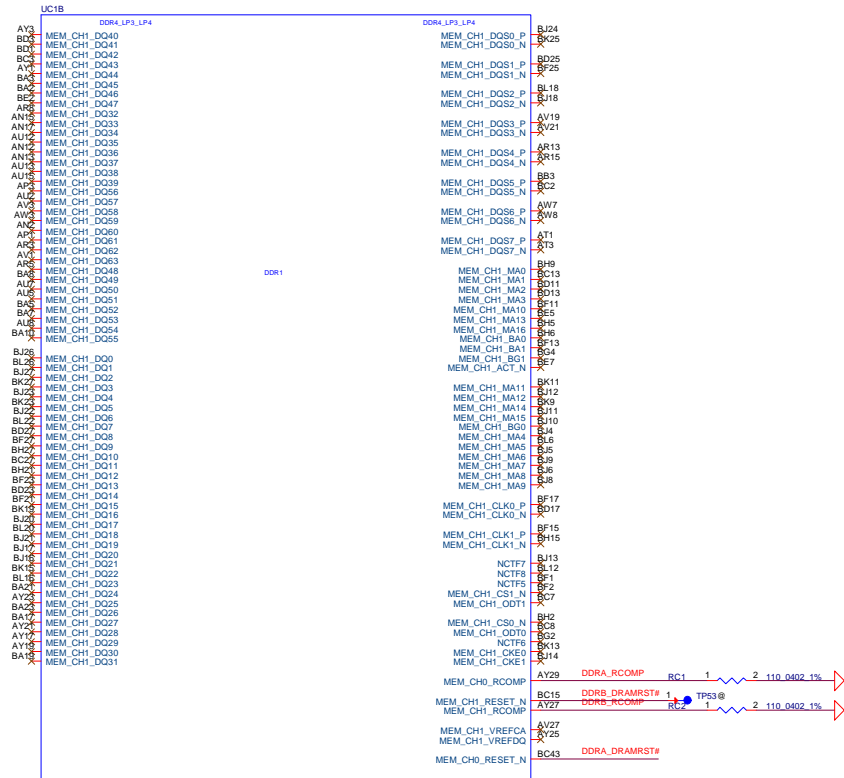
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-  DDRA_DQS[7:0] 17
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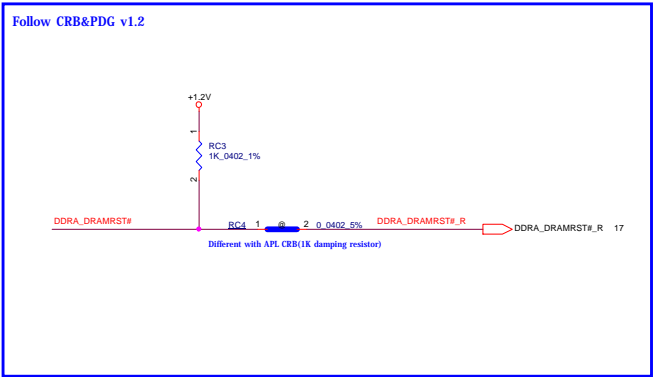
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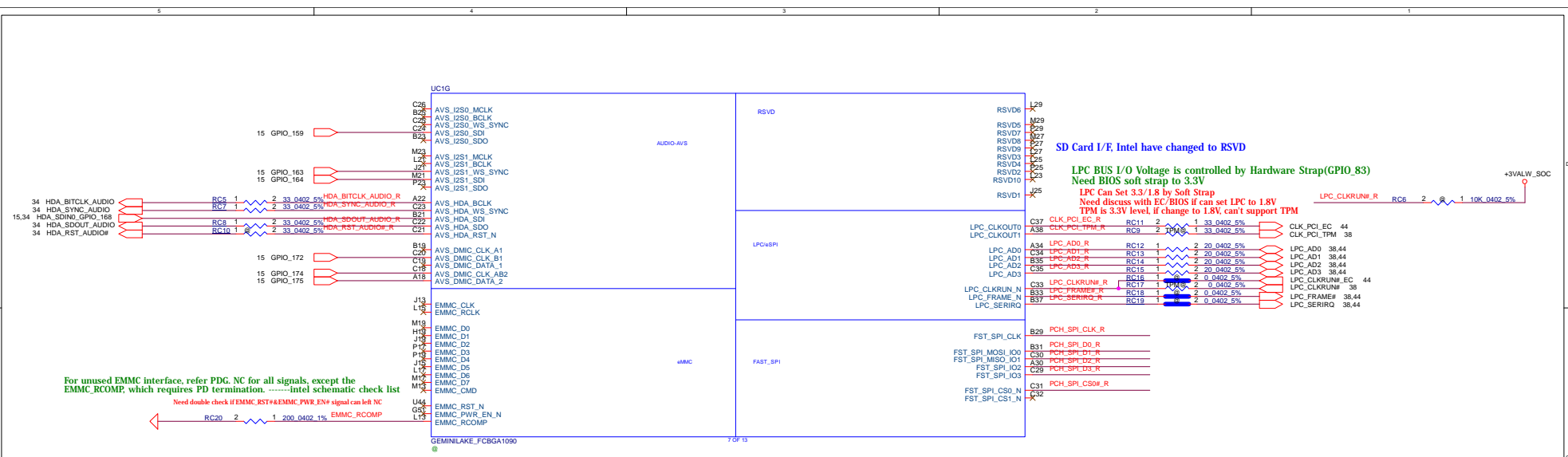
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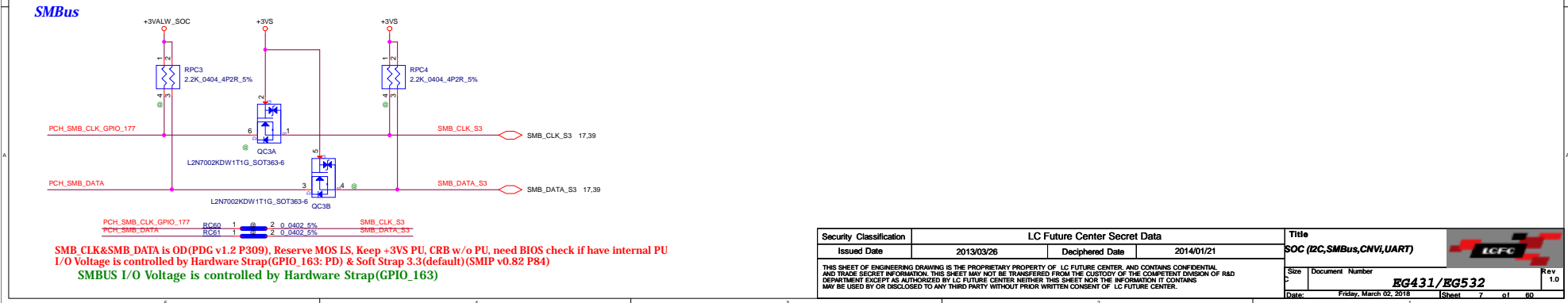
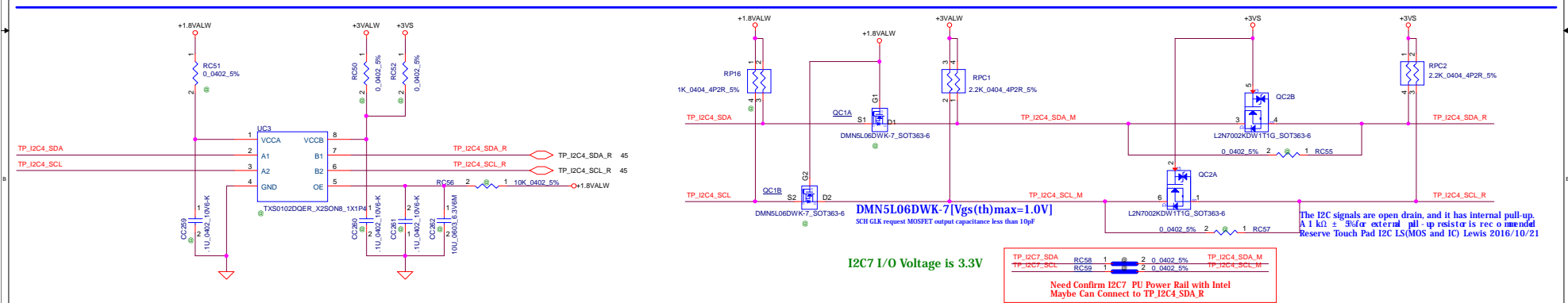
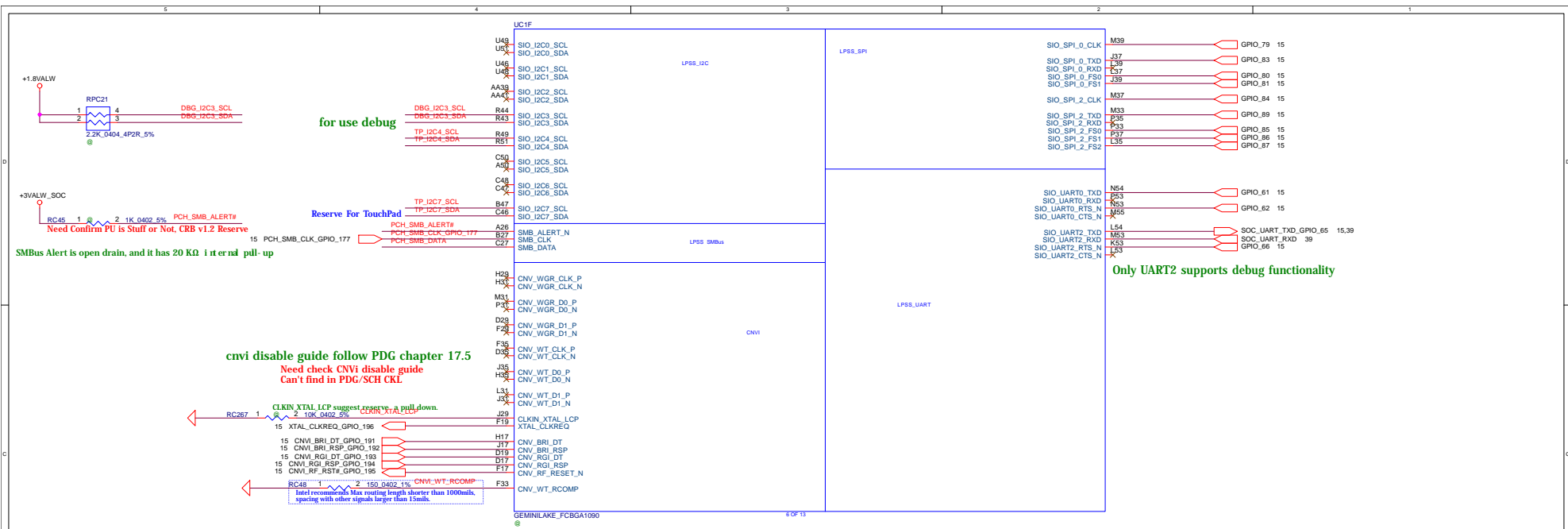
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SOC (DDR3L CHB)		Document Number	EG431/EG532
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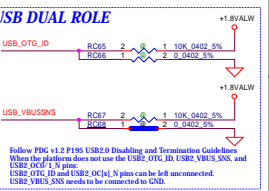
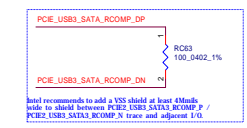
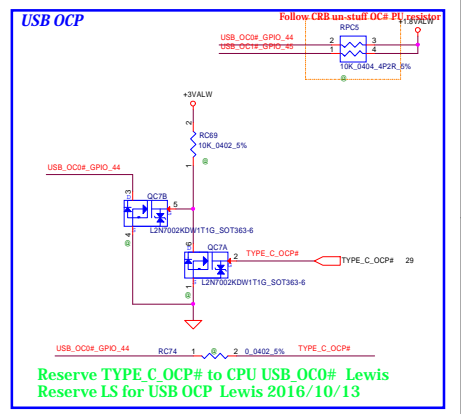
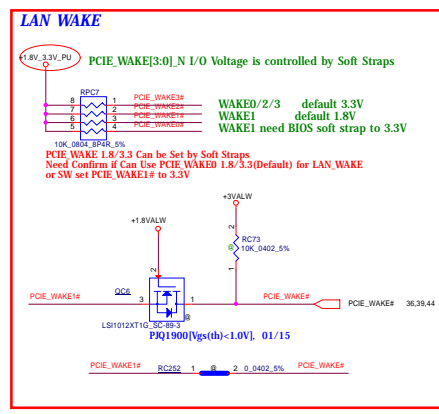
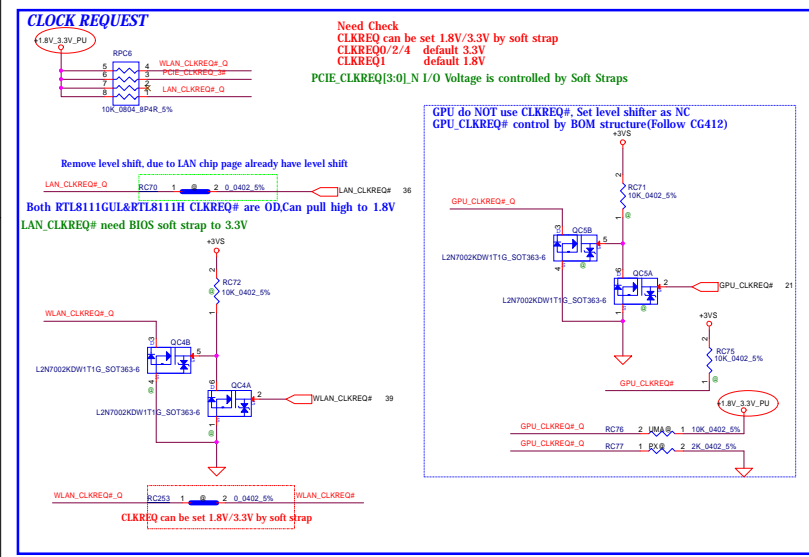
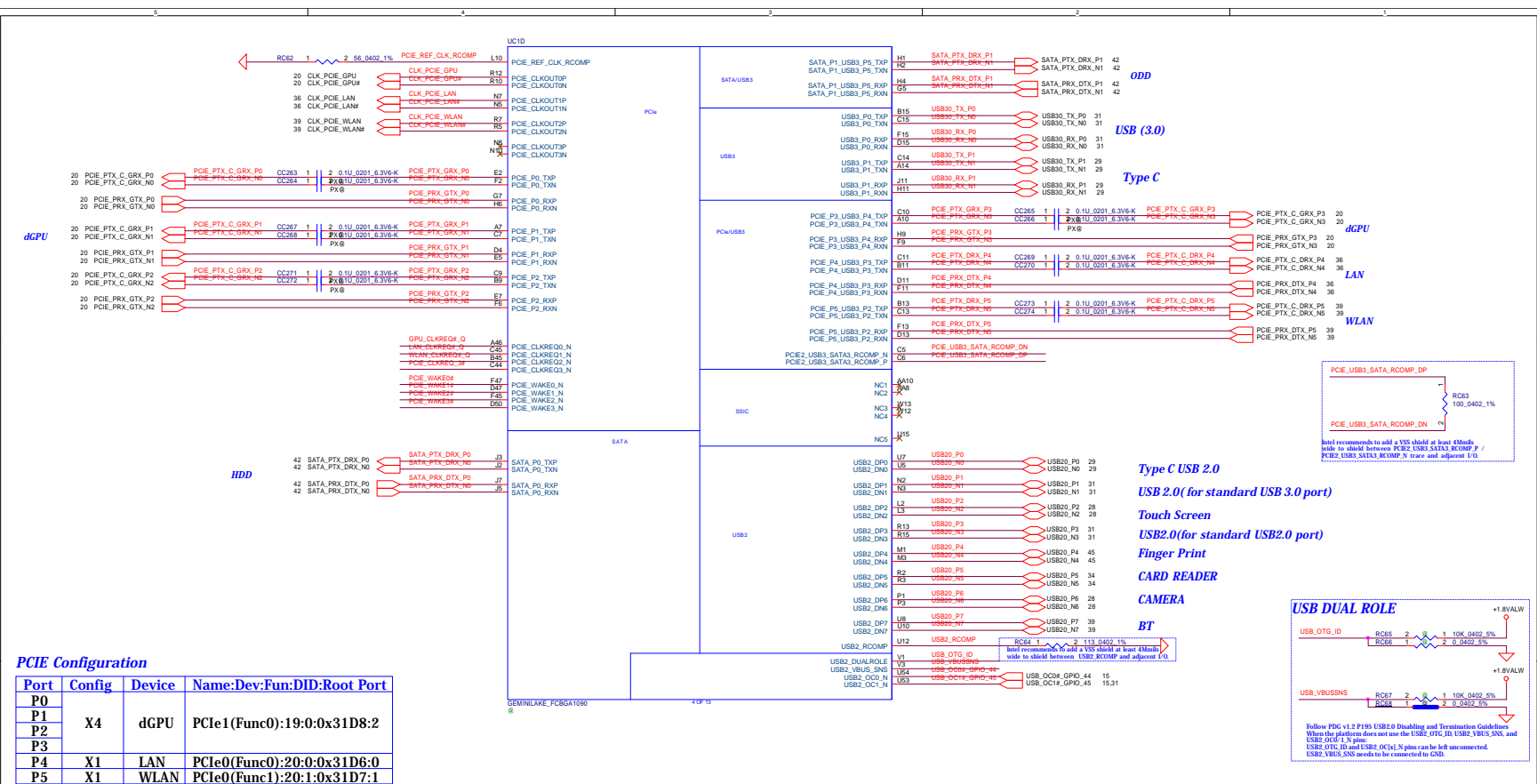


SPI ROM





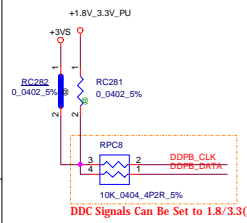
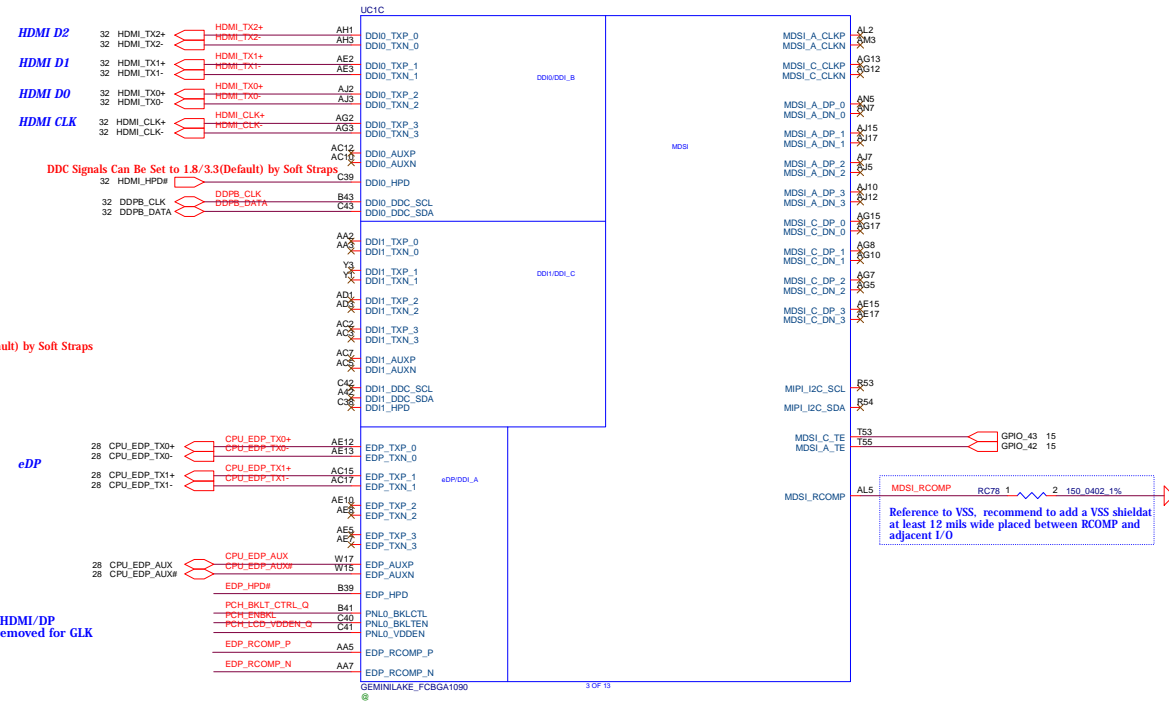
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Issued Date	2013/03/26	Deciphered Date	2014/01/21	SOC (I2C,SMBus,CNVi,UART)	
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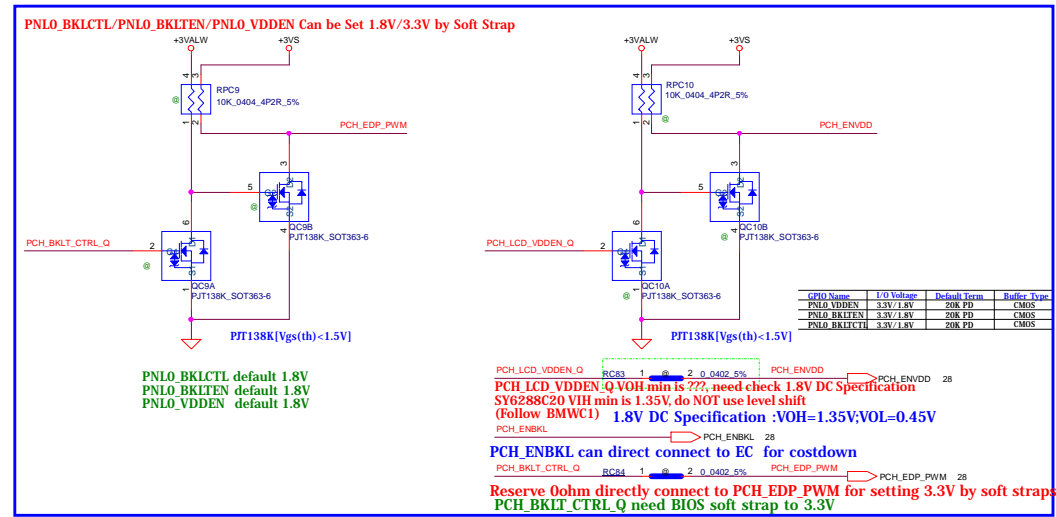
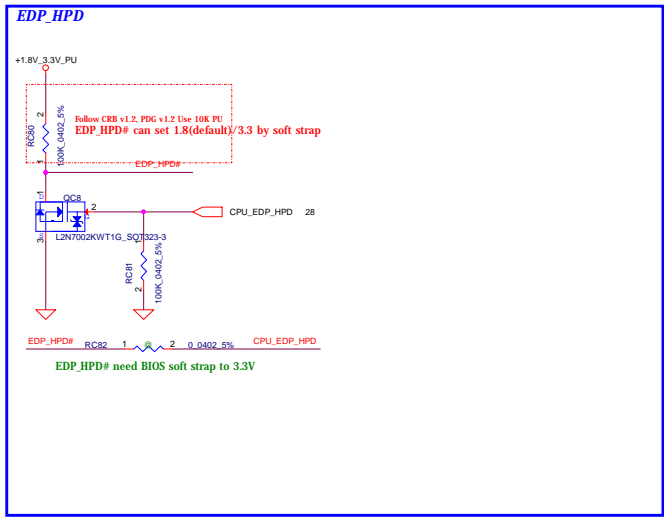
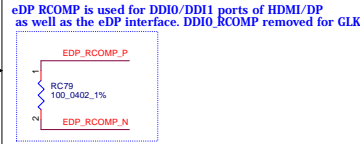
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Issue Date	2013/03/26	Deciphered Date	2014/01/21	SOC (PCIe&GPIO&SPI)	
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DDI PORT LIST

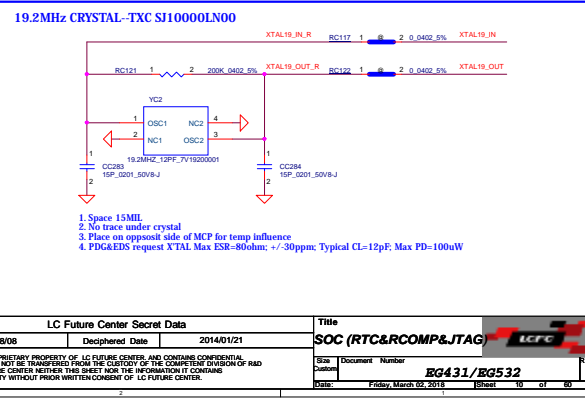
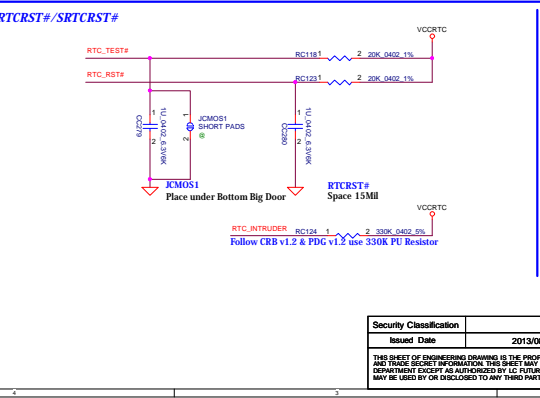
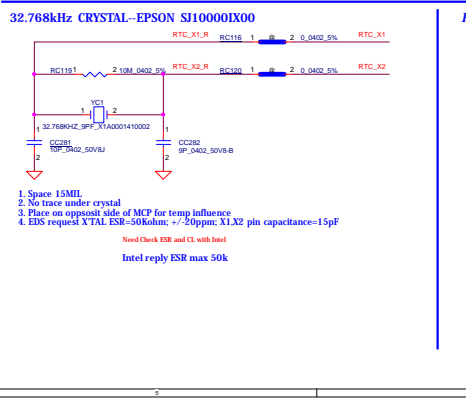
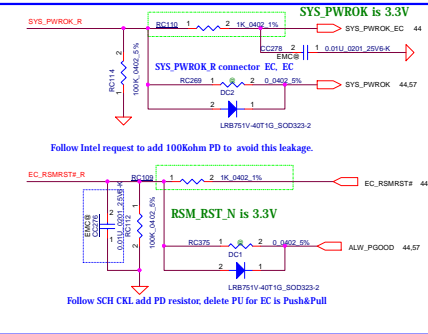
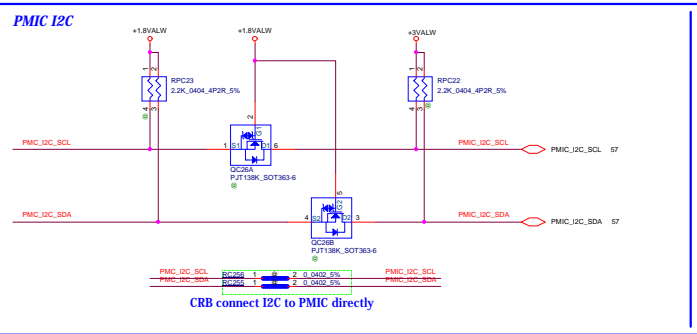
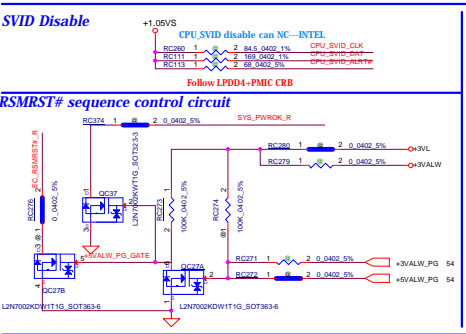
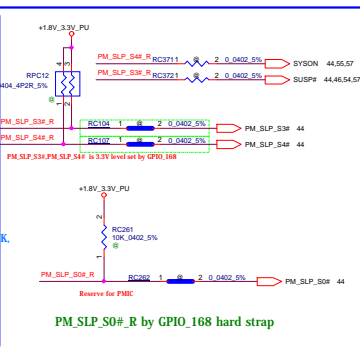
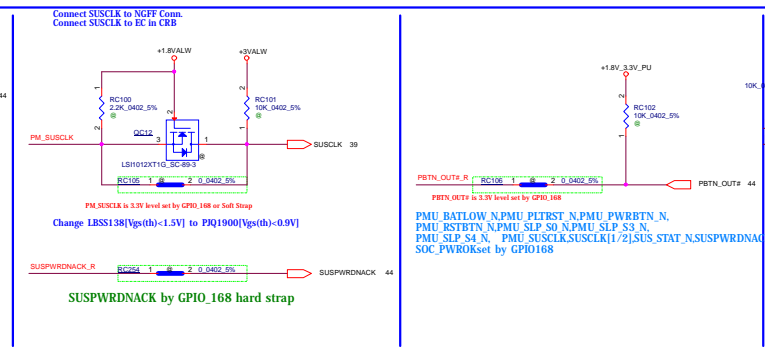
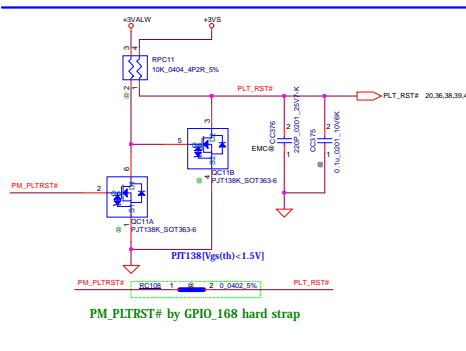
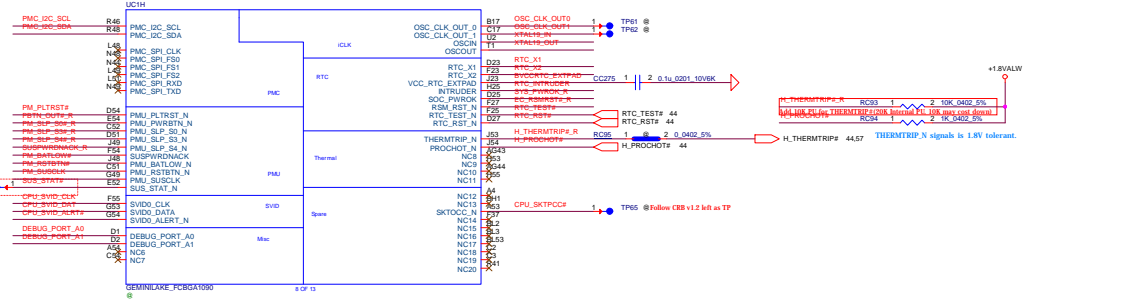
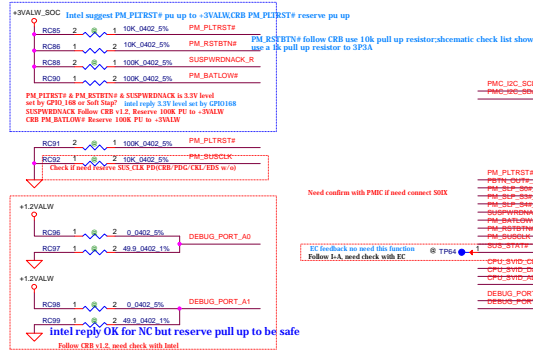
Port	Device	HPD Net	HPD Pin
DDIO	HDMI	HDMI_HPD#	C39
DDI1	N/A	N/A	C38
EDP	eDP	EDP_HPD#	B39



Reference to VSS, recommend to add a VSS shield at at least 12 mils wide placed between RCOMP and adjacent I/O



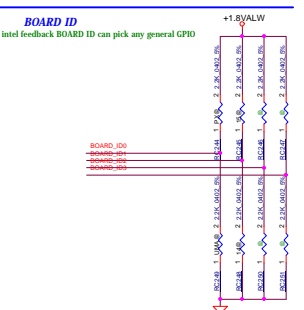
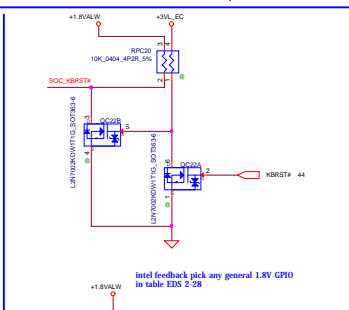
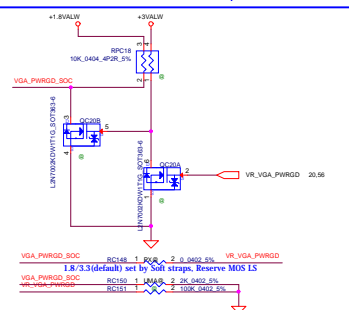
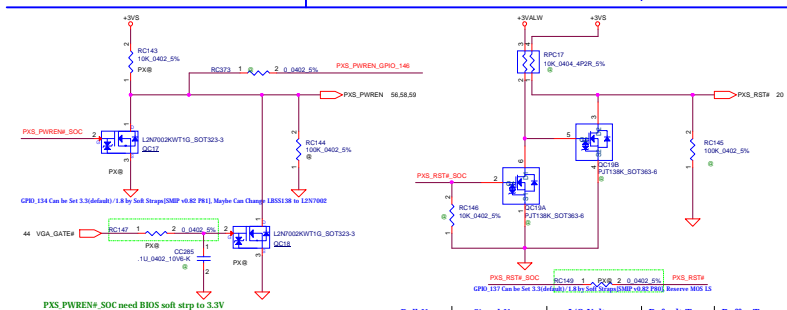
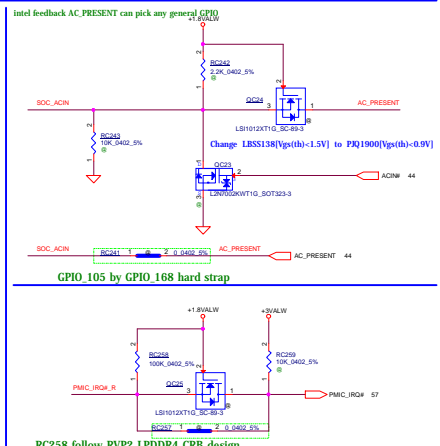
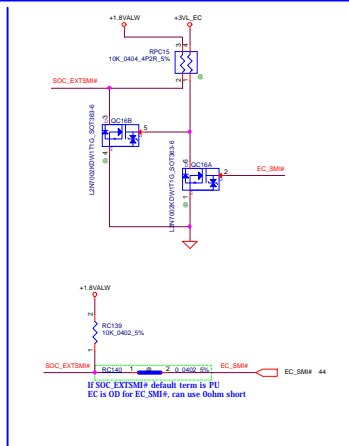
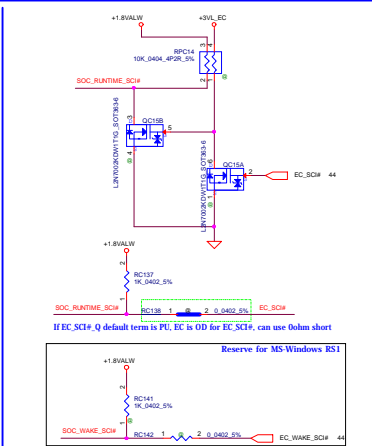
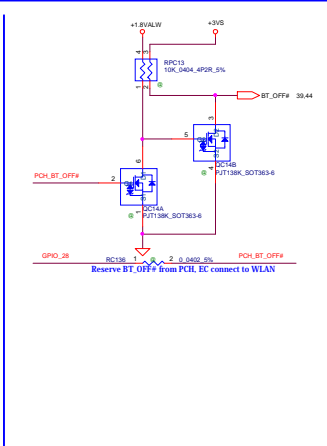
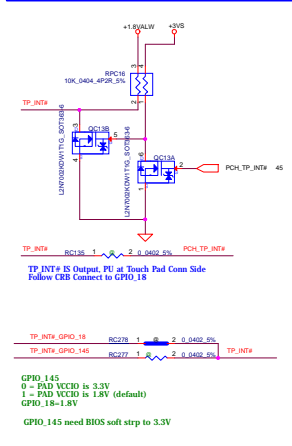
GPIO Name	I/O Voltage	Default Term	Buffer Type
PNL0_VDDEN	3.3V/1.8V	20R_PD	CMOS
PNL0_BKLTEN	3.3V/1.8V	20R_PD	CMOS
PNL0_BKLTCTH	3.3V/1.8V	20R_PD	CMOS



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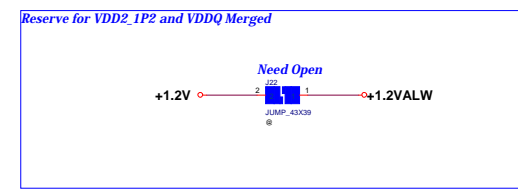
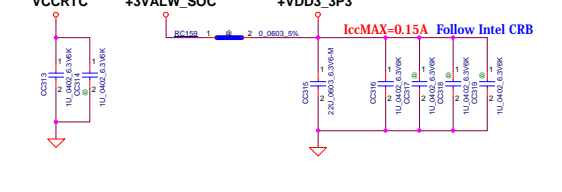
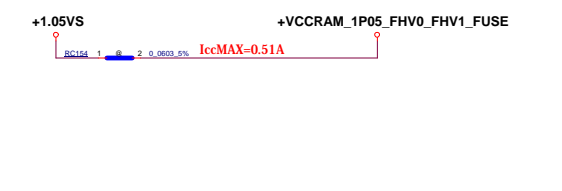
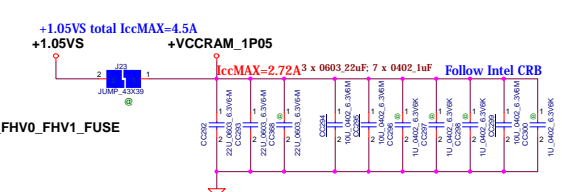
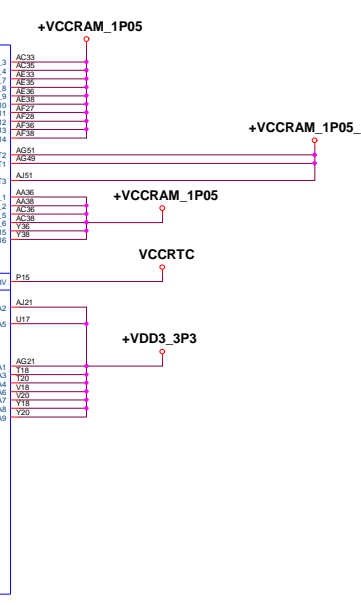
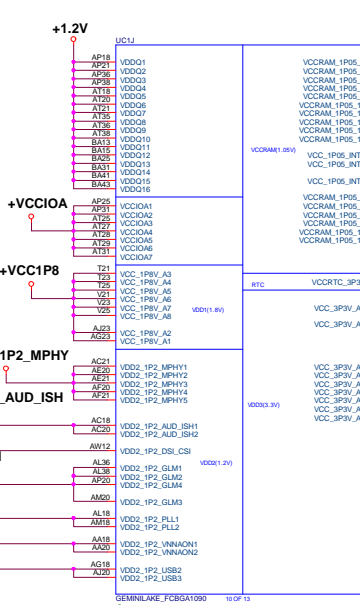
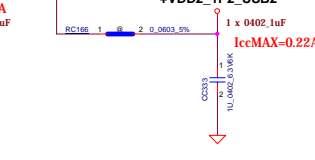
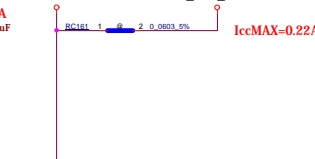
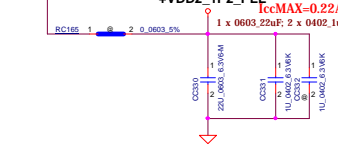
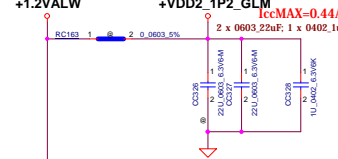
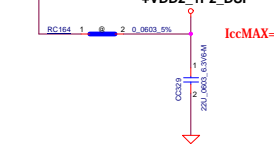
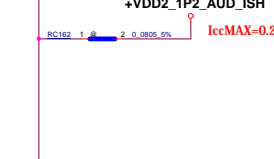
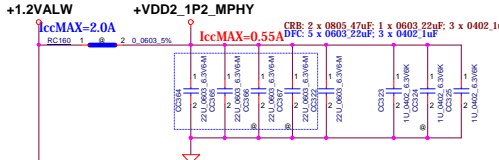
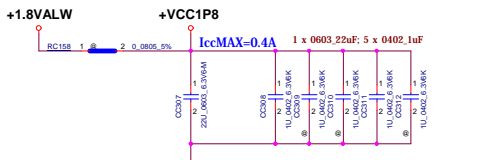
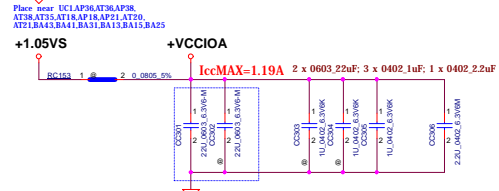
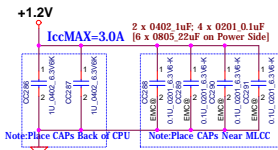


GPIO	Signal	Notes
GPIO_8	DBG_PT_CLK0	
GPIO_9	DBG_PT_CLK1	
GPIO_10	DBG_PT_CLK2	
GPIO_11	DBG_PT_CLK3	
GPIO_12	DBG_PT_CLK4	
GPIO_13	DBG_PT_CLK5	
GPIO_14	DBG_PT_CLK6	
GPIO_15	DBG_PT_CLK7	
GPIO_16	DBG_PT_CLK8	
GPIO_17	DBG_PT_CLK9	
GPIO_18	DBG_PT_CLK10	
GPIO_19	DBG_PT_CLK11	
GPIO_20	DBG_PT_CLK12	
GPIO_21	DBG_PT_CLK13	
GPIO_22	DBG_PT_CLK14	
GPIO_23	DBG_PT_CLK15	
GPIO_24	DBG_PT_CLK16	
GPIO_25	DBG_PT_CLK17	
GPIO_26	DBG_PT_CLK18	
GPIO_27	DBG_PT_CLK19	
GPIO_28	DBG_PT_CLK20	
GPIO_29	DBG_PT_CLK21	
GPIO_30	DBG_PT_CLK22	
GPIO_31	DBG_PT_CLK23	
GPIO_32	DBG_PT_CLK24	
GPIO_33	DBG_PT_CLK25	
GPIO_34	DBG_PT_CLK26	
GPIO_35	DBG_PT_CLK27	
GPIO_36	DBG_PT_CLK28	
GPIO_37	DBG_PT_CLK29	
GPIO_38	DBG_PT_CLK30	
GPIO_39	DBG_PT_CLK31	
GPIO_40	DBG_PT_CLK32	
GPIO_41	DBG_PT_CLK33	
GPIO_105	SOC_AGIN	GPIO 105 use set 1.8V (3.3V default) by soft strap
GPIO_106	SOC_PWREN_SOC	
GPIO_107	SOC_RST#_SOC	
GPIO_108	SOC_EXTM#	
GPIO_109	SOC_WAKE_SOC	
GPIO_110	SOC_RUNTIME_SOC	
GPIO_111	SOC_ERR#	
GPIO_112	SOC_ERR#	
GPIO_113	SOC_ERR#	
GPIO_114	SOC_ERR#	
GPIO_115	SOC_ERR#	
GPIO_116	SOC_ERR#	
GPIO_117	SOC_ERR#	
GPIO_118	SOC_ERR#	
GPIO_119	SOC_ERR#	
GPIO_120	SOC_ERR#	
GPIO_121	SOC_ERR#	
GPIO_122	SOC_ERR#	
GPIO_123	SOC_ERR#	
GPIO_124	SOC_ERR#	
GPIO_125	SOC_ERR#	
GPIO_126	SOC_ERR#	
GPIO_127	SOC_ERR#	
GPIO_128	SOC_ERR#	
GPIO_129	SOC_ERR#	
GPIO_130	SOC_ERR#	
GPIO_131	SOC_ERR#	
GPIO_132	SOC_ERR#	
GPIO_133	SOC_ERR#	
GPIO_134	SOC_ERR#	
GPIO_135	SOC_ERR#	
GPIO_136	SOC_ERR#	
GPIO_137	SOC_ERR#	
GPIO_138	SOC_ERR#	
GPIO_139	SOC_ERR#	
GPIO_140	SOC_ERR#	
GPIO_141	SOC_ERR#	
GPIO_142	SOC_ERR#	
GPIO_143	SOC_ERR#	
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GPIO_157	SOC_ERR#	
GPIO_158	SOC_ERR#	
GPIO_159	SOC_ERR#	
GPIO_160	SOC_ERR#	
GPIO_161	SOC_ERR#	
GPIO_162	SOC_ERR#	
GPIO_163	SOC_ERR#	
GPIO_164	SOC_ERR#	
GPIO_165	SOC_ERR#	
GPIO_166	SOC_ERR#	
GPIO_167	SOC_ERR#	
GPIO_168	SOC_ERR#	
GPIO_169	SOC_ERR#	
GPIO_170	SOC_ERR#	
GPIO_171	SOC_ERR#	
GPIO_172	SOC_ERR#	
GPIO_173	SOC_ERR#	
GPIO_174	SOC_ERR#	
GPIO_175	SOC_ERR#	
GPIO_176	SOC_ERR#	
GPIO_177	SOC_ERR#	
GPIO_178	SOC_ERR#	
GPIO_179	SOC_ERR#	
GPIO_180	SOC_ERR#	
GPIO_181	SOC_ERR#	
GPIO_182	SOC_ERR#	
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GPIO_184	SOC_ERR#	
GPIO_185	SOC_ERR#	
GPIO_186	SOC_ERR#	
GPIO_187	SOC_ERR#	
GPIO_188	SOC_ERR#	
GPIO_189	SOC_ERR#	
GPIO_190	SOC_ERR#	
GPIO_191	SOC_ERR#	
GPIO_192	SOC_ERR#	
GPIO_193	SOC_ERR#	
GPIO_194	SOC_ERR#	
GPIO_195	SOC_ERR#	
GPIO_196	SOC_ERR#	
GPIO_197	SOC_ERR#	
GPIO_198	SOC_ERR#	
GPIO_199	SOC_ERR#	
GPIO_200	SOC_ERR#	

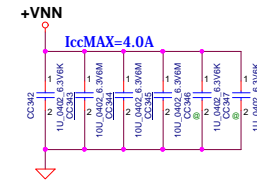
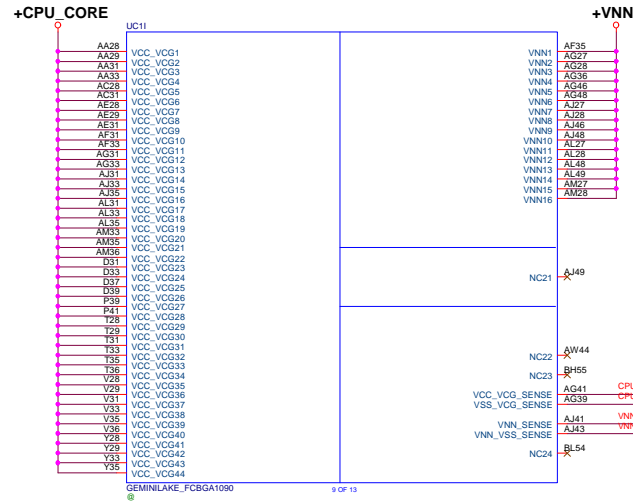
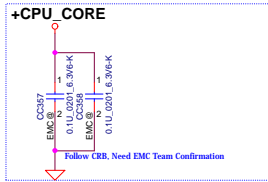
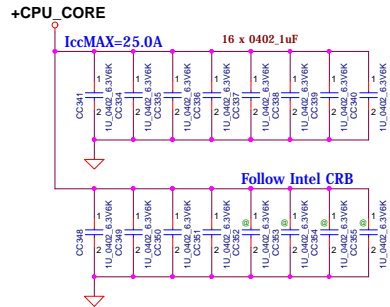


Ball Name	Signal Name	I/O Voltage	Default Term	Buffer Type
GPIO_134	PXS_PWREN#_SOC	1.8/3.3(Default)	20K PD	HSIV
GPIO_137	PXS_RST#_SOC	1.8/3.3(Default)	20K PD	HSIV

ID0	ID1	ID2	ID3	Description
0				UMA SKU
1	RSVD	RSVD		GPU SKU
0				14" Panel
1				15" Panel



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UC1K

A3	VSS_6	AF44	VSS_53
A6	VSS_13	AF45	VSS_54
A12	VSS_1	AF47	VSS_56
A16	VSS_2	AF48	VSS_57
A20	VSS_3	AF49	VSS_58
A24	VSS_4	AF50	VSS_59
A28	VSS_5	AF51	VSS_60
A32	VSS_7	AF52	VSS_61
A36	VSS_8	AF53	VSS_62
A40	VSS_9	AF54	VSS_63
A44	VSS_10	AF55	VSS_64
A48	VSS_11	AF56	VSS_65
A51	VSS_12	AF57	VSS_66
AA12	VSS_14	AF58	VSS_67
AA13	VSS_15	AF59	VSS_68
AA15	VSS_16	AF60	VSS_69
AA17	VSS_17	AF61	VSS_70
AA21	VSS_18	AF62	VSS_71
AA23	VSS_19	AF63	VSS_72
AA25	VSS_20	AF64	VSS_73
AA27	VSS_21	AF65	VSS_74
AA35	VSS_22	AF66	VSS_75
AA43	VSS_23	AF67	VSS_76
AA48	VSS_24	AF68	VSS_77
AB1	VSS_25	AF69	VSS_78
AB3	VSS_26	AF70	VSS_79
AB5	VSS_27	AF71	VSS_80
AC5	VSS_33	AF72	VSS_81
AC13	VSS_28	AF73	VSS_82
AC23	VSS_29	AF74	VSS_83
AC25	VSS_30	AF75	VSS_84
AC27	VSS_31	AF76	VSS_85
AC29	VSS_32	AF77	VSS_86
AE18	VSS_34	AF78	VSS_87
AE23	VSS_35	AF79	VSS_88
AE25	VSS_36	AF80	VSS_89
AE27	VSS_37	AF81	VSS_90
AE43	VSS_38	AF82	VSS_91
AE46	VSS_39	AF83	VSS_92
AF1	VSS_40	AF84	VSS_93
AF3	VSS_41	AF85	VSS_94
AF4	VSS_42	AF86	VSS_95
AF6	VSS_43	AF87	VSS_96
AF8	VSS_44	AF88	VSS_97
AF9	VSS_45	AF89	VSS_98
AF11	VSS_46	AF90	VSS_99
AF12	VSS_47	AF91	VSS_100
AF14	VSS_48	AF92	VSS_101
AF16	VSS_49	AF93	VSS_102
AF18	VSS_50	AF94	VSS_103
AF23	VSS_51	AF95	VSS_104
AF25	VSS_52	AF96	VSS_105
AF29		AF97	
AF40		AF98	
AF42		AF99	
VSS_106		AF100	

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UC1L


AN48	VSS_111	BC11	VSS_165
AN49	VSS_112	BC17	VSS_166
AN51	VSS_113	BC19	VSS_168
AN53	VSS_114	BC21	VSS_169
AP23	VSS_115	BC23	VSS_170
AP27	VSS_116	BC25	VSS_171
AP28	VSS_117	BC27	VSS_172
AP29	VSS_118	BC33	VSS_173
AP33	VSS_119	BC35	VSS_174
AP35	VSS_120	BC37	VSS_175
AR2	VSS_124	BC39	VSS_176
AR29	VSS_125	BC41	VSS_177
AR7	VSS_126	BC45	VSS_178
AR10	VSS_127	BC47	VSS_179
AR12	VSS_128	BD1	VSS_180
AR17	VSS_129	BD3	VSS_181
AR39	VSS_130	BD5	VSS_182
AR44	VSS_131	BD9	VSS_183
AJ18	VSS_132	BD15	VSS_184
AJ25	VSS_133	BD19	VSS_185
AJ29	VSS_134	BD21	VSS_186
AJ38	VSS_135	BD28	VSS_187
AJ39	VSS_136	BD35	VSS_188
AJ38	VSS_137	BD36	VSS_189
AJ38	VSS_138	BD37	VSS_190
AJ38	VSS_139	BD47	VSS_191
AJ38	VSS_140	BD5	VSS_192
AJ38	VSS_141	BE28	VSS_193
AJ38	VSS_142	BE3	VSS_194
AJ38	VSS_143	BE5	VSS_195
AJ38	VSS_144	BF19	VSS_196
AJ38	VSS_145	BF37	VSS_197
AJ38	VSS_146	BF47	VSS_198
AJ38	VSS_147	BG1	VSS_199
AJ38	VSS_148	BG6	VSS_200
AJ38	VSS_149	BG28	VSS_201
AJ38	VSS_150	BG50	VSS_202
AJ38	VSS_151	BG55	VSS_203
AJ38	VSS_152	BH11	VSS_204
AJ38	VSS_153	BH13	VSS_205
AJ38	VSS_154	BH17	VSS_206
AJ38	VSS_155	BH19	VSS_207
AJ38	VSS_156	BH25	VSS_208
AJ38	VSS_157	BH28	VSS_209
AJ38	VSS_158	BH33	VSS_210
AJ38	VSS_159	BH37	VSS_211
AJ38	VSS_160	BH39	VSS_212
AJ38	VSS_161	BH45	VSS_213
AJ38	VSS_162	BH45	VSS_214
AJ38	VSS_163	BH45	VSS_215
AJ38	VSS_164	BH45	VSS_216
AJ38	VSS_165	BH45	VSS_217
AJ38	VSS_166	BH45	VSS_218
AJ38	VSS_167	BH45	VSS_219
AJ38	VSS_168	BH45	VSS_220

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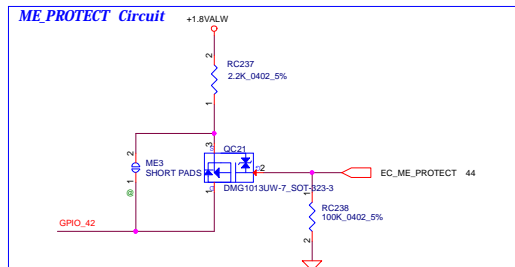
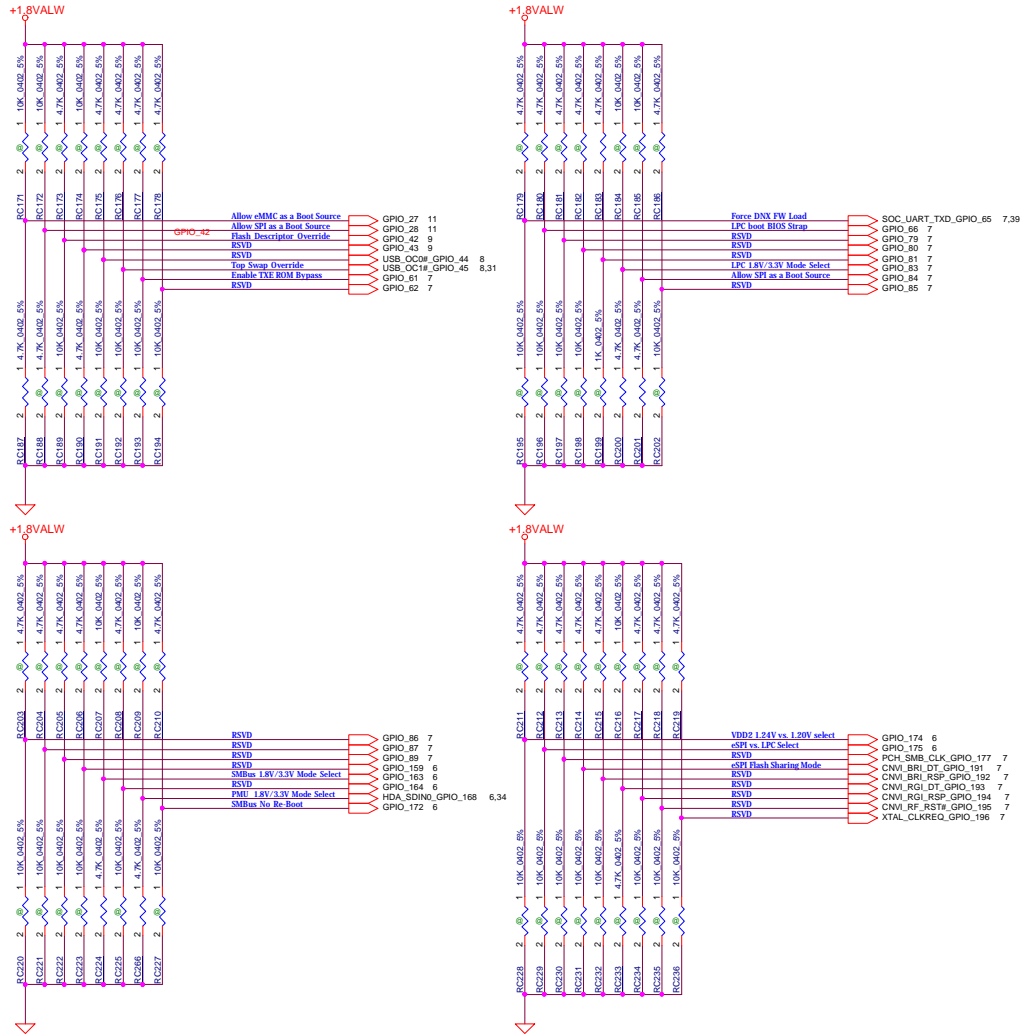
UC1M

AL23	VSS_221	J51	VSS_272
BK54	VSS_222	K3	VSS_273
BK1	VSS_223	K28	VSS_274
BK17	VSS_224	K28	VSS_275
BK21	VSS_225	L5	VSS_276
BK35	VSS_226	L7	VSS_277
BK39	VSS_227	L8	VSS_278
BL5	VSS_228	L19	VSS_279
BL8	VSS_229	L31	VSS_280
BL10	VSS_230	M15	VSS_281
BL14	VSS_231	M25	VSS_282
BL24	VSS_232	M28	VSS_283
BL28	VSS_233	M35	VSS_284
BL32	VSS_234	M41	VSS_285
BL42	VSS_235	N12	VSS_286
BL46	VSS_236	N28	VSS_287
BL48	VSS_237	N46	VSS_288
BL51	VSS_238	N51	VSS_289
C1	VSS_239	P21	VSS_290
C12	VSS_240	P55	VSS_291
C16	VSS_241	R8	VSS_292
C28	VSS_243	R28	VSS_293
C36	VSS_244	R28	VSS_294
D6	VSS_245	R38	VSS_295
D9	VSS_246	U13	VSS_296
D21	VSS_247	V27	VSS_297
D41	VSS_248	V35	VSS_298
D45	VSS_249	V55	VSS_299
D55	VSS_250	W2	VSS_300
E28	VSS_251	W3	VSS_301
E50	VSS_252	W5	VSS_302
E55	VSS_253	W7	VSS_303
F1	VSS_254	W8	VSS_304
F4	VSS_255	W10	VSS_305
F21	VSS_256	W38	VSS_306
F31	VSS_257	W41	VSS_307
G28	VSS_258	W43	VSS_308
G28	VSS_259	W43	VSS_309
H13	VSS_260	W46	VSS_310
H15	VSS_261	W48	VSS_311
H21	VSS_262	W49	VSS_312
H23	VSS_263	W51	VSS_313
H28	VSS_264	Y1	VSS_314
H33	VSS_265	Y23	VSS_315
H39	VSS_266	Y27	VSS_316
J8	VSS_267	Y31	VSS_317
J27	VSS_268	Y31	VSS_318
J33	VSS_269	Y31	VSS_319
J41	VSS_270	U3	VSS_320
J45	VSS_271	VSS_321	VSS_321

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Hardware STRAPS(Follow up CRB)



EC_ME_PROTECT	GPIO_42	TXE Flash Descriptor Override
Low	High	Override
High	Low	No Override (Normal Operation)

GPIO#	Purpose	Internal Termination	Schematics Setting	Pin Usage	Remark
GPIO_27	Allow eMMC as a Boot Source	20K PU	4.7K PD	1 = Enable(Default); 0 = Disable[V] If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_28	Allow SPI as a Boot Source	20K PU	Floating	1 = Enable(Default); 0 = Disable If platform is using eMMC as boot device, then provide a pull-down for this strap to disable SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P469)
GPIO_42	Flash Descriptor Override	20K PD	Floating	1 = Override; 0 = No Override(Normal Operation)[V] This strap enables the platform to override security features in the SPI	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_43	RSVD	20K PU	Floating	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_44	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_45	Top swap override	20K PD	Floating	1 = Enable; 0 = Disable(Default)[V] This strap enables platform to change where the core will look for BDS code for a SPI boot only	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_61	Enable TXE ROM Bypass	20K PD	Floating	1 = Enable Bypass; 0 = Disable Bypass(Default)[V] This strap tells TXE SIO to bypass Read-Only Memory (ROM) that it has on SoC	Follow CRB(v1.2 P58); EDS(v1.2 P39); PDG(v1.2 P380)
GPIO_62	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P39)
GPIO_65	Force DNX FW Load	20K PD	Floating	1 = Force; 0 = Do Not Force(Default)[V] This strap is a recovery strap for corrupted FW image. will force TXE33 to execute a DNX flow	Follow CRB(v1.2 P58); EDS(v1.2 P40); PDG(v1.2 P471)
GPIO_66	LPC boot BIOS strap	20K PD	Floating	1 = Boot From LPC; 0 = Do Not(Default)[V] The board should strap this low and do not use otherwise	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_79	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_80	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_81	RSVD	20K PU	4.7K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_83	LPC 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_84	Allow SPI as a boot source	20K PU	4.7K PD	1=disable 0=enable (default)[V]	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_85	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_86	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P58); EDS(v1.2 P40)
GPIO_87	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_89	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_159	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_163	SMBus 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_164	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_168	PMU 1.8V/3.3V mode select	20K PD	4.7K PD	1= buffers set to 1.8V mode 0= buffers set to 3.3V mode (default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_172	SMBus No Re-Boot	20K PD	Floating	1 = Enable; 0 = Disable (default)[V] Note: Platform should strap this LOW. Functionality is handled by the PMU.	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_174	VDD2 1.24V vs. 1.20V select	20K PD	Floating	1=VDD2 is 1.24V. 0=VDD2 is 1.20V (default) Need Check	Follow CRB(v1.2 P57); EDS(v1.2 P40)
GPIO_175	eSPI vs. LPC	20K PD	Floating	1=eSPI mode; 0=LPC mode (default) Note: The default for AD will be eSPI due to a bug on LPC	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_177	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_191	eSPI Flash Sharing Mode	20K PD	Floating	eSPI Flash Sharing Mode: 0=slave attached flash sharing (SAFS); 1=master attached flash sharing (MAFS, default)[V]	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_192	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_193	RSVD	20K PU	Floating	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_194	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_195	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)
GPIO_196	RSVD	20K PD	Floating	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation	Follow CRB(v1.2 P57); EDS(v1.2 P41)

Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date
		2014/01/21

Title	
SOC (STRAPS & OTHERS)	
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		Sheet	12
		Date	Friday, March 10, 2018 10:41:52 AM



Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

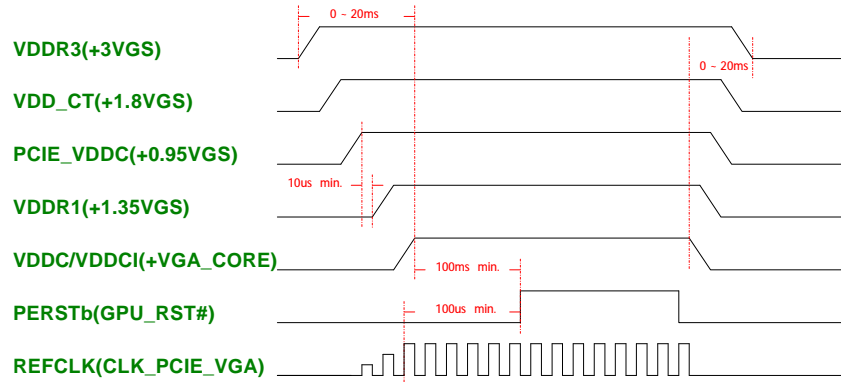
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as \leq 50 mV/ μ s)

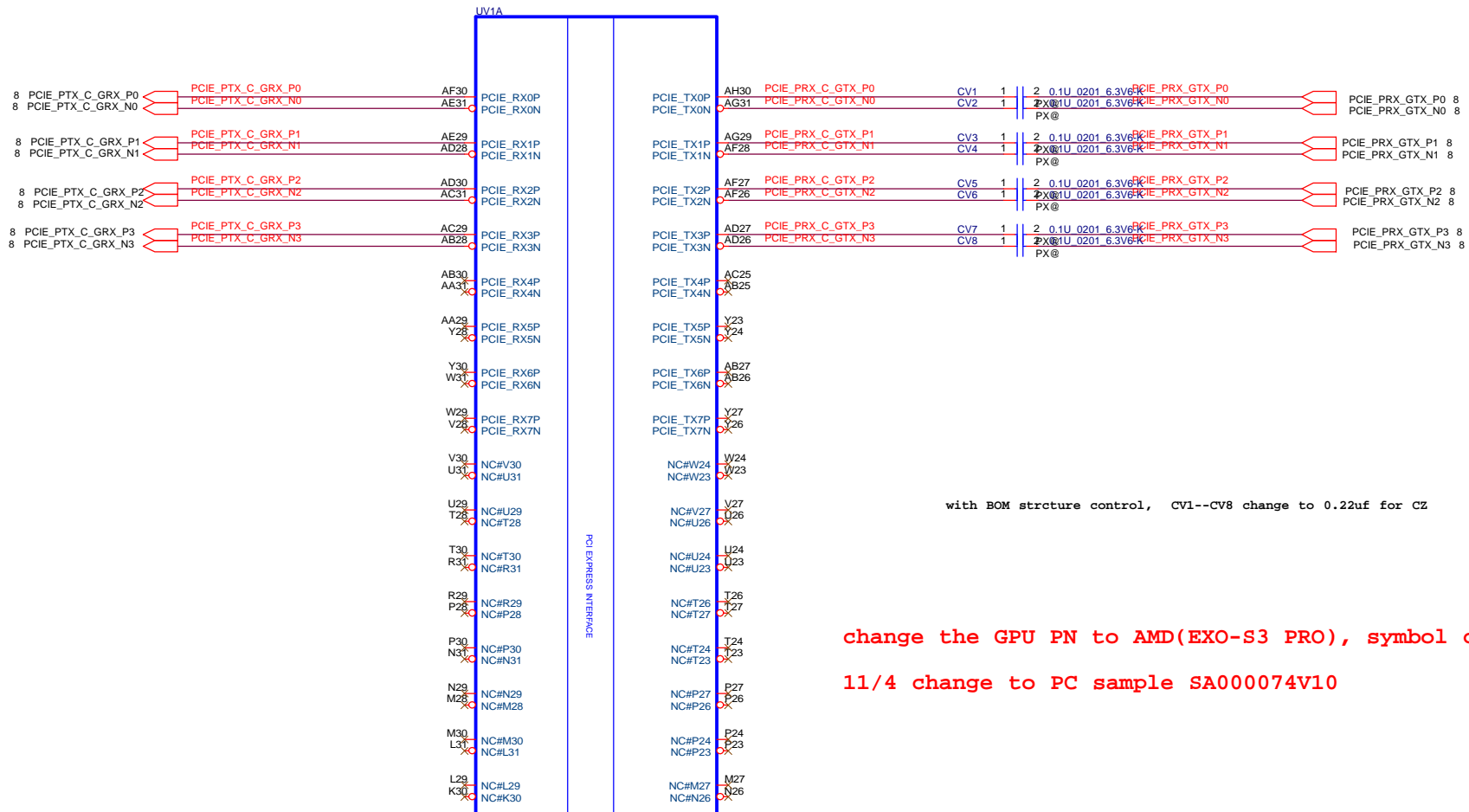
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

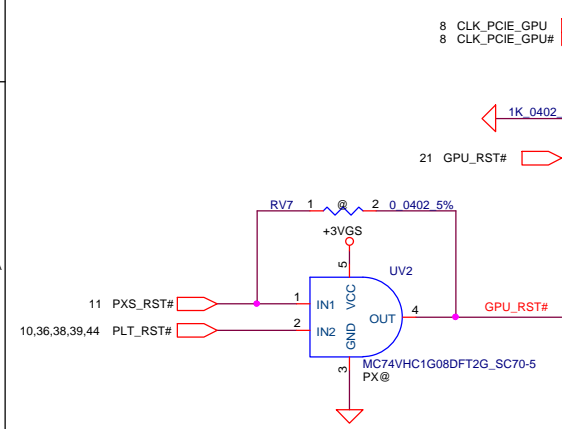
Memory Type	VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70	
256Mx16	Hynix H5GC8H24MJR-R0C	100	4.53K	4.99K
	Micron MT51J256M32HF-70:A	111	4.75K	NC
	Samsung K4G80325FB-HC28	110	3.4K	10K
	000	NC	4.75K	
	010	4.53K	2K	
	001	8.45K	2K	

FBGA Code: D9SXD

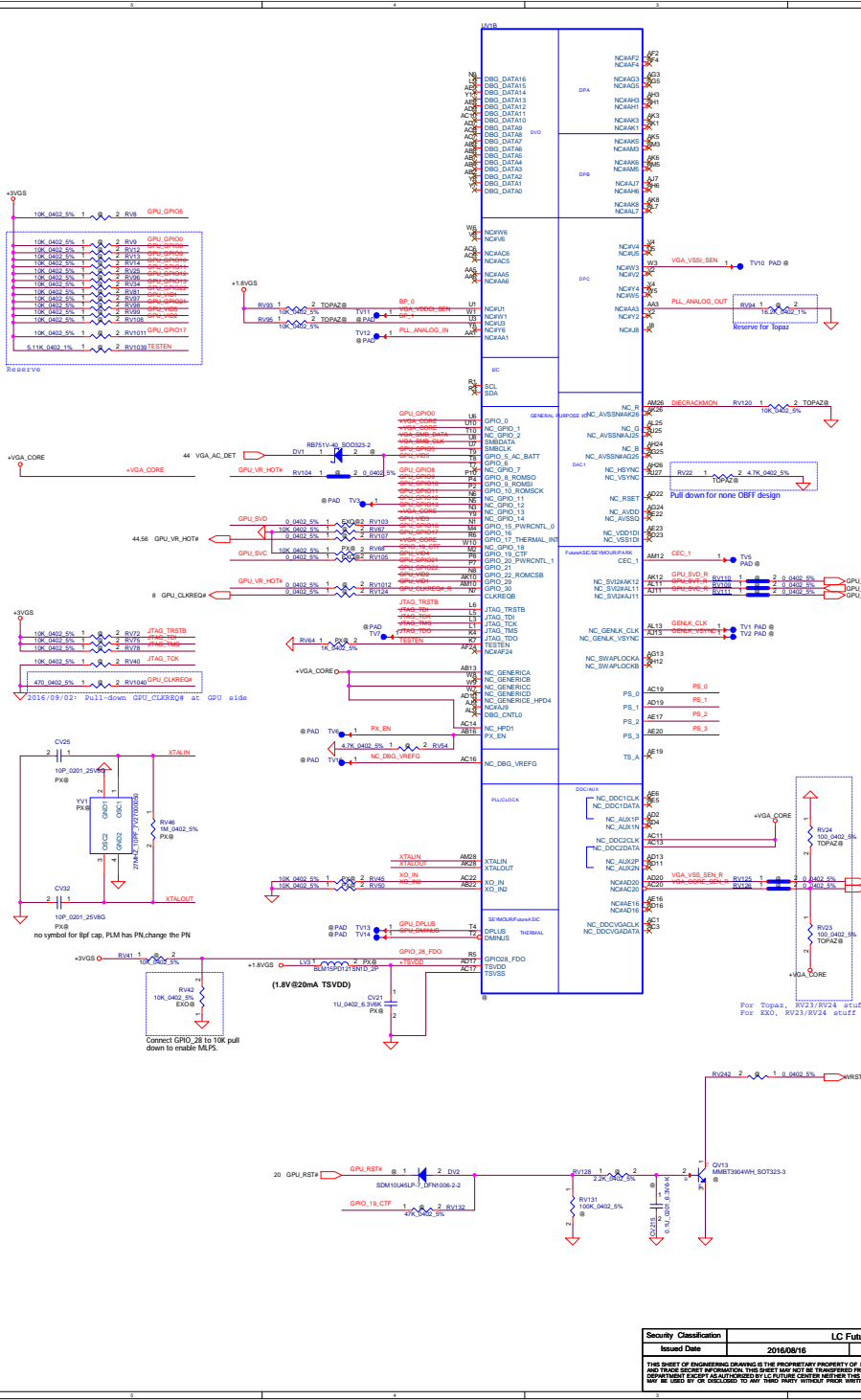


with BOM structure control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok
11/4 change to PC sample SA000074V10



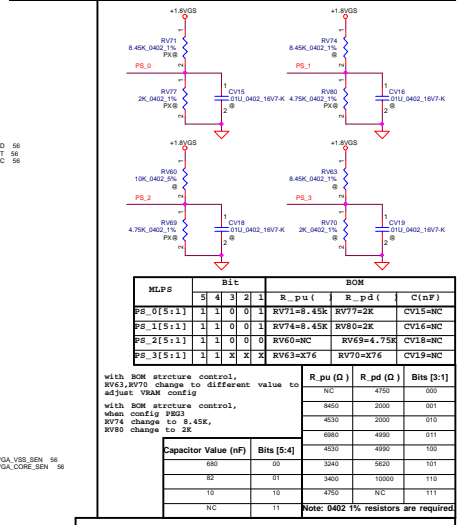
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Issued Date	2016/08/16	Deciphered Date	2017/08/15	ATI_EXO-PRO_PCIE	
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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	BOOT_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1.	
PS_0[2]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0.	X
PS_0[3]	ROM_CONFIG[0]		0x1 = 2048K
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUX_PORT_CONN_PINSTRAP[0]	The USB Reset signal type of the strap device that indicates the number of auto-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN0_EN	1 = PCH GEN0 is supported 0 = PCH GEN0 is not supported	0 = GEN0 is not supported
PS_1[2]	STRAP_BIF_GEN0_PMIEN	0 = The CLKREQ0 power management capability is disabled 1 = The CLKREQ0 power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 1 at reset.	0
PS_1[4]	STRAP_TX_DRV_FULL_SWING	0 = The transmitter full-swing is disabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPHEN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled	1 = Enable
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_CLK_DIS	0 = PCH controller capability is enabled 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	0
PS_3[1]	BOARD_CONFIG[1]	Board configuration related straps, such as for memory ID	X
PS_3[2]	BOARD_CONFIG[0]		100 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G
PS_3[3]	BOARD_CONFIG[2]		
PS_3[4]	AUX_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display auto-endpoints that will be presented to the OS and used. (Combine with PS_3[5])	111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 000 = Six usable endpoints.
PS_3[5]	AUX_PORT_CONN_PINSTRAP[0]		111 = No usable endpoints.



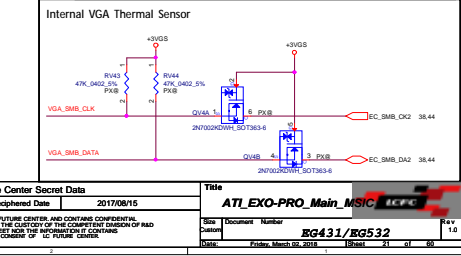
MLPS	Bit	ROM
PS_0[5:1]	1 1 1 0 0	RV71=8.45K, RV77=2K, CV15=NC
PS_1[5:1]	1 1 1 0 0	RV74=8.45K, RV80=2K, CV16=NC
PS_2[5:1]	1 1 1 0 0	RV60=NC, RV69=4.75K, CV18=NC
PS_3[5:1]	1 1 1 1 1	RV63=2K, RV70=2K, CV19=NC

with BOM structure control, RV63, RV70 change to different value to adjust VRAM control

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6550	4990	011
4330	4990	100
60	3240	5620
10	3450	10500
10	4990	100
NC	11	Note: 0402 % resistors are required


Capacitor Value (nF) Bits [5:4]

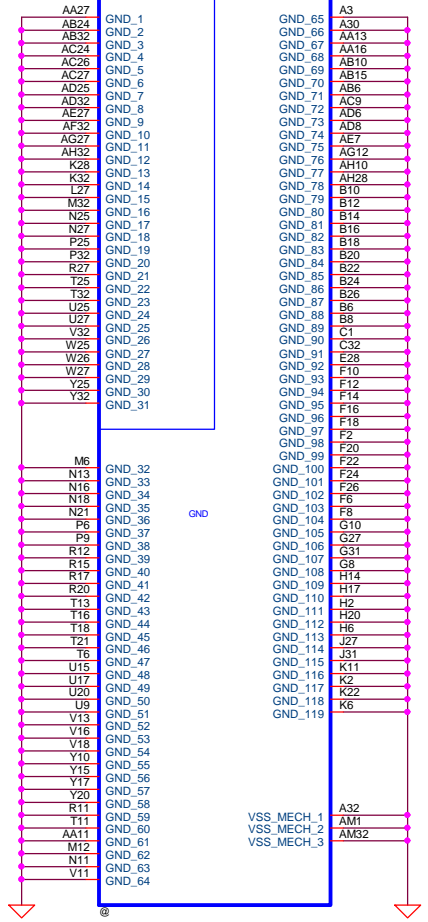
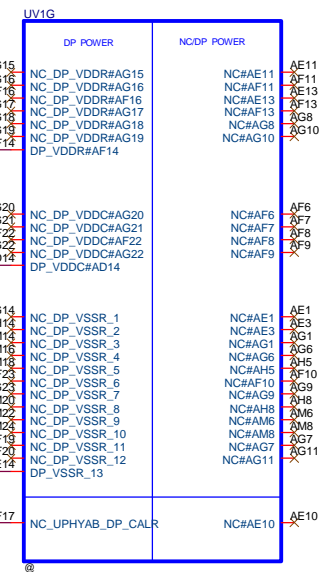
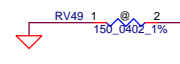
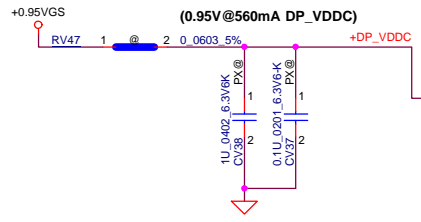
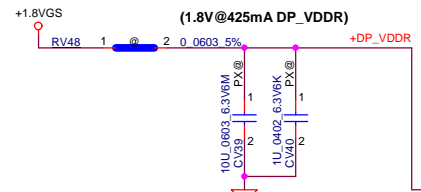
Capacitor Value (nF)	Bits [5:4]
6550	00
10	01
10	10
NC	11




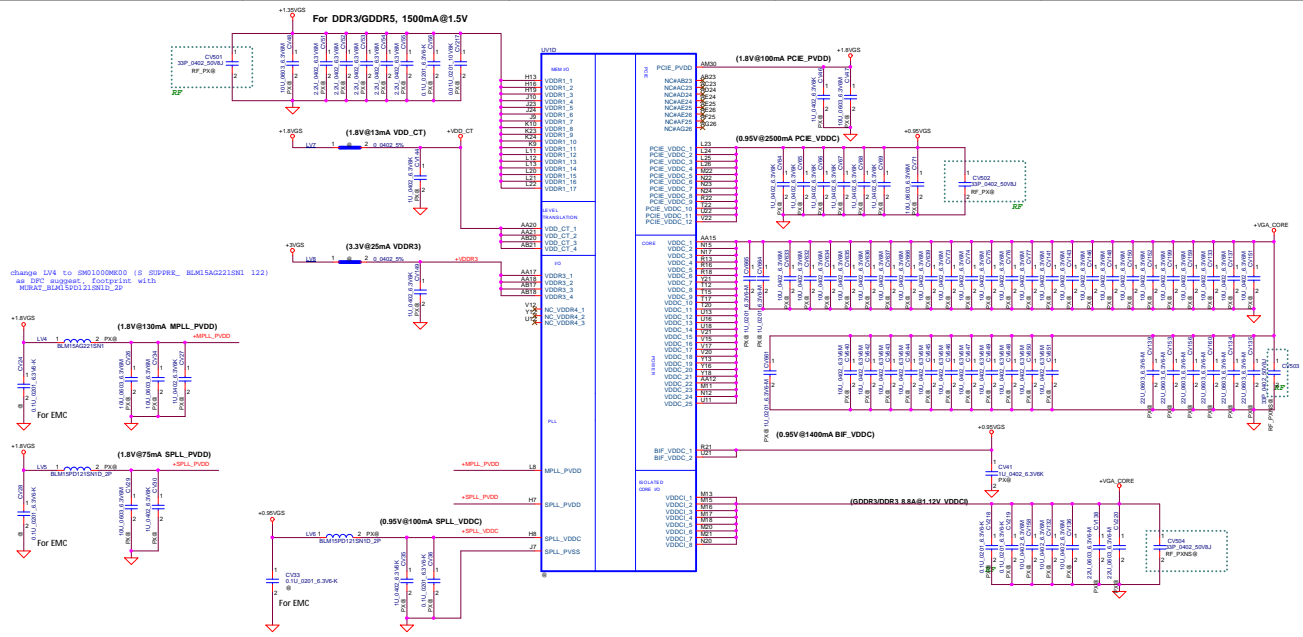


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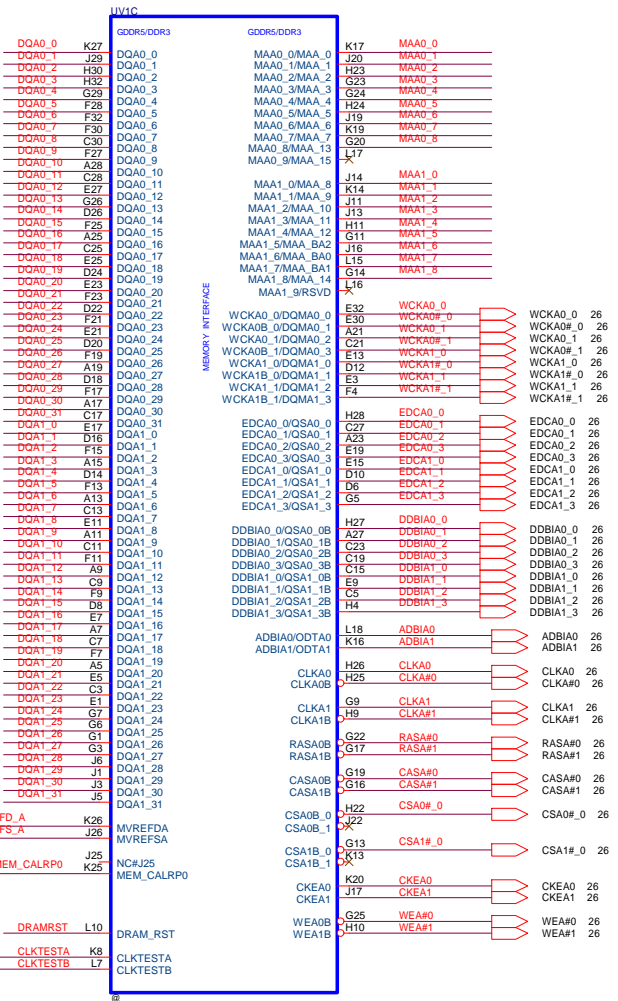
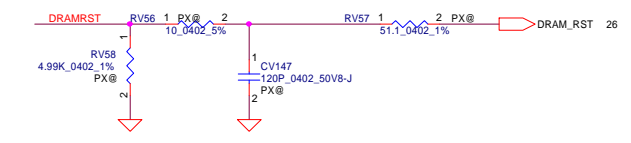
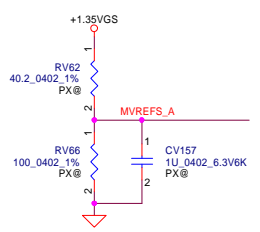
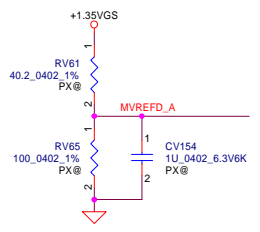
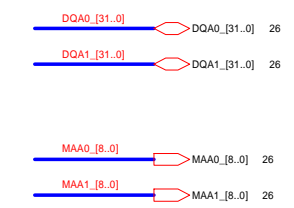
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ATI_EXO-PRO_TMDP		
Size	Document Number	Rev
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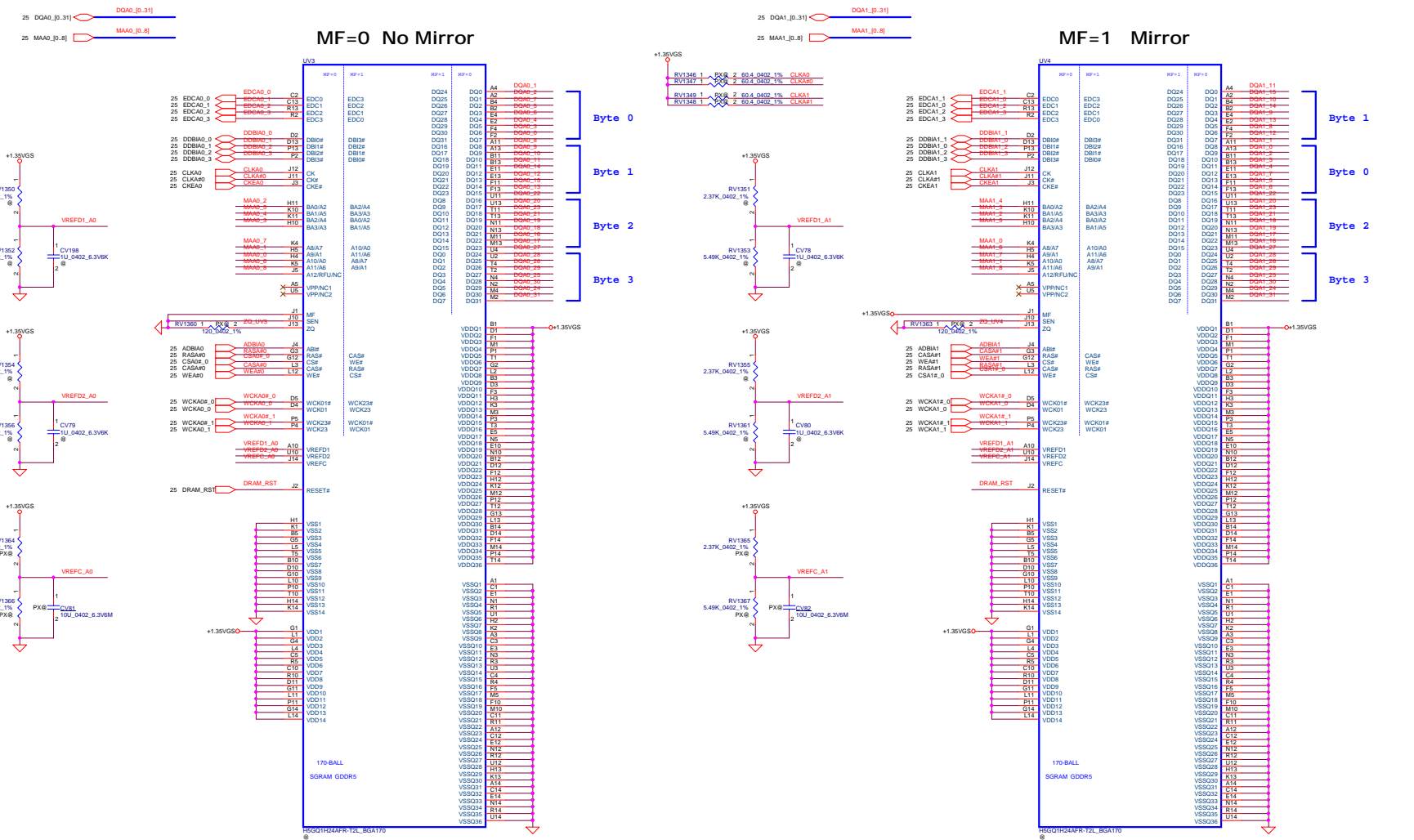
change LV4 to SM1000W600 (S SUPP9K_BLM15A2221SN1 122)
 in BPC change: 1000000000 WITH
 MURAV_BLM15P0121SN10_0



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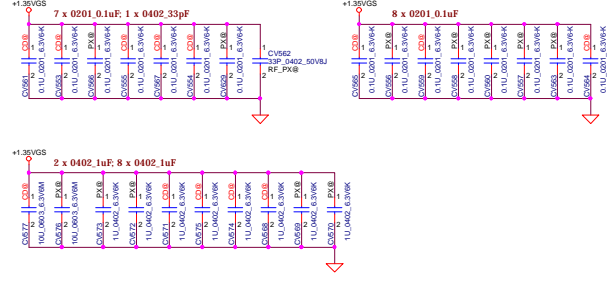
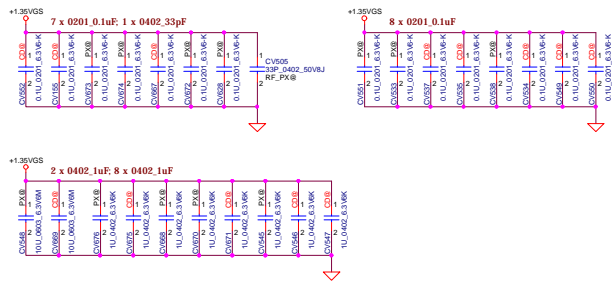
MF=0 No Mirror

MF=1 Mirror



Place Near at UV3 Side

Place Near at UV4 Side



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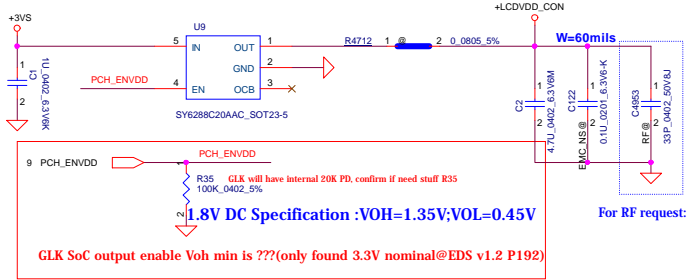
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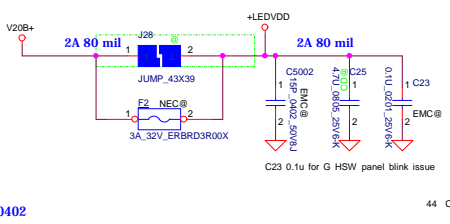
LCD POWER CIRCUIT



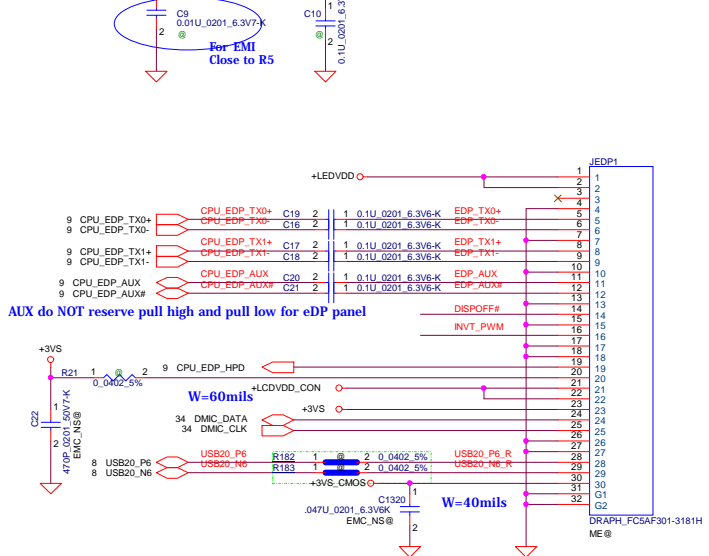
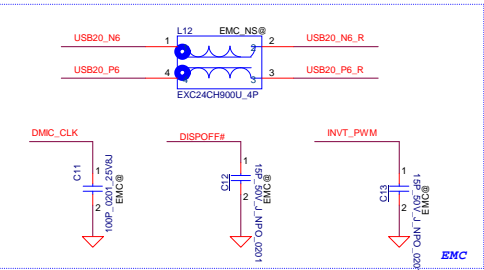
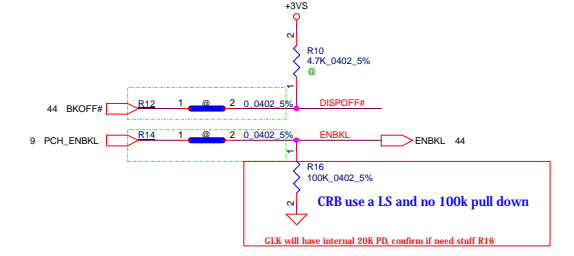
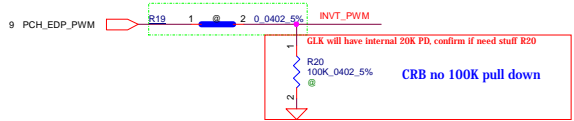
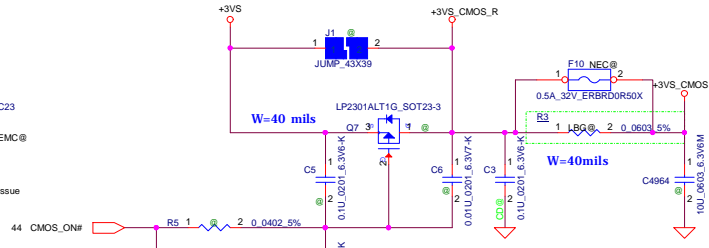
1.8V DC Specification :VOH=1.35V;VOL=0.45V

GLK SoC output enable Voh min is ???(only found 3.3V nominal@EDS v1.2 P192)

B+ to +LEDVDD POWER

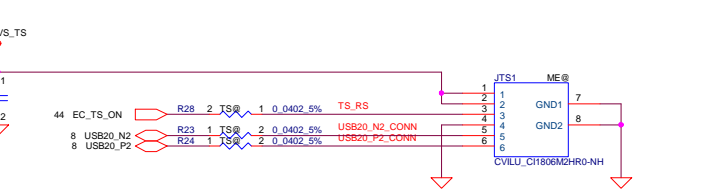
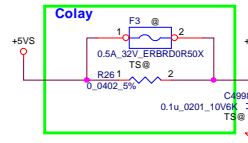
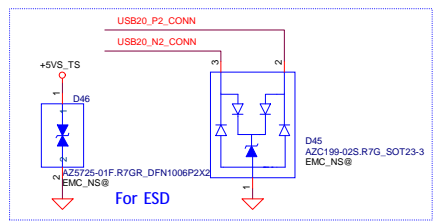
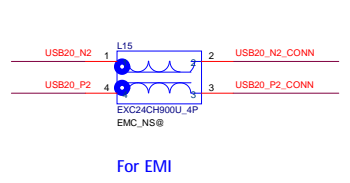


CMOS CAMERA

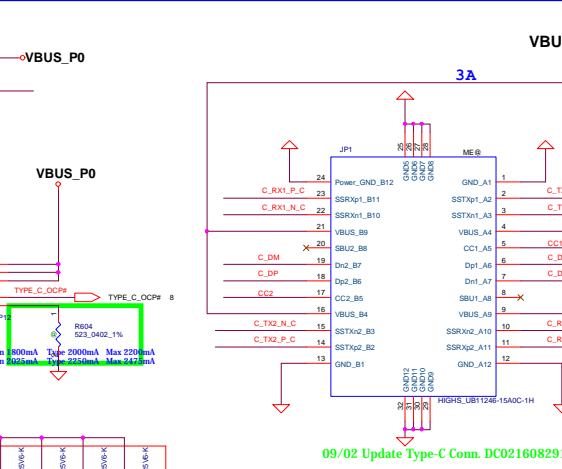
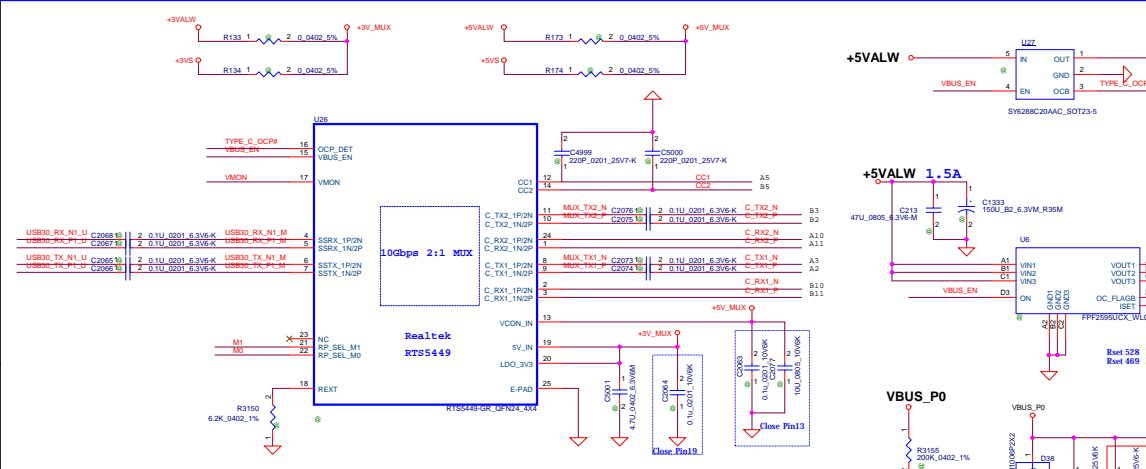
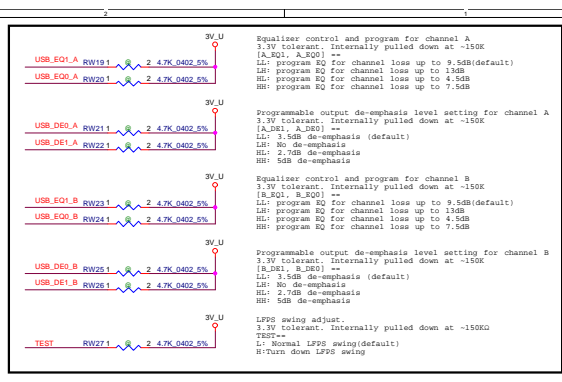
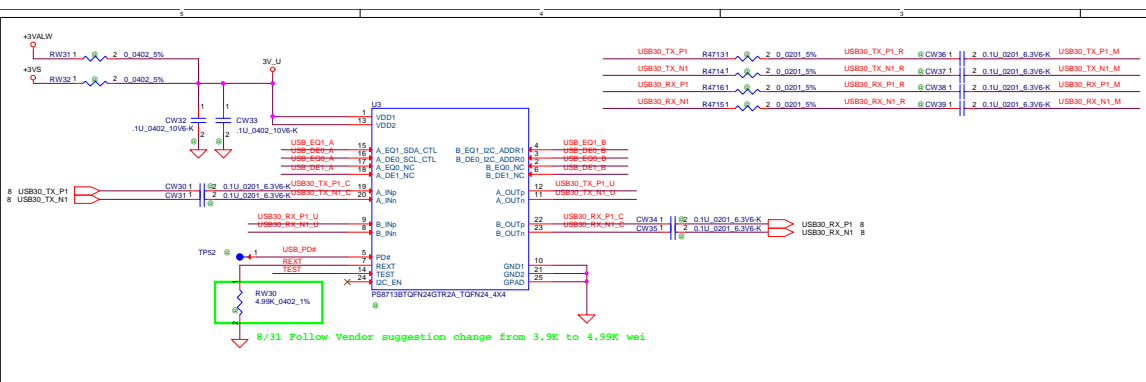


Touch Screen

Touch Screen



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Rp configuration

Rp:1.5A (now)

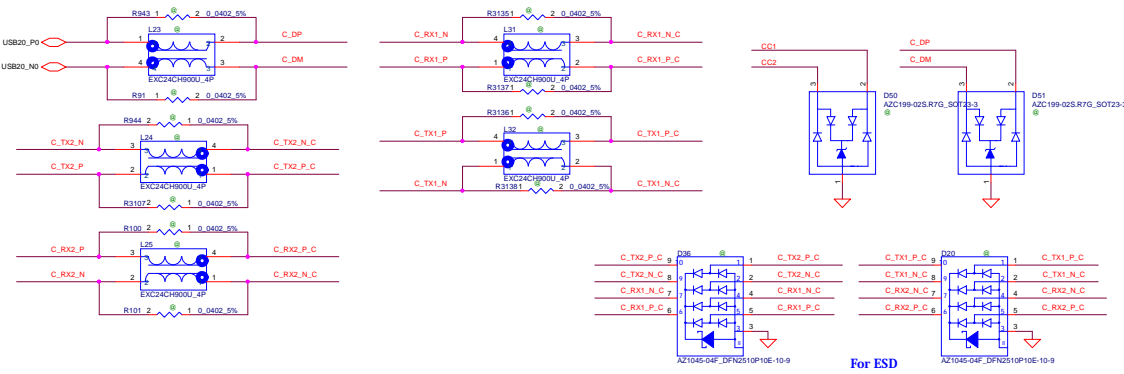
	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

For C_VBUS power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount



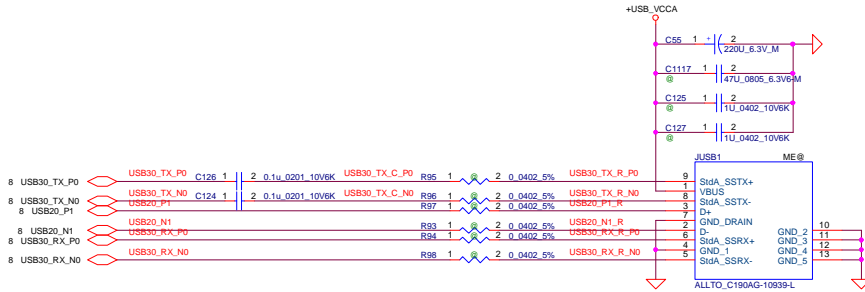
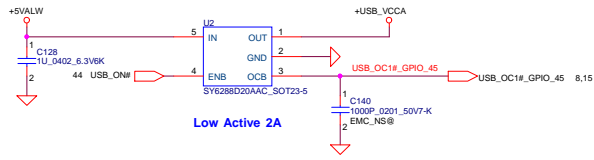


Security Classification	LC Future Center Secret Data		
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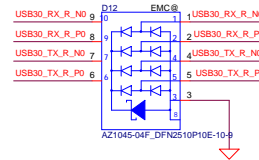
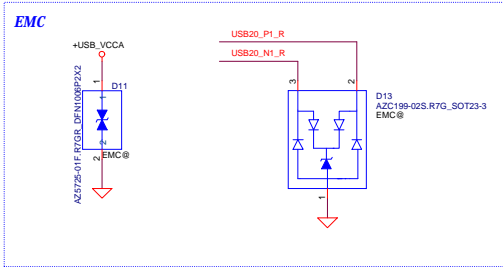
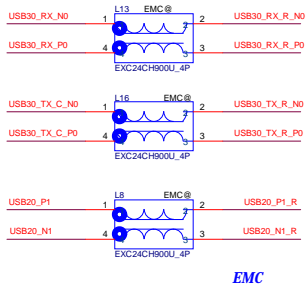
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Size	Document Number	Rev	
	EG431/EG532	1.0	
Date:	Friday, March 02, 2016	Sheet	30 of 60



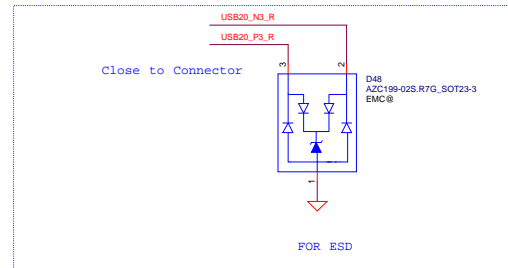
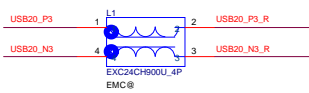
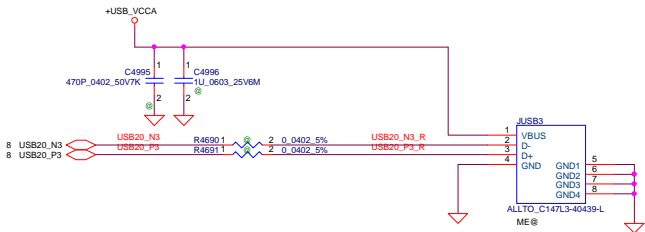
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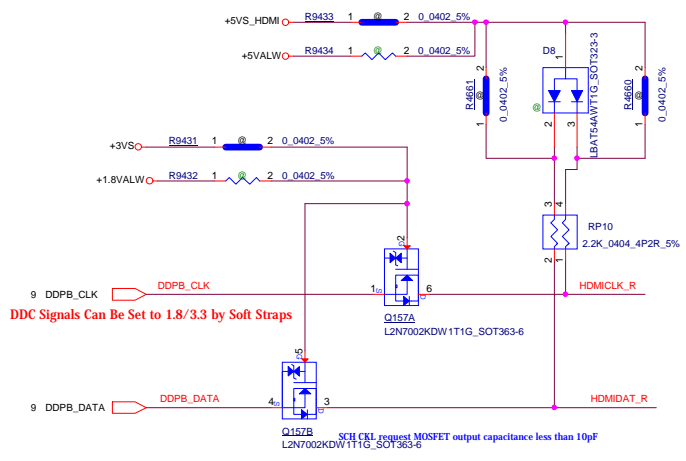
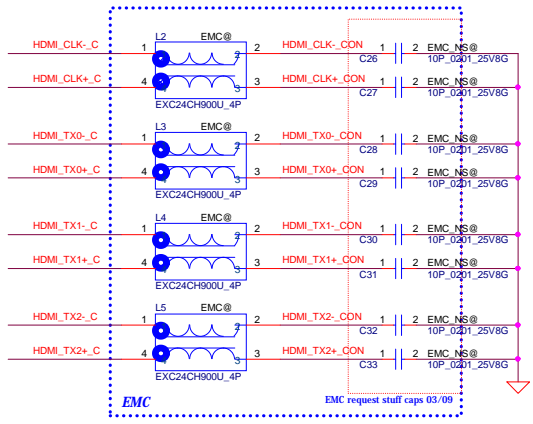
09/05 Update USBConn. P/N DC021609011 wei



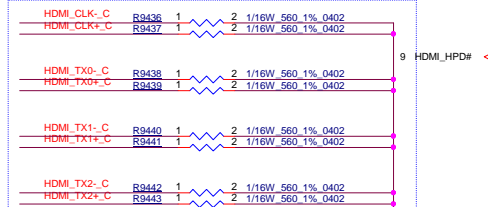
Update footprint symbol lewis



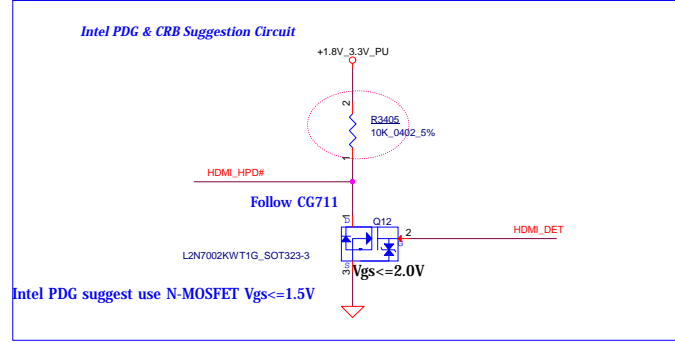
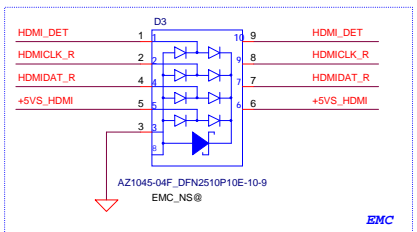
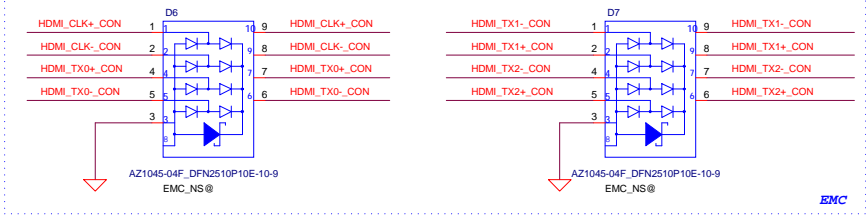
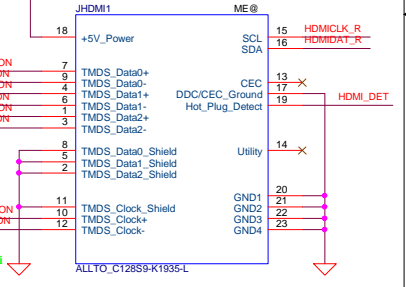
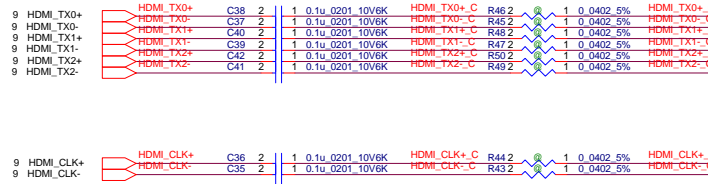
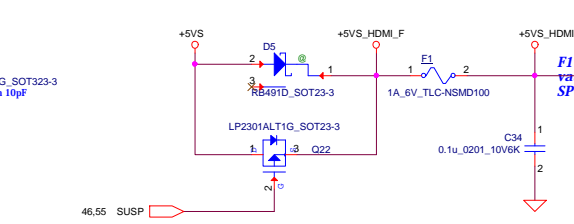
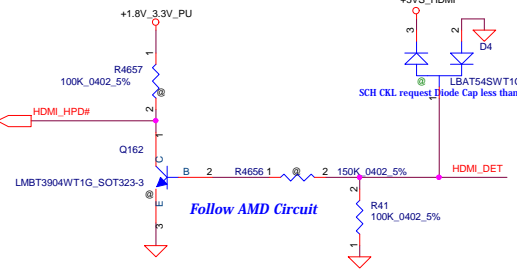
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	
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				Rev: 1.0



Follow PDG & CRB use 470ohm.SVT change 470 to 560 for HDMI issue



Change to 0404 RP 04/29



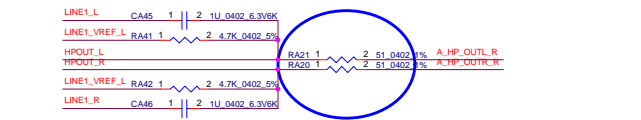
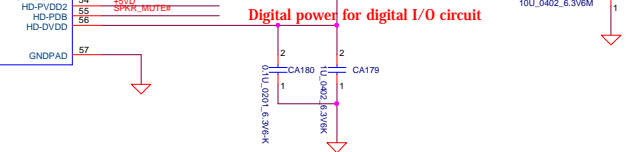
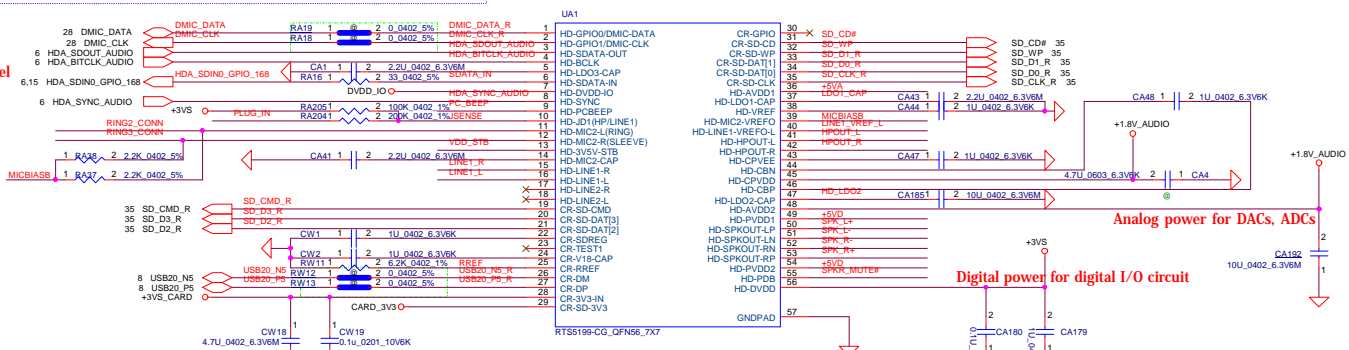
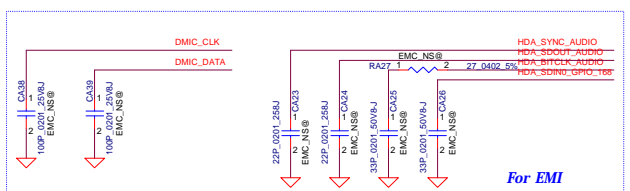
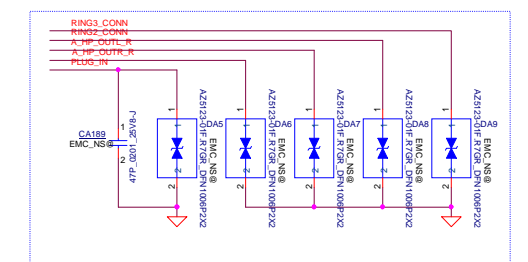
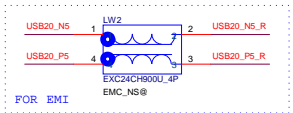
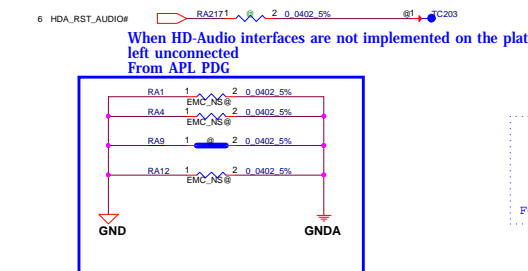
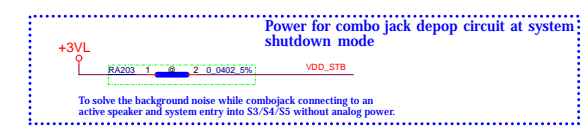
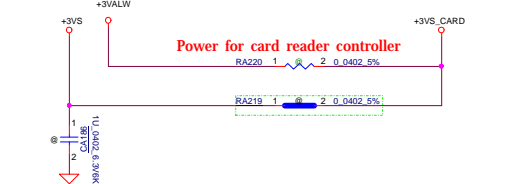
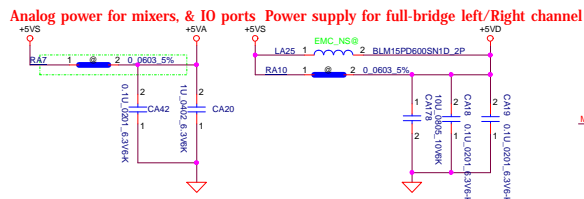
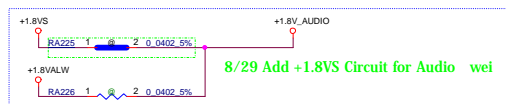
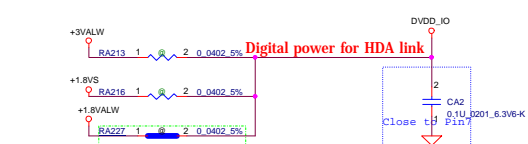
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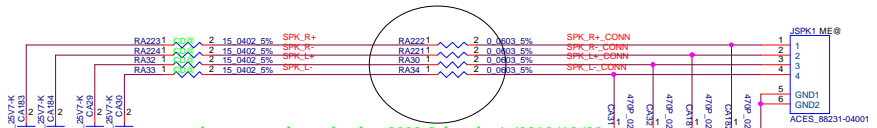
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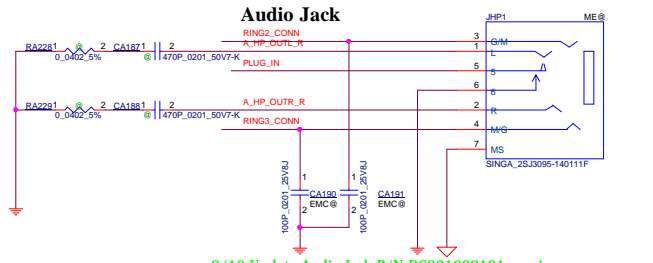




11/8 SIT Vendor suggestion form 47 ohm change to 51ohm wei

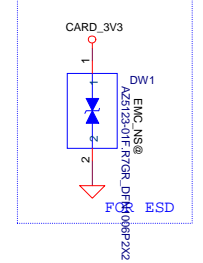
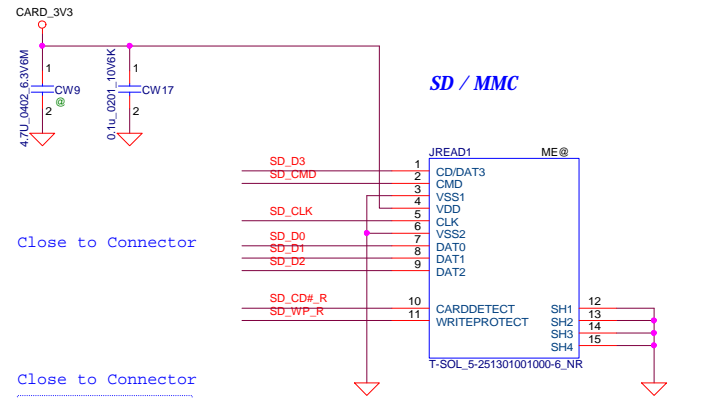


8/16 Update Audio Jack P/N SP011509163 wei

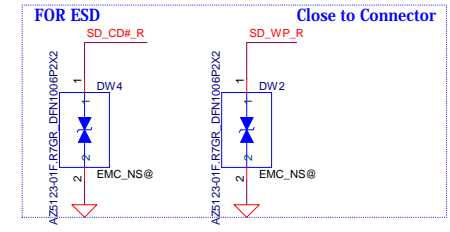


8/16 Update Audio Jack P/N DC021608101 wei

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8/16 Update Conn. P/N SP07000WG00 wei



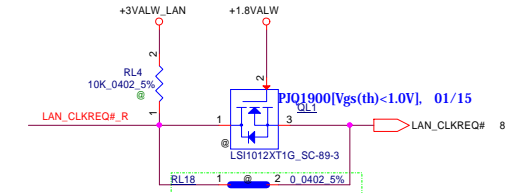
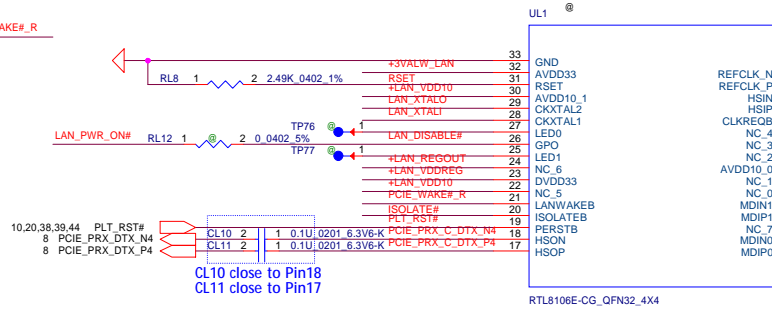
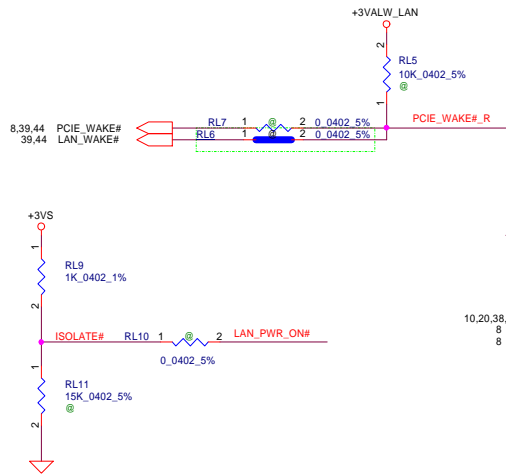
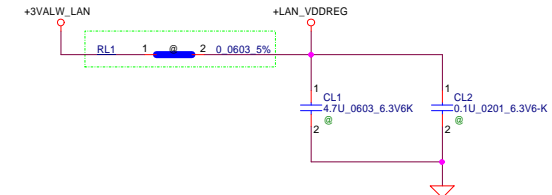
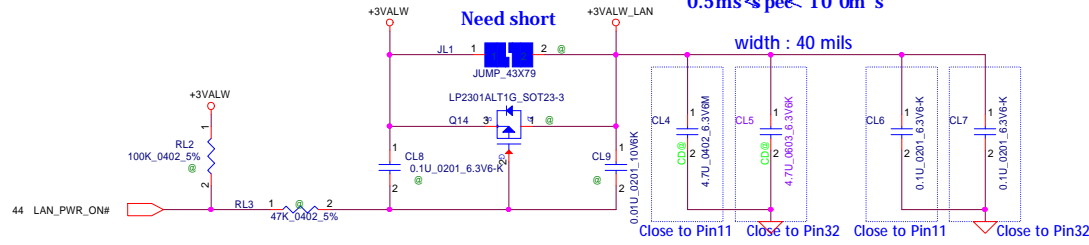
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+3VALW TO +3VALW_LAN

**+3VALW_LAN rising time (10%~90%):
0.5ms ≤ pe ≤ 10 0m s**

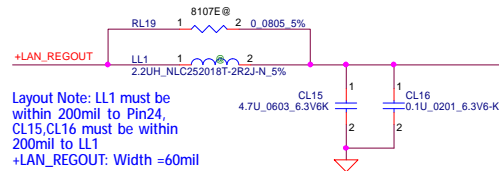
Need short

width : 40 mils

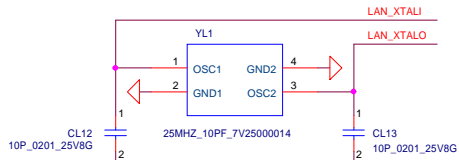


APL SOC CLKREQ are 1.8VALW power plane

**For RTL8111GUL(SWR mode)/RTL8106E LL1&RL19 un-stuff
For RTL8111H /RTL 8107E (LDO mode) RL19 stuff**



Layout Note: LL1 must be within 200mil to Pin24, CL15, CL16 must be within 200mil to LL1 +LAN_REGOUT: Width =60mil



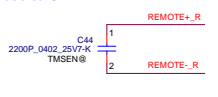
25MHz Crystal--TXC SJ10000G500

Follow common pool change 25MHz X'tal from EPSON to TXC. 03/01

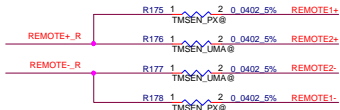
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THERMAL SENSOR

Close to U1

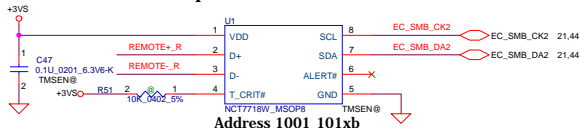


Set Thermal Sensor as a BOM Structure

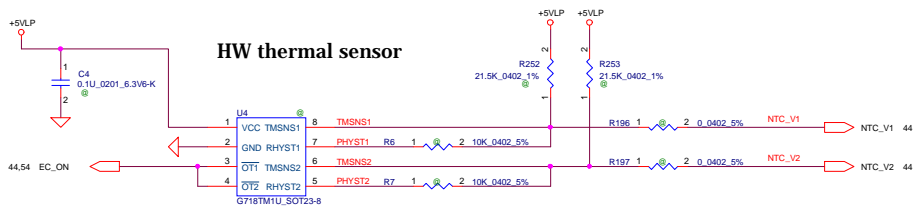


REMOTE+/_R, REMOTE1+/_R, REMOTE2+/_R
Trace width/space:10/10 mil
Trace length:8°

SMSC thermal sensor placed near DIMM

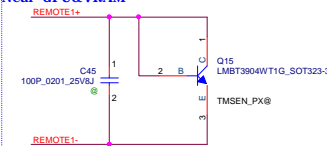


Address 1001_101xb

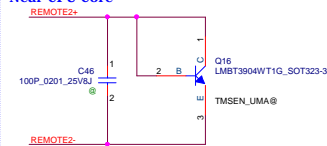


Over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold:
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

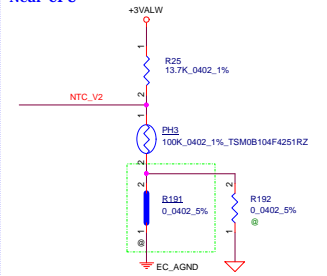
Near GPU&VRAM



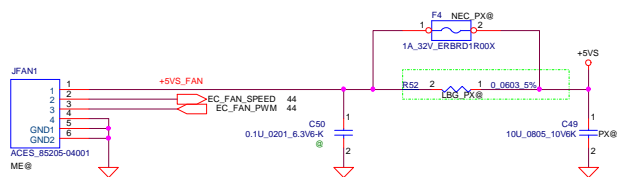
Near CPU Core



Near CPU

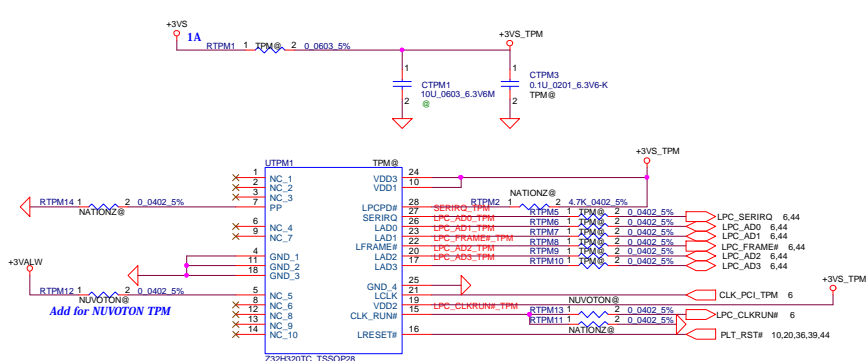


FAN Conn



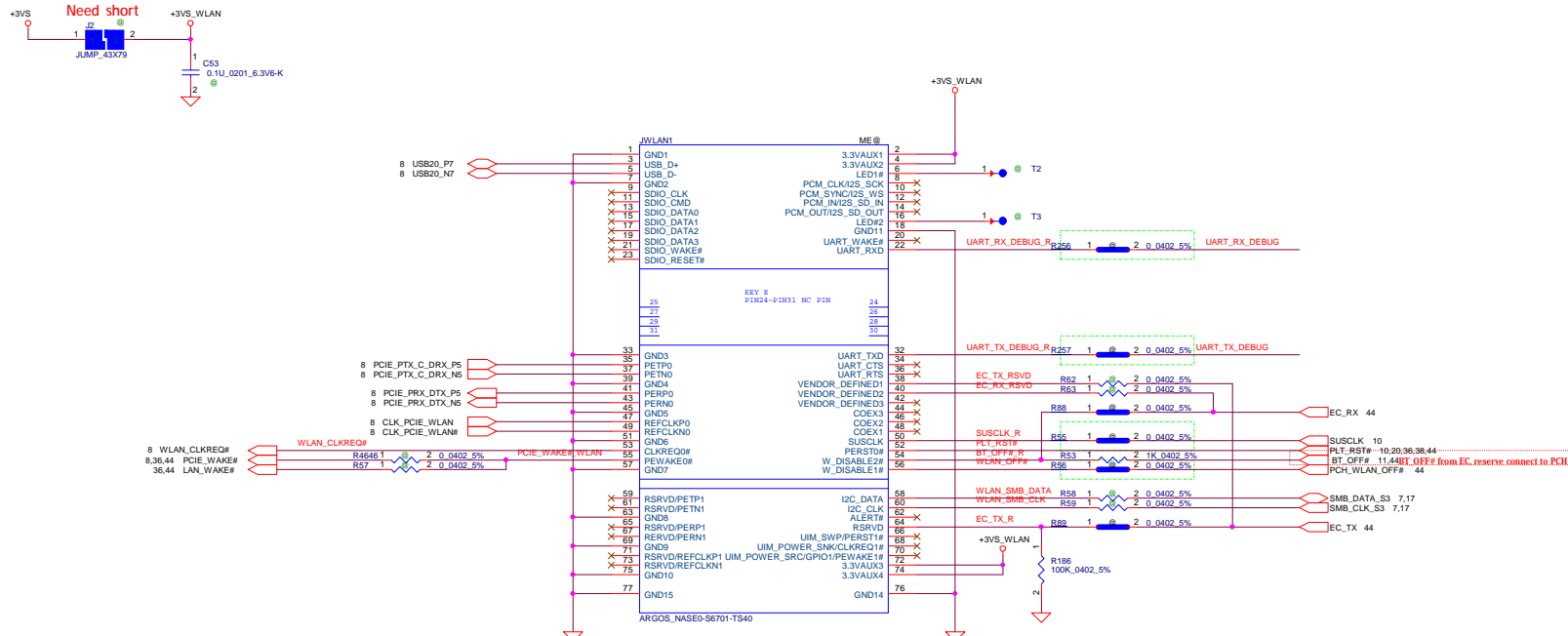
Update FAN conn. footprint to SP02008X0J
SP020012200 main source is SP020008X0J
Lewis 2016/10/14

TPM

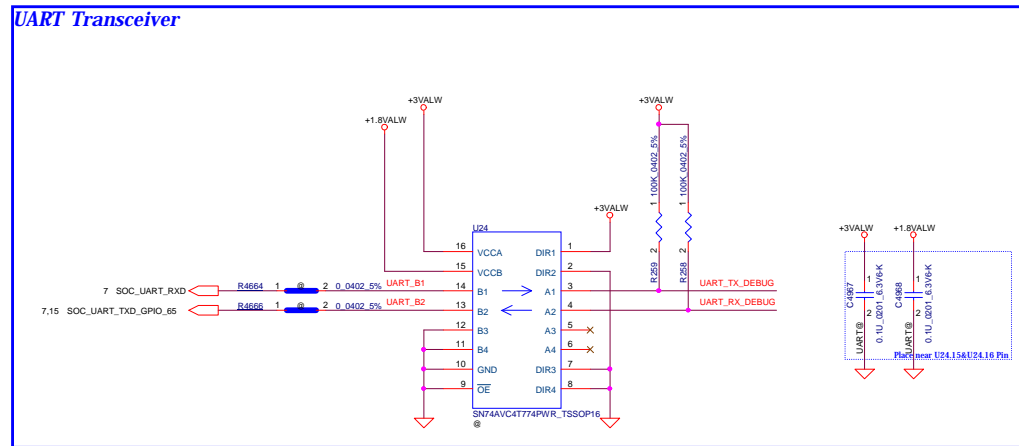


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Mini-Express Card(WLAN/WiMAX)



8/16 Update Conn. P/N SP070013200 wei
Copy DG421 symbol



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NGFF WLAN

LCFC

EG431/EG532

A

B

C

D

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A

B

C

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C

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A

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				Custom	EG431/EG532	1.0
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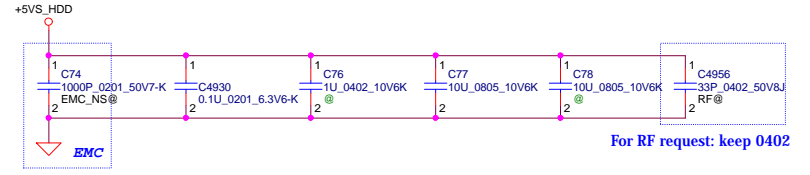
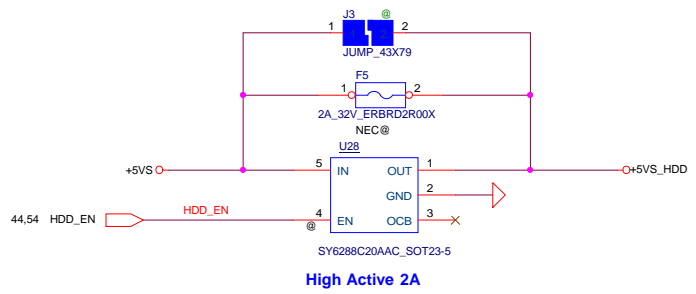
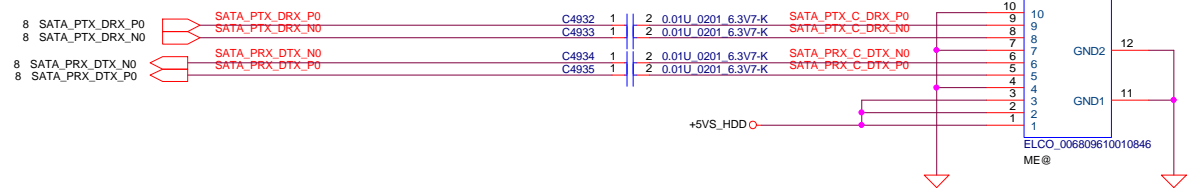
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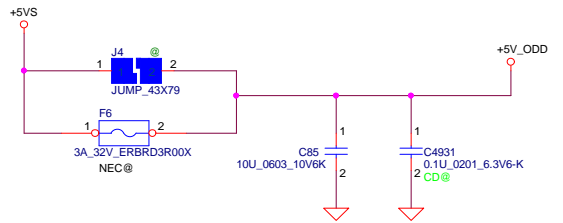
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SATA HDD Conn.

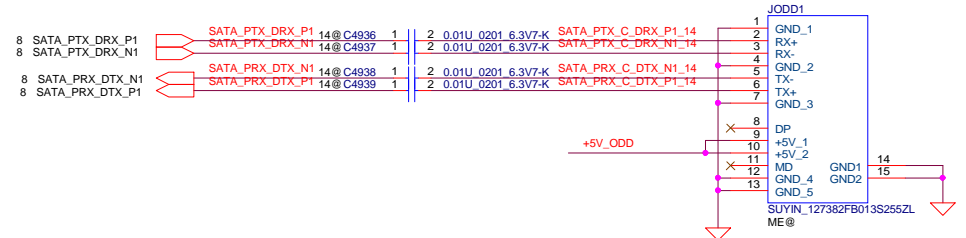
SATA HDD P/N Pin Define Same as CG411



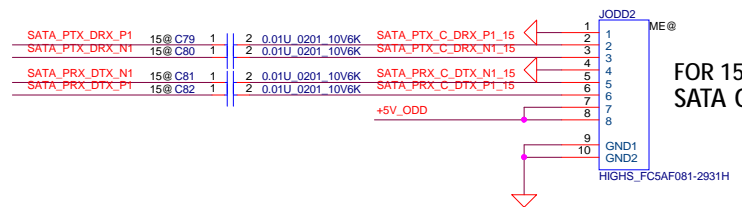
+5VS to +5V_ODD



FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn



8/16 Update Conn. P/N SP01001YV00 wei

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Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title		
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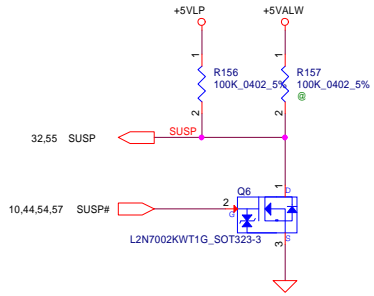
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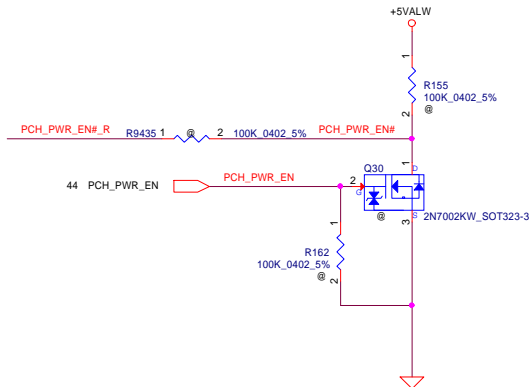
2

1

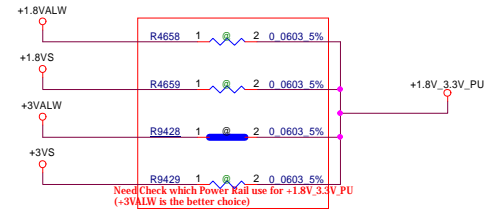
Delete +5VS/+3VS Load Switch



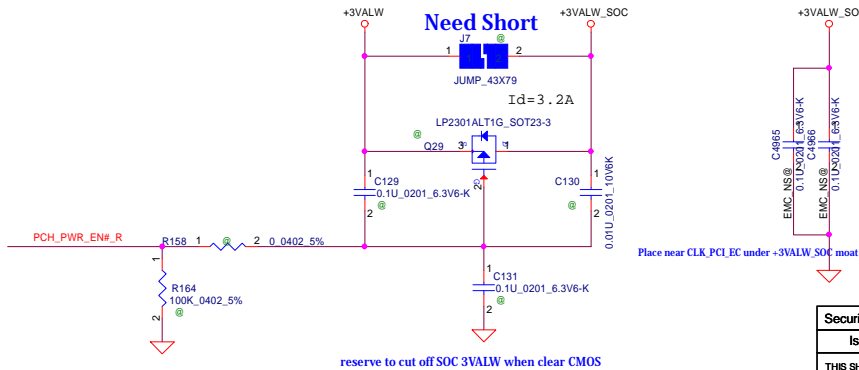
+3VALW to +3VALW_SOC



+1.8V_3.3V_PU Power Rail for 1.8/3.3 Select by Soft Strap

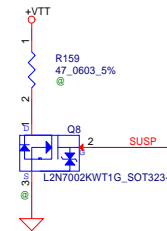


Need Short

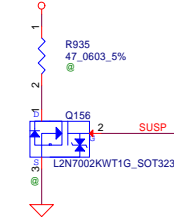


For DisCharge

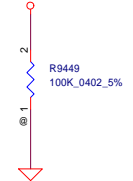
Need Check with power discharge



+1.2V



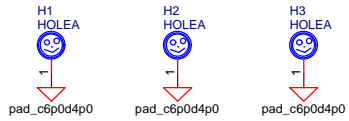
+2.5V_DDR



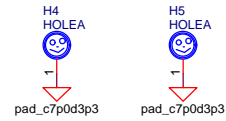
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		2013/08/15
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Title		
DC V TO VS INTERFACE		
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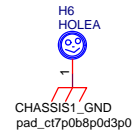
CPU Thermal Holes3



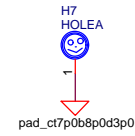
GPU Thermal Holes2



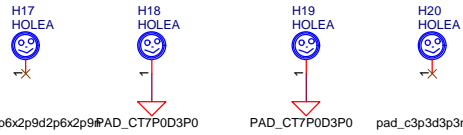
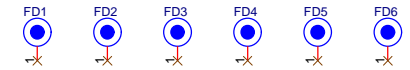
Close to RJ45



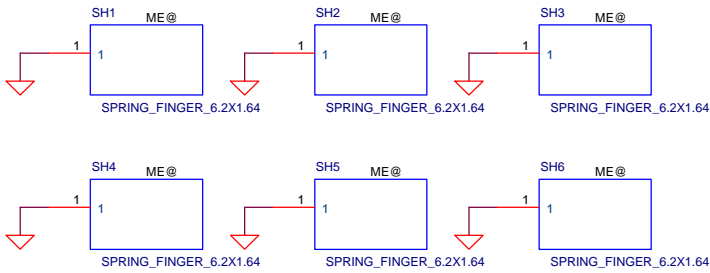
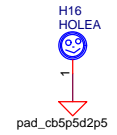
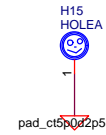
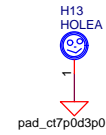
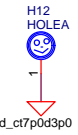
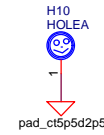
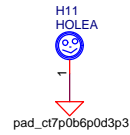
Close to Audio jack



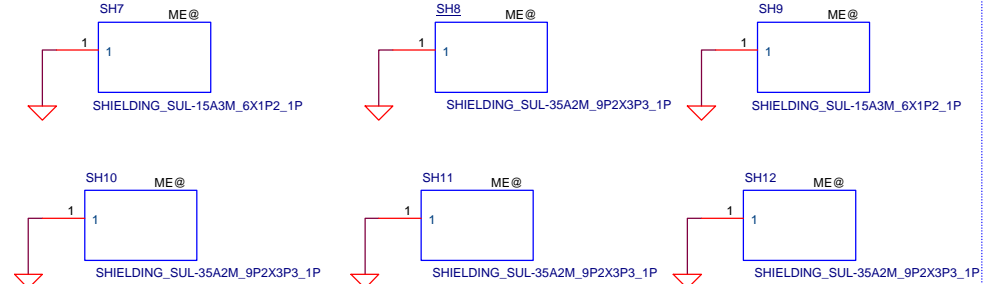
PCB Federal Mark PAD



WLAN Standoff

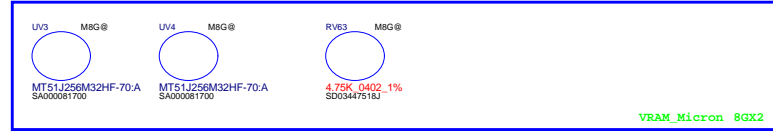
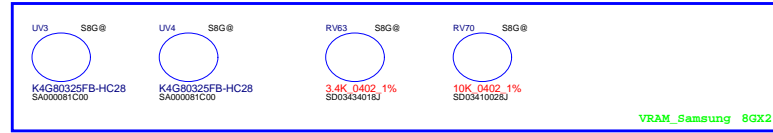
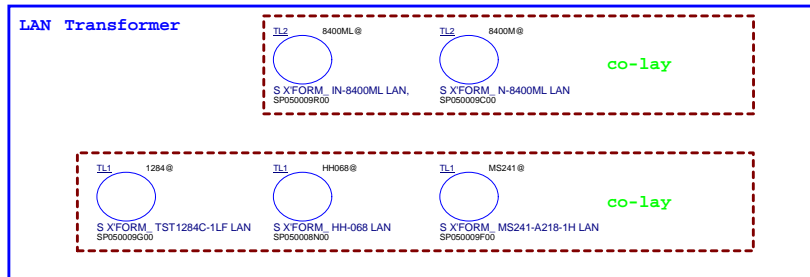
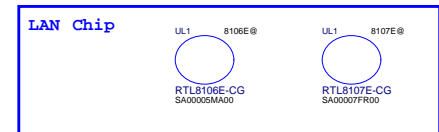
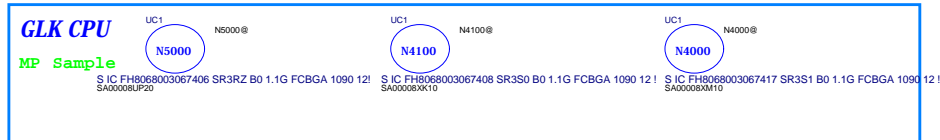
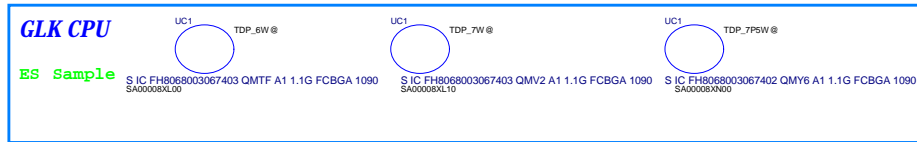
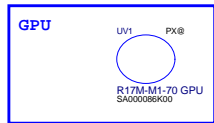
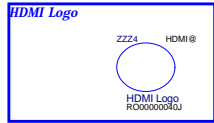
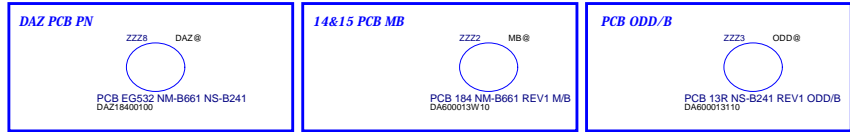


USB3.0 Shielding



DDR4 Shielding

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Issued Date		2013/08/08		Hole	
Deciphered Date		2013/08/05		LCFC	
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VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC8H24MJR-R0C	100	4.53K	4.99K
	Micron MT51J256M32HF-70:A	111	4.75K	NC
	Samsung K4G80325FB-HC28	110	3.4K	10K
		000	NC	4.75K
		010	4.53K	2K
		001	8.45K	2K

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Virtual symbol
EG431/EG532

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Title		
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Size	Document Number	Rev
Custom	EG431/EG532	1.0
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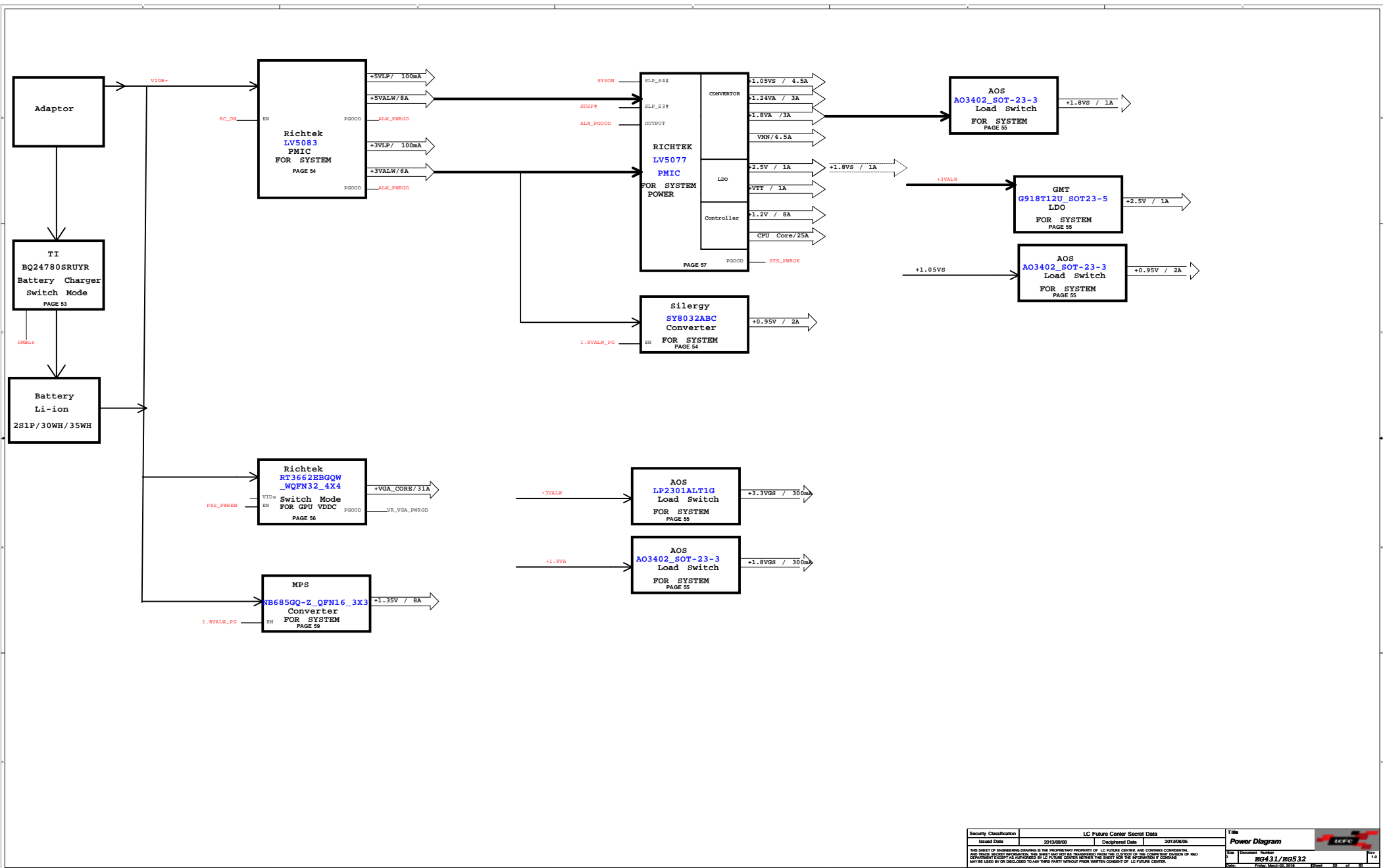
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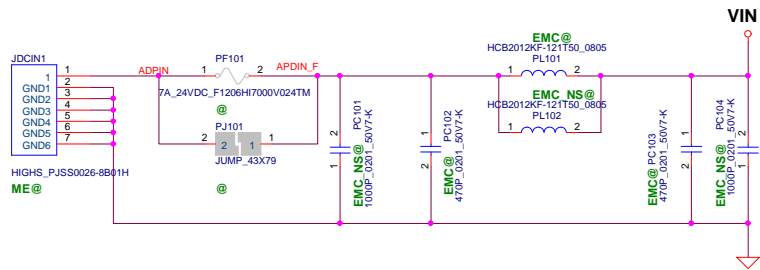
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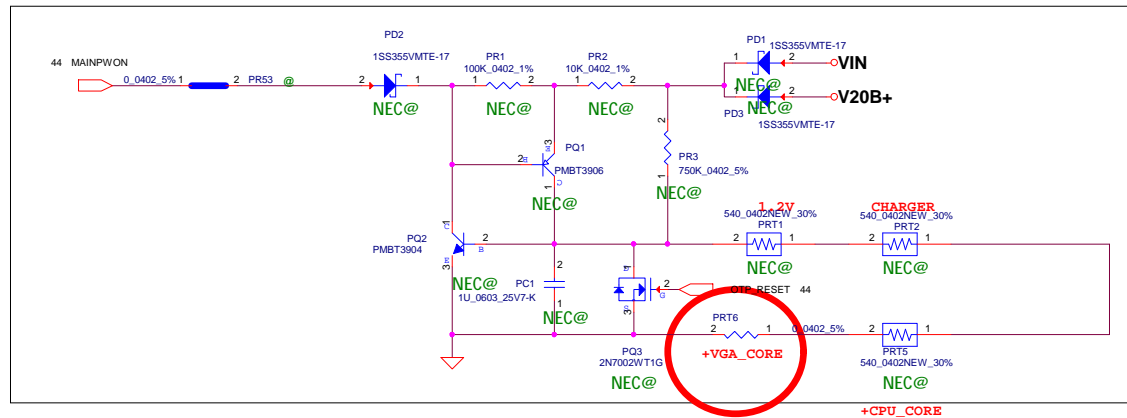
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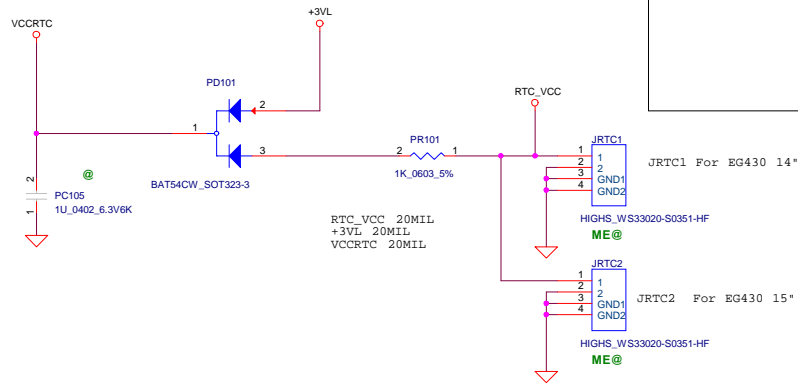




OTP

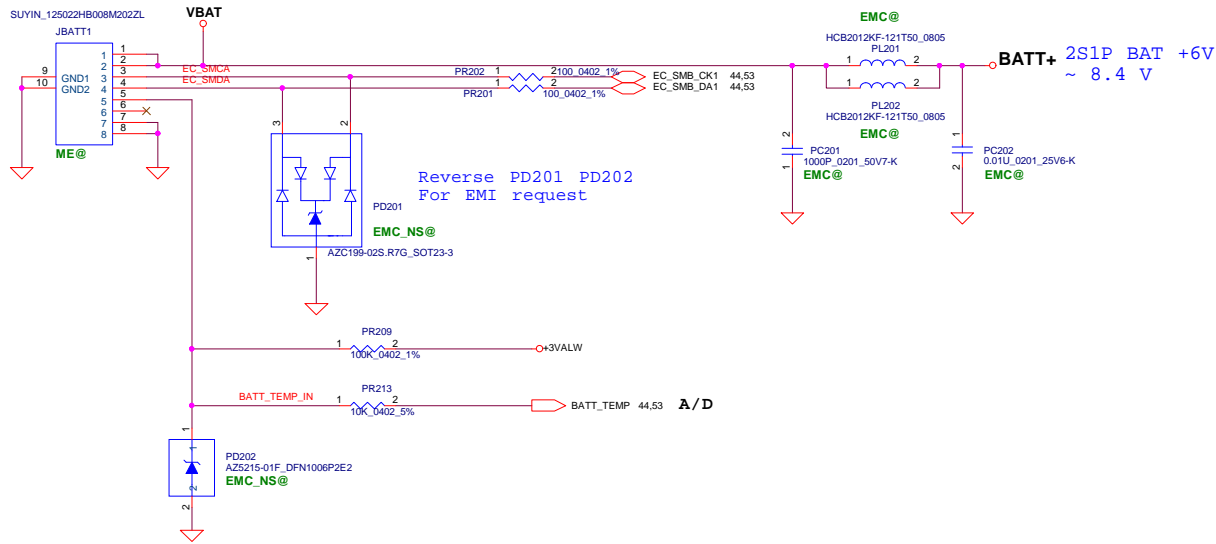


NEC NO DIS SKU change this NTC to Resistor.




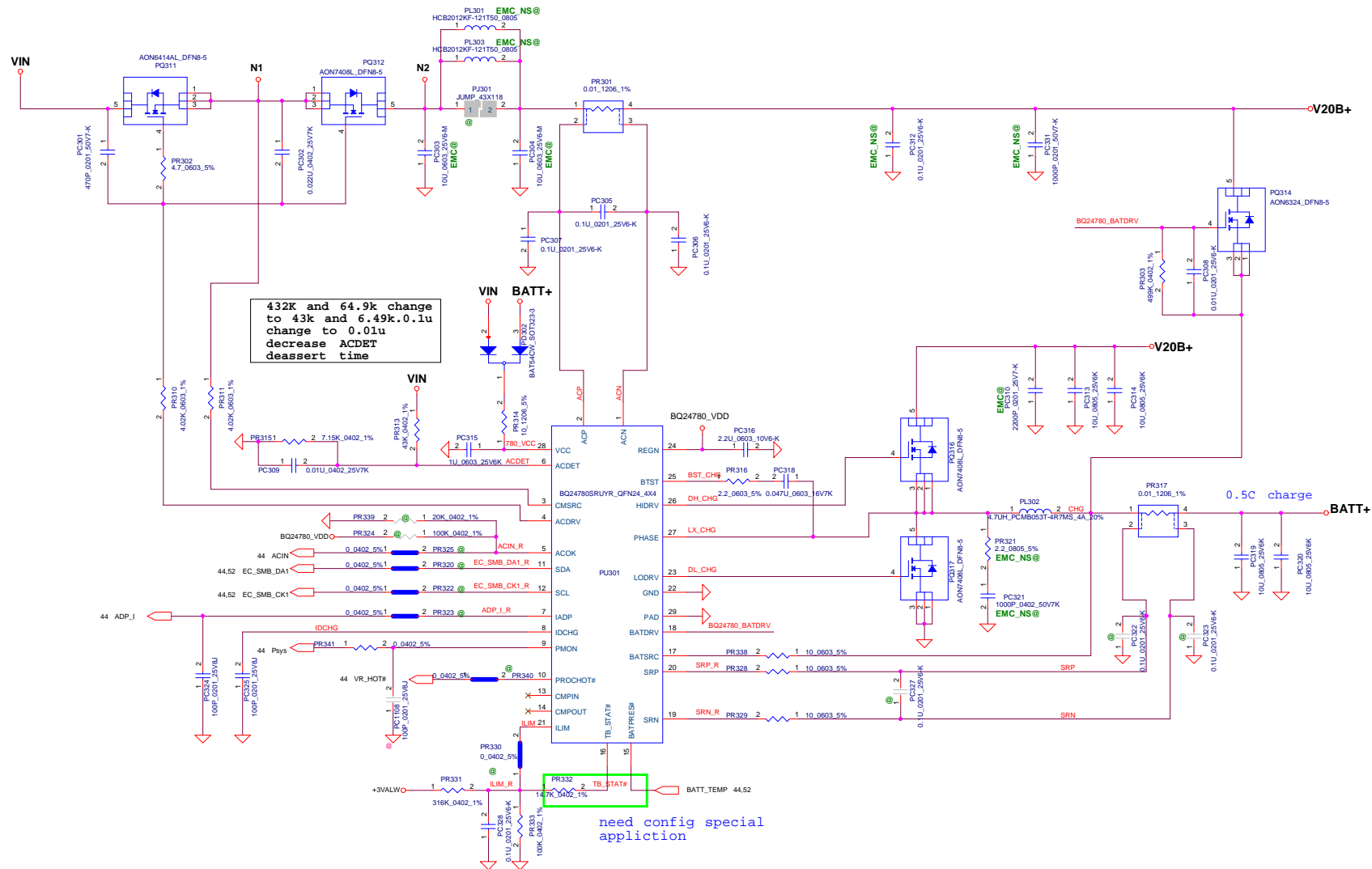
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Title		
PWR-DCIN / RTC charger		
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Issued Date	2015/08/20	Deciphered Date	2016/08/20
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Title		
PWR-BATTERY CONN		
Size	Document Number	Rev
Custom	EG431/BG532	1.0
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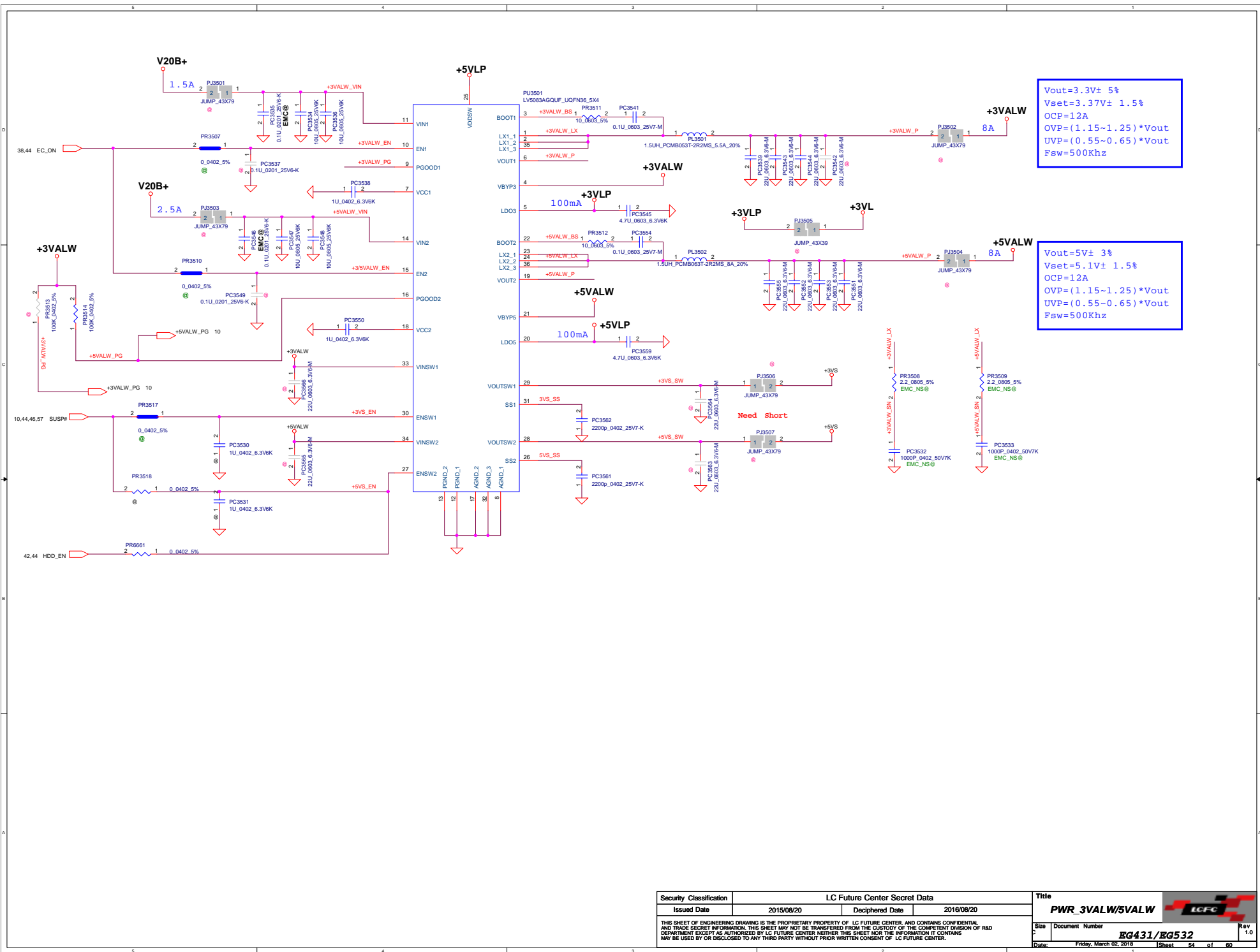
432k and 64.9k change to 43k and 6.49k. 0.1u change to 0.01u decrease ACDET deassert time

need config special application

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Title	PWR-CHARGER	
Size	Document Number	Rev
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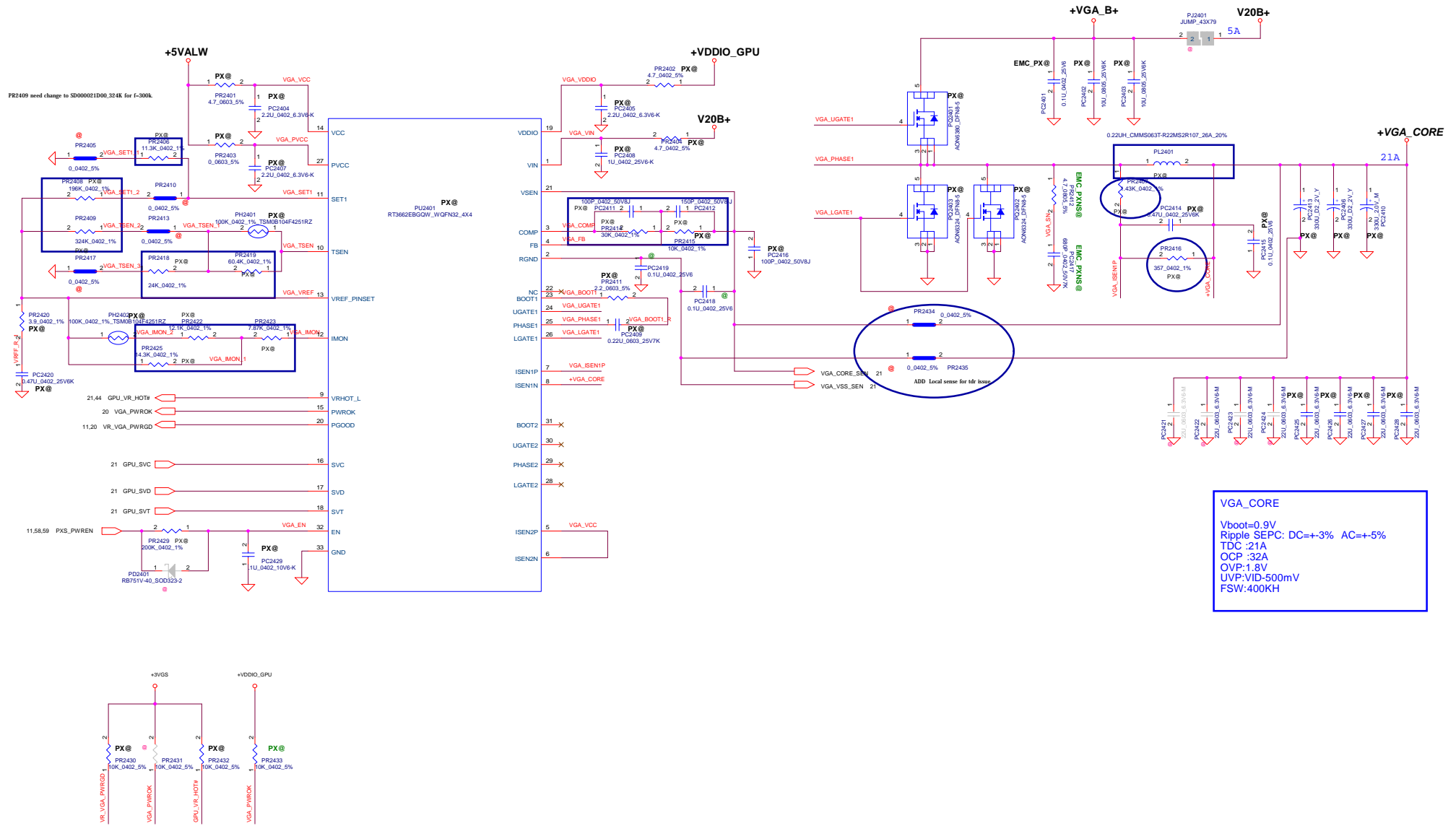
$V_{out} = 3.3V \pm 5\%$
 $V_{set} = 3.37V \pm 1.5\%$
 $OCP = 12A$
 $OVp = (1.15 \sim 1.25) * V_{out}$
 $UVp = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 500Khz$

$V_{out} = 5V \pm 3\%$
 $V_{set} = 5.1V \pm 1.5\%$
 $OCP = 12A$
 $OVp = (1.15 \sim 1.25) * V_{out}$
 $UVp = (0.55 \sim 0.65) * V_{out}$
 $F_{sw} = 500Khz$

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Title	PWR_3VALW/5VALW	
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PR2409 need change to SD000021D00.324K for I-300K.



+VGA_CORE

Vboot=0.9V
 Ripple SEPC: DC=+3% AC=+5%
 TDC :21A
 OCP :32A
 OVP:1.8V
 LVP:VID=500mV
 FSW:400KH


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20161216:SDV to SIT
 1.p56-p57 add R=100ohm,C=680pF in FB pin;
 2.pr3324 change to 55.4kohm,pr3323 change to 24.3k;
 3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
 4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
 5. GPU change 14 items to support AMD request.

20161219:SDV to SIT
 1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT
 1. PMIC change 1.24V Vin from 3VALW to1.8VALW;
 2.change PR2431 from PX@ to @, PR2433 from @ to PX@,
 3.change PR734 to @.

20170104:SDV to SIT
 1. PMIC change LV5075B TO LV5075A

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				Date: Friday, March 02, 2018	Rev 1.0
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