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NM_C511 M/B Schematics Document

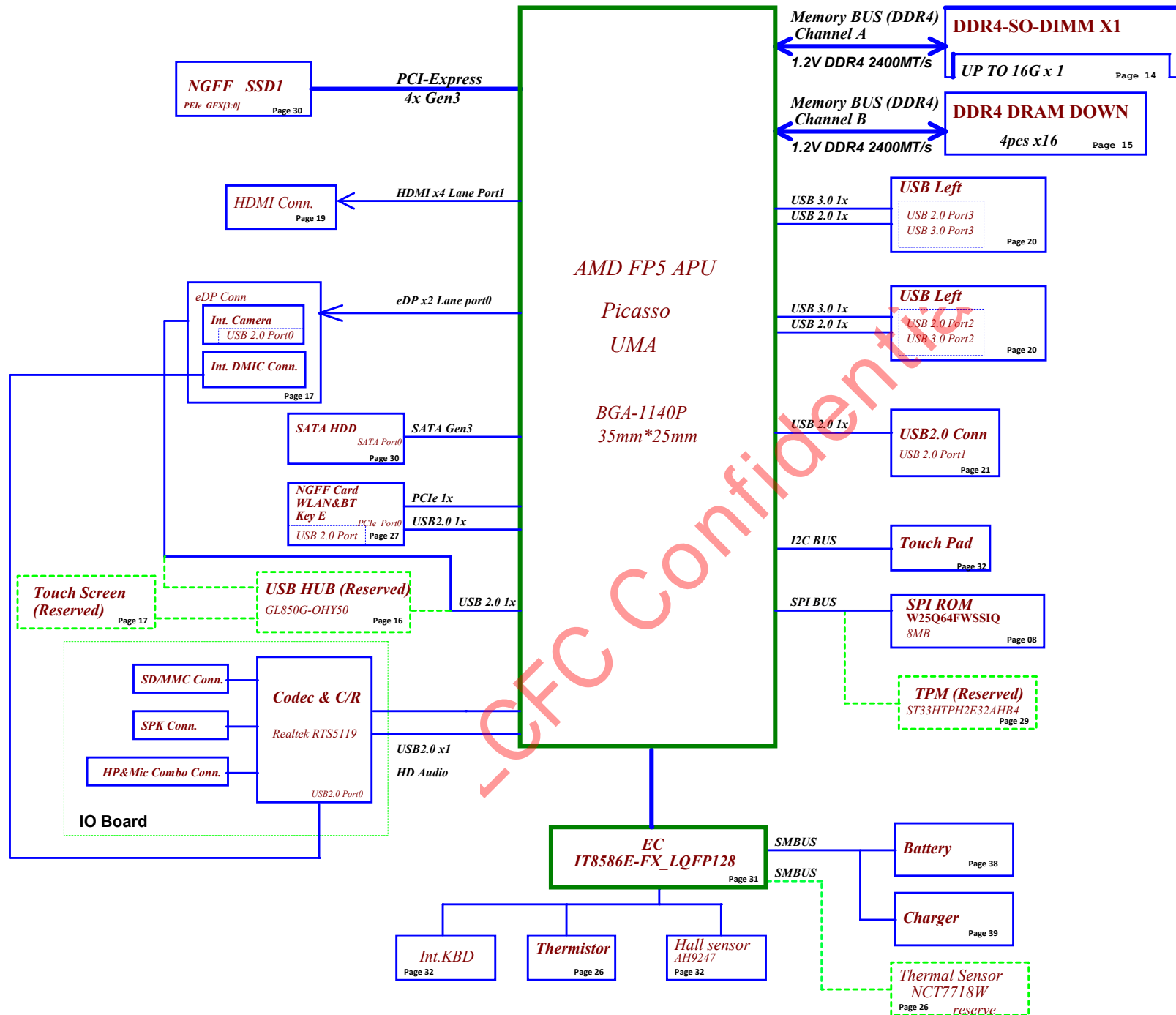
AMD FP5 PICASSO SOC with DDRIV

2019-05-28

REV: 1.0

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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Block Diagram	
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Size	Document Number	Rev		1.0	
Custom	S145 API	Date:		Tuesday, May 28, 2018	
Sheet		2		of 44	

Voltage Rails (O --> Means ON , X --> Means OFF)

power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_VDD +VDDCR_SOC +VDDC +VDDCI +3VGS +1.8VGS +1.35VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

I2C Control Table

	SOURCE	Device
TP_I2C0_SCL	APU	Touch Pad
TP_I2C0_SDA	+3VALW	+3VS

APU I2C address

Device	Address
Elan: SA469D-22HA 69x104x1.0	?
Synaptics: TM-P3255-008 69x104x1.0	?

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8586 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586 +3VL	X	X		X	X	V +3VS	X	X	V
EC_SMB_CK3 EC_SMB_DA3	IT8586 +3VS	V +3VS_VGA	X		X	X	X	V	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

Port List

HSIO Port	Device
GPP	0 WLAN
	1 LAN
	2 N/A
	3 N/A
	4 N/A
	5 N/A
	6 HDD
	7 ODD
GFX	0
	1 SSD
	2
	3
	4
	5
	6
	7
USB3.0	0 N/A
	1 Type C
	2 LEFT USB (3.0) lower
	3 LEFT USB (3.0) upper
	4 N/A
USB2.0	0 Camera
	1 Type C
	2 LEFT USB (3.0) lower
	3 LEFT USB (3.0) upper
	4 Touch
5 BT	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
EMC@	EMC Part
EMC_NS@	EMC reserve Part
RF@	RF Part
TPM@	TPM part
HDT@	HDT Debug part
REDRV@	Redriver part

EC SM Bus1 address


EC SM Bus2 address

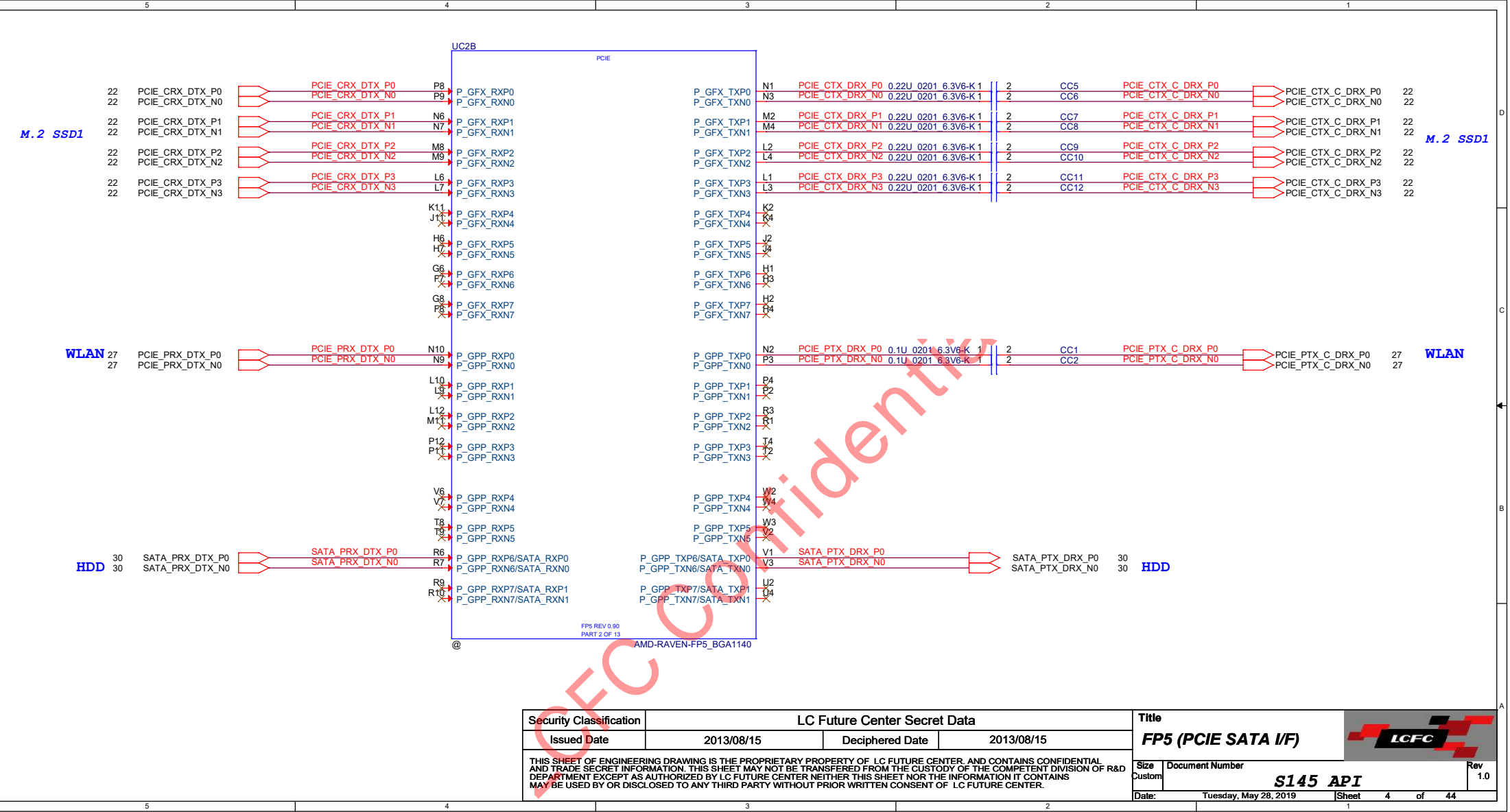
EC SM Bus3 address

Device	Address	Device	Address	Device	Address
Battery	?	PMIC	0X34	GPU	0x41(default)
Charger	0001_0010 b	Thermal Sensor	1001_100xb(reserve)	APU SB-TSI	relate to F3x1E4[SbiAddr] or Address Select Pins setting

APU SM Bus address

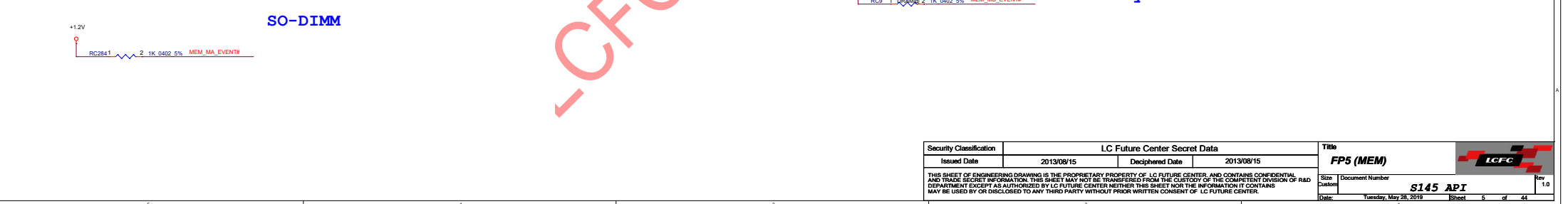
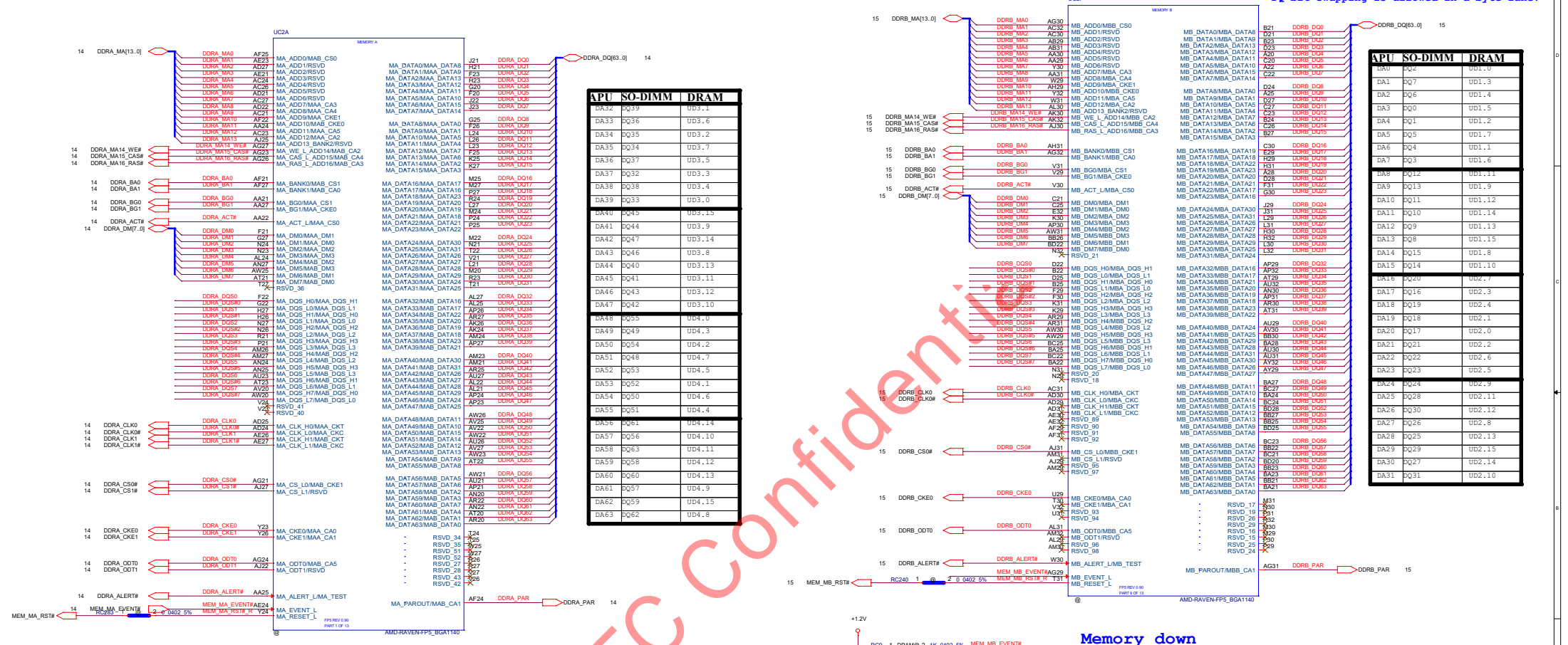
Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

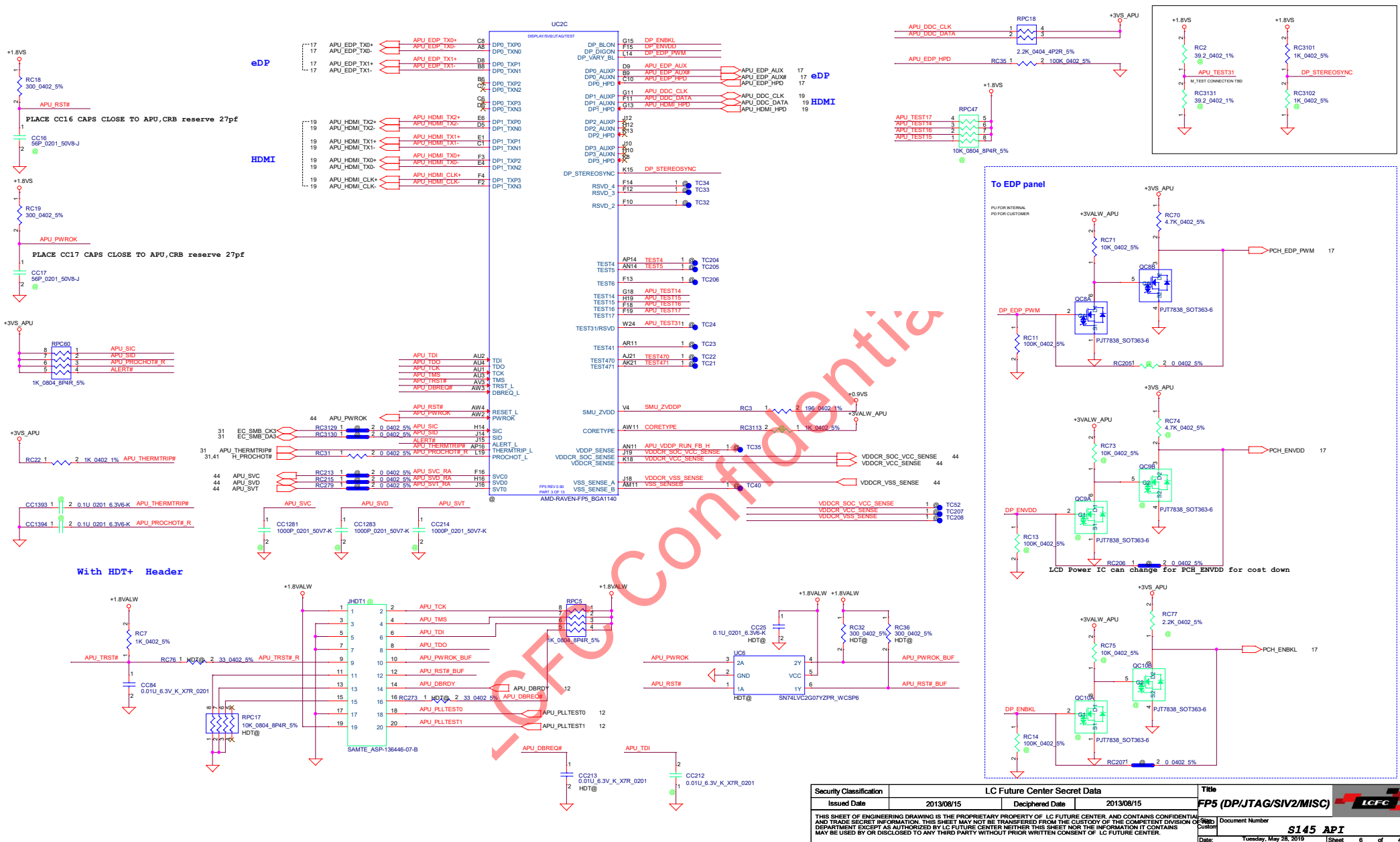
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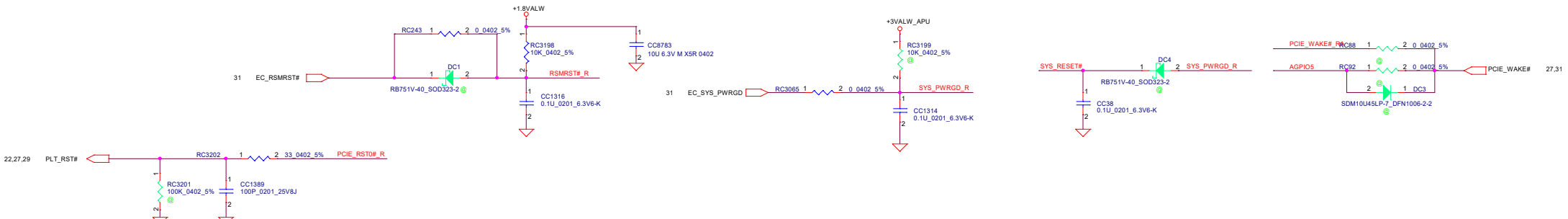
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Title			
FP5 (PCIE SATA I/F)			
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Date:	Tuesday, May 28, 2019	Sheet	4 of 44

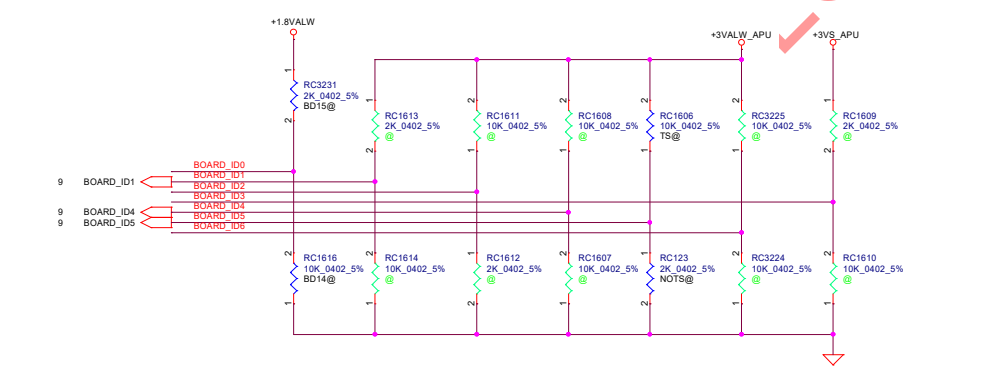
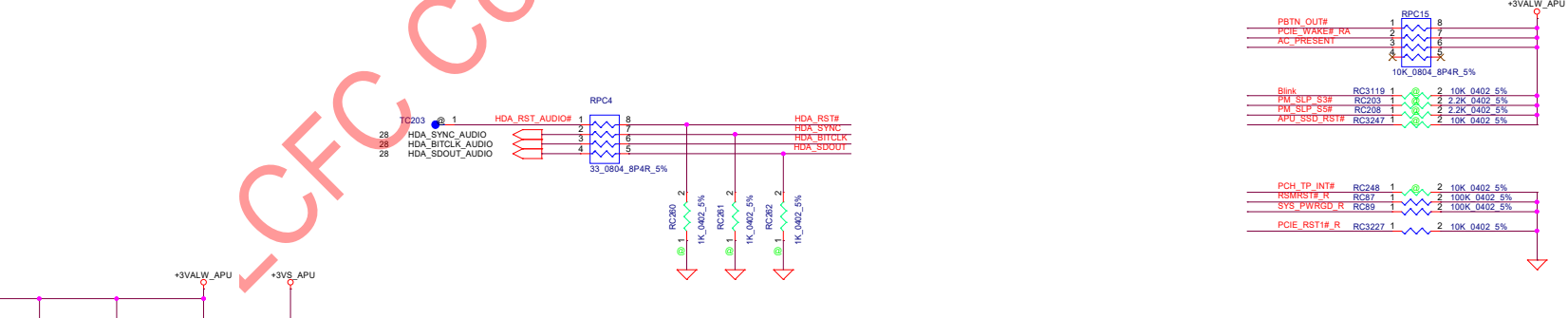
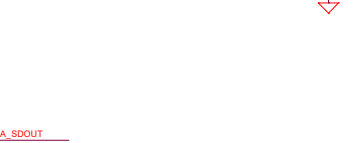
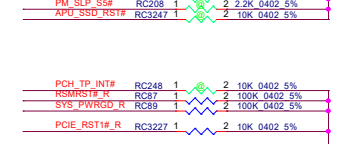
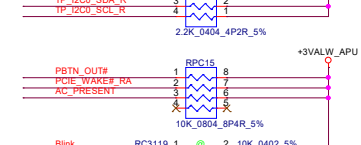
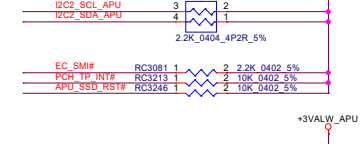
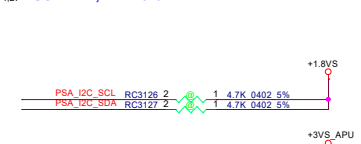
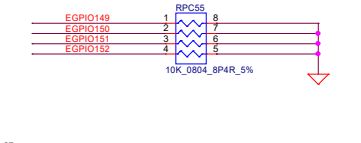
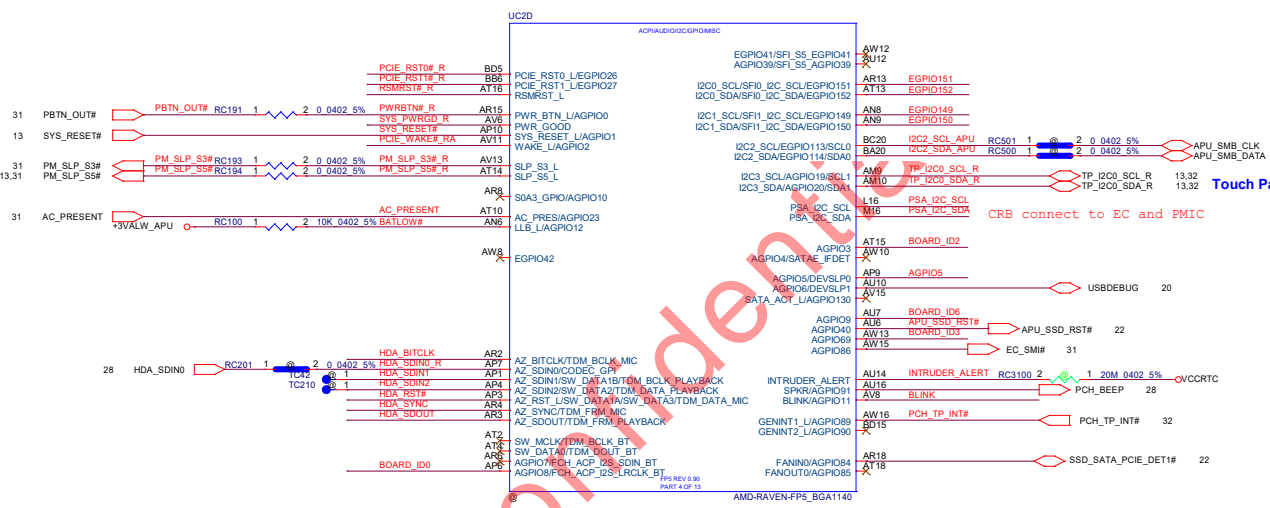




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Date:	Tuesday, May 28, 2019	Sheet	6	of	44

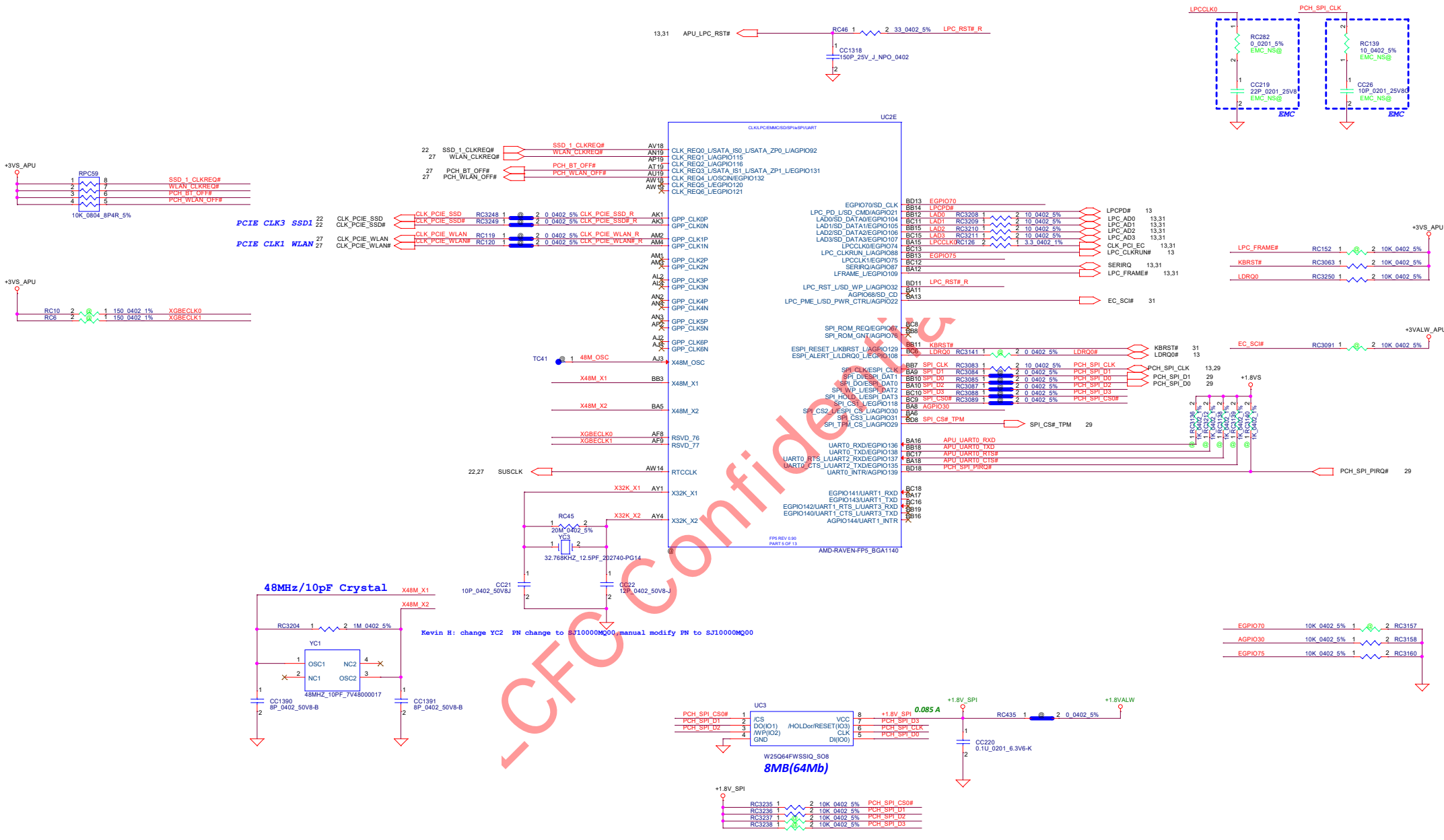


Board ID	Description	Stuff R
Board_ID0	0	14
	1	15
Board_ID1	0	Reserved
	1	Reserved
Board_ID [2,3,4]	000	Hynix 8Gb
	001	Micron 8Gb
	010	DIMM_ONLY
	011	Samsung 8Gb
	100	HT Micron 8Gb
	101	SMART 8Gb
Board_ID5	0	NON-TS
	1	TS
Board_ID6	0	Reserved
	1	Reserved

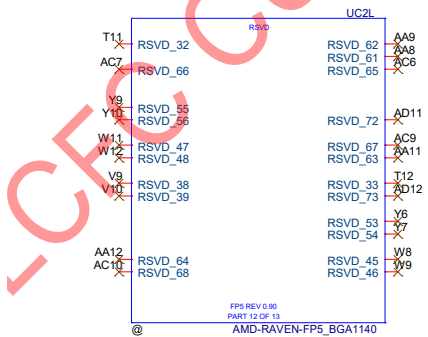
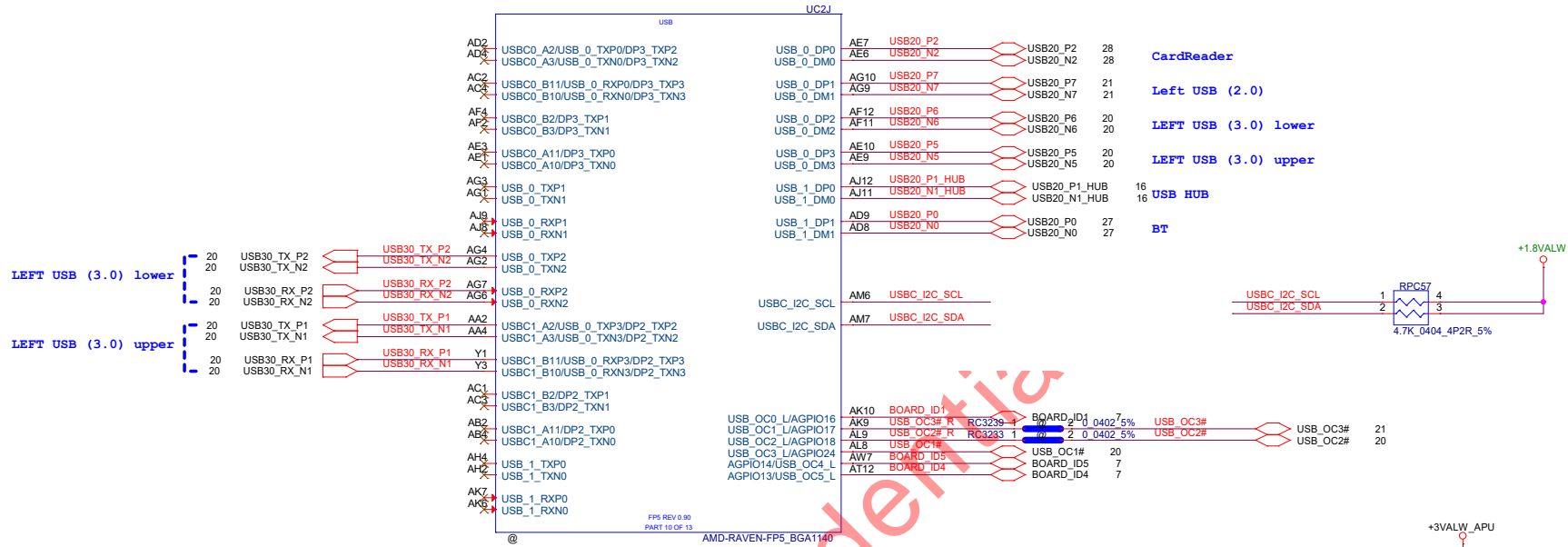


3/18 CC4220 stuff for S145API EMC request

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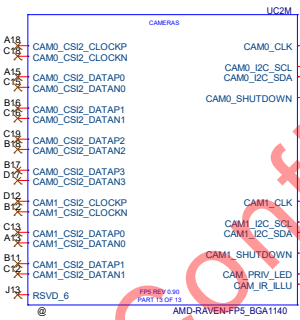


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	S145 API	V1.0	
Date	Tuesday, May 28, 2019	Sheet	8 of 44



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Size	Custom	Document Number	S145 API		Rev
Date:	Tuesday, May 28, 2019	Sheet	9	of	44

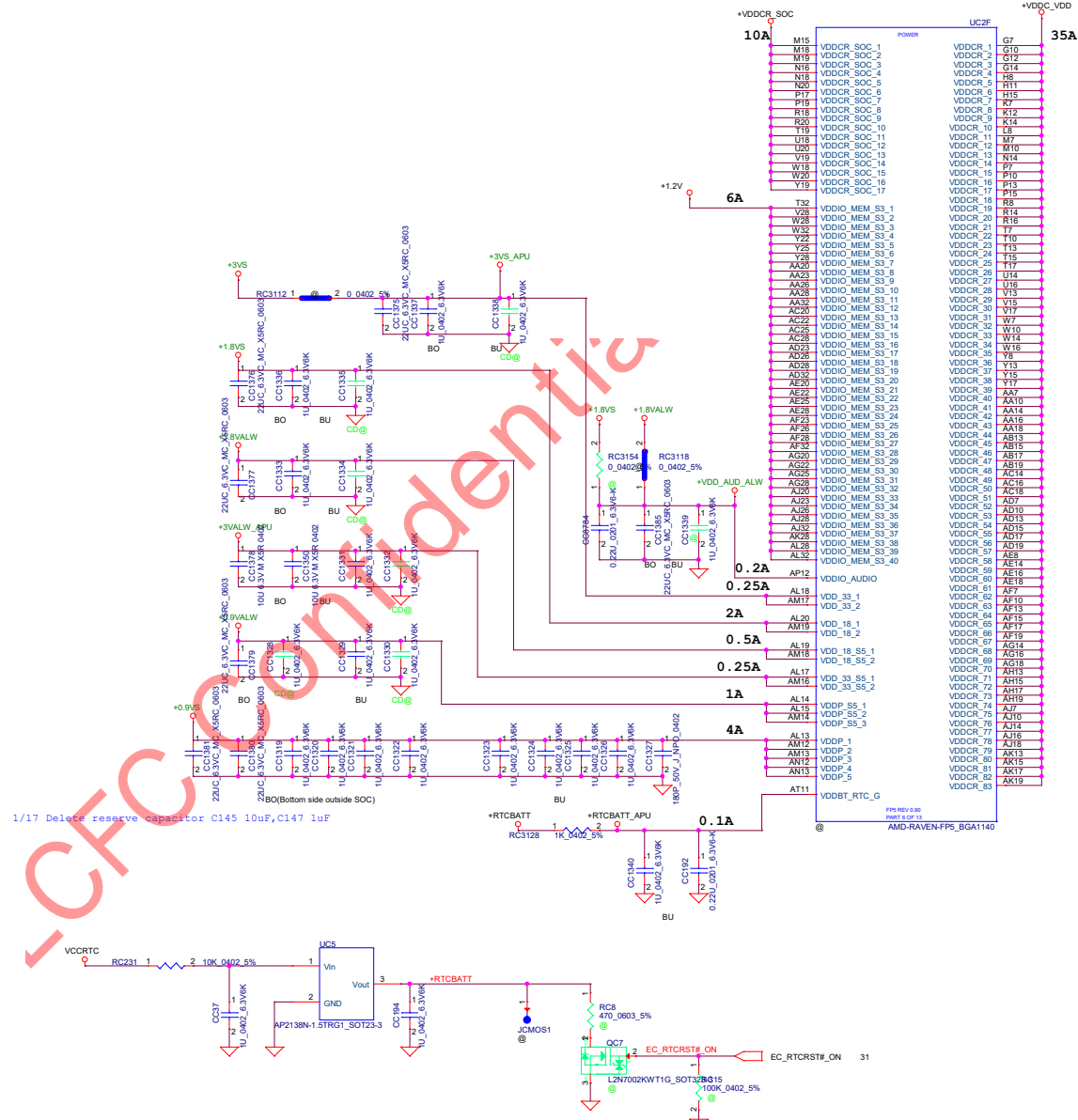
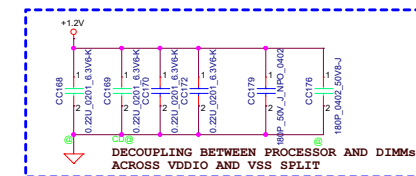
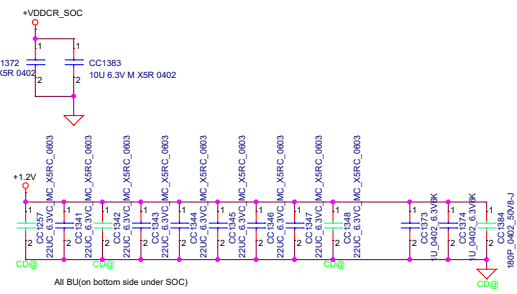
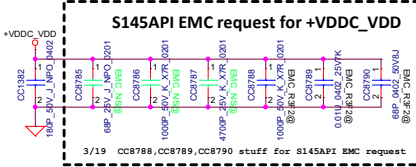
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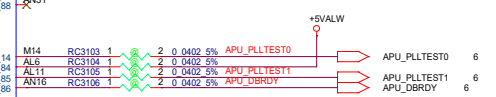
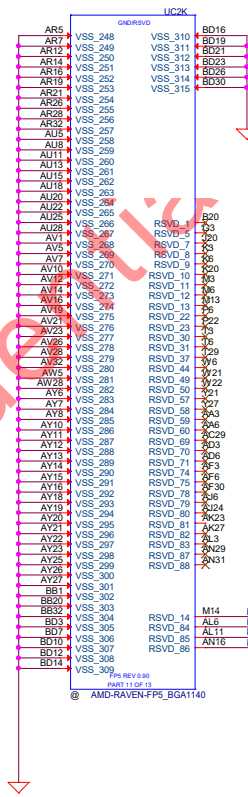
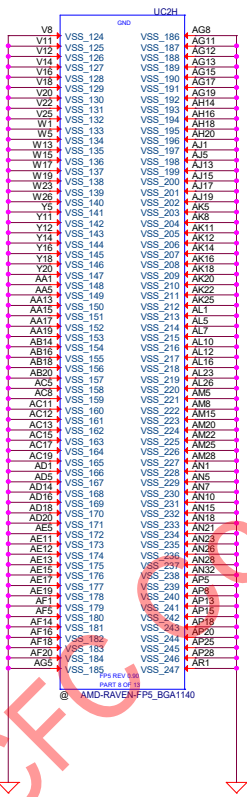
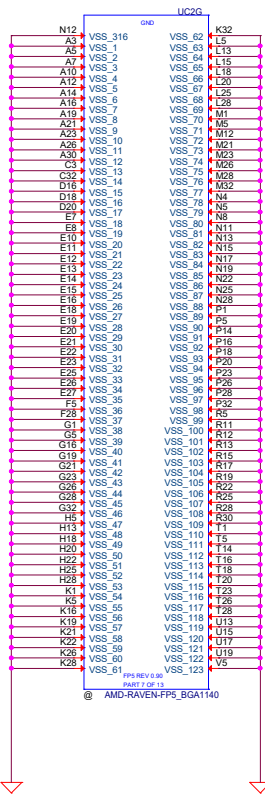


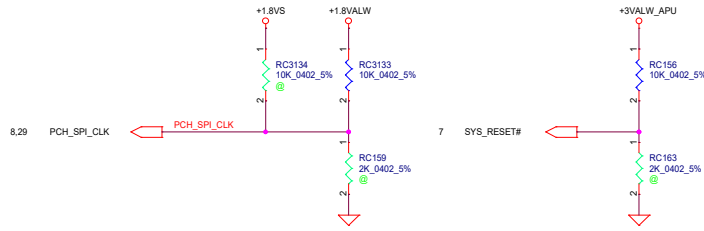
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					S145 API
				Date:	Tuesday, May 28, 2013
				Sheet	10 of 44
				Rev	1.0



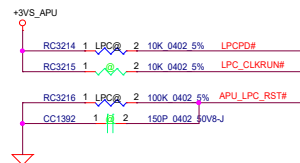
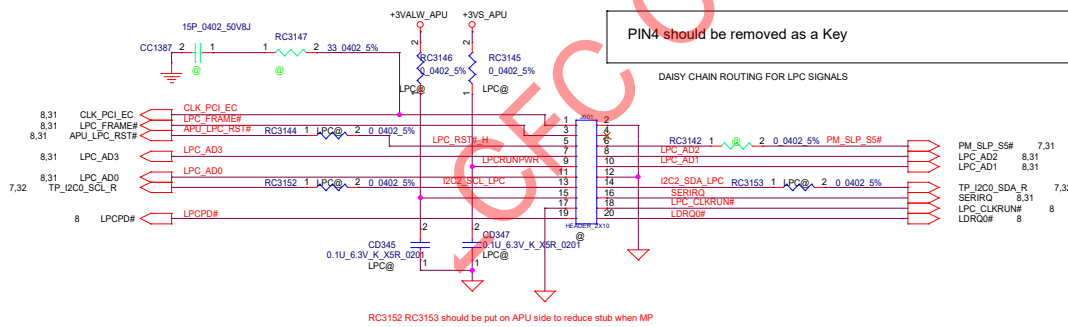




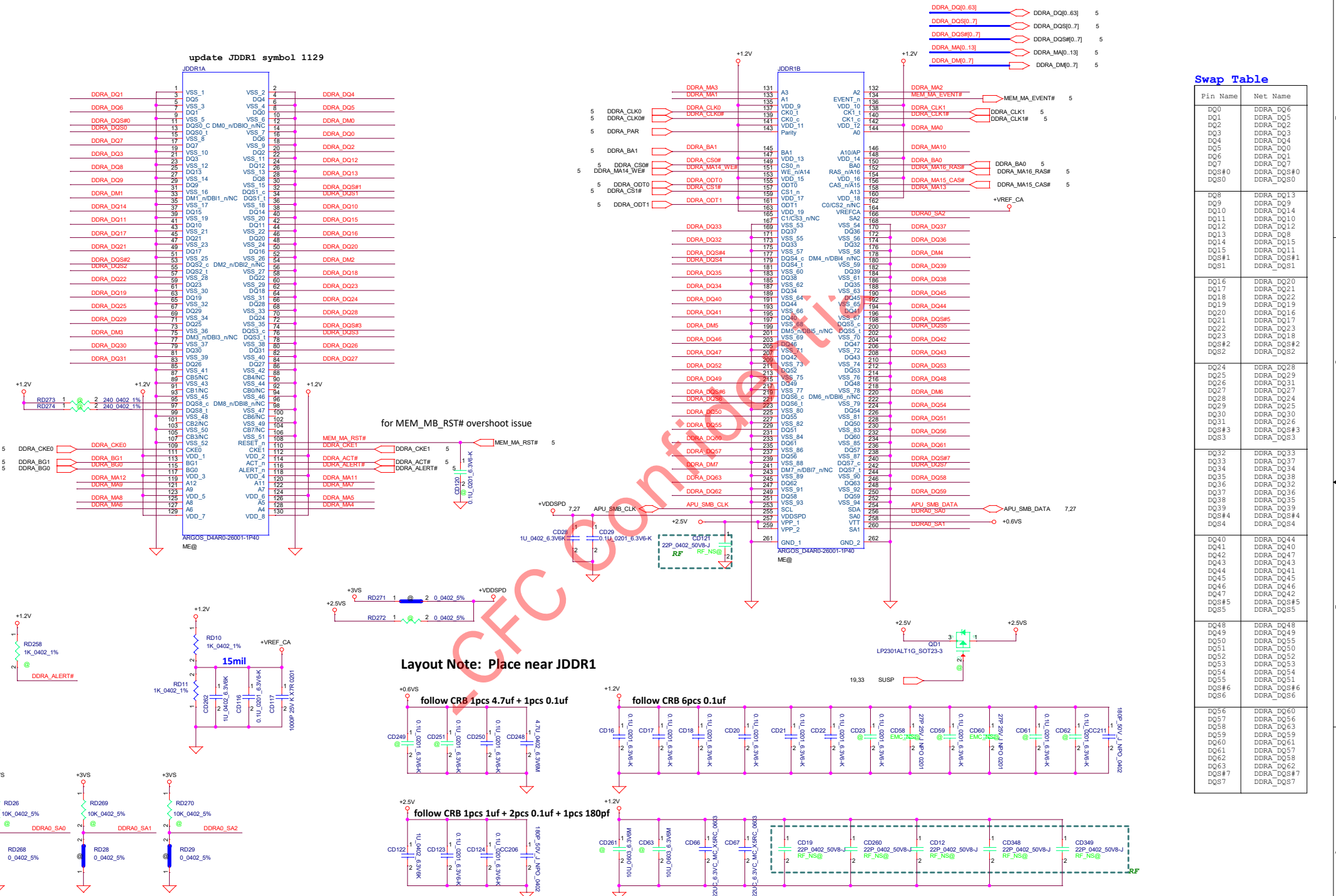


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

LPC ROM EMULATOR HEADER



update JDDR1 symbol 1129



Swap Table

Pin Name	Net Name
DQ0	DDR4_DQ0
DQ1	DDR4_DQ1
DQ2	DDR4_DQ2
DQ3	DDR4_DQ3
DQ4	DDR4_DQ4
DQ5	DDR4_DQ5
DQ6	DDR4_DQ6
DQ7	DDR4_DQ7
DQ8	DDR4_DQ8
DQ9	DDR4_DQ9
DQ10	DDR4_DQ10
DQ11	DDR4_DQ11
DQ12	DDR4_DQ12
DQ13	DDR4_DQ13
DQ14	DDR4_DQ14
DQ15	DDR4_DQ15
DQ16	DDR4_DQ16
DQ17	DDR4_DQ17
DQ18	DDR4_DQ18
DQ19	DDR4_DQ19
DQ20	DDR4_DQ20
DQ21	DDR4_DQ21
DQ22	DDR4_DQ22
DQ23	DDR4_DQ23
DQ24	DDR4_DQ24
DQ25	DDR4_DQ25
DQ26	DDR4_DQ26
DQ27	DDR4_DQ27
DQ28	DDR4_DQ28
DQ29	DDR4_DQ29
DQ30	DDR4_DQ30
DQ31	DDR4_DQ31
DQ32	DDR4_DQ32
DQ33	DDR4_DQ33
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DQ36	DDR4_DQ36
DQ37	DDR4_DQ37
DQ38	DDR4_DQ38
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DQ40	DDR4_DQ40
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DQ95	DDR4_DQ95
DQ96	DDR4_DQ96
DQ97	DDR4_DQ97
DQ98	DDR4_DQ98
DQ99	DDR4_DQ99
DQ100	DDR4_DQ100

Layout Note: Place near JDDR1

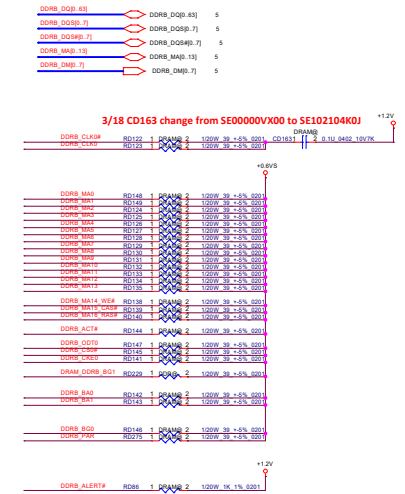
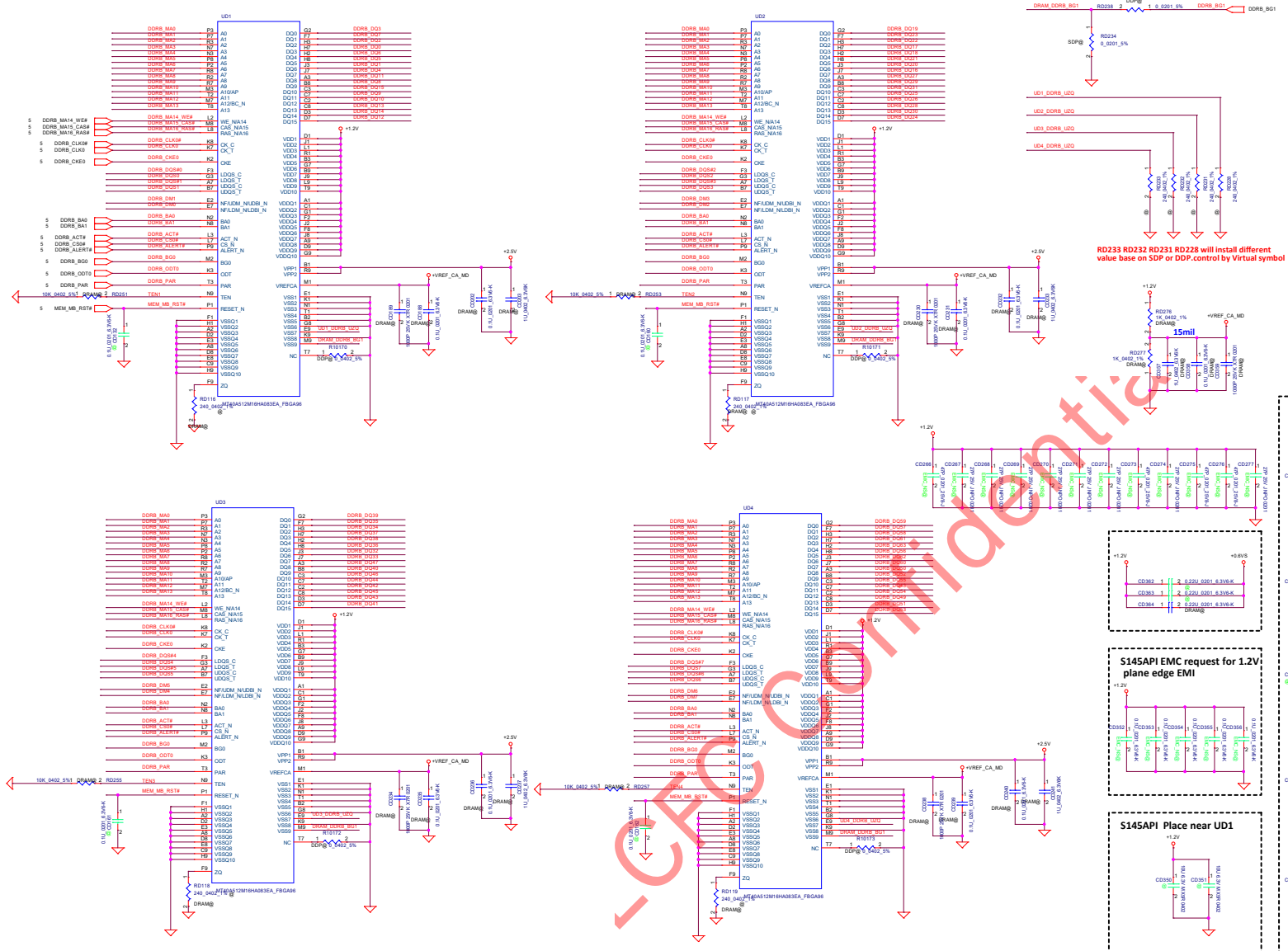
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follow CRB 6pcs 0.1uf

follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf

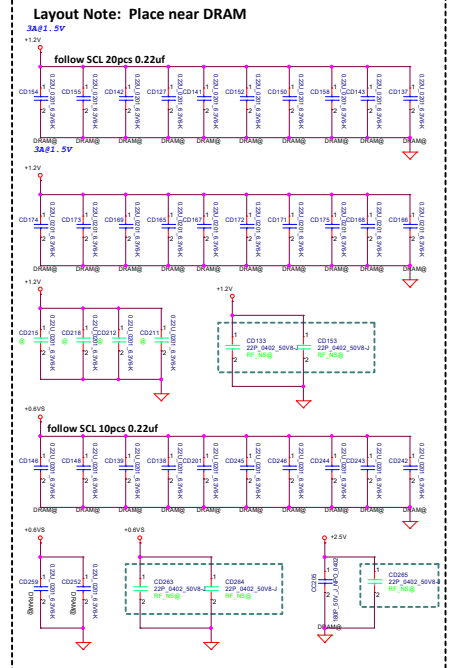
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Subj	Disruption Number	S145 API		Rev 1.0	
Date:	Tuesday, May 28, 2018	Sheet 14 of 44			



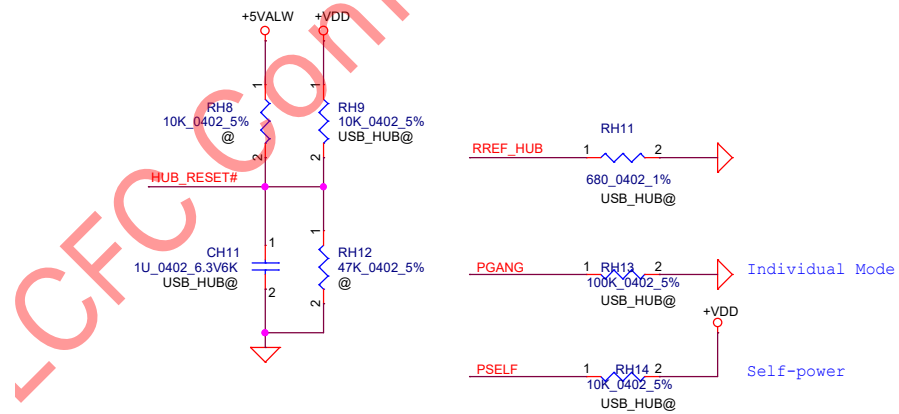
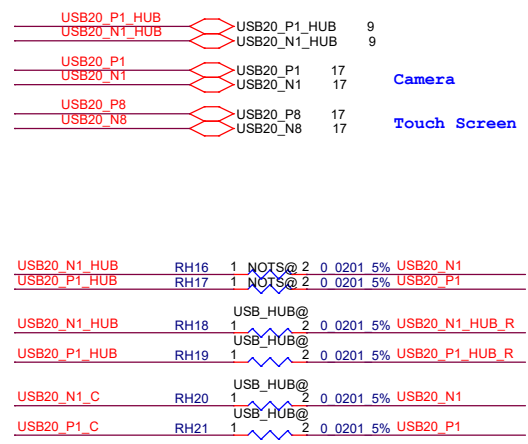
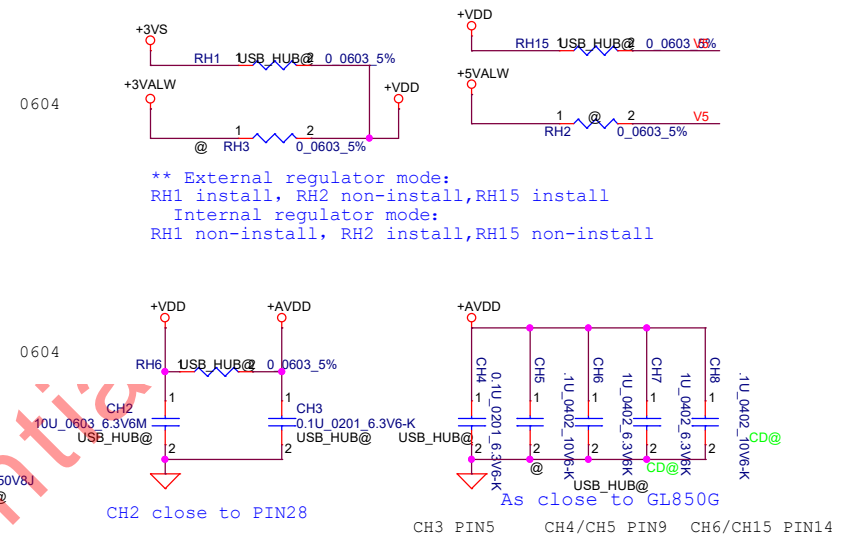
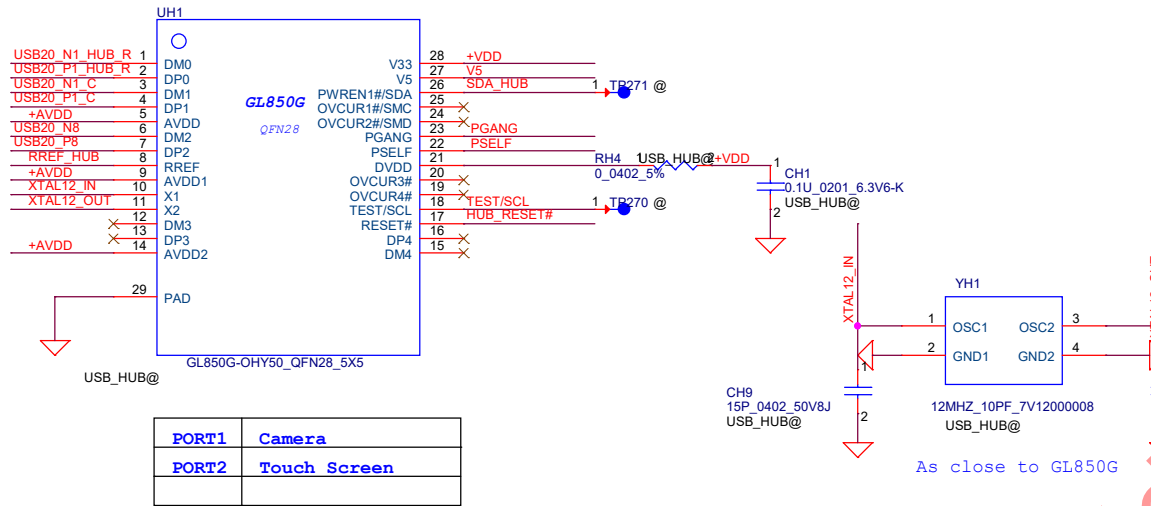
Swap Table


Pin Name	Mac Name
DQ0	DDR3_DQ0
DQ1	DDR3_DQ1
DQ2	DDR3_DQ2
DQ3	DDR3_DQ3
DQ4	DDR3_DQ4
DQ5	DDR3_DQ5
DQ6	DDR3_DQ6
DQ7	DDR3_DQ7
DQ8	DDR3_DQ8
DQ9	DDR3_DQ9
DQ10	DDR3_DQ10
DQ11	DDR3_DQ11
DQ12	DDR3_DQ12
DQ13	DDR3_DQ13
DQ14	DDR3_DQ14
DQ15	DDR3_DQ15
DQ16	DDR3_DQ16
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DQ28	DDR3_DQ28
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DQS2	DDR3_DQS2
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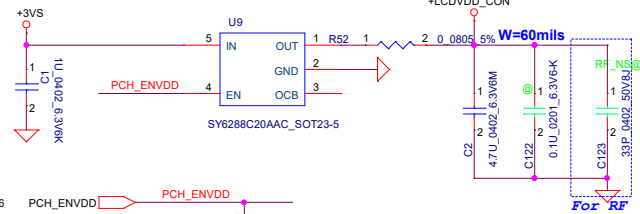
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for USB HUB update to OHY50, manual modify PN to GL850G-OHY50

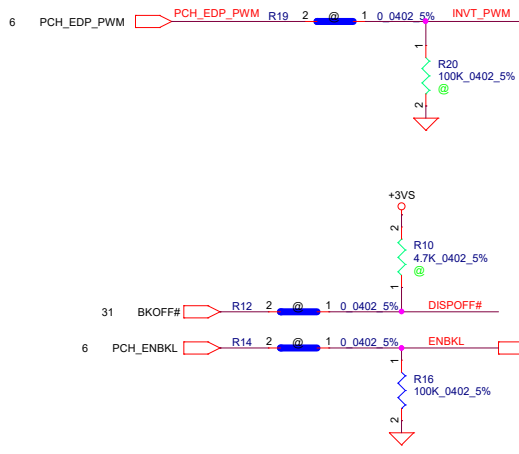


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				Rev 1.0 Sheet 16 of 44

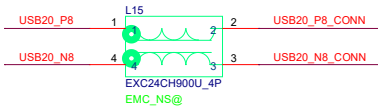
LCD POWER CIRCUIT



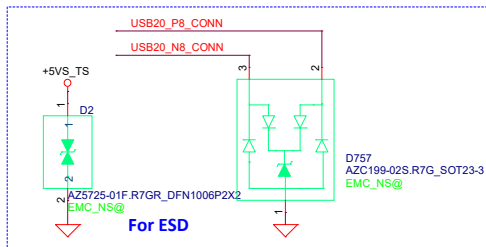
APU output enable Voh min is 1.8V-0.45V=1.35V



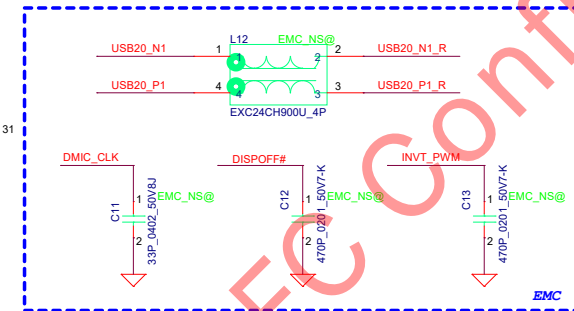
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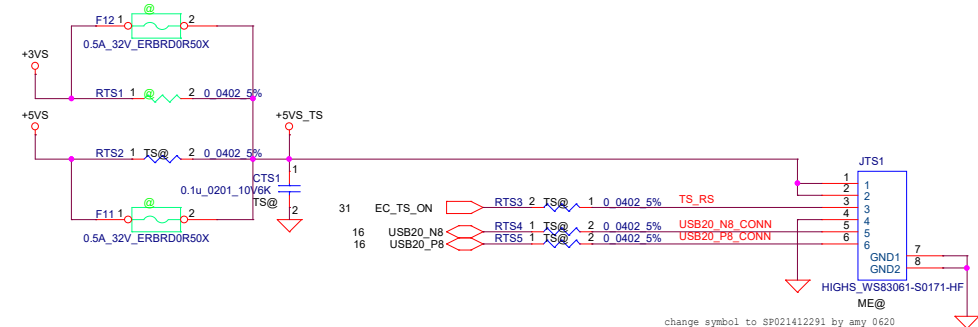
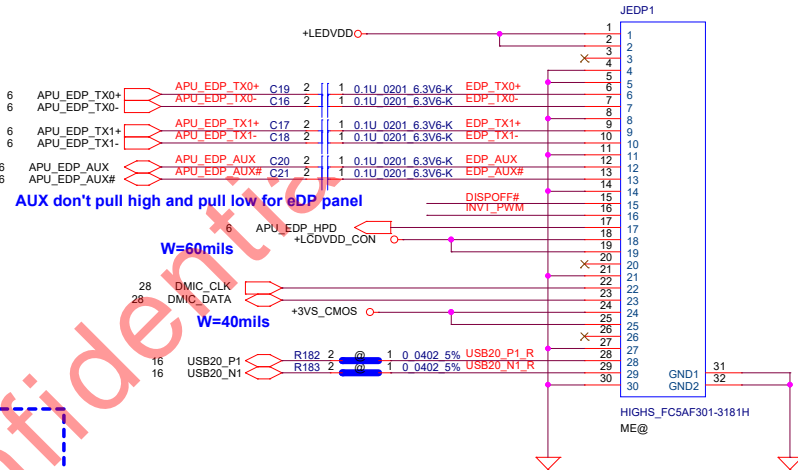
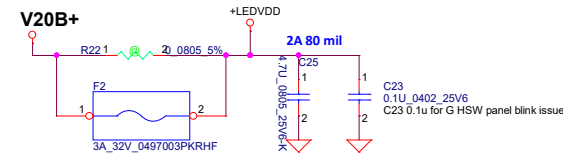
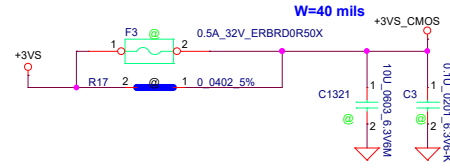
For EMI



CMOS Camera




B+ to +LEDVDD POWER

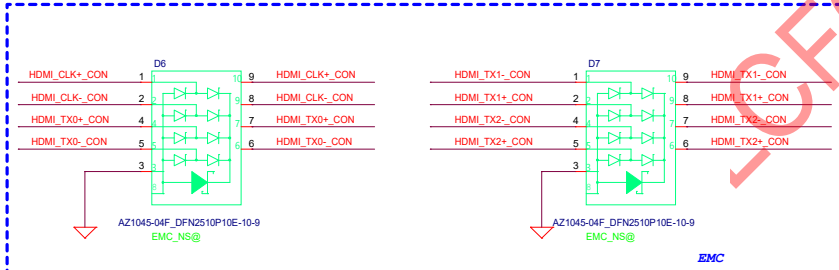
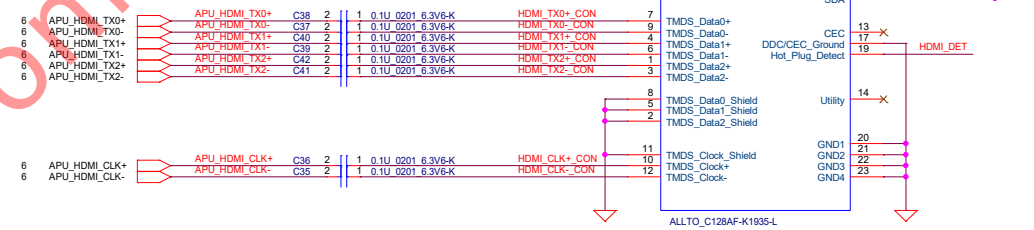
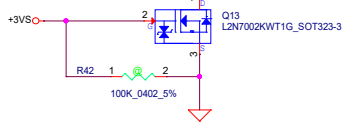
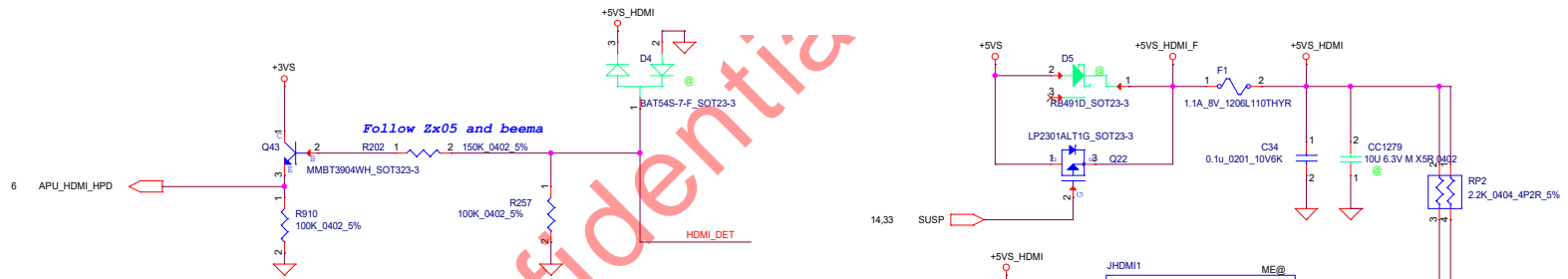
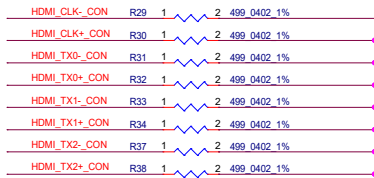
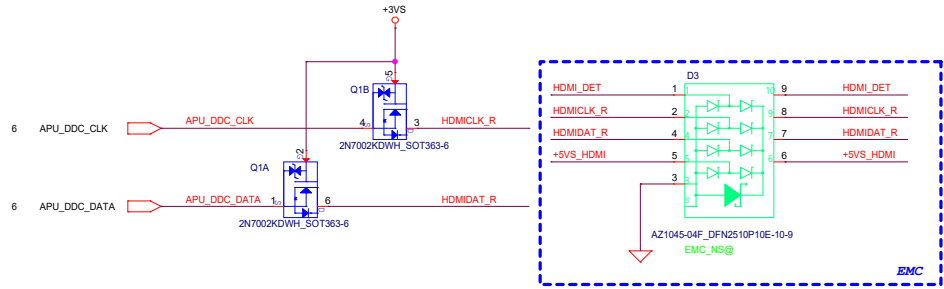
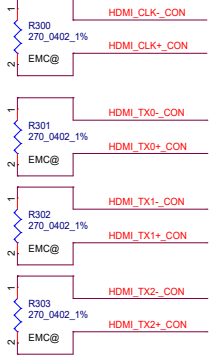


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Size	Document Number	Date				Tuesday, May 28, 2019		Sheet	17 of 44
Custom	S145 API	Rev		1.0					

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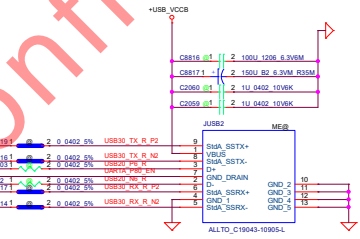
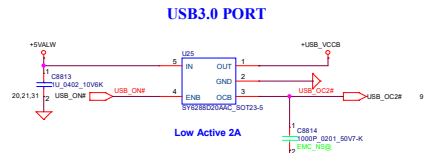
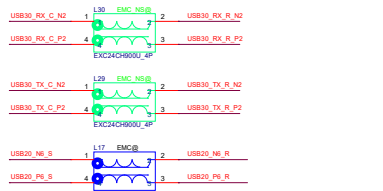
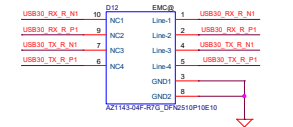
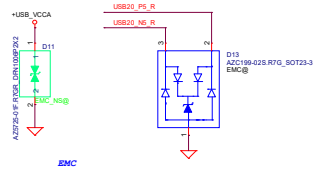
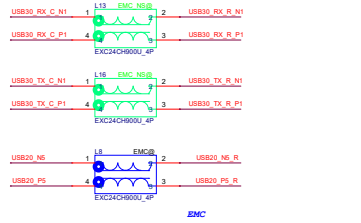
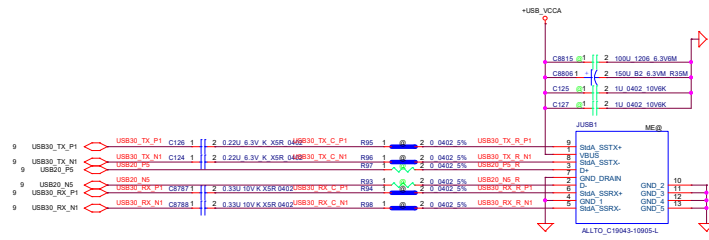
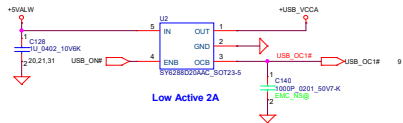
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3/19 S145API EMC request for HDMI

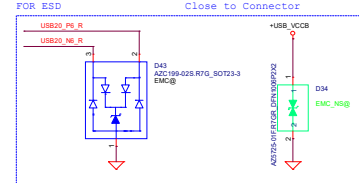
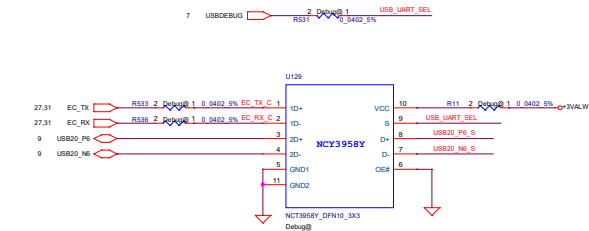


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Date:	Tuesday, May 28, 2010	Sheet	19	of 44

LEFT SIDE USB3.0 PORT x2



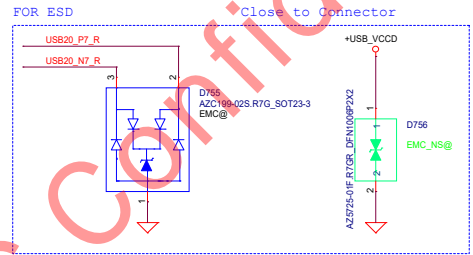
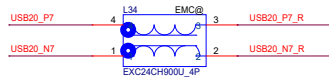
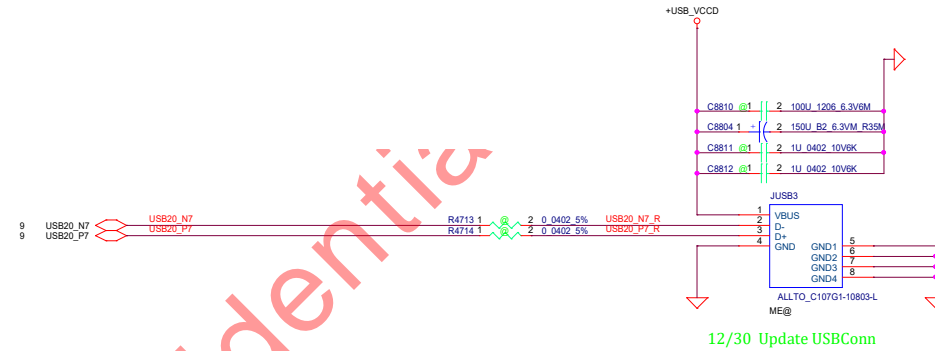
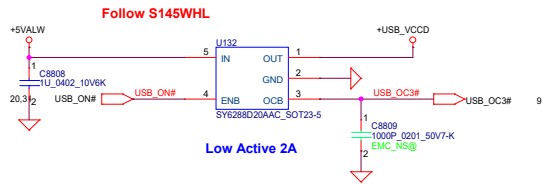
For USB Debug Function



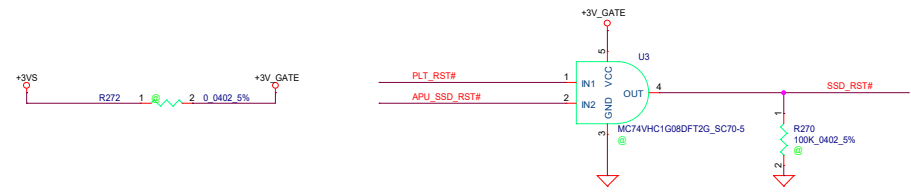
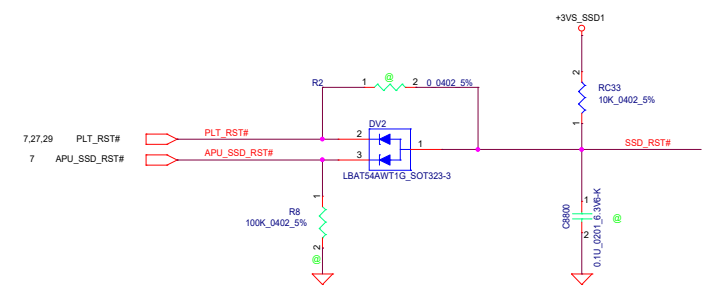
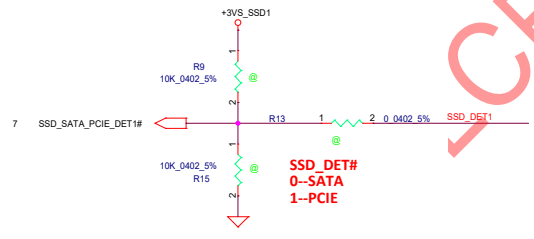
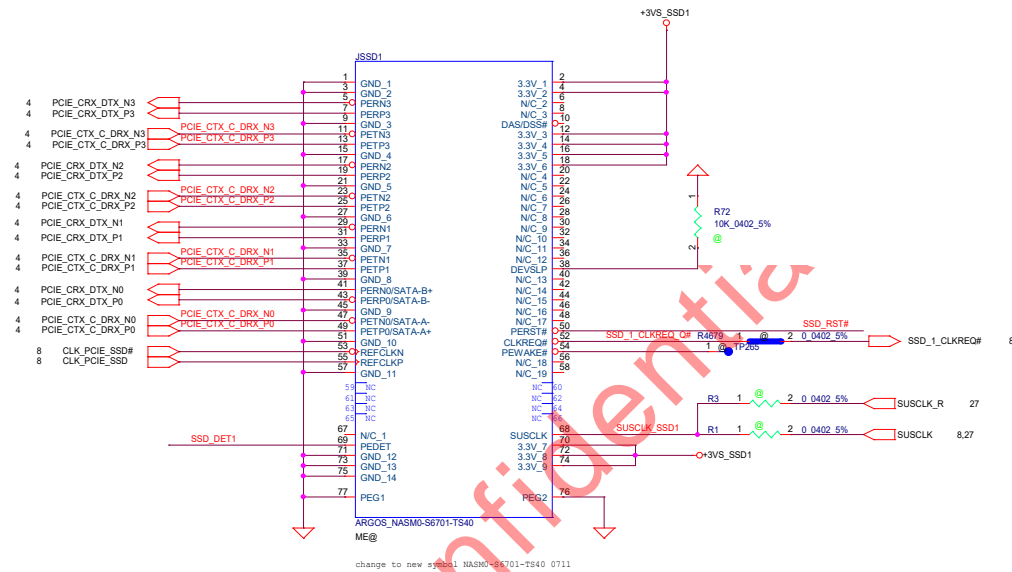
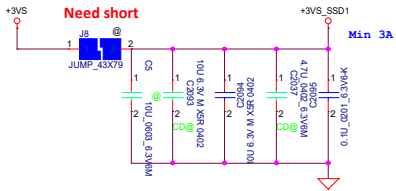
USBDEB	Kernel debug
Set Logpt	Set Logpt
Set Output Low	ENABLE

JART_A_P80_EN	POST 80
Set Logpt	DISABLE
Set Output Low	ENABLE


DE#	S	FUNCTION
H	0	DISABLE
L	1	DI4(+/-) to DI4(+/-)
L	0	DI4(+/-) to DI4(+/-)




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			Date: Tuesday, May 28, 2019	Sheet 21 of 44



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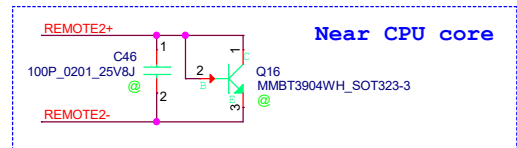
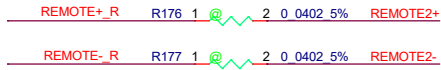
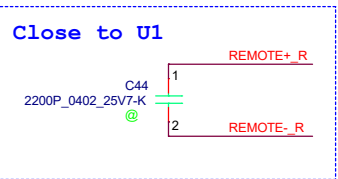
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				Date:	Tuesday, May 28, 2019	Sheet 24 of 44

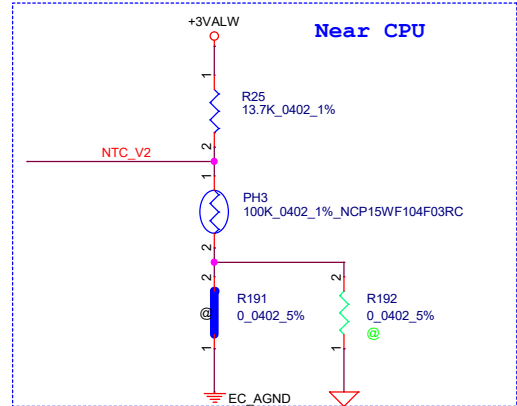
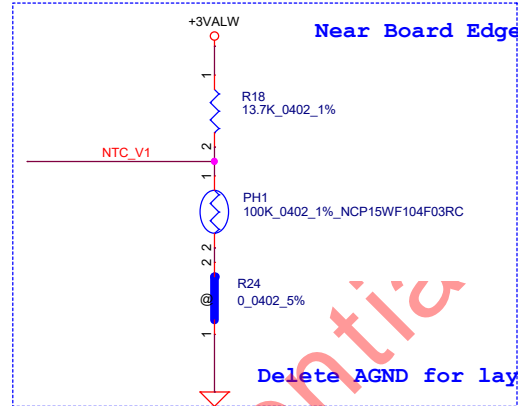
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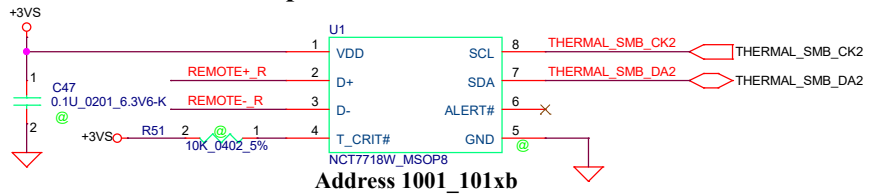
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Date:	Tuesday, May 28, 2019	Sheet	25 of 44
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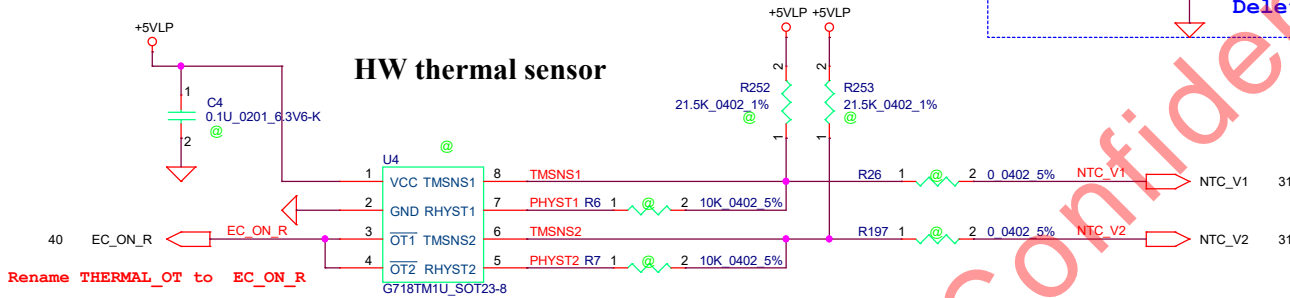
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



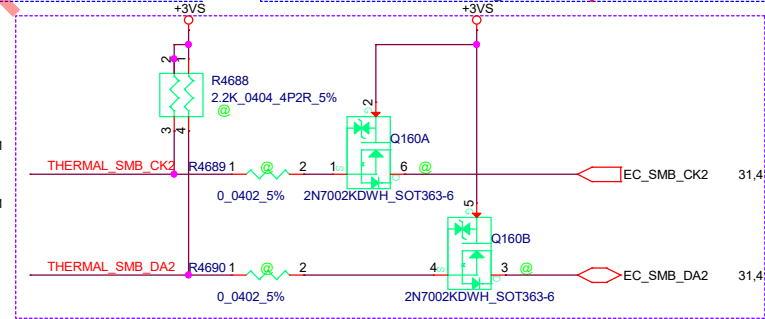
SMSC thermal sensor placed near DIMM



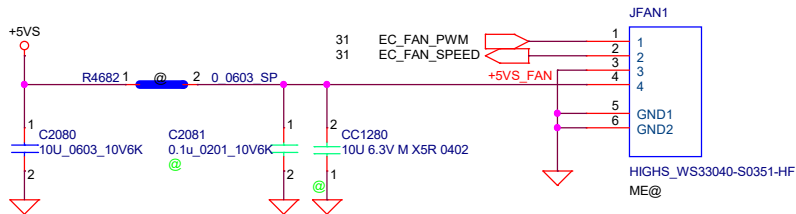
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

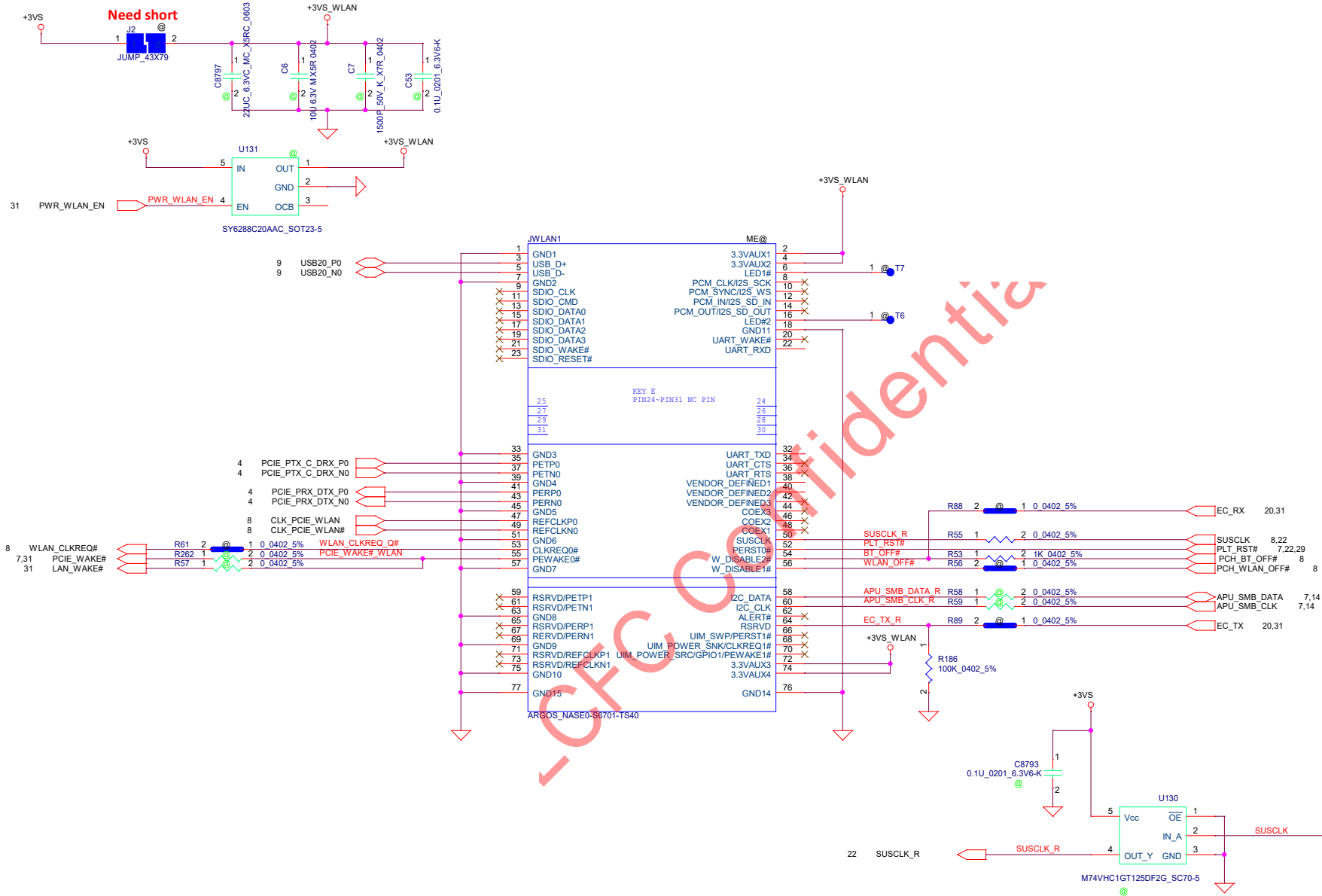


FAN Conn



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Date:	Tuesday, May 28, 2019	Sheet	26	of	44	

Mini-Express Card(WLAN/WiMAX)



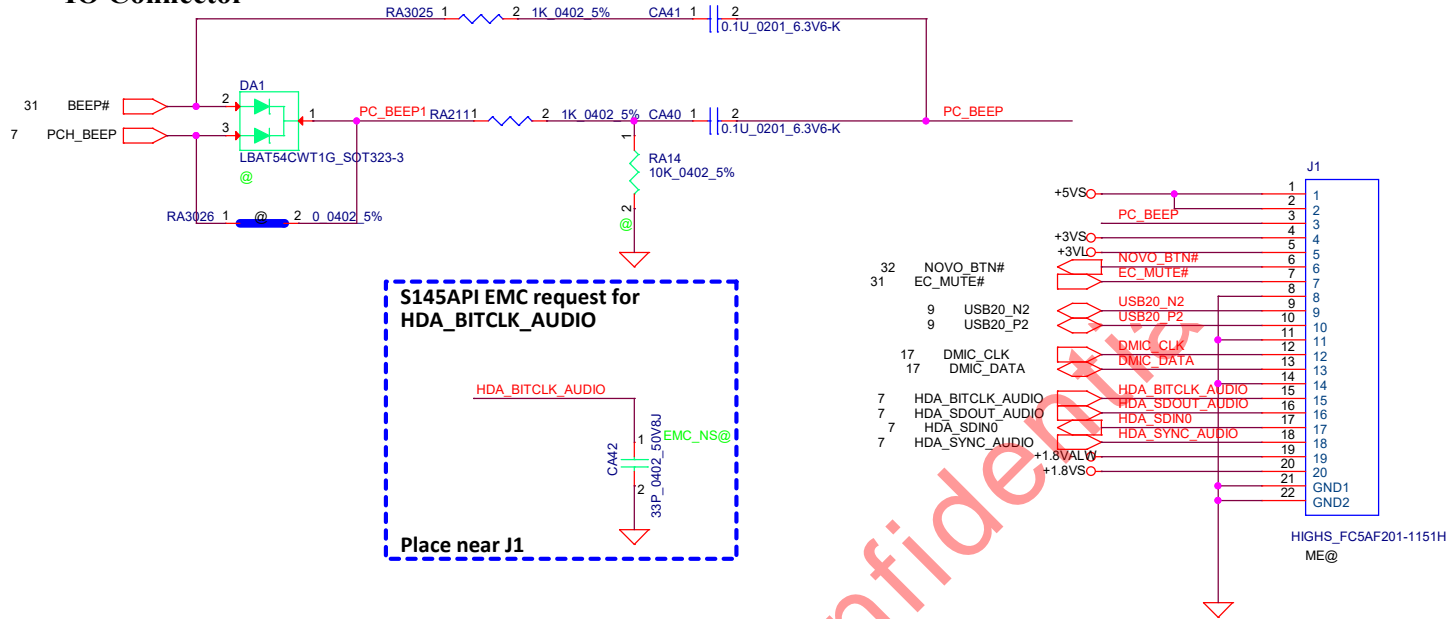
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Title	
NGFF WLAN	

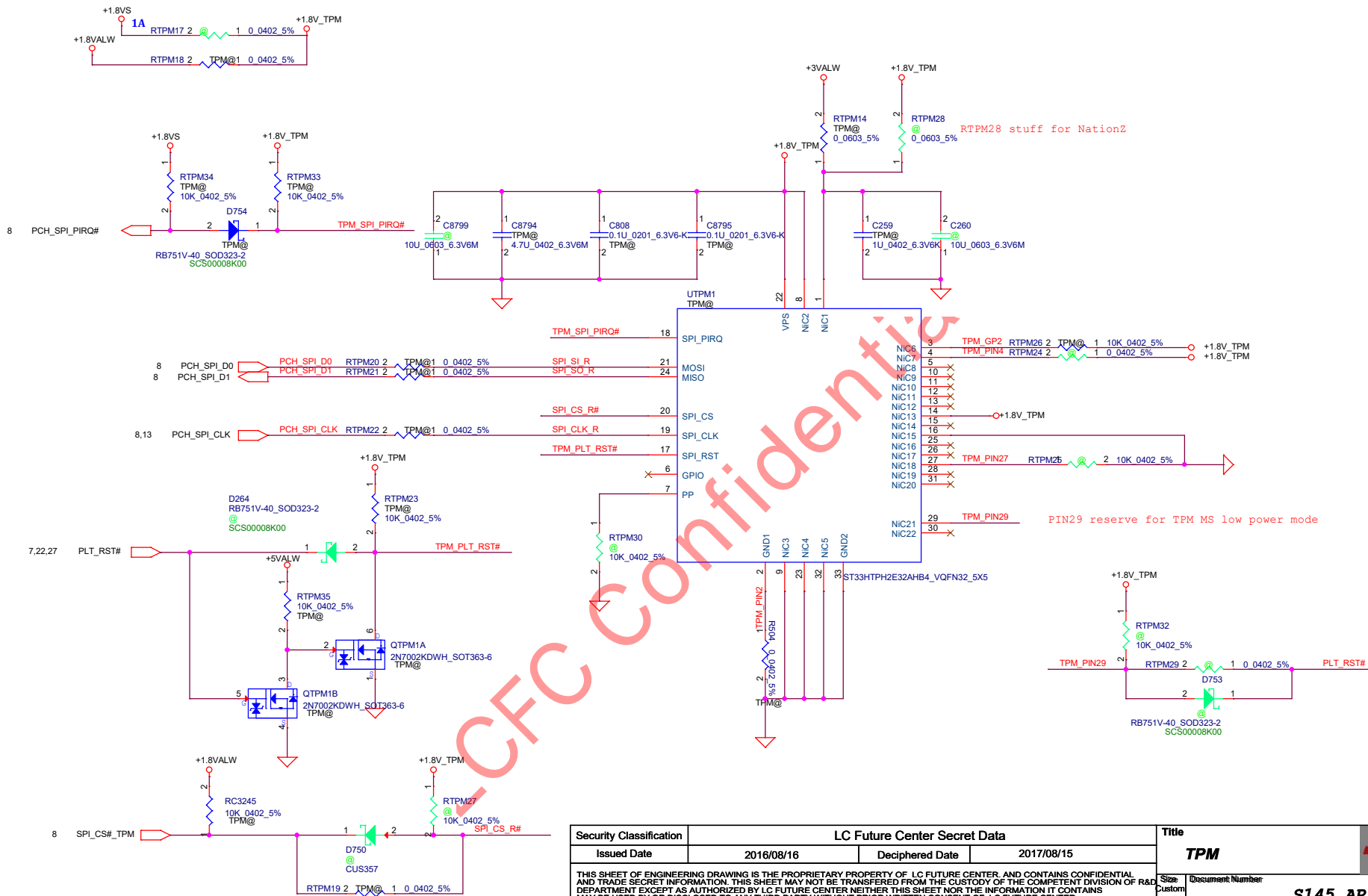
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IO Connector




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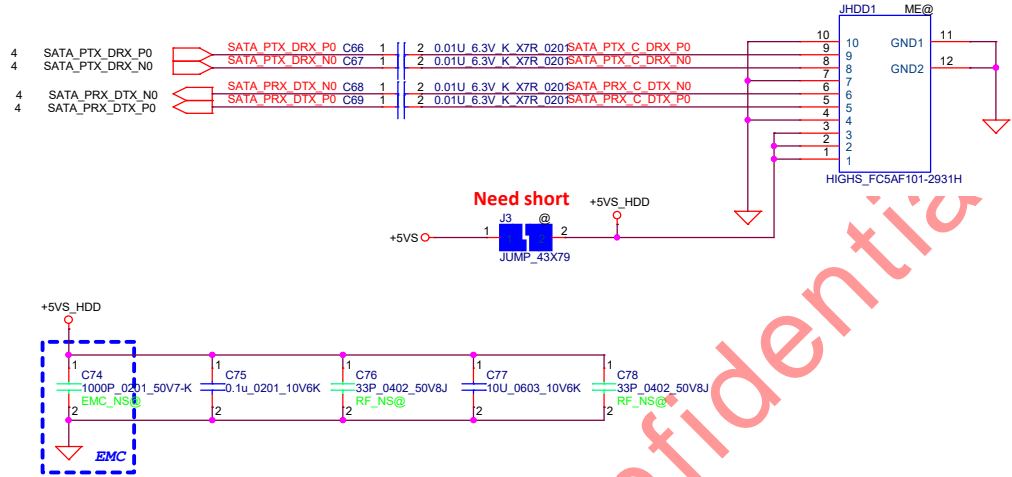
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2016/08/16	Deciphered Date	2017/08/15	IO CONN		
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					S145 API	1.0
				Date:	Tuesday, May 28, 2019	Sheet 28 of 44



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Issued Date	2016/08/16	Deciphered Date	2017/08/15		
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Title		
TPM		
Size	Document Number	S145 API
Custom		
Date	Tuesday, May 28, 2019	Sheet 29 of 44
Rev	1.0	

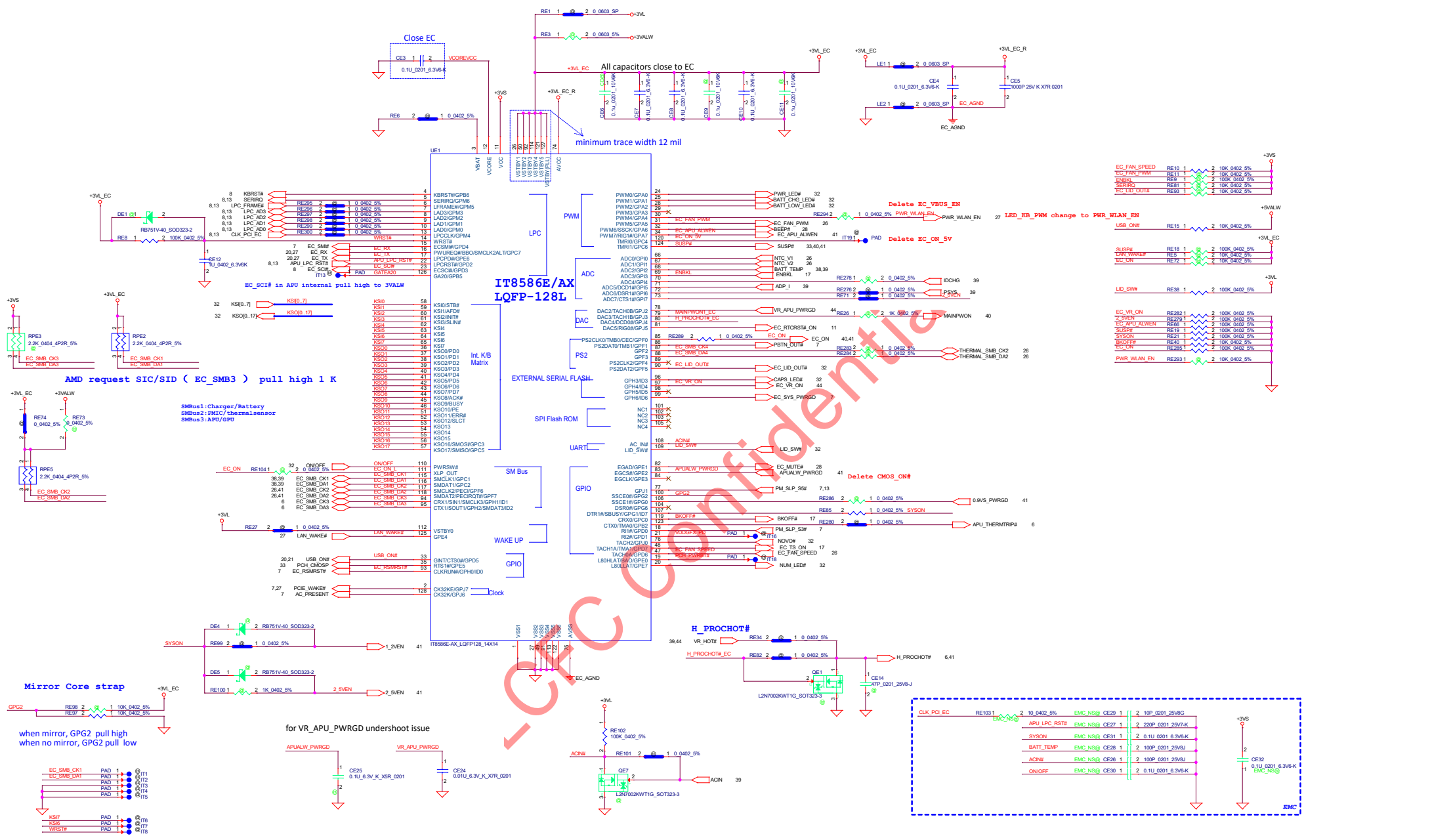
SATA HDD Conn.



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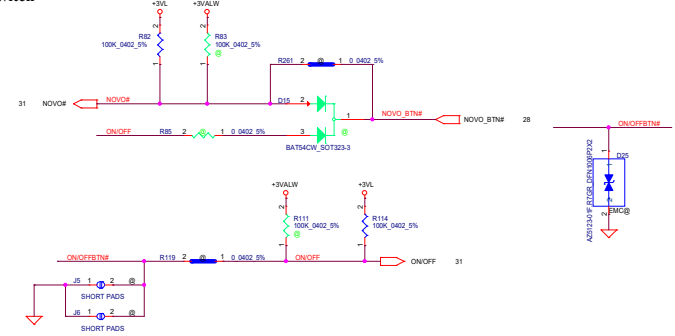
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HDD CONN		
Size	Document Number	Rev
Custom	S145 API	1.0
Date:	Tuesday, May 28, 2019	Sheet 30 of 44



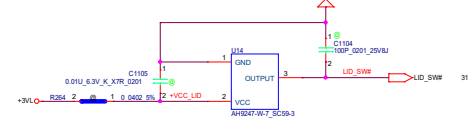
Reserve Factory EC flash, need confirm with ITE

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Page	31	Document Number	S145 API	Rev
Date	Tuesday, May 28, 2019	Sheet	31	of 44

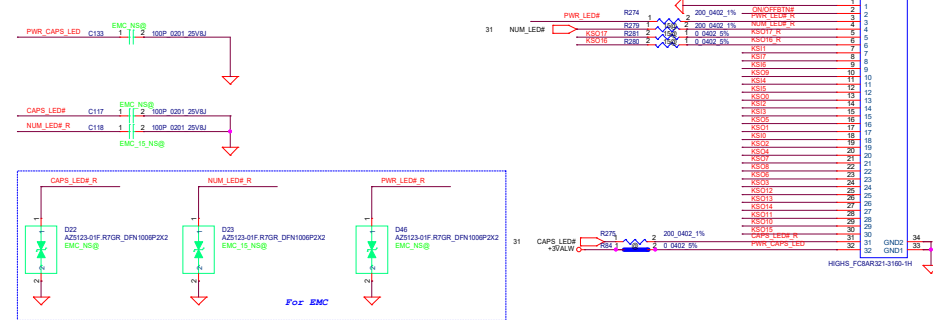
ON/OFF switch



LID switch



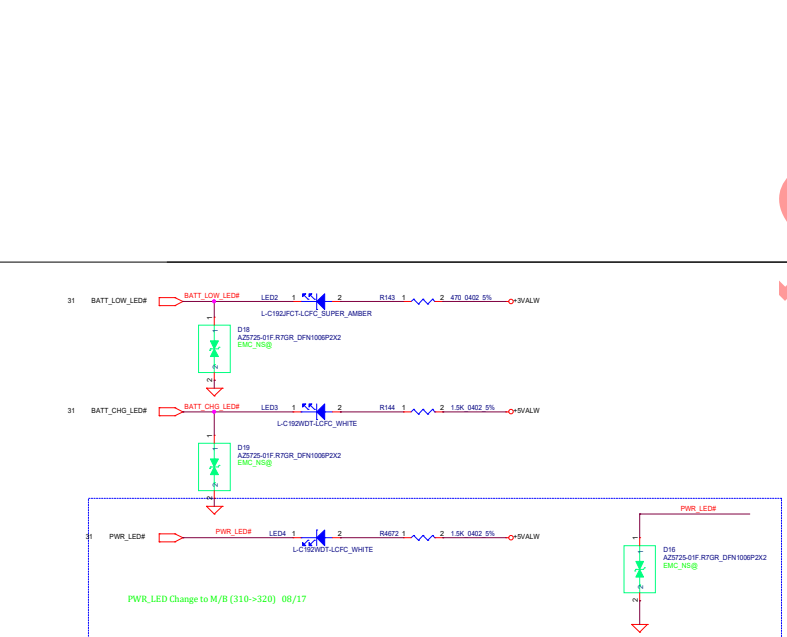
K/B Connector



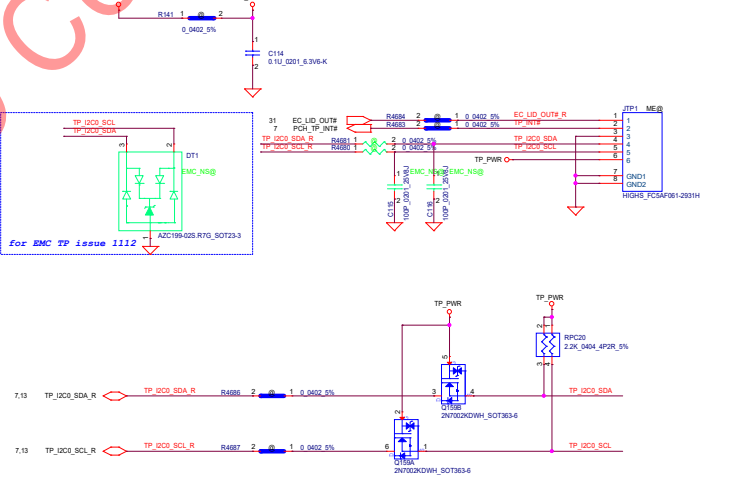
KB Backlight Connector



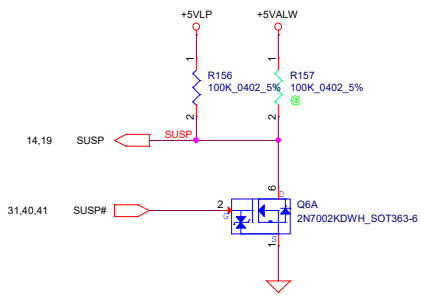
Finger Print Connector



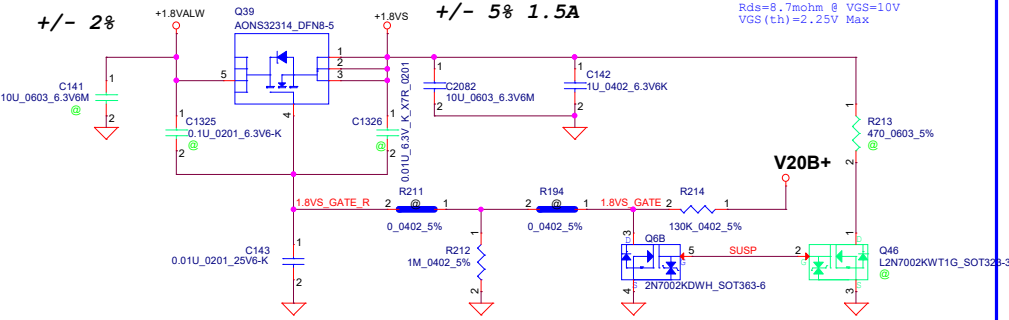
TP/B Connector



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Issued Date	2016/08/16	Deciphered Date	2017/08/15	KBD/PWR/IO/LED/TP Conn. ICFC	
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Size	Custom	Document Number	S145 API	Rev	1.0
Date	Tuesday, May 28, 2019	ISheet	32	of	44



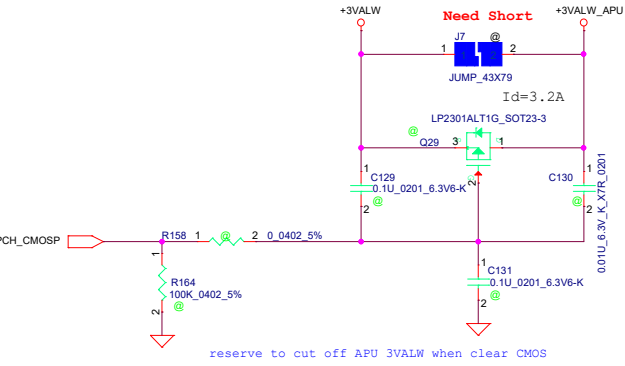
+1.8VALW to +1.8VS



AONS32314
 VDS=30V VGS=20V, ID=32A,
 Rds=6.7mohm @ VGS=10V
 VGS(th)=2.25V Max

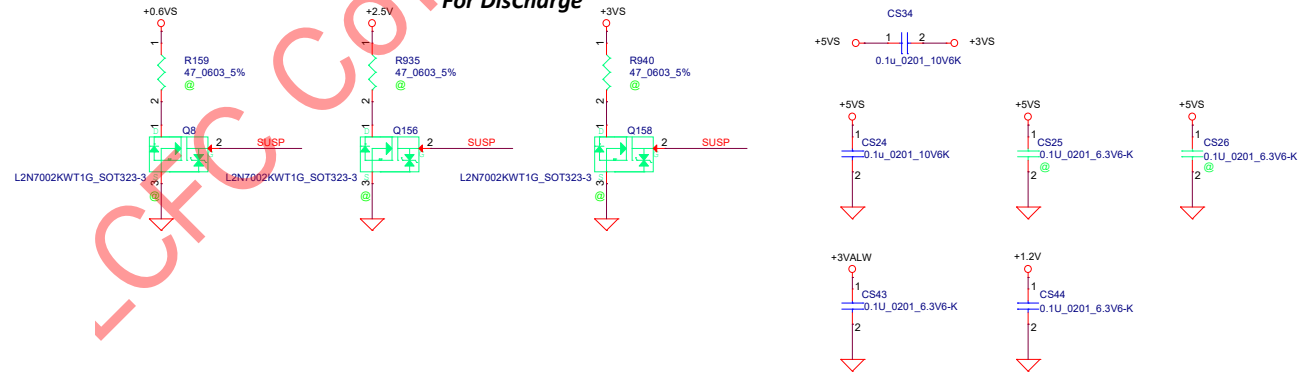
20VSB will change to 6V in DC mode, careful the Res divide voltage

+3VALW to +3VALW_APU



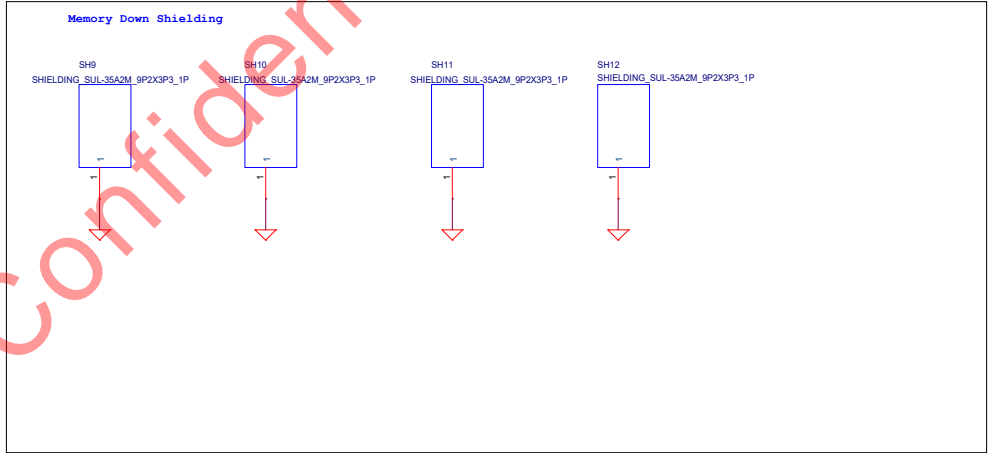
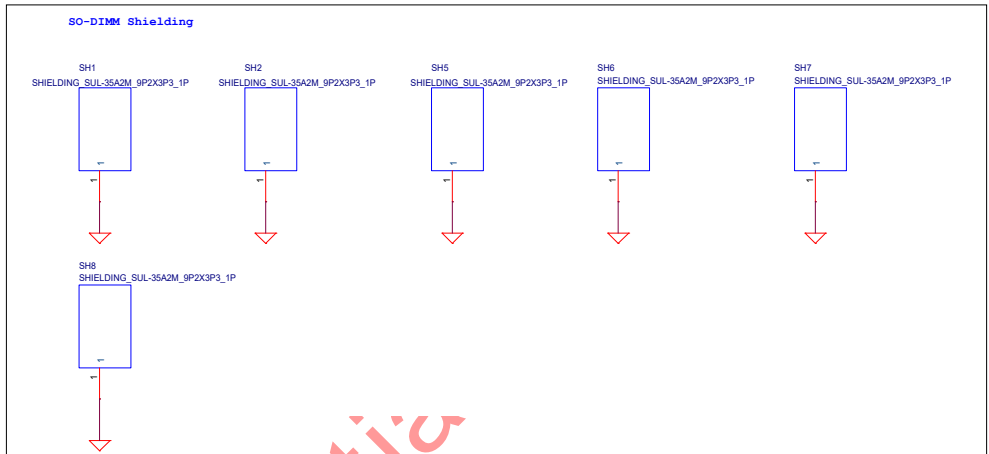
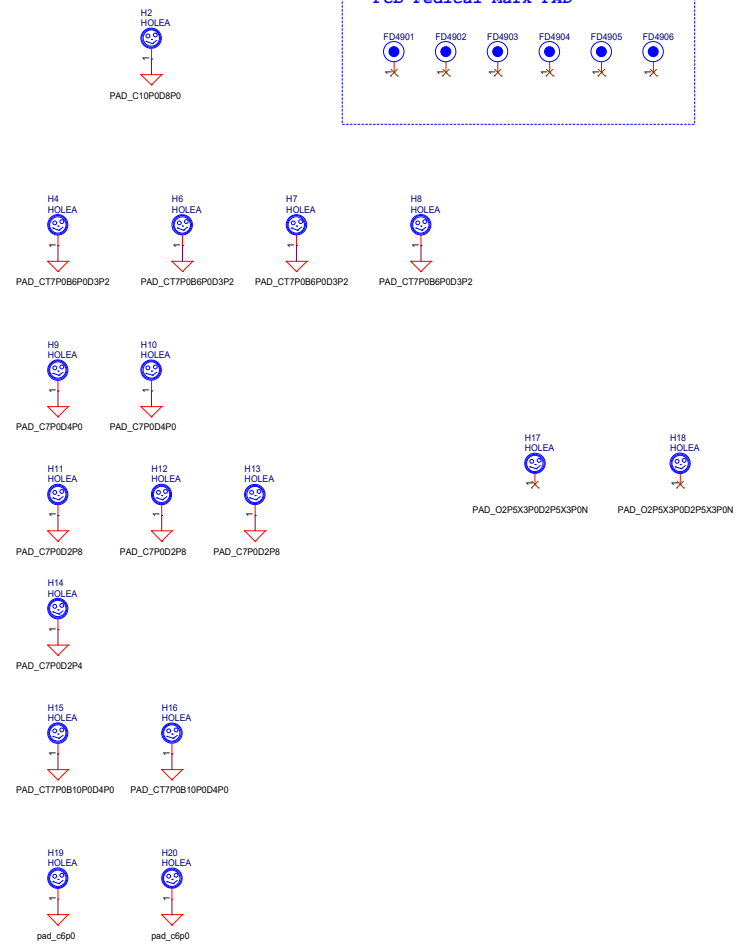
reserve to cut off APU 3VALW when clear CMOS

For DisCharge



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		S145 API	1.0	
Date:	Tuesday, May 28, 2019	Sheet	33	of 44


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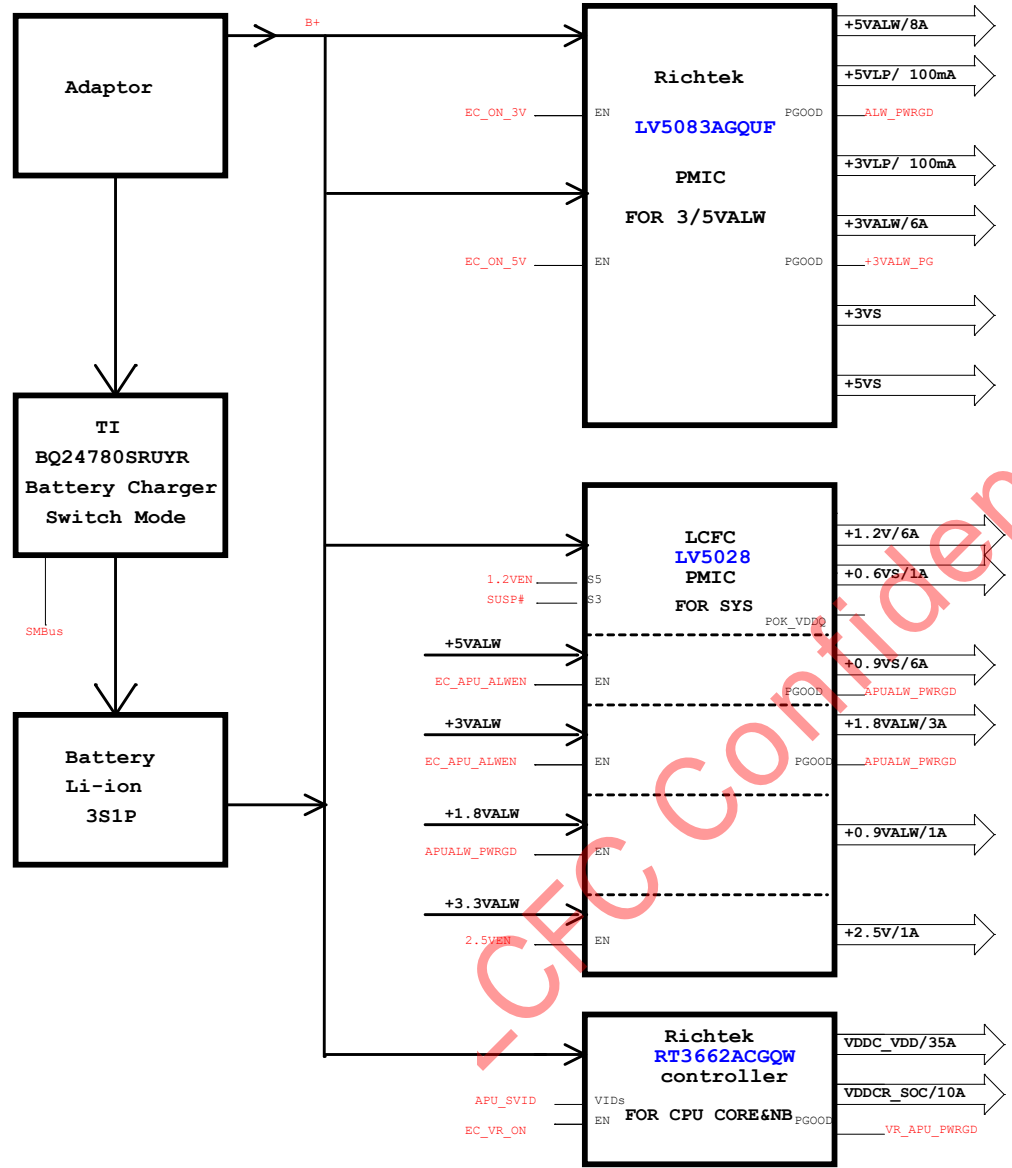
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Hole	
2013/08/08		2013/08/05		LCFC	
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Size	Document Number	S145 API		Rev	1.0
C		Date: Tuesday, May 28, 2013		Sheet	34 of 44


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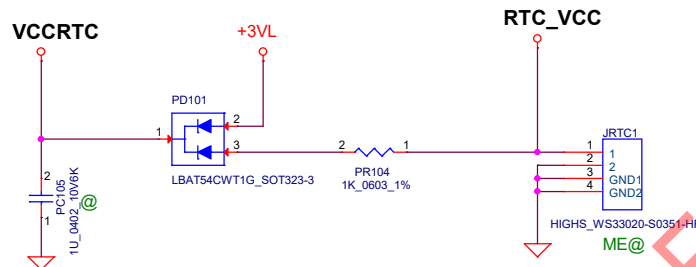
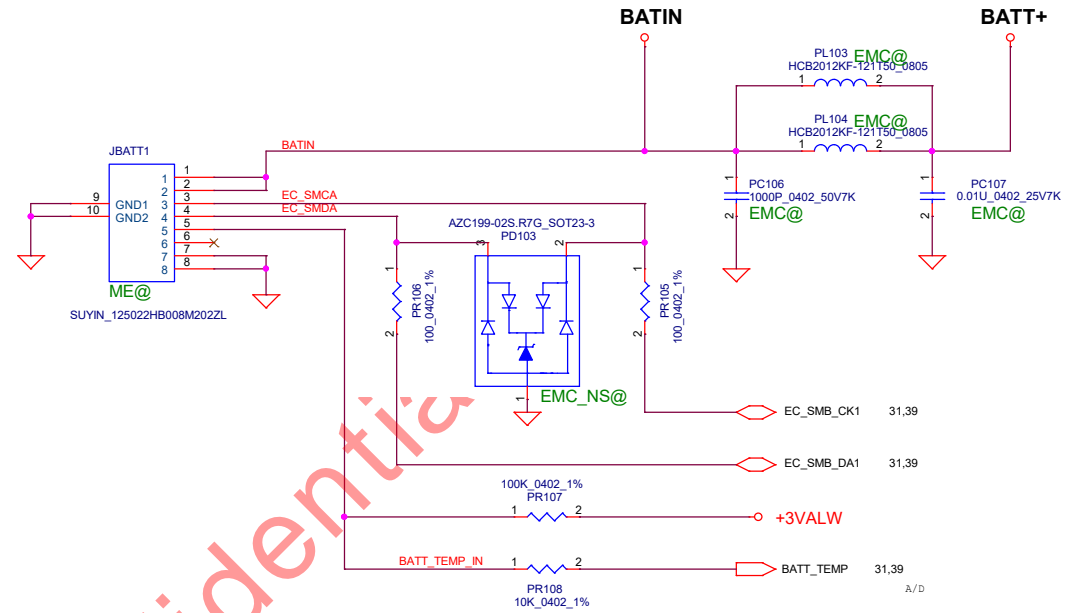
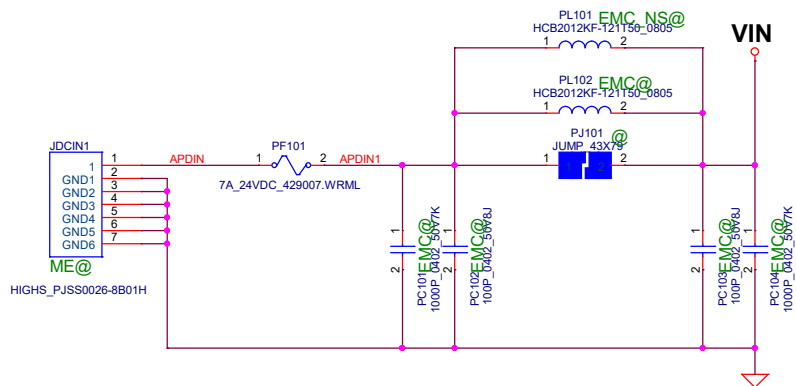
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	Power sequence Block	
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				Document Number S145 API	
				Date Tuesday, May 28, 2019	Sheet 36 of 44



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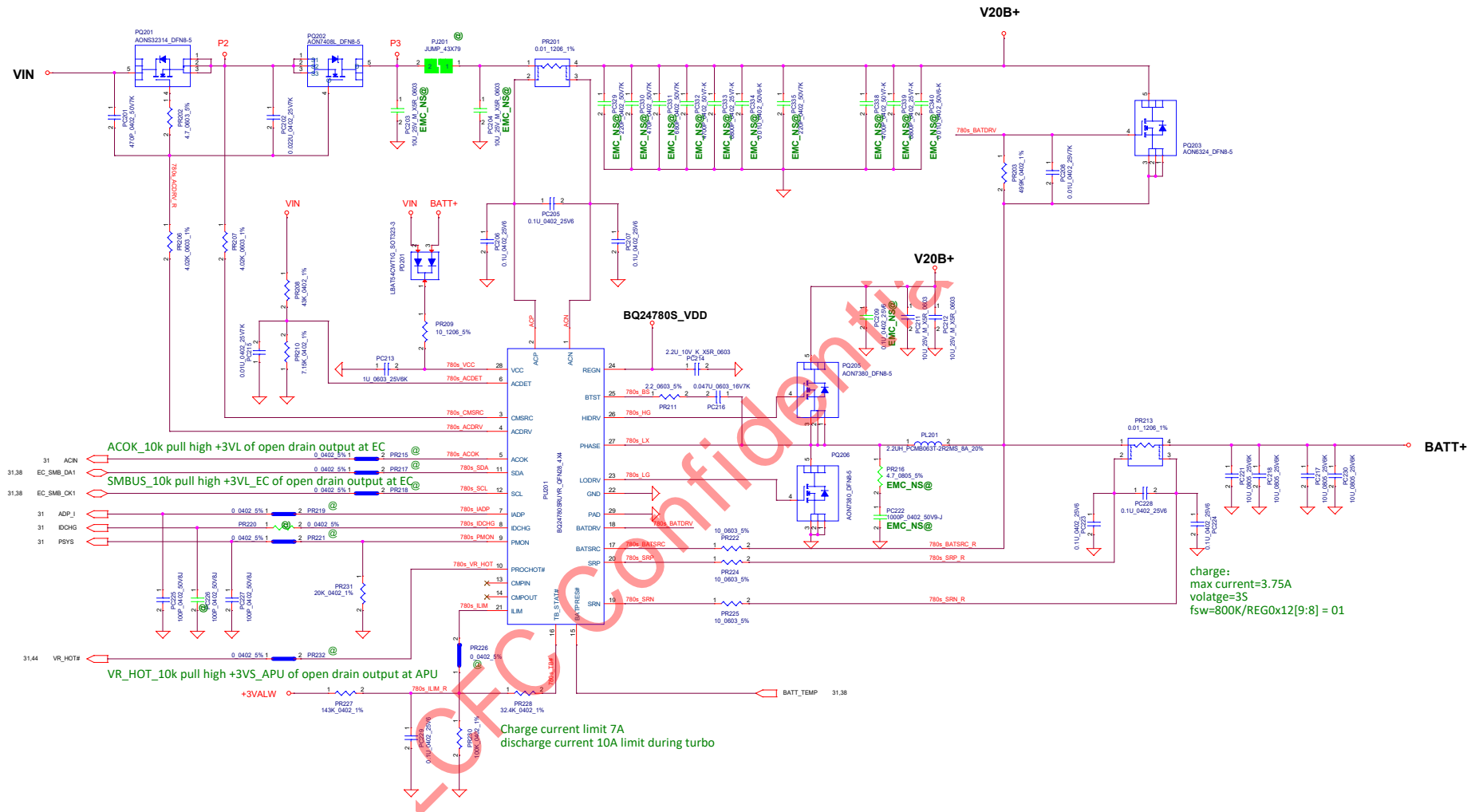


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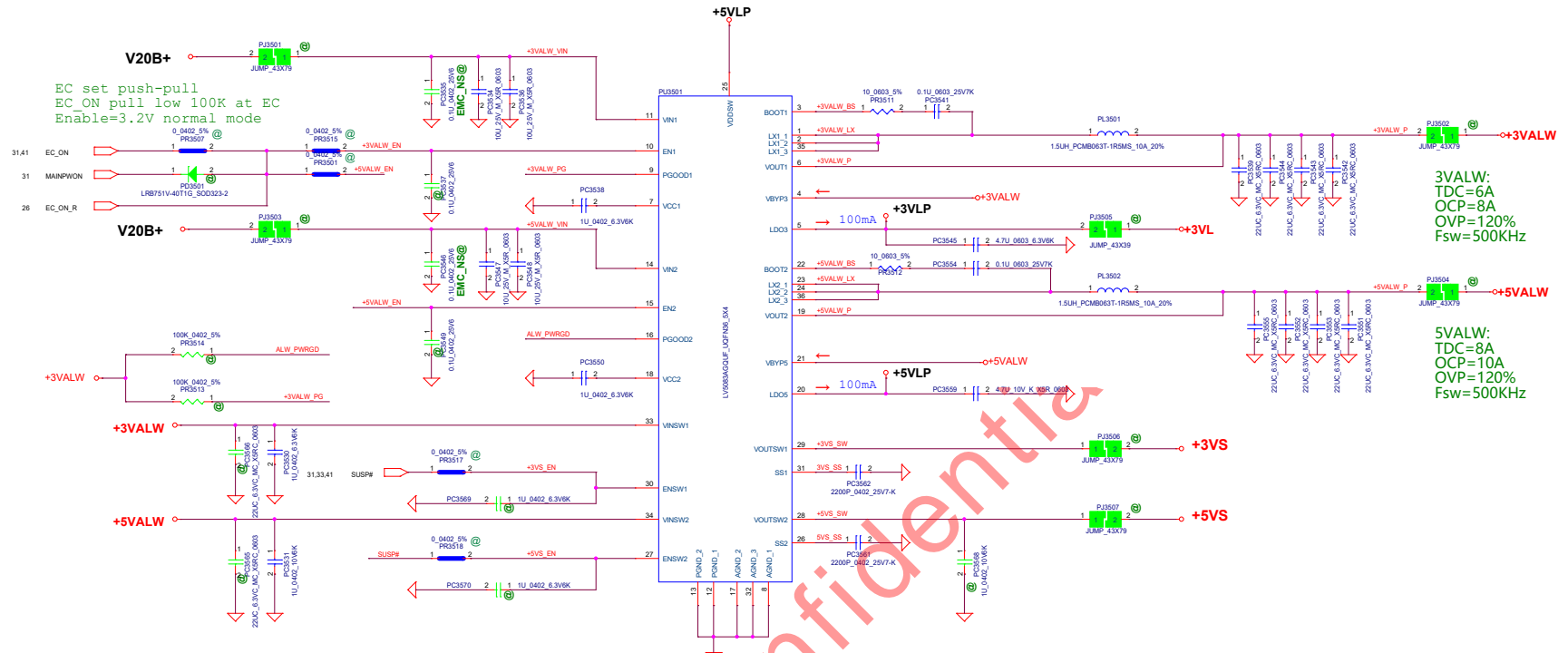
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	DCIN / RTC		
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				Date: Tuesday, May 28, 2019	Sheet 38	of 44



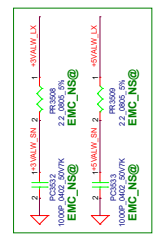
S145 API



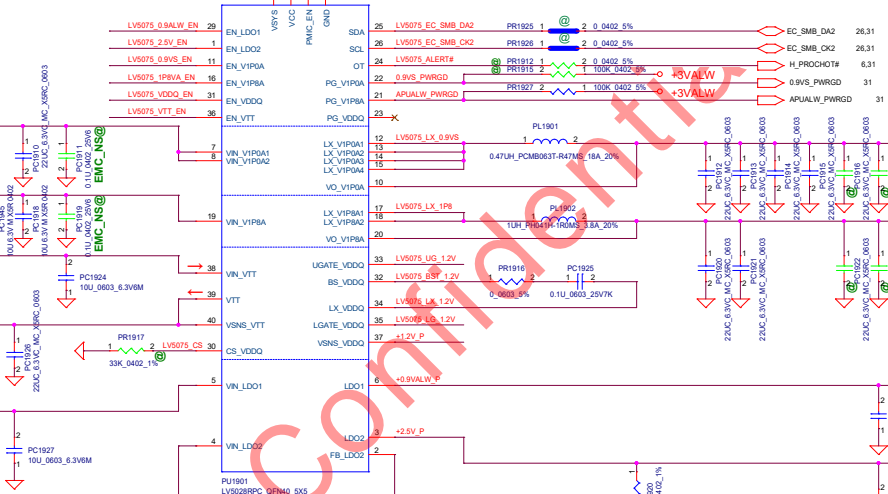
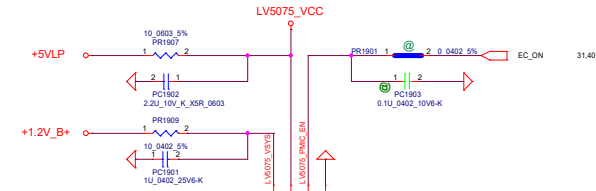
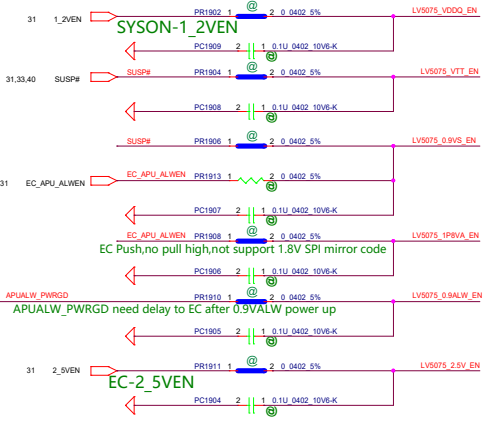
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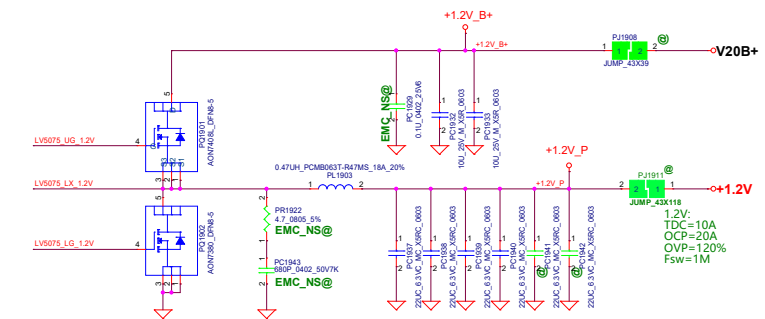
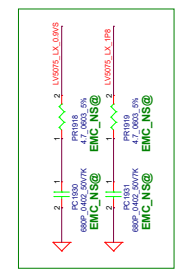
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Doc Number	S145 API
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Date:	Tuesday, May 28, 2019	Sheet:	40	of	44




+0.9VS
 0.9V:
 0.9VS/VDDP=4A
 TDC=6A
 OCP=10A
 OVP=120%
 Fsw=1M
 +1.8VALW
 1.8VALW:
 APU VDD18=2A(TDC)
 TDC=3A
 OCP=5A
 OVP=120%
 Fsw=1M
 +0.9VALW
 0.9V:
 VDDP_S5=1A
 +2.5V
 2.5V:
 TDC=1A
 FB=0.75V



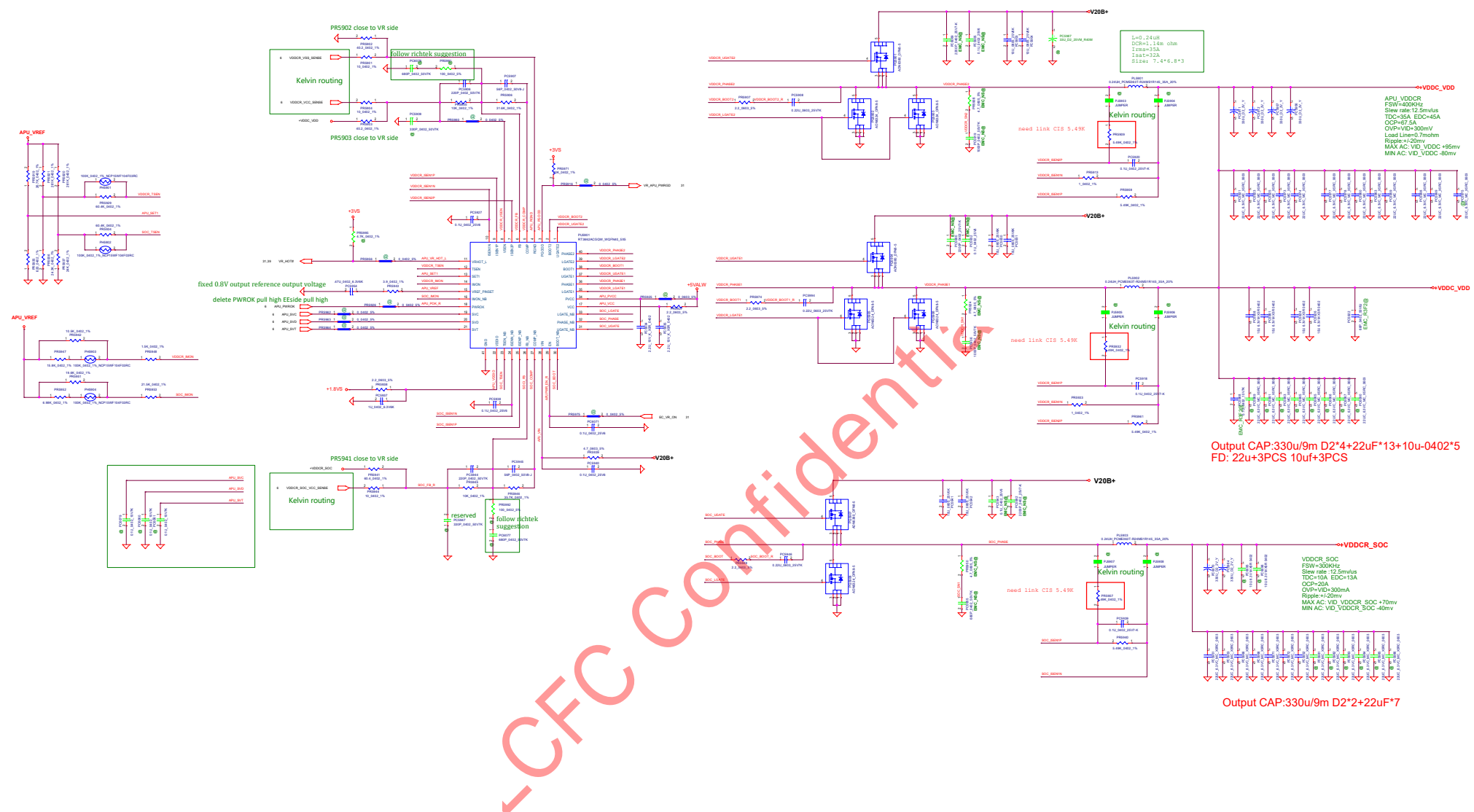
Security Classification	LC Future Center Secret Data		Title
Issued Date	2014/02/20	Deciphered Date	2014/02/20
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Issued Date	2013/08/15	Deciphered Date	2013/08/15		PWR_1.35VGS
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				S145 API	0.3
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			23



fixed 0.8V output reference output voltage
delete PWROK pull high ESide pull high

L=0.2448
DCR=1.148 03m
I=88=15A
I=84=12A
SI=at 7.4*6.8*3

VDDCR_VDD
APU_VDDCR
FSW=400kHz
Slew rate=12.5mV/us
TDC=15A, EDC=45A
OCP=67.5A
OVP=VE+300mV
Load Line=0.7mohm
Ripple=+120mV
MAX AC_VID_VDDCR +95mV
MIN AC_VID_VDDCR -80mV

Output CAP:330u/9m D2*4+22uF*13+10u-0402*5
FD: 22u+3PCS 10u+3PCS

VDDCR_SOC
VDDCR_SOC
FSW=500kHz
Slew rate=12.5mV/us
TDC=10A, EDC=15A
OCP=20A
OVP=VD+300mV
Ripple=+120mV
MAX AC_VID_VDDCR_SOC +70mV
MIN AC_VID_VDDCR_SOC -40mV

Output CAP:330u/9m D2*2+22uF*7

Security Classification	LC Future Center Secret Data	Rev	1.0
Item Code	20702914	Design Code	20702908
Part Name	PWR-VDDCR/SOC		ECFC
Doc No	S145 AP1		