

Oasis-1 SHB SOVP LOGIC SCHEMATICS

OAS1H-0

VER 1.01

Aug/08/2013

- 1.TITLE PAGE
- 2.EC HISTORY
- 3.CPU(1/8) : DMI/FDI/PEG
- 4.CPU(2/8) : MISC/JTAG/CLK
- 5.CPU(3/8) : DDR3L CHANNEL- A
- 6.CPU(4/8) : DDR3L CHANNEL- B
- 7.CPU(5/8) : POWER
- 8.CPU(6/8) : GND
- 9.CPU(7/8) : EDP/DDI
- 10.CPU(8/8) : CFG/RESERVED
- 11.PCH(1/10) : RTC/HDA/SATA/JTAG
- 12.PCH(2/10) : LPC/SPI/SMBUS/C-LINK/THERMAL
- 13.PCH(3/10) : DMI/FDI/PM
- 14.PCH(4/10) : LCD/CRT/PCI/DDI CONTROL
- 15.PCH(5/10) : GPIO/CPU/MISC/NCTF/RSVD
- 16.PCH(6/10) : PCIE/USB
- 17.PCH(7/10) : CLOCKS
- 18.PCH(8/10) : POWER
- 19.PCH(9/10) : POWER
- 20.PCH(10/10):GND
- 21.XDP CONNECTOR
- 22.RTC BATTERY
- 23.SPI FLASH
- 24.DDR3L SO DIMM CHANNEL-A
- 25.BLANK
- 26.DDR3L SO DIMM CHANNEL-B
- 27.DDR3L DECOUPLING
- 28.N14M-GS(1/6) : PEG I/F
- 29.N14M-GS(2/6) : DIGITAL OUT I/F
- 30.N14M-GS(3/6) : VRAM I/F
- 31.N14M-GS(4/6) : GPIO
- 32.N14M-GS(5/6) : POWER
- 33.N14M-GS(6/6) : GND
- 34.VRAM CHANNEL-A
- 35.BLANK
- 36.MEMORY TERMINATION
- 37.BLANK
- 38.LCD CONNECTOR
- 39.BLANK
- 40.EXT CRT INTERFACE
- 41.DISPLAY PORT CONNECTOR
- 42.BLANK
- 43.SATA HDD CONN
- 44.SATA BAY I/F CONN
- 45.USB CONNECTOR
- 46.AOU/USB POWER SWITCH
- 47.GBE LAN CLARKVILLE
- 48.GBE LAN SWITCH
- 49.RJ45 SUB CARD I/F
- 50.PCIE NGFF CARD SLOT
- 51.MEDIA CARD CONTROLLER
- 52.MEDIA CARD INTERFACE
- 53.SMART CARD/3rd NGFF I/F
- 54.AUDIO ALC3232
- 55.AUDIO CONNECTOR
- 56.AUDIO JACK SENSE
- 57.AUDIO EXT MIC I/F
- 58.AUDIO SPEAKER
- 59.AUDIO BEEP
- 60.DOCKING CONNECTOR
- 61.MEC1633L(1/3)
- 62.MEC1633L(2/3)
- 63.MEC1633L(3/3)
- 64.KEYBOARD CONNECTOR
- 65.CLICK PAD/NFC/FPR CONNECTOR
- 66.BLANK
- 67.FAN CONNECTOR
- 68.G-SENSOR
- 69.TPM
- 70.EEPROM/SMBUS SW
- 71.THINK ENGINE(1/2)
- 72.THINK ENGINE(2/2)
- 73.DC-IN
- 74.BATTERY INPUT
- 75.BATTERY CHARGER(BQ24760)
- 76.CHARGER SELECTOR
- 77.BATTERY MONITOR
- 78.DC/DC VCC5M/VCC3M (TPS51220A)
- 79.DC/DC VCCCPUCORE(TPS51631)
- 80.DC/DC VCCCPUCORE(CSD97374)
- 81.BLANK
- 82.VCCCPUCORE DECOUPLING
- 83.DC/DC VCCGFXCORE_D (TPS51219)
- 84.BLANK
- 85.DC/DC VCC1R05AMT(VT384B)
- 86.DC/DC VCC1R35A(VT387B)
- 87.DC/DC VCC0R675B(TPS51200)
- 88.DC/DC VCC1R5VIDEO(VT382B)
- 89.DC/DC VCC1R05VIDEO_PLL(TPS74801)
- 90.BLANK
- 91.BLANK
- 92.DC/DC VCC1R5B(BD3551)
- 93.LOAD SW PCH SUS
- 94.LOAD SW LAN
- 95.LOAD SW VIDEO
- 96.LOAD SW B
- 97.LOAD SW VCC5MUBAY
- 98.LOAD SW WWAN & WLAN
- 99.PTH FOR SCREW HOLES

EC HISTORY

Oasis-1 SP ASSESS (BASE LOGIC :NZM5H-0 VER 0.44 May/18/2012)

SDV stage

VER.0.01 05/29/2012 APPLIED OAS1_SP_EC001
 VER.0.02 05/31/2012 APPLIED OAS1_SP_EC002
 VER.0.03 06/05/2012 APPLIED OAS1_SP_EC003,004
 VER.0.04 06/06/2012 APPLIED OAS1_SP_EC005
 VER.0.05 06/07/2012 APPLIED OAS1_SP_EC006-010
 VER.0.06 06/08/2012 APPLIED OAS1_SP_EC011,012,014-016
 VER.0.07 06/13/2012 APPLIED OAS1_SP_EC017-019
 VER.0.08 06/14/2012 APPLIED OAS1_SP_EC020
 VER.0.09 06/18/2012 APPLIED OAS1_SP_EC021-024
 VER.0.10 06/20/2012 APPLIED OAS1_SP_EC025-027
 VER.0.11 06/27/2012 APPLIED OAS1_SP_EC028-040,042
 VER.0.12 06/28/2012 APPLIED OAS1_SP_EC043-055
 VER.0.13 06/29/2012 APPLIED OAS1_SP_EC056,057
 VER.0.14 07/02/2012 APPLIED OAS1_SP_EC058-062
 VER.0.15 07/03/2012 APPLIED OAS1_SP_EC063,064
 VER.0.16 07/04/2012 APPLIED OAS1_SP_EC065,066
 VER.0.17 07/05/2012 APPLIED OAS1_SP_EC069-073,075,078,079
 VER.0.18 07/06/2012 APPLIED OAS1_SP_EC067,068,074,076,077
 VER.0.19 07/10/2012 APPLIED OAS1_SP_EC080,081
 VER.0.20 07/12/2012 APPLIED OAS1_SP_EC082-087
 VER.0.21 07/31/2012 APPLIED OA1_MB_SDV_EC001_0727
 VER.0.22 08/03/2012 APPLIED OA1_MB_SDV_EC002_0803
 VER.0.23 08/07/2012 APPLIED OA1_MB_SDV_EC003_0807
 VER.0.24 08/10/2012 APPLIED OA1_MB_SDV_EC004_0810
 08/14/2012 APPLIED OA1_MB_SDV_EC005_0814
 VER.0.25 08/15/2012 APPLIED OA1_MB_SDV_EC006_0815
 VER.0.26 08/17/2012 APPLIED OA1_MB_SDV_EC007_0817
 VER.0.27 08/23/2012 APPLIED OA1_MB_SDV_EC008_0823
 VER.0.28 08/28/2012 APPLIED OA1_MB_SDV_EC009_0828
 VER.0.29 08/29/2012 APPLIED OA1_MB_SDV_EC010_0829
 VER.0.30 08/31/2012 APPLIED OA1_MB_SDV_EC011_0831
 VER.0.31 09/04/2012 APPLIED OA1_MB_SDV_EC012_0904
 VER.0.32 09/06/2012 APPLIED OA1_MB_SDV_EC013_0906
 VER.0.33 09/10/2012 APPLIED OA1_MB_SDV_EC014_0910
 09/11/2012 APPLIED OA1_MB_SDV_EC015_0911
 VER.0.34 09/12/2012 APPLIED OA1_MB_SDV_EC016_0912
 VER.0.35 09/14/2012 APPLIED OA1_MB_SDV_EC017_0914
 VER.0.36 09/20/2012 APPLIED OA1_MB_SDV_EC018_0920
 09/21/2012 APPLIED OA1_MB_SDV_EC019_0921
 VER.0.37 09/24/2012 APPLIED OA1_MB_SDV_EC020_0924
 VER.0.38 09/26/2012 APPLIED OA1_MB_SDV_EC021_0926
 VER.0.39 09/28/2012 APPLIED OA1_MB_SDV_EC022_0928
 VER.0.40 10/02/2012 APPLIED OA1_MB_SDV_EC023_1002
 VER.0.41 10/04/2012 APPLIED OA1_MB_SDV_EC024_1004
 10/04/2012 APPLIED OA1_MB_SDV_EC025_1004a
 10/05/2012 APPLIED OA1_MB_SDV_EC026_1005
 VER.0.42 10/08/2012 APPLIED OA1_MB_SDV_EC027_1008
 10/11/2012 APPLIED OA1_MB_SDV_EC028_1011
 VER.0.43 10/16/2012 APPLIED OA1_MB_SDV_EC029_1015
 VER.0.44 10/16/2012 APPLIED OA1_MB_SDV_EC030_1016
 10/17/2012 APPLIED OA1_MB_SDV_EC031_1017
 VER.0.45 10/18/2012 APPLIED OA1_MB_SDV_EC032_1018
 VER.0.46 10/29/2012 APPLIED OA1_MB_SDV_EC033_1029
 VER.0.47 11/02/2012 APPLIED OA1_MB_SDV_EC034_1102

MFVT stage

VER.1.01 11/22/2012 APPLIED OA1_MB_MFVT_EC001_1120
 VER.1.02 12/03/2012 APPLIED OA1_MB_MFVT_EC002_1203
 12/05/2012 APPLIED OA1_MB_MFVT_EC003_1205
 VER.1.03 12/10/2012 APPLIED OA1_MB_MFVT_EC004_1210

FVT stage

VER.0.01 12/19/2012 APPLIED OA1_MB_FVT_EC001_1219
 12/21/2012 APPLIED OA1_MB_FVT_EC002_1221
 VER.0.02 12/21/2012 APPLIED OA1_MB_FVT_EC003_1221_R1
 12/25/2012 APPLIED OA1_MB_FVT_EC004_1225
 VER.0.03 12/26/2012 APPLIED OA1_MB_FVT_EC005_1226
 VER.0.04 12/27/2012 APPLIED OA1_MB_FVT_EC006_1227
 VER.0.05 12/28/2012 APPLIED OA1_MB_FVT_EC007_1228
 VER.0.06 01/03/2012 APPLIED ECR_1R05VIDEO_PLL discharge.ppt
 RF_EC_FVT_0103-oscar.ppt
 VER.1.00 01/04/2012 APPLIED FVT gerber out
 VER.1.01 01/08/2013 APPLIED OA1_MB_FVT_EC008_0108
 OA1_MB_FVT_EC008_0108_R1
 VER.1.02 01/17/2013 APPLIED OA1_MB_FVT_EC009_0117

SIT stage

VER.0.01 02/06/2013 APPLIED OA1_MB_SIT_EC001_0206
 VER.0.02 02/18/2013 APPLIED OA1_MB_SIT_EC002_0218
 VER.0.03 02/25/2013 APPLIED OA1_MB_SIT_EC003_0225
 VER.0.04 03/07/2013 APPLIED OA1_MB_SIT_EC004_0307
 VER.0.05 03/08/2013 APPLIED OA1_MB_SIT_EC005_0308
 VER.0.06 03/11/2013 APPLIED OA1_MB_SIT_EC006_0311
 03/12/2013 APPLIED OA1_MB_SIT_EC007_0312
 VER.0.07 03/13/2013 APPLIED OA1_MB_SIT_EC008_0313
 03/14/2013 APPLIED RF_EC_SIT_0305-Tony.pptx
 Oasis EMC solution list on FVT stage 20130204
 VER.0.08 03/14/2013 APPLIED OA1_MB_SIT_EC009_0314
 VER.1.00 03/19/2013 APPLIED SIT gerber out
 VER.1.01 03/25/2013 APPLIED OA1_MB_SIT_EC010_0325
 VER.1.02 04/02/2013 Applied ECR_20130416

SIT-v stage

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 VER.0.02 04/25/2013 APPLIED OA1_MB_SITV_EC002_0425
 VER.1.00 05/02/2013 Applied ECR_20130502
 VER.1.01 05/09/2013 APPLIED OA1_MB_SITV_EC003_05/09
 05/10/2013 APPLIED OA1_MB_SITV_EC004_05/10
 VER.1.02 05/20/2013 APPLIED ECR_20130520
 06/14/2013 APPLIED ECR_20130614

SVT stage

VER.0.01 06/12/2013 APPLIED OA1_MB_SVT_EC001_0612
 VER.0.02 06/18/2013 APPLIED OA1_MB_SVT_EC002_0618
 06/18/2013 APPLIED OA1_MB_SVT_EC003_0618
 VER.0.03 06/24/2013 APPLIED OA1_MB_SVT_EC004_0624
 06/25/2013 APPLIED OA1_MB_SVT_EC005_0625
 VER.1.00 06/26/2013 APPLIED OA1_MB_SVT_EC006_0626
 06/26/2013 APPLIED OA1_MB_SVT_EC007_0626
 VER.1.01 06/28/2013 APPLIED OA1_MB_SVT_EC008_0628
 VER.1.02 07/11/2013 APPLIED OA1_MB_SVT_EC009_0711

SOVP stage

VER.1.00 08/06/2013 APPLIED ECR_20130806
 VER.1.01 08/08/2013 APPLIED ECR_20130808

General BOM Structure

@ : No ASM for all model
 UMA@ : ASM for UMA model, No ASM for SWG model
 SWG@ : No ASM for UMA model, ASM for SWG model
 CONN_ASM@ : ASM connector
 CONN_NOASM@ : NO ASM connector
 PLM@ : For PCB material

VRAM BOM Structure

MIG@ : ASM for SWG model with Micron 1G VRAM.
 SIG@ : ASM for SWG model with Samsung 1G VRAM.

SPI ROM BOM Structure

SPI_1ST@ : ASM for Winbond SPI ROM.
 SPI_2ND@ : ASM for Macronix SPI ROM.

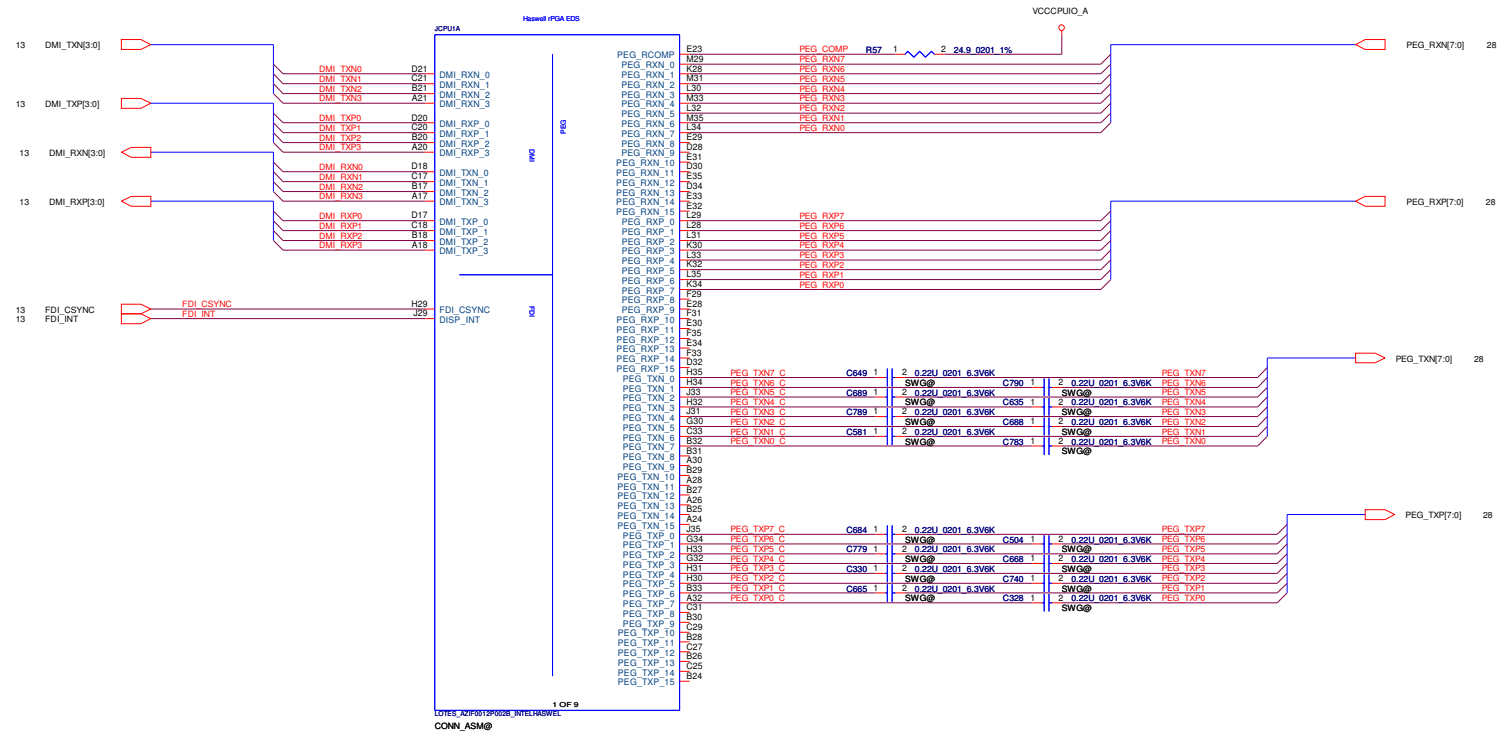
BOM option

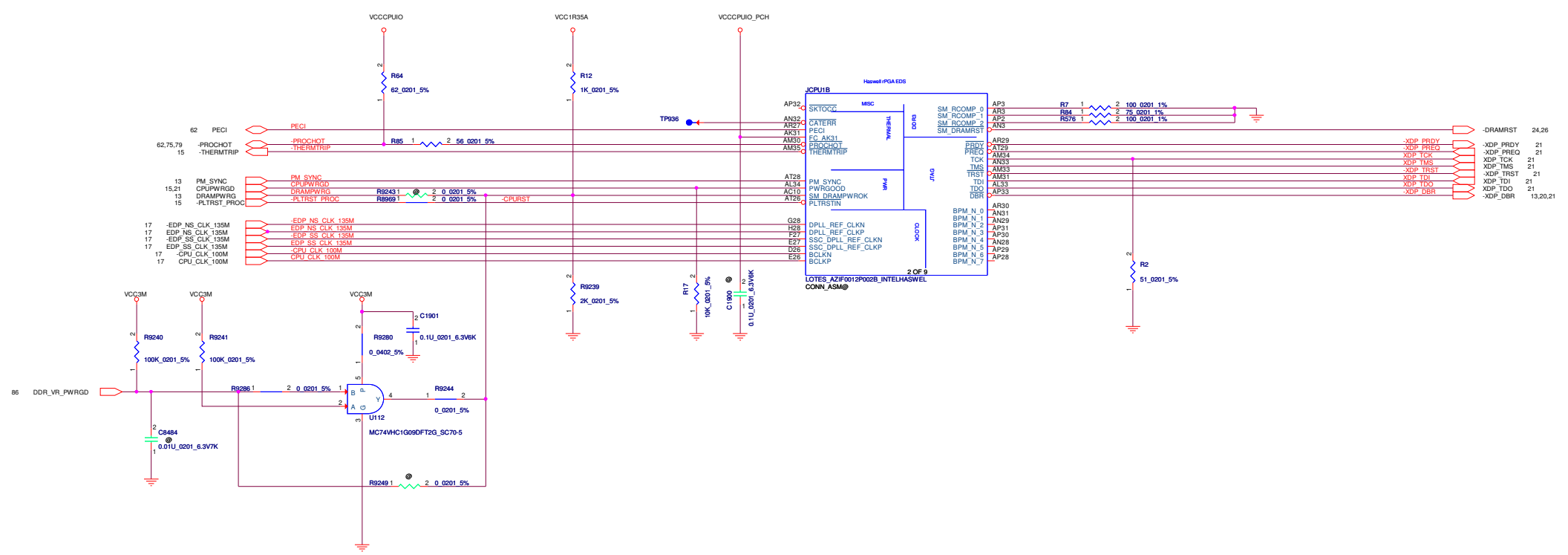
UMA :
 PLM@ / UMA@ / CONN_ASM@

SWG + Samsung 1G VRAM :
 PLM@ / SWG@ / CONN_ASM@ / X76_SIG@

SWG + Micron 1G VRAM :
 PLM@ / SWG@ / CONN_ASM@ / X76_MIG@



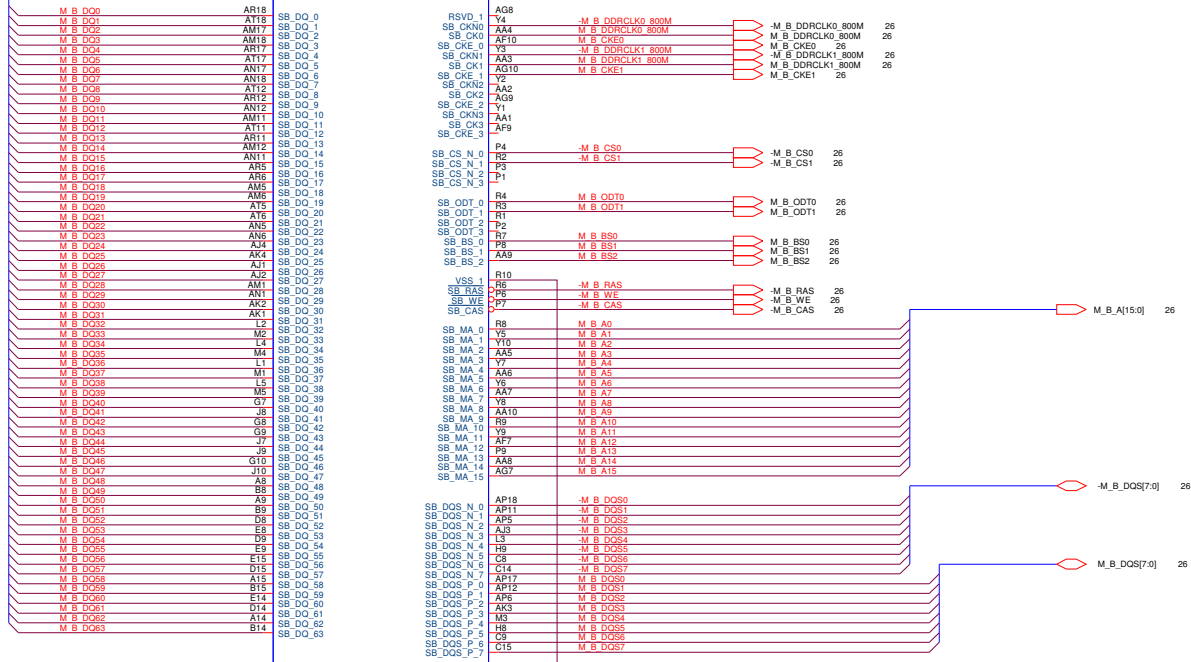




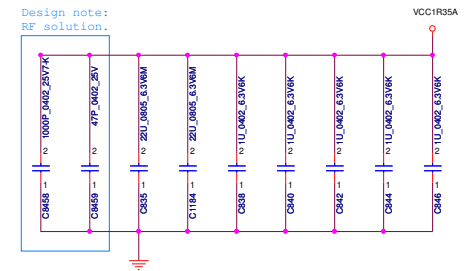
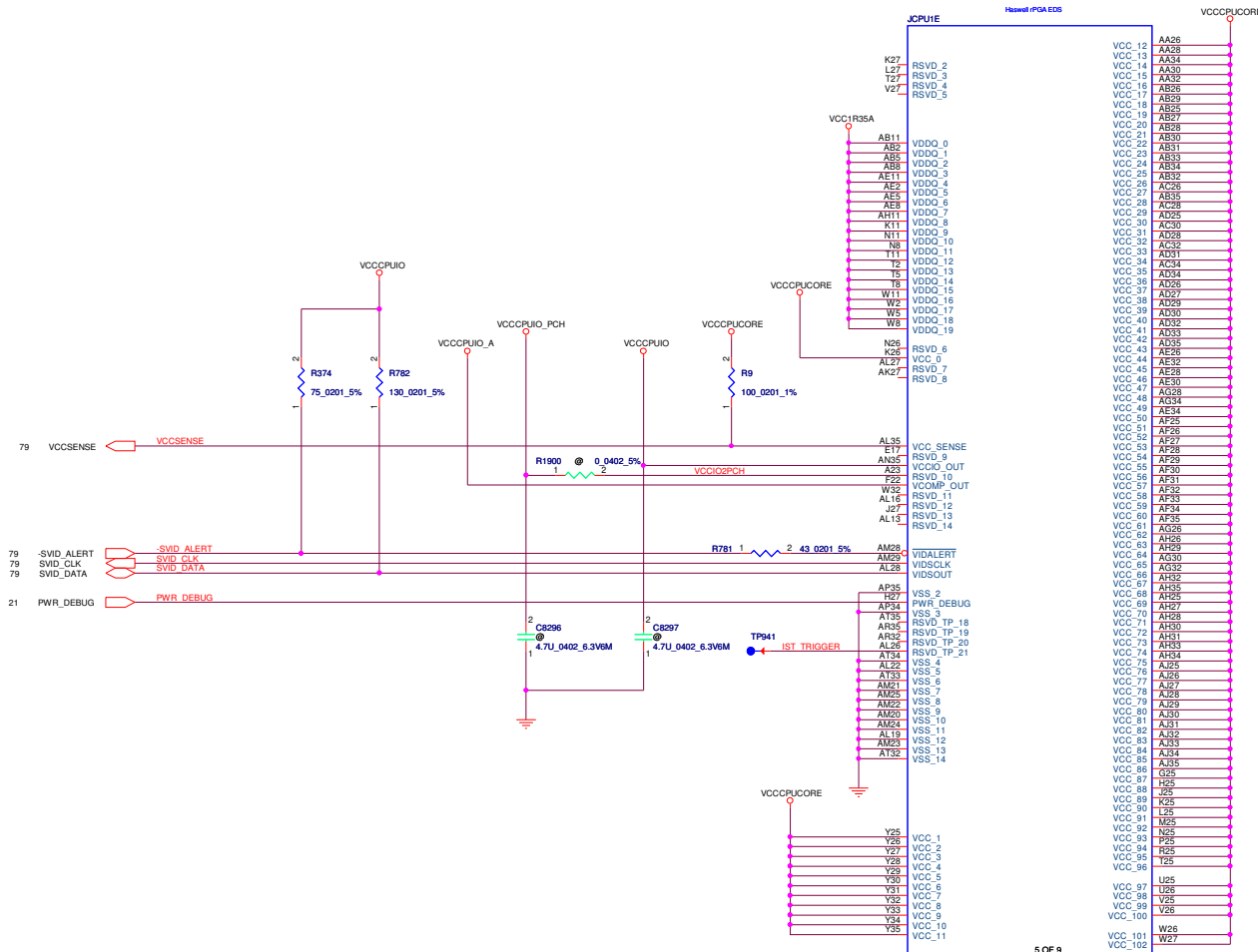
26 M_B_DQ[63:0]

Haswell iPGA EDS

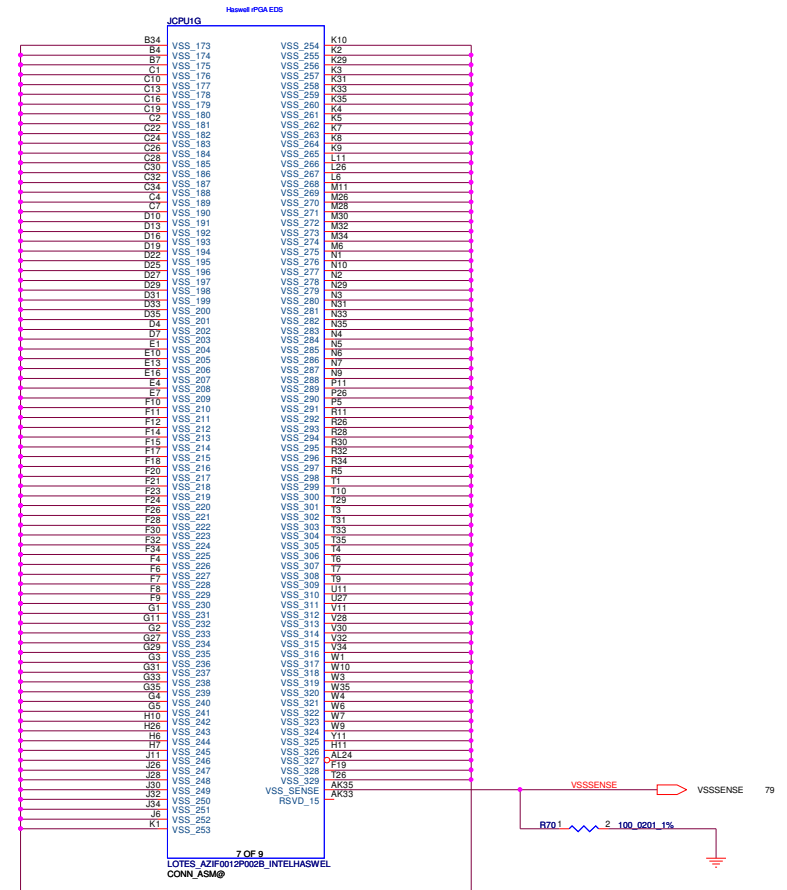
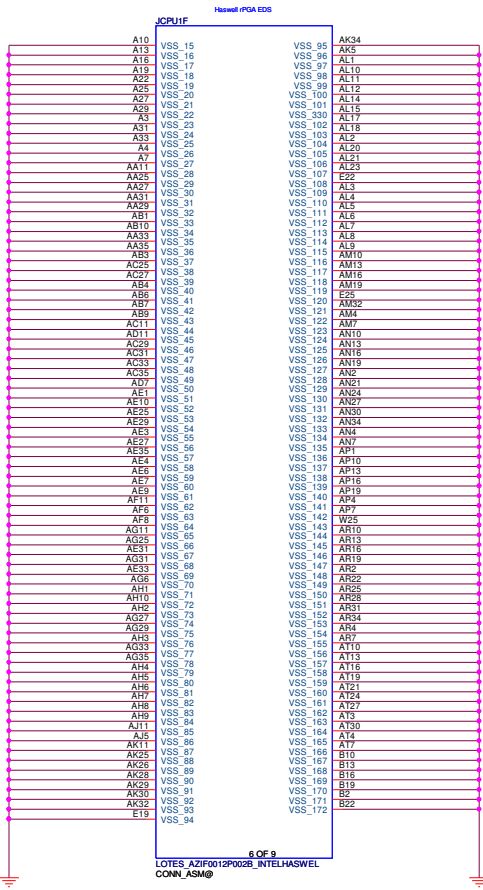
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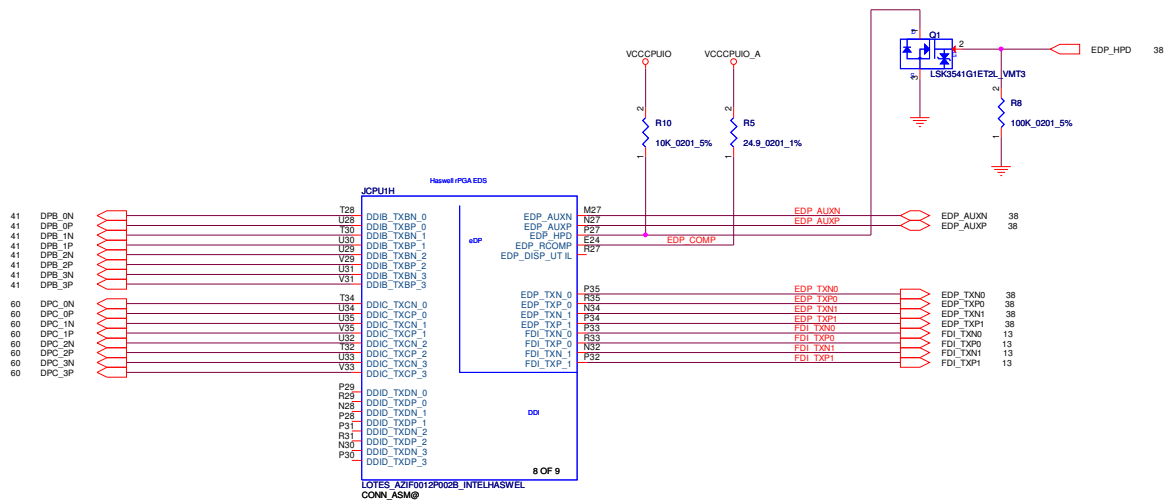


4 OF 6
LOTES_AZ\F0012P002B_INTELHASWEL
CONN_ASM



5 OF 9
 LOTES_AZIF0012P002B_INTELHASWEL
 CCNN_ASM@





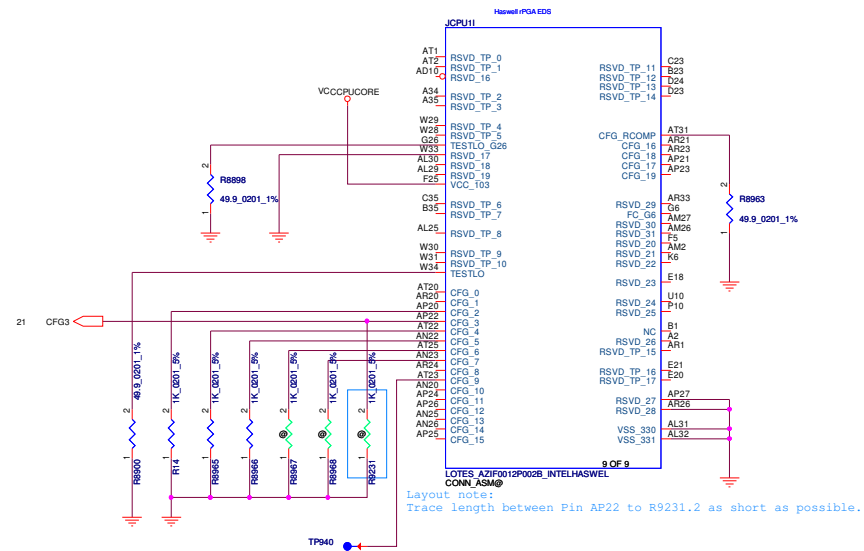


Table 10-1

CFG2 : PEG Static Lane Reversal
1 : Normal Operation
0 : Lane Reversal
CFG4 : Display Port Presence
1 : Disabled
0 : Enabled
CFG[6:5] : PEG Bifurcation
11 : Func 1 Disabled, Func 2 Disabled (x16,---,---)
10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---)
01 : Func 1 Disabled, Func 2 Enabled
00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)
CFG7 : PEG Defer Training
1 : PEG Train Immediately Following XXRESETB Deassertion
0 : PEG Wait for BIOS for Training

Table 11-4

Tamper	Enable	Disable
SW1	ASM	NO_ASM
R9248	ASM	NO_ASM
C8486	ASM	NO_ASM
D255	ASM	NO_ASM
R9291	ASM	NO_ASM



Table 11-1

32.768KHz 9pF 20ppm:
 KDS 1TJF090DP1A0004
 TXC 9H03200033
 Epson Q13FC1350000300

Table 11-2

SPKR TCO TIMER SYSTEM REBOOT	
HIGH	DISABLED (NO REBOOT)
LOW	ENABLED

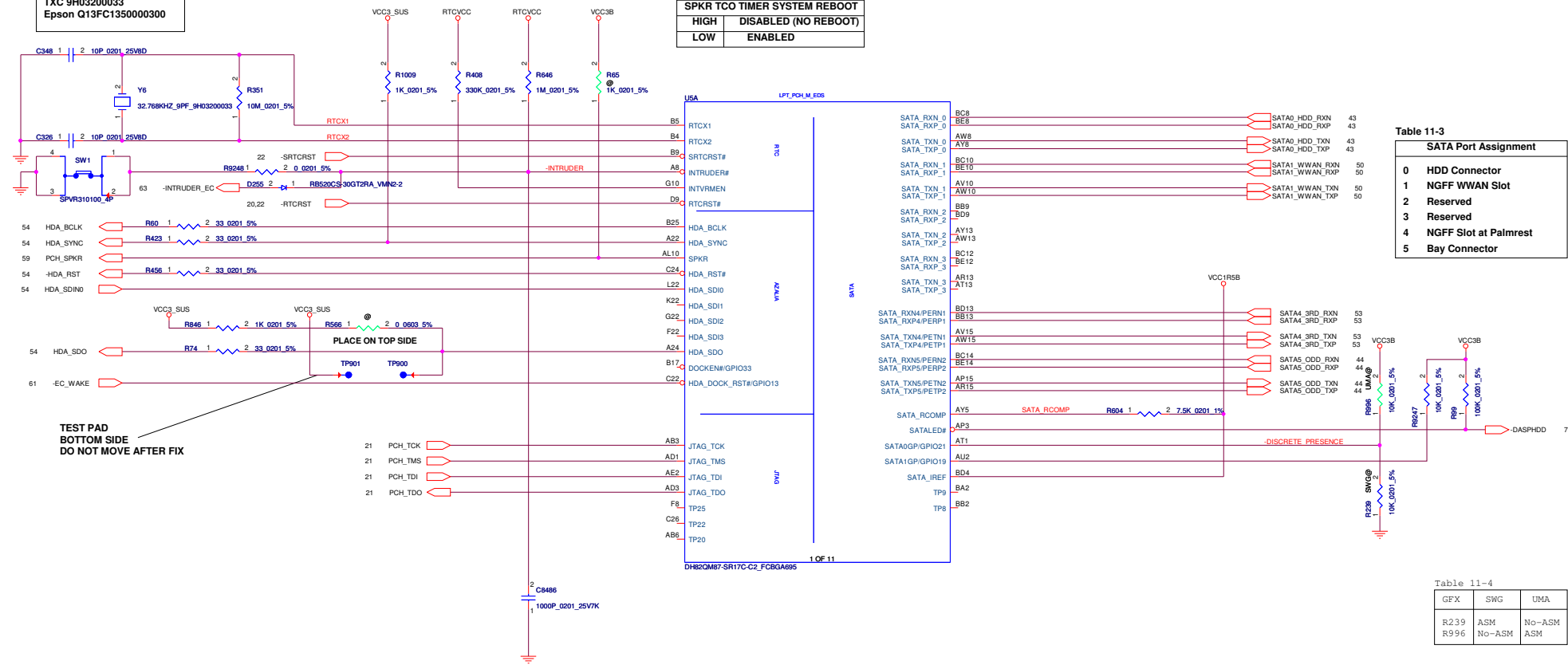


Table 11-3

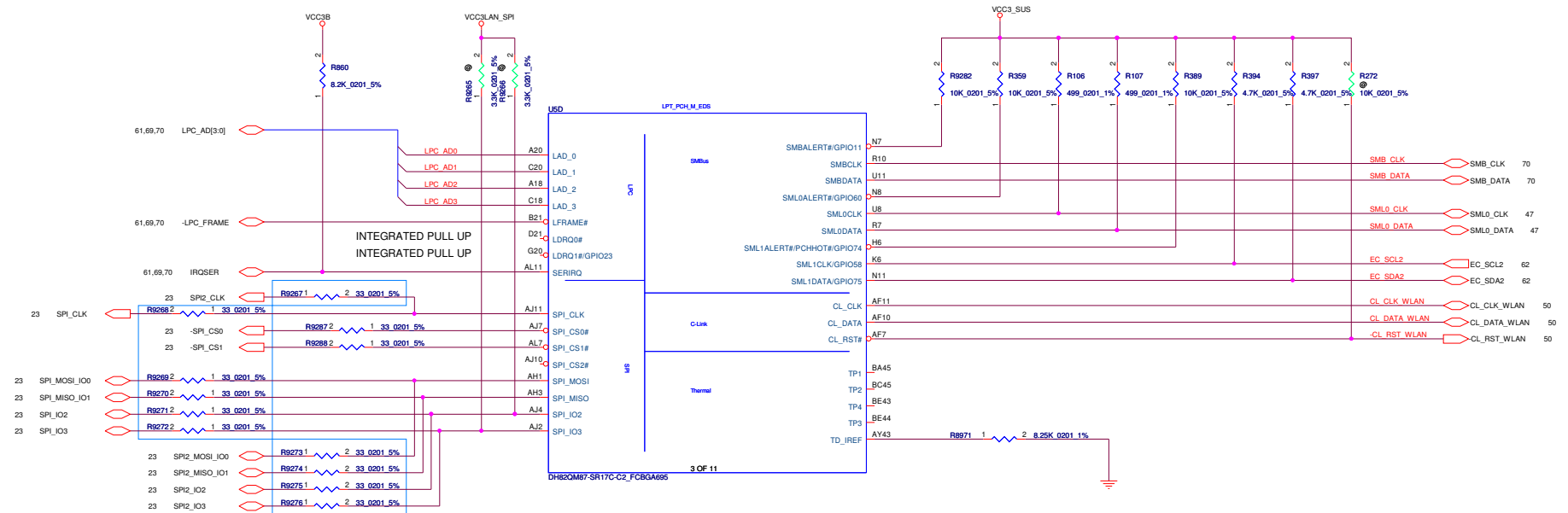
SATA Port Assignment	
0	HDD Connector
1	NGFF WWAN Slot
2	Reserved
3	Reserved
4	NGFF Slot at Palmrest
5	Bay Connector

Table 11-4

GFX	SWG	UMA
R239	ASM	No-ASM
R996	No-ASM	ASM

TEST PAD
 BOTTOM SIDE
 DO NOT MOVE AFTER FIX

PLACE ON TOP SIDE



Layout note:
 Put on below resistors near PCH (U5):
 R9268, R9269, R9270, R9271, R9272
 R9267, R9273, R9274, R9275, R9276

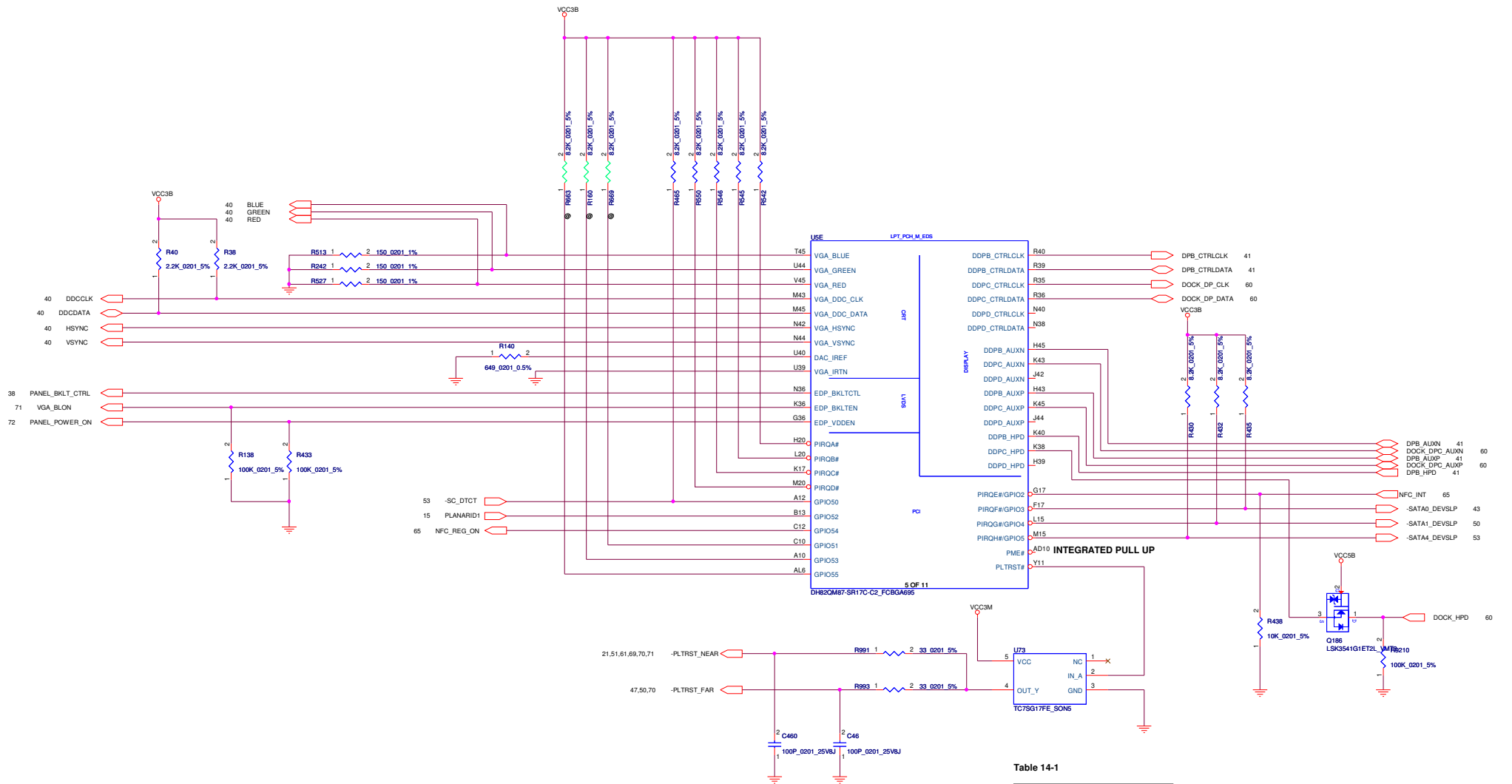


Table 14-1

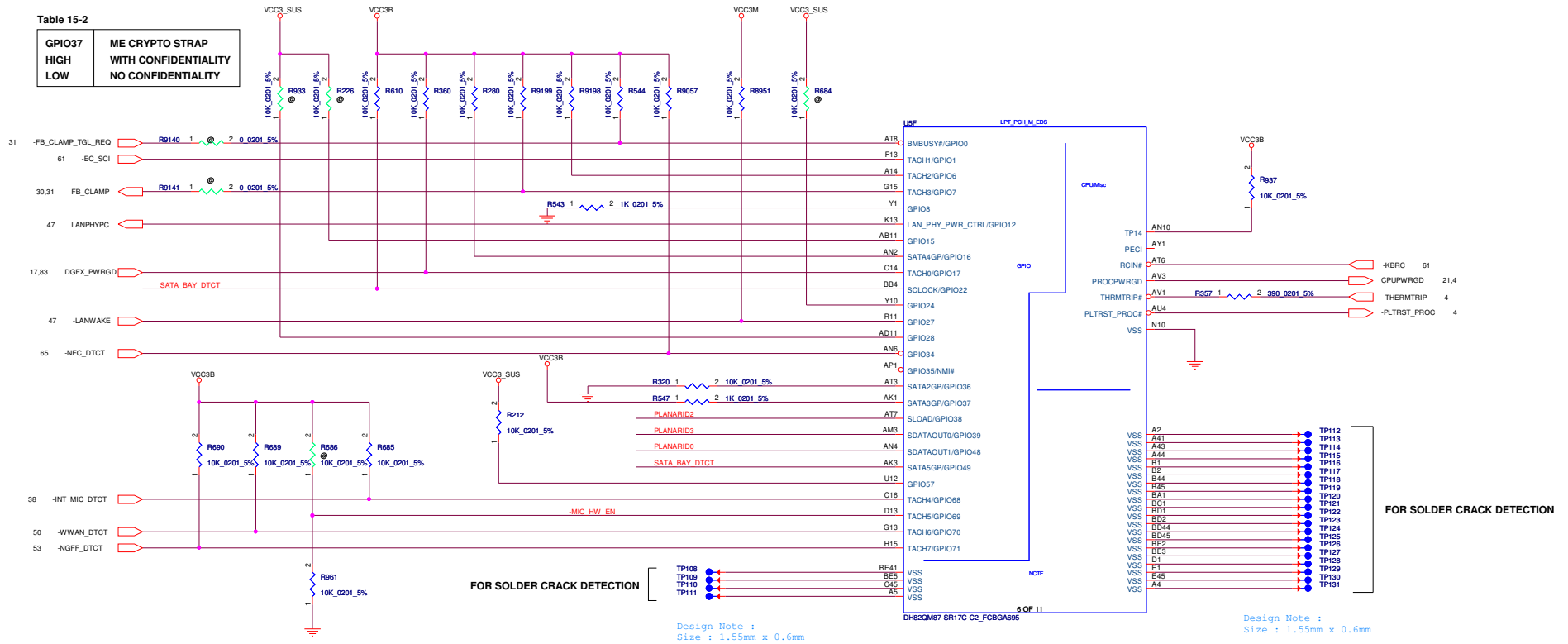
Buffer (U73)	
Toshiba	TC7SG17FE
Onsemi	NL17SZ17XV5T2G

Table 15-1

GPIO8	INTEGRATED CLOCKING
HIGH	DISABLED(BTM)
LOW	ENABLED(FCIM)

Table 15-2

GPIO37	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY



FOR SOLDER CRACK DETECTION

- TP108
- TP109
- TP110
- TP111

Design Note :
Size : 1.55mm x 0.6mm

FOR SOLDER CRACK DETECTION

Design Note :
Size : 1.55mm x 0.6mm

Table 15-3

LEVEL	PLANAR ID			
	3	2	1	0
1	R39	R505	R37	R671
0	R43	R47	R113	R48

Table 15-4

LEVEL	PLANARID[3..0]
SDV	0000B
FVT	0001B
SIT	0010B
SIT-v	0011B
SVT	0100B

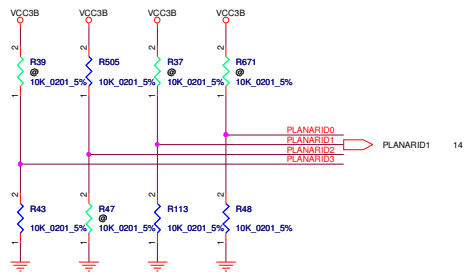


Table 16-1

Flexible I/O Configuration				
I/O	High Speed Signals	Configuration	Net Name	Port Assignment
Port 1	USB3 1	USB3 1	USB3P1_SYS0	USB 3.0 System Port 0
Port 2	USB3 2	USB3 2	USB3P2_SYS1	USB 3.0 System Port 1
Port 3	USB3 5	USB3 5	USB3P5_DOCK	USB 3.0 Docking
Port 4	USB3 6	USB3 6	NC	Reserved
Port 5	PCIE 1/USB3 3	PCIE 1	PCIE1_MCC	Media Card Controller
Port 6	PCIE 2/USB3 4	PCIE 2	PCIE2_WLAN	NGFF WLAN Slot
Port 7	PCIE 3	PCIE 3	NC	Reserved
Port 8	PCIE 4	PCIE 4	PCIE4_GBE	GbE PHY
Port 9	PCIE 5	PCIE 5	NC	Reserved
Port 10	PCIE 6	PCIE 6	NC	Reserved
Port 11	PCIE 7	PCIE 7	NC	Reserved
Port 12	PCIE 8	PCIE 8	NC	Reserved
Port 13	SATA 4/PCIE 1	SATA 4	SATA4_3RD	NGFF Slot at Palmrest
Port 14	SATA 5/PCIE 2	SATA 5	SATA5_ODD	Bay Connector
Port 15	SATA 0	SATA 0	SATA0_HDD	HDD Connector
Port 16	SATA 1	SATA 1	SATA1_WWAN	NGFF WWAN Slot
Port 17	SATA 2	SATA 2	NC	Reserved
Port 18	SATA 3	SATA 3	NC	Reserved

Table 16-2

PCIe Port Assignment	
1	Media Card Controller
2	NGFF WLAN Slot
3	Reserved
4	GbE PHY
5	Reserved
6	Reserved
7	Reserved
8	Reserved

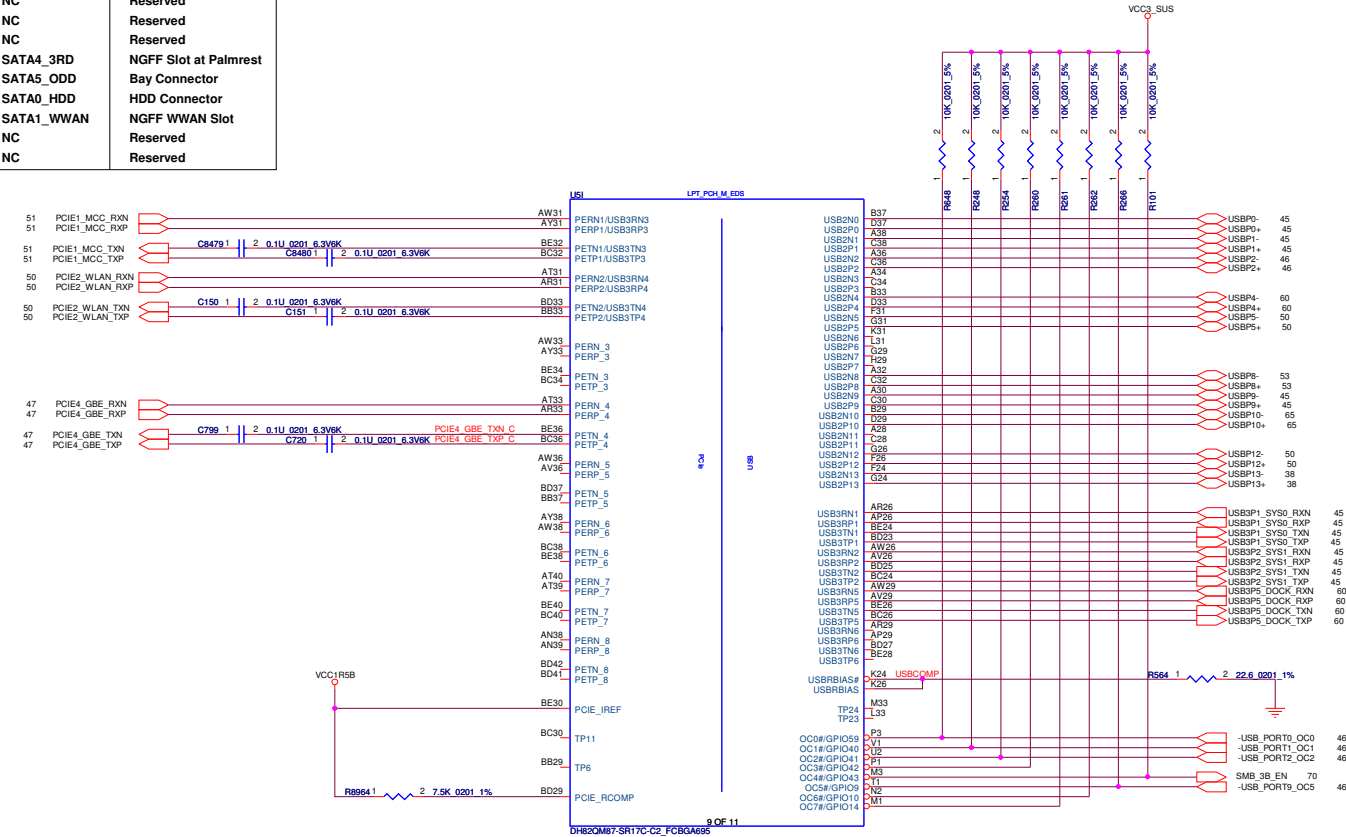
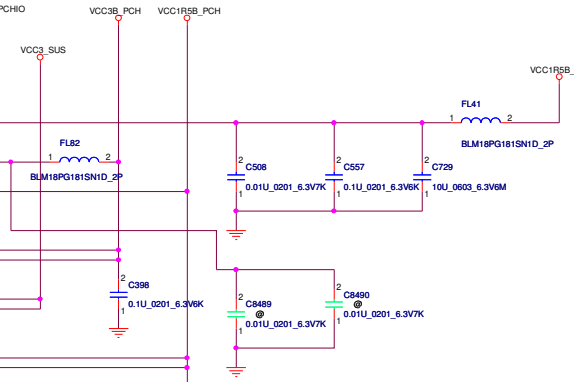
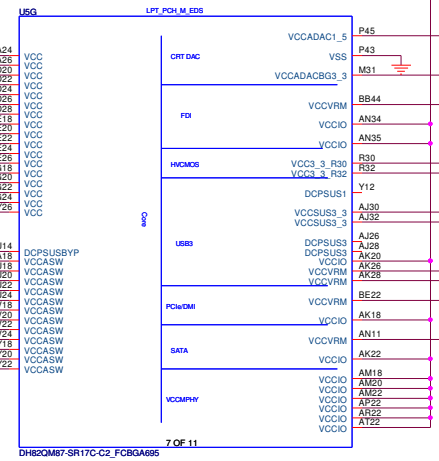
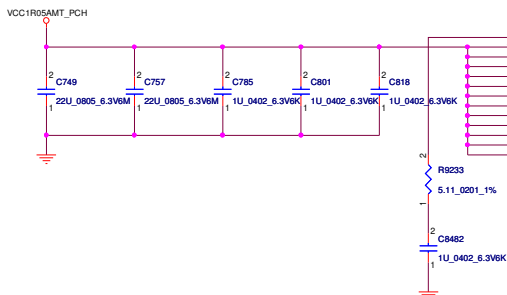
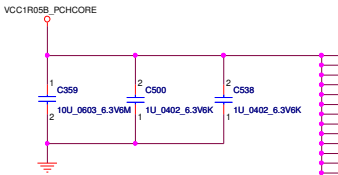
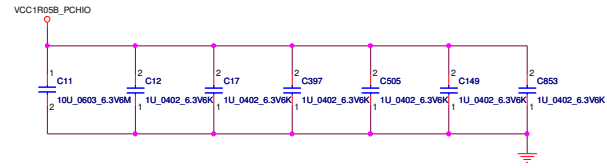
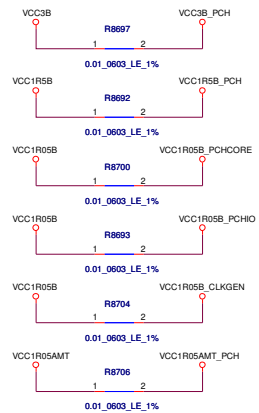


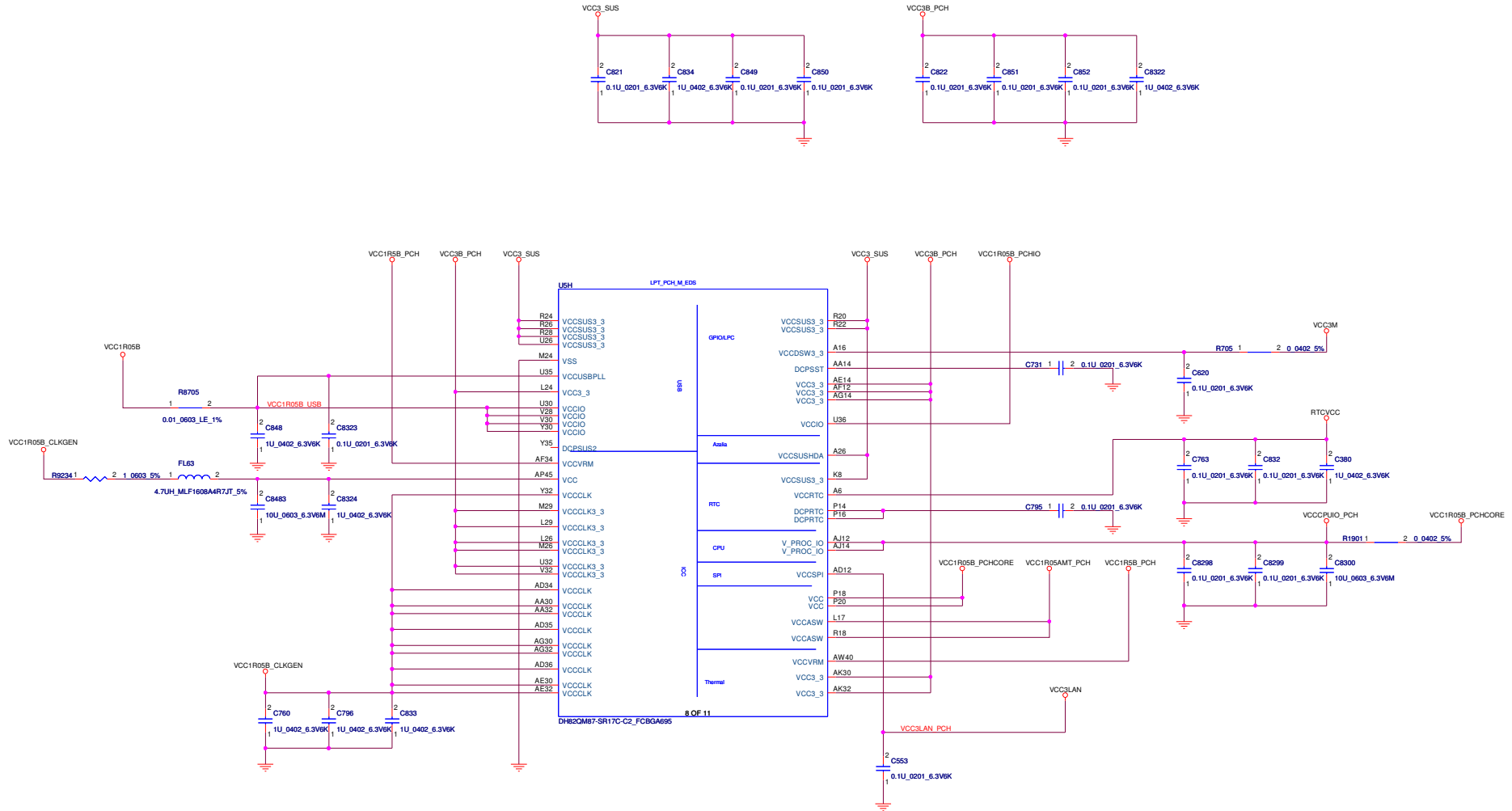
Table 16-3

USB 2.0 Port Assignment	
0	USB 3.0 System Port 0
1	USB 3.0 System Port 1
2	USB 2.0 System Port 2 (AOU)
3	Reserved
4	USB 3.0 Docking
5	NGFF WWAN Slot
6	Reserved
7	Reserved
8	Smart Card Slot
9	USB 2.0 System Port 3 (Debug)
10	Fingerprint Reader
11	Reserved
12	NGFF WLAN Slot
13	USB Camera

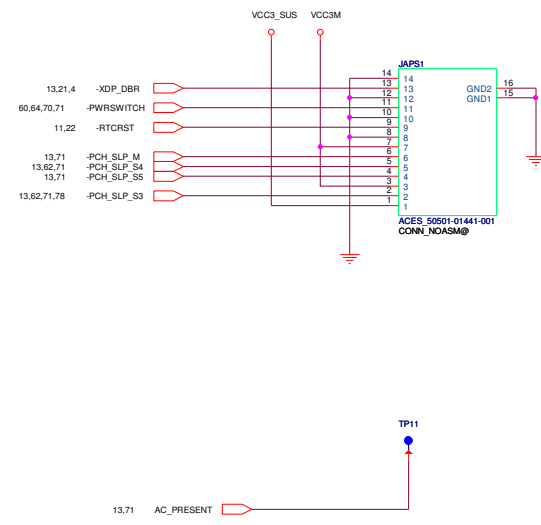
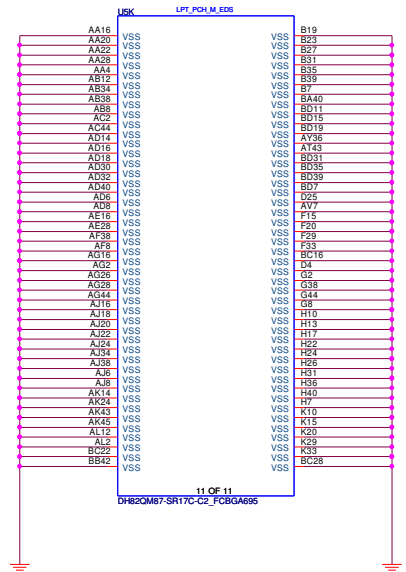
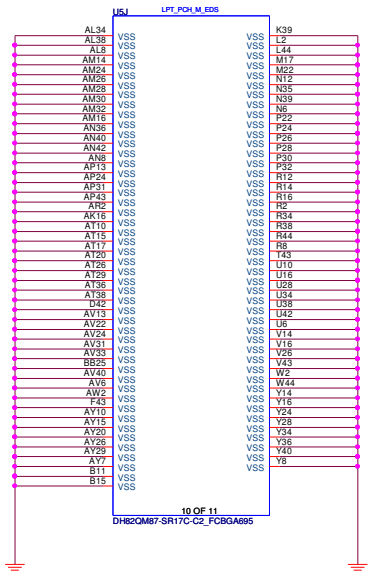
Table 16-4

USB 3.0 Port Assignment	
1	USB 3.0 System Port 0
2	USB 3.0 System Port 1
3	(N/A)
4	(N/A)
5	USB 3.0 Docking
6	Reserved





TEST PAD FOR METS/APS



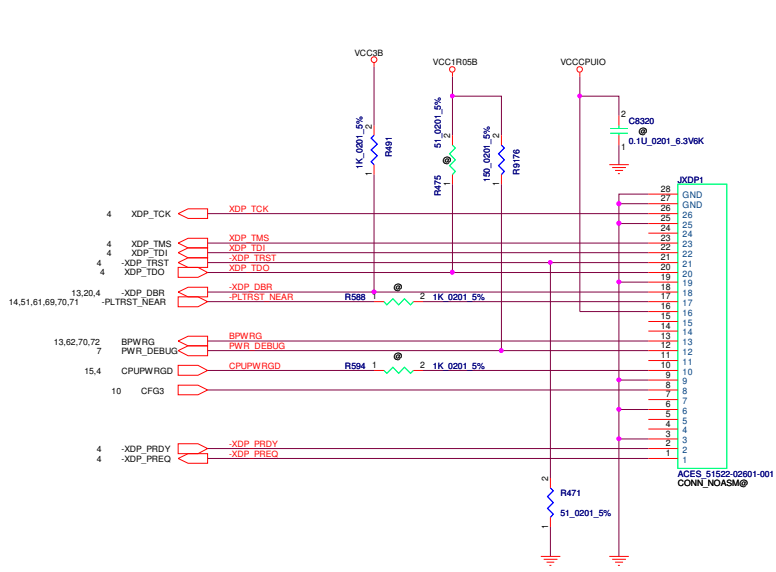


Table 21-1

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R475	ASM	NO ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	NO ASM
CPUPWRGD	R594	ASM	NO ASM
PWR_DEBUG	R9176	ASM	ASM
	C8320	ASM	NO ASM
	JXDP1	ASM	NO ASM

↑
LOGIC

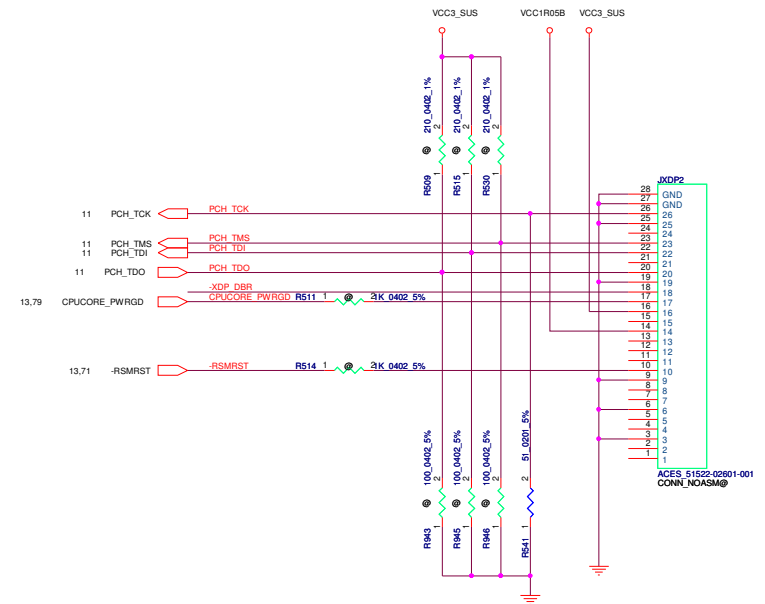
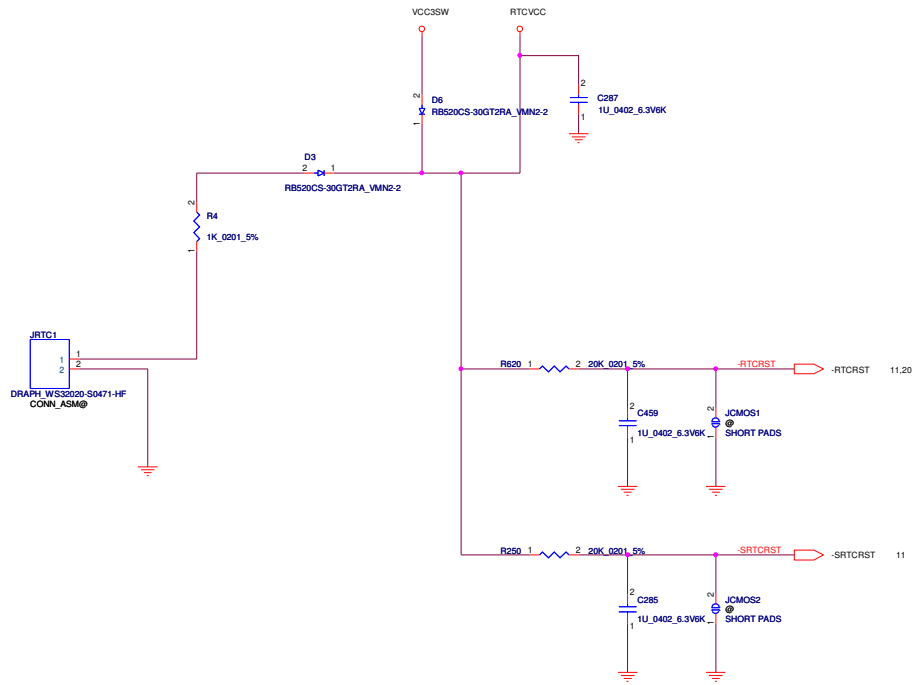


Table 21-2

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R509 R943	220 100	NO ASM NO ASM
TMS	R530 R946	220 100	NO ASM NO ASM
TDI	R515 R945	220 100	NO ASM NO ASM
TCK	R541	51	51
CPUCORE_PWRGD	R511	ASM	NO ASM
-RSMRST	R514	ASM	NO ASM
	JXDP2	ASM	NO ASM

↑
LOGIC



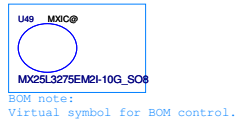
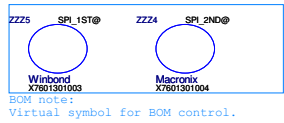
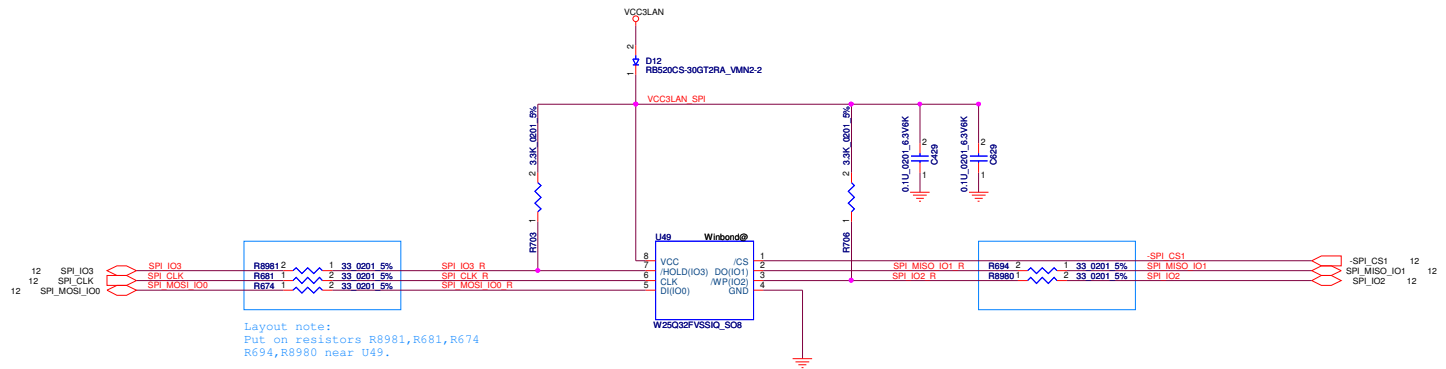
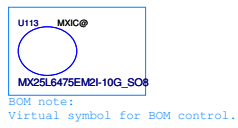
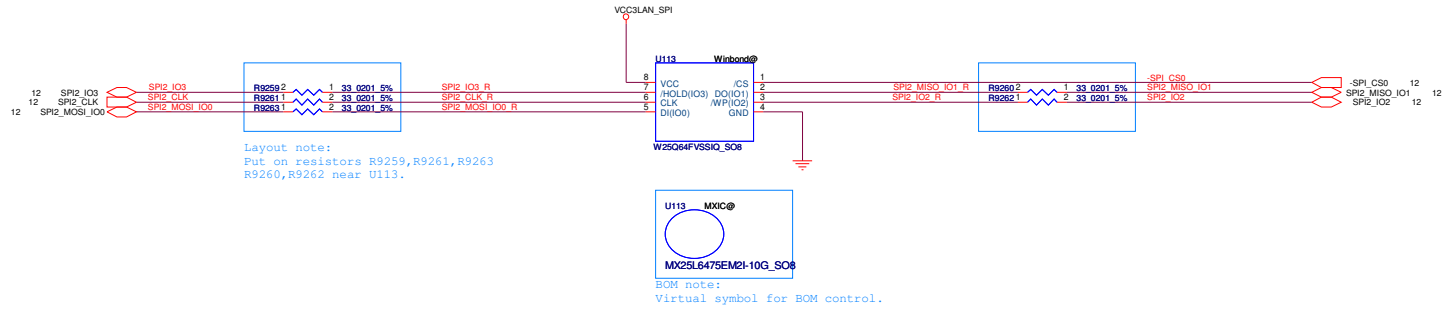


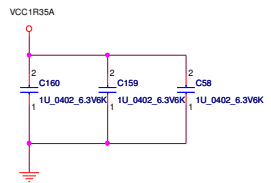
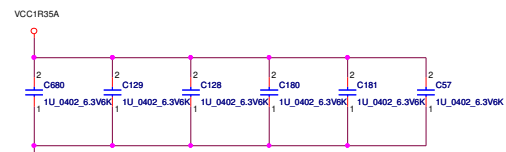
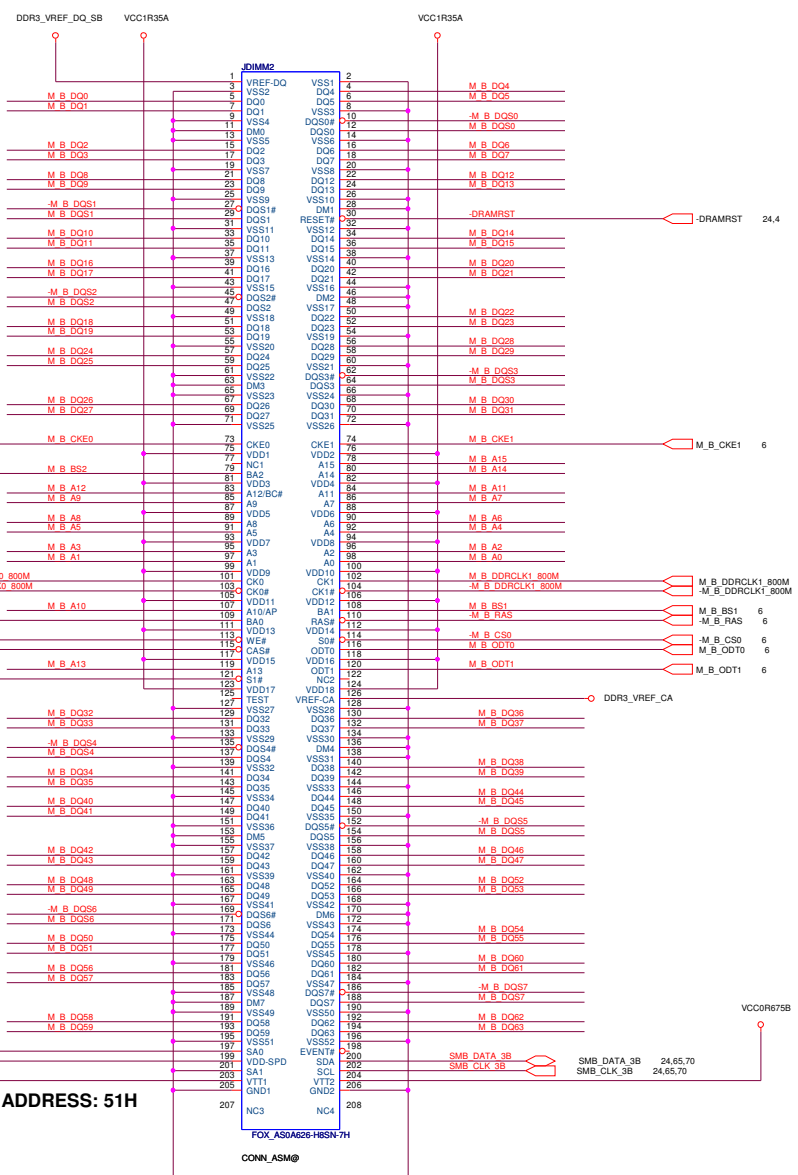
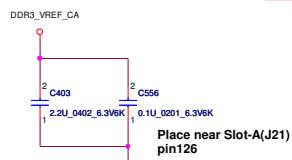
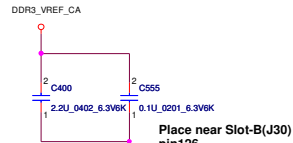
Table 23-1

SPI Configuration		Supplier	P/N
Single	Dual		
U113 (CS0#)		16MB Macronix Winbond (Numonyx)	MX25L12875FM2I-10G W25Q128FVSIQ
	U113 (CS0#)	8MB Macronix Winbond (Numonyx)	MX25L6475EM2I-10G W25Q64FVSIQ
	U49 (CS1#)	4MB Macronix Winbond (Numonyx)	MX25L3275EM2I-10G W25Q32FVSIQ

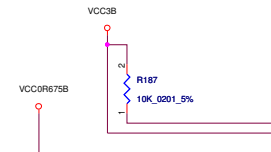
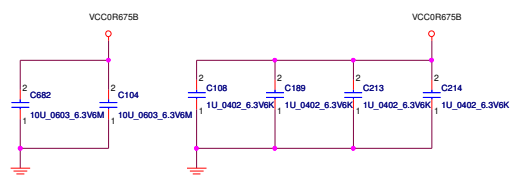
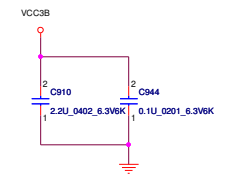
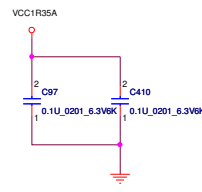
↑
LOGIC

Design Note:
MX25Lxxx73E may be mixed from SIT.
Don't mix it from FVT.



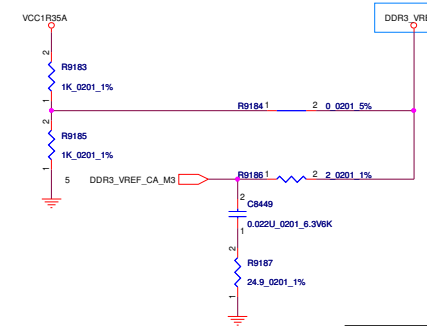


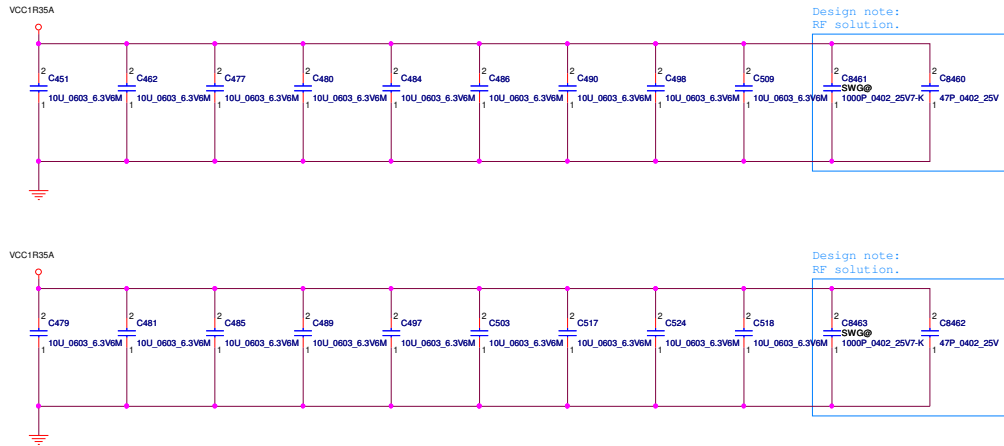
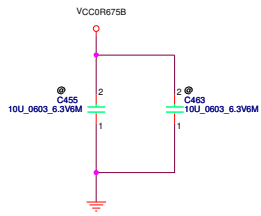
PLACE 1UF NEAR VCC1R35A PIN.



SPD ADDRESS: 51H

Layout note: trace width / spacing = 20/20mils

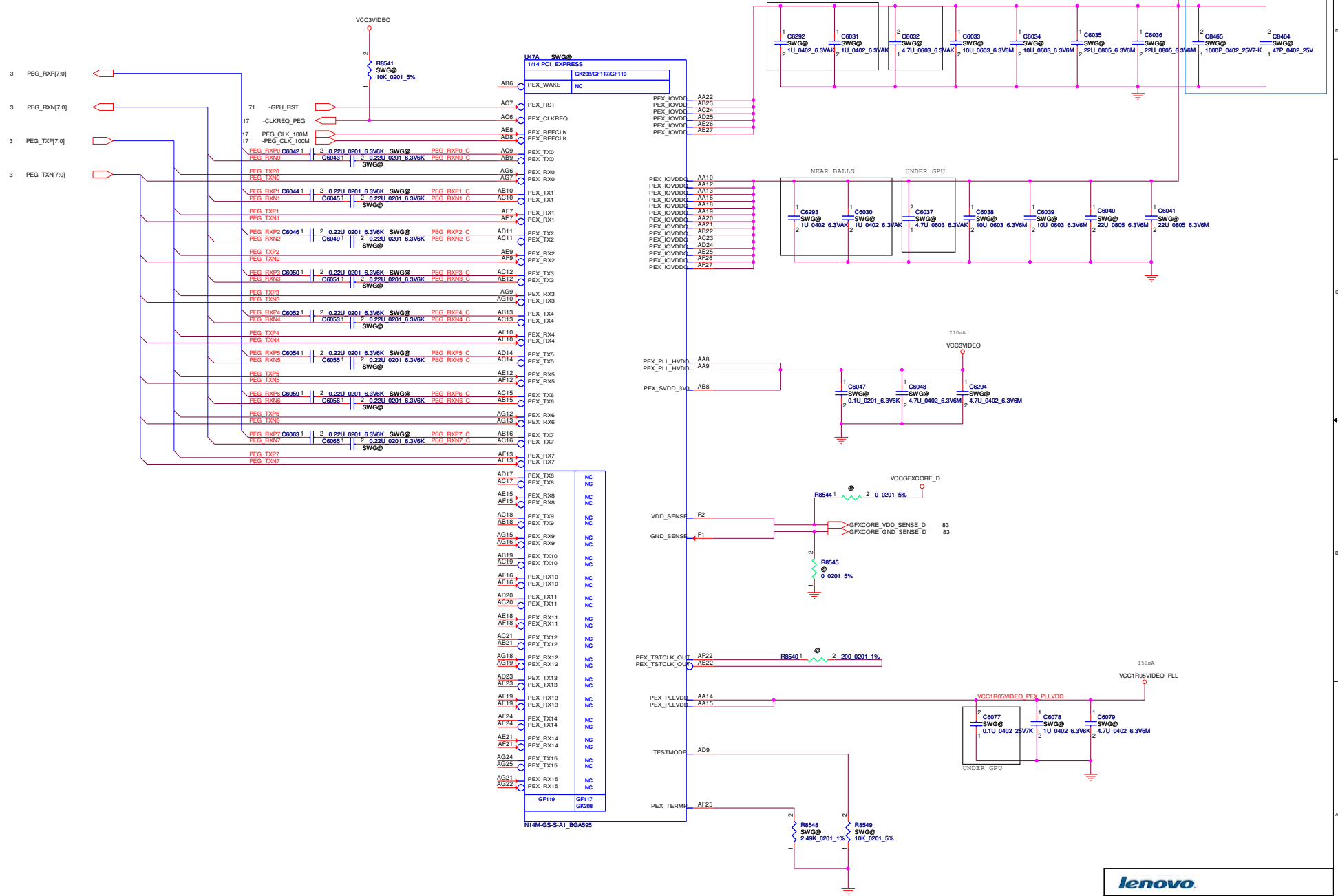




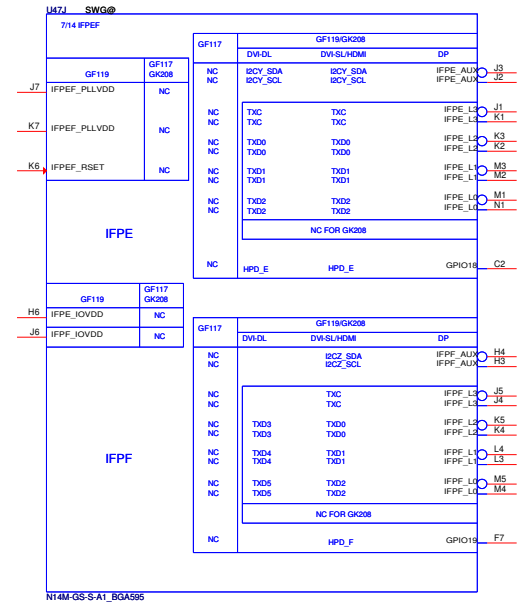
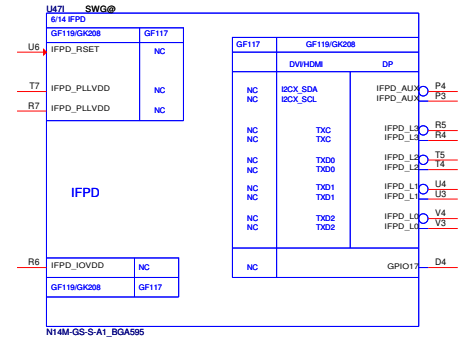
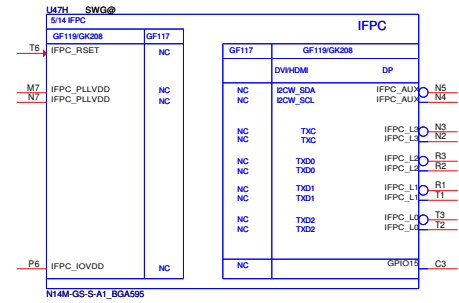
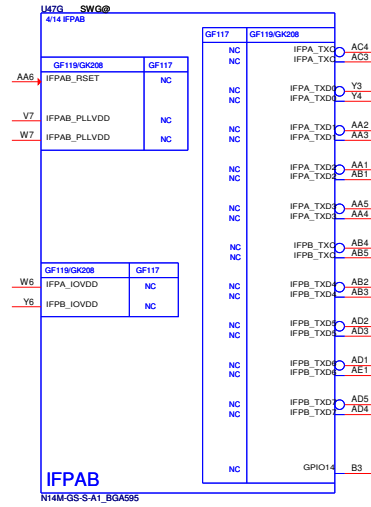
BOM note:
Virtual symbol for BOM control.



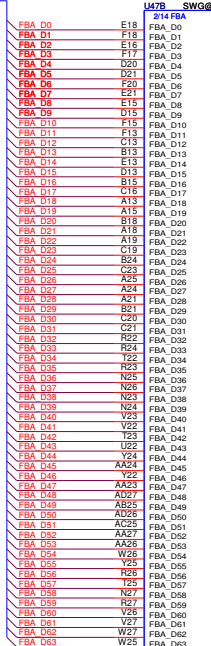
BOM note:
Virtual symbol for BOM control.



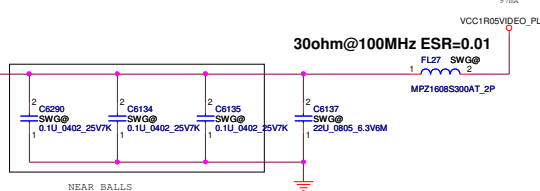
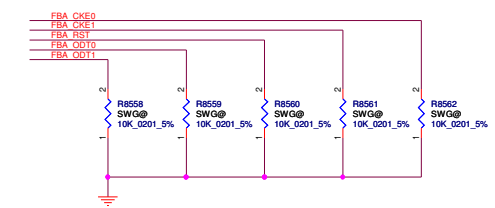
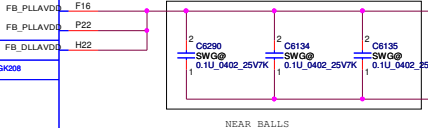
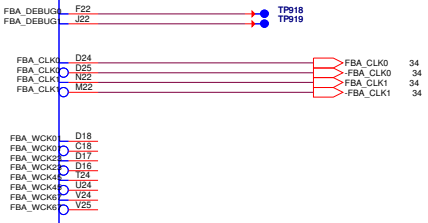
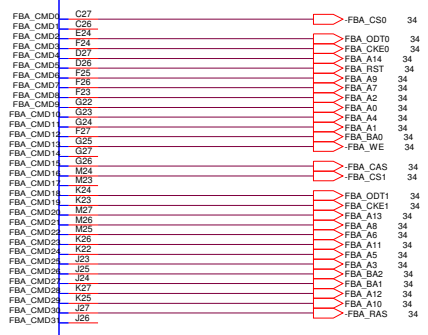
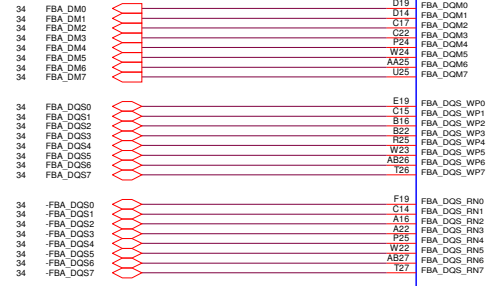
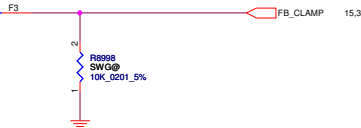
Design note:
RF solution.



34 FBA_D[63:0]



NC	FB_CLAMP
GF119	GF117GK208



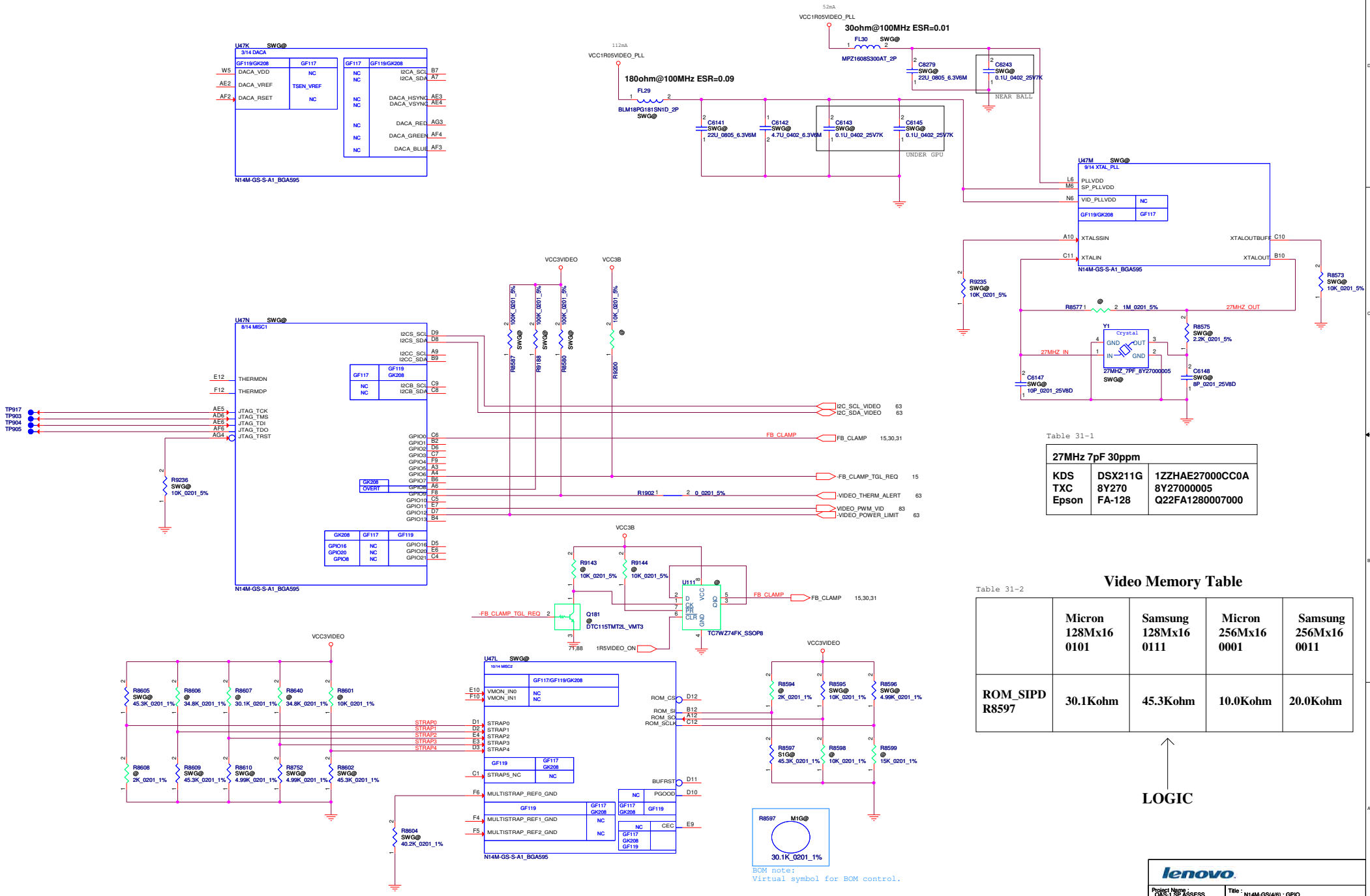


Table 31-1

27MHz 7pF 30ppm		
KDS	DSX211G	1ZZHAE27000CC0A
TXC	8Y270	8Y27000005
Epson	FA-128	Q22FA1280007000

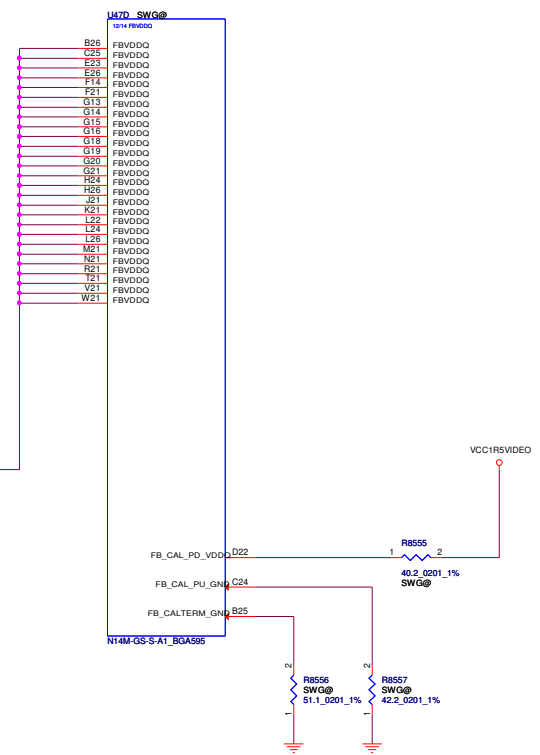
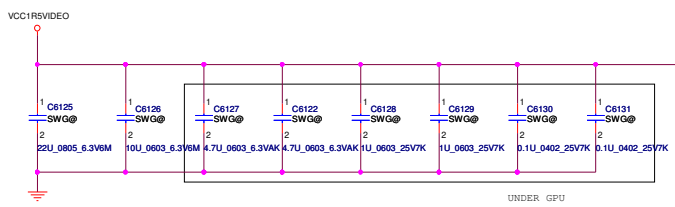
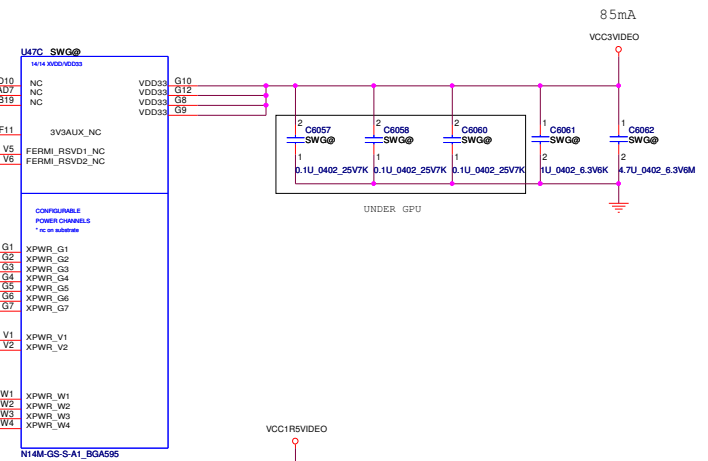
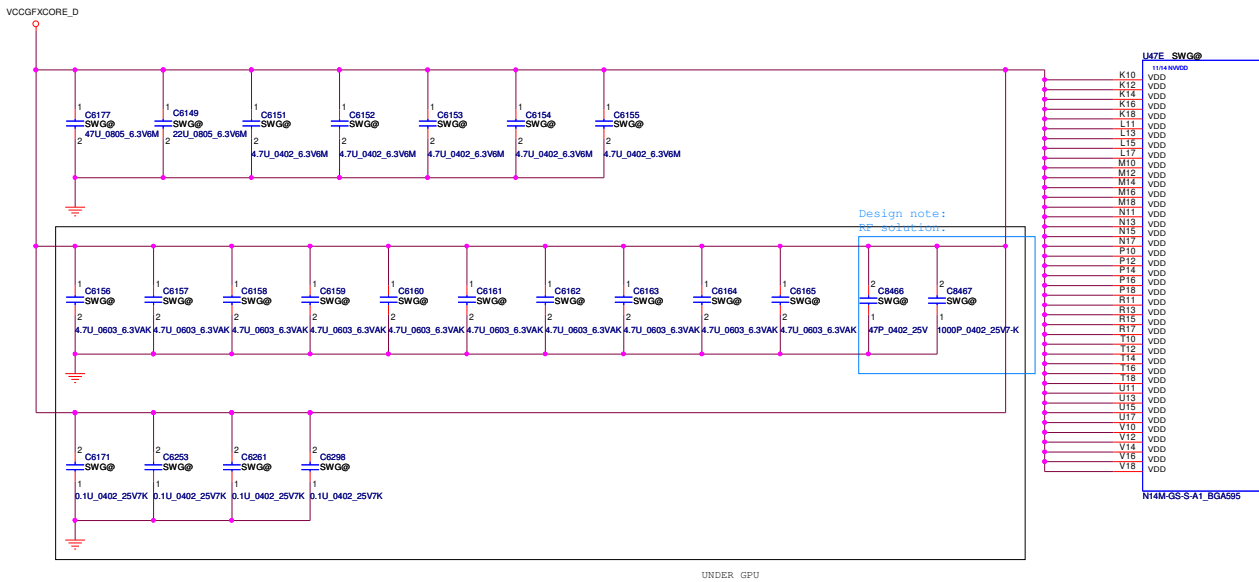
Table 31-2

Video Memory Table				
	Micron 128Mx16 0101	Samsung 128Mx16 0111	Micron 256Mx16 0001	Samsung 256Mx16 0011
ROM_SIPD R8597	30.1Kohm	45.3Kohm	10.0Kohm	20.0Kohm

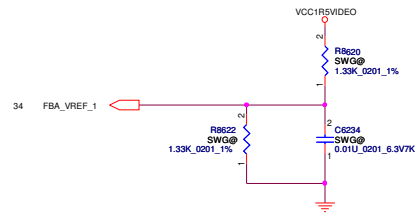
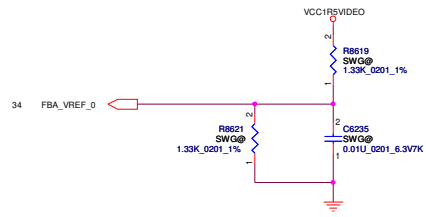
↑
LOGIC



BOM note:
Virtual symbol for BOM control.



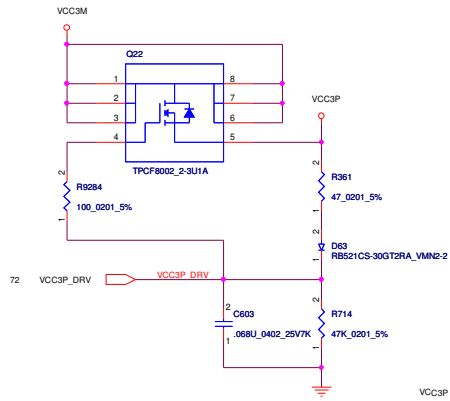




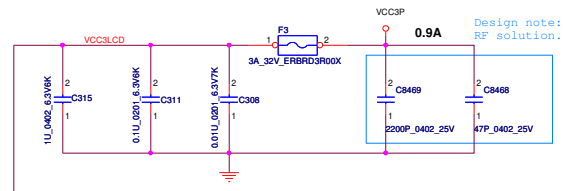
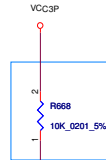
BLANK



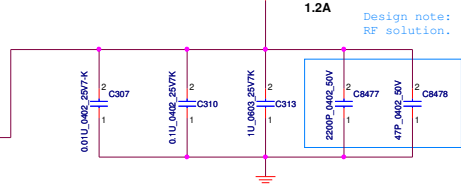
Project Name : CDS-1307-ASSESS		Title : BLANK	
Size : C	Document Number :	Rev :	1.01
Date : Monday, August 12, 2013		Sheet :	37 of 99



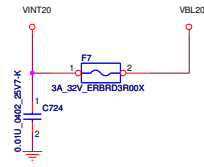
Design note:
14.0"HD/HD+ panels have 100Kohm PD,
it affects Backlight_On signal voltage
there is no margin for on threshold.



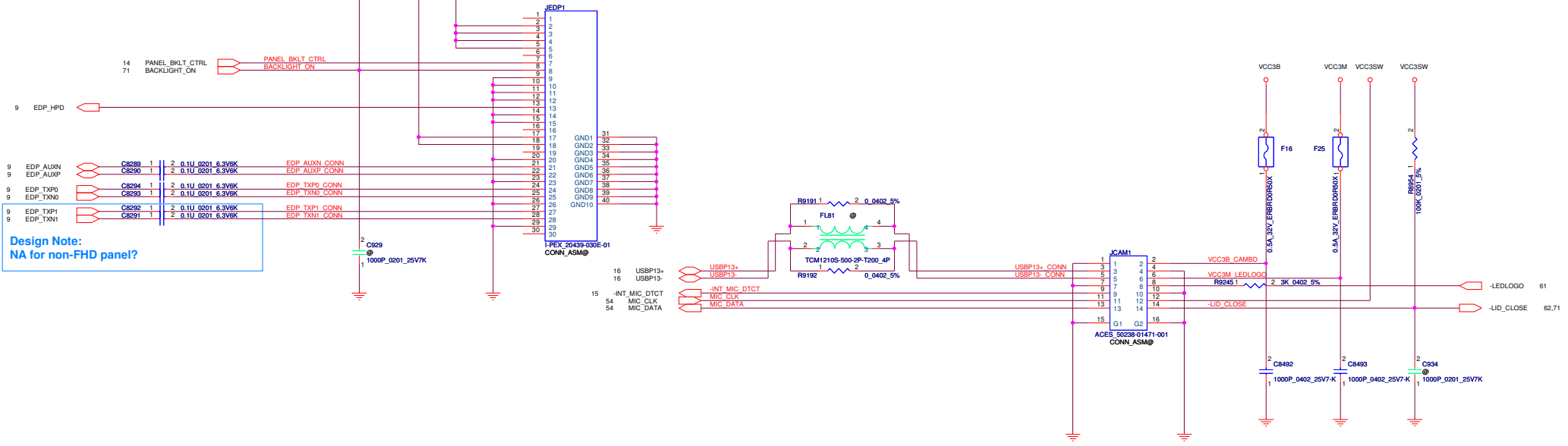
Design note:
RF solution.



Design note:
RF solution.



LCD CONNECTOR



Design Note:
NA for non-FHD panel?

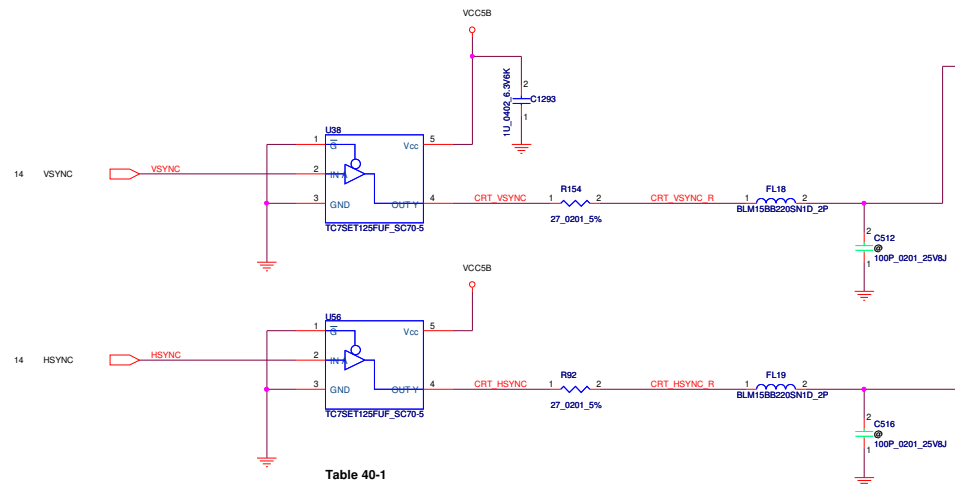
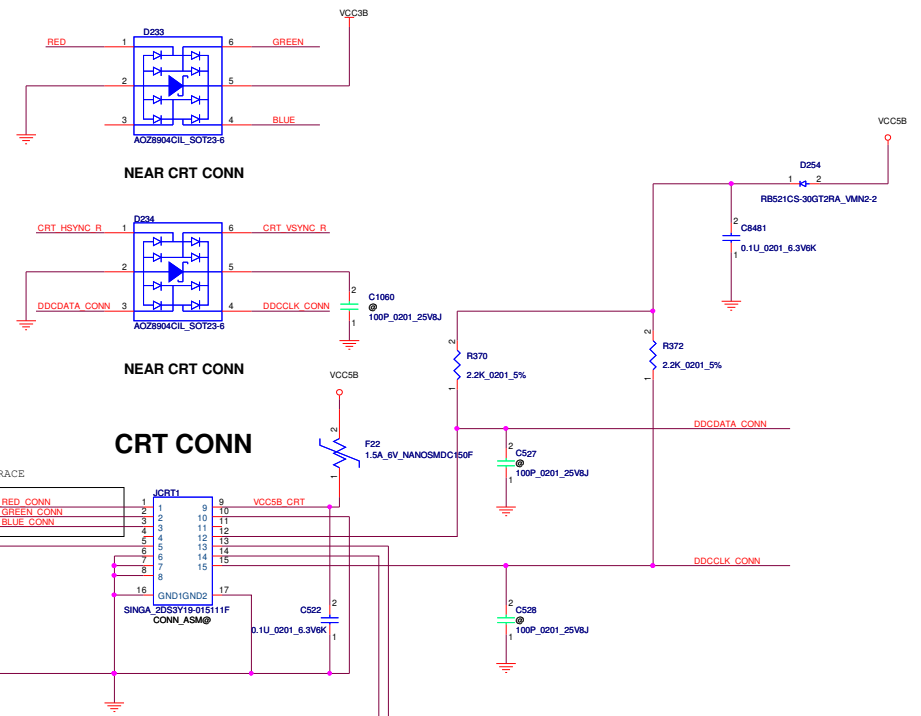
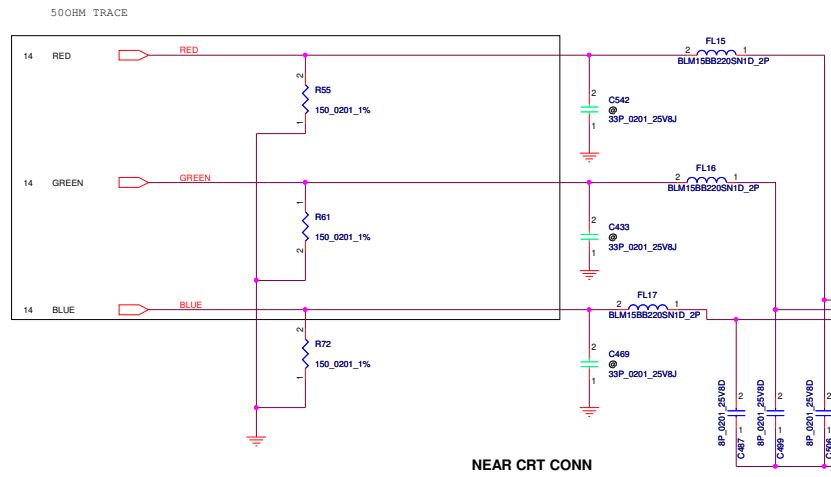
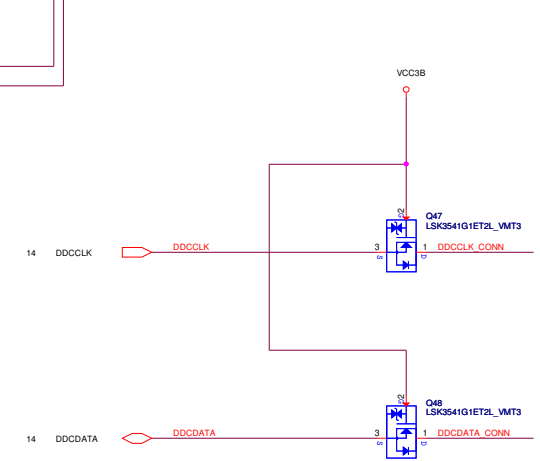
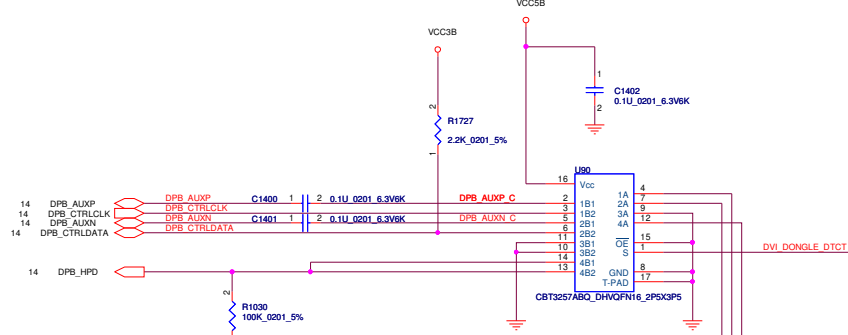


Table 40-1

CRT Sync Buffer table (U38, U56)	
TOSHIBA	TC7SET125FU
NXP	74AHCT1G125GW





Design Note:
To check the direction of
body diode with vendor.

Table 41-1

U90 assignment	
NXP	CBT3257ABQ
ON-Semi	74FST3257MNTWG

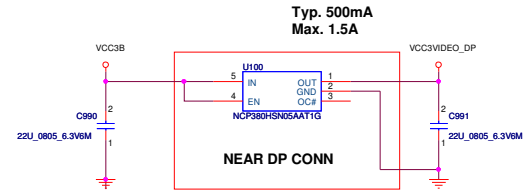
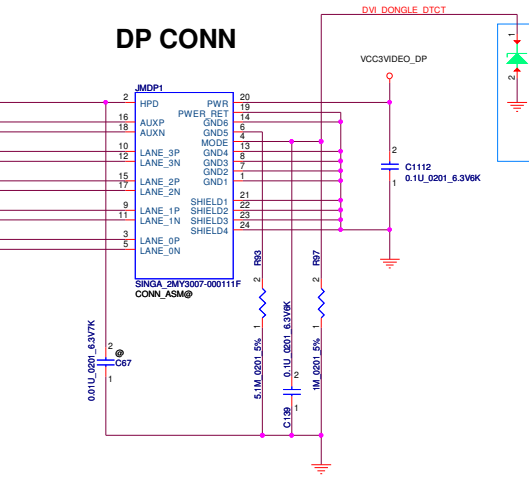
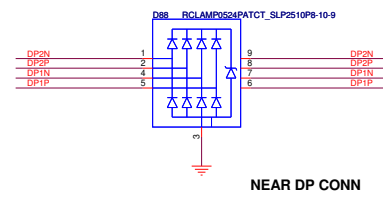
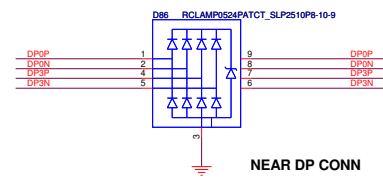
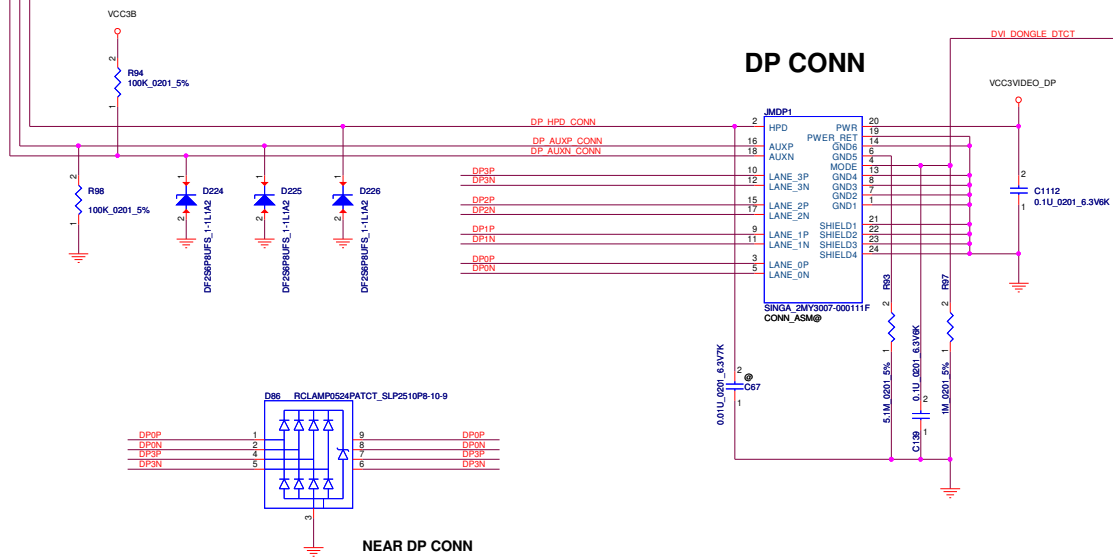
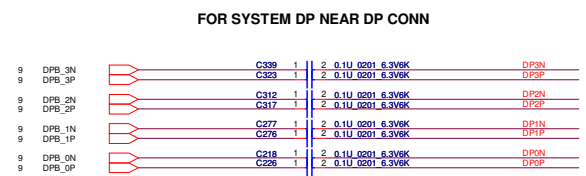
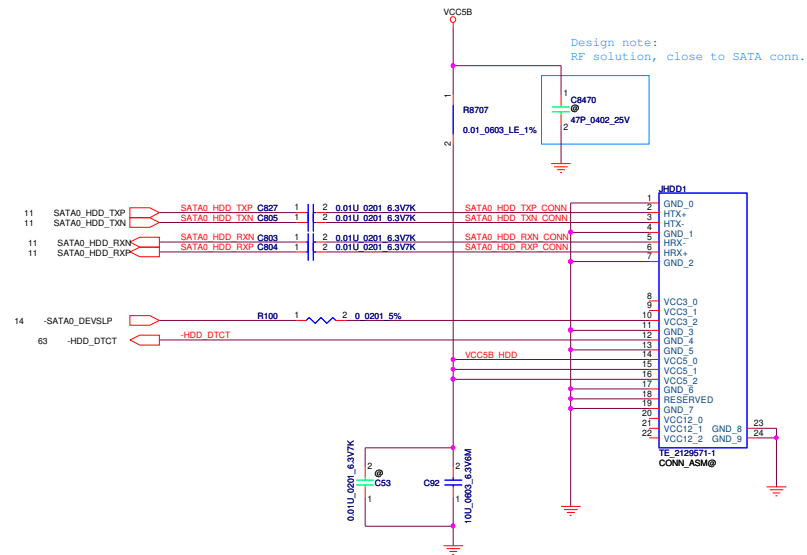
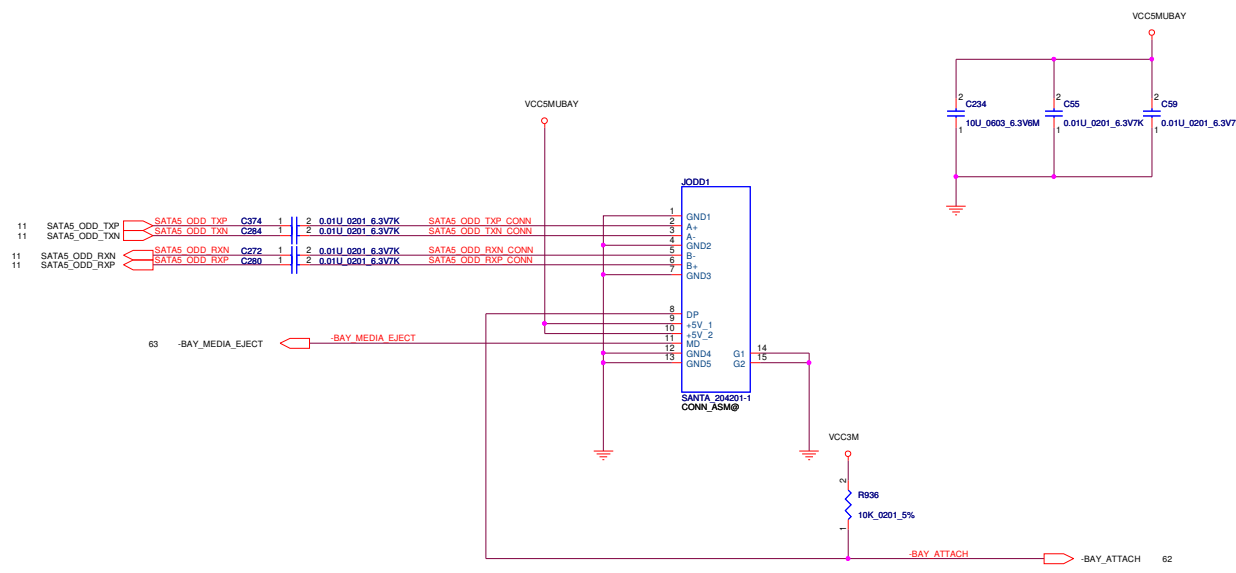


Table 41-2

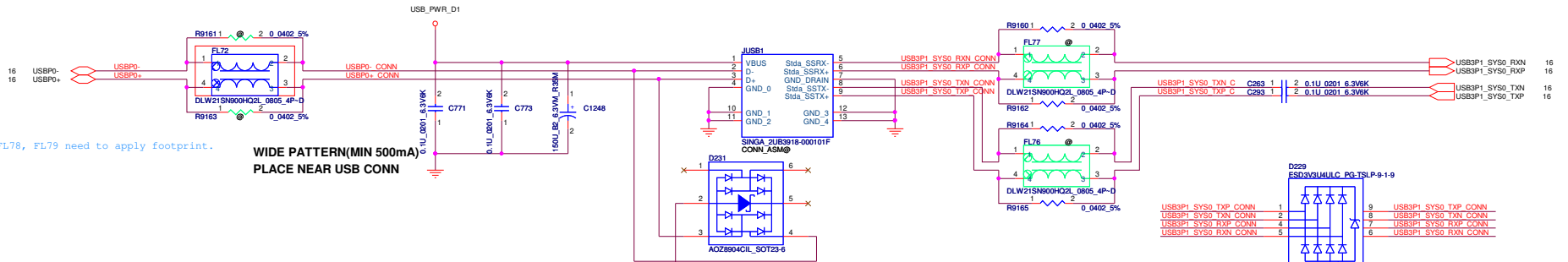
U100 assignment	
TI	TPS2530
ON-Semi	NCP380HSN05AATG



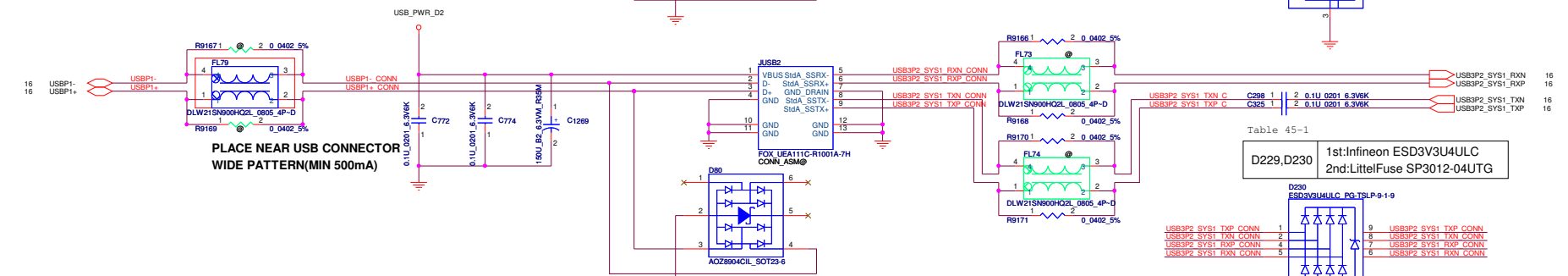


11	SATAS_ODD_TXP	SATAS_ODD_TXP	C374	1	2	0.01U	0201	6.3V7K	SATAS_ODD_TXP_CONN
11	SATAS_ODD_TXN	SATAS_ODD_TXN	C284	1	2	0.01U	0201	6.3V7K	SATAS_ODD_TXN_CONN
11	SATAS_ODD_RXN	SATAS_ODD_RXN	C272	1	2	0.01U	0201	6.3V7K	SATAS_ODD_RXN_CONN
11	SATAS_ODD_RXP	SATAS_ODD_RXP	C280	1	2	0.01U	0201	6.3V7K	SATAS_ODD_RXP_CONN

Layout note:
FL72, FL75, FL78, FL79 need to apply footprint.



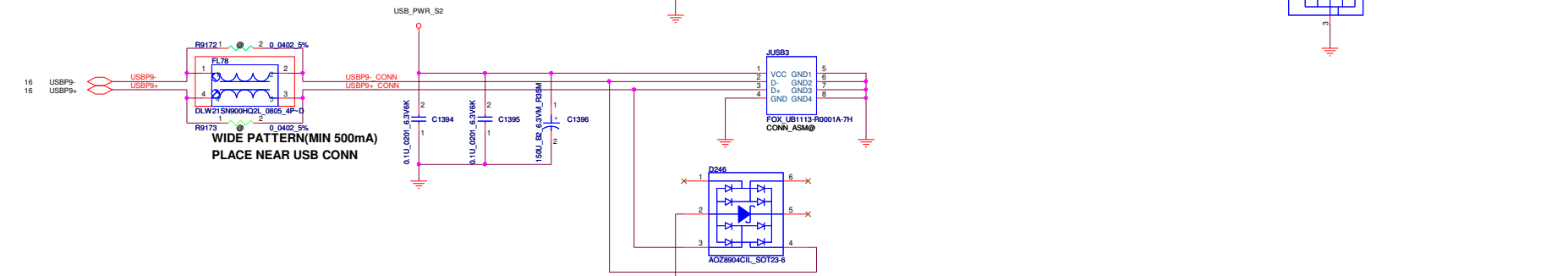
WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONN



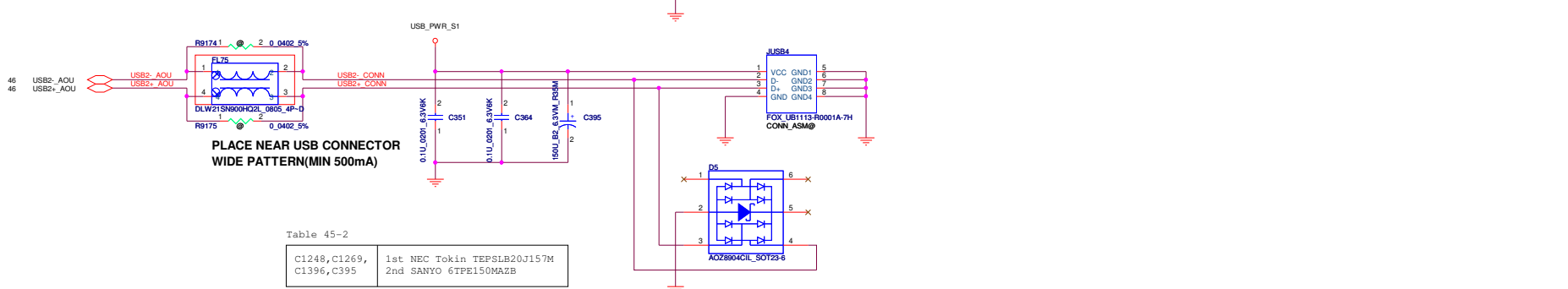
PLACE NEAR USB CONNECTOR
WIDE PATTERN(MIN 500mA)

Table 45-1

D229, D230	1st:Infineon ESD3V3U4ULC
	2nd:Littelfuse SP3012-04UTG



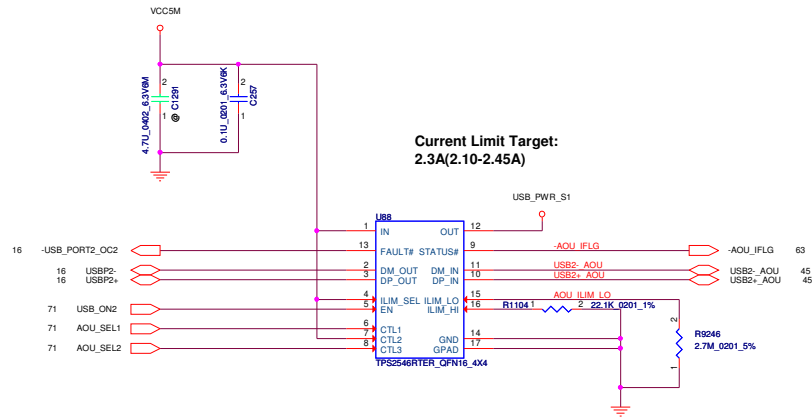
WIDE PATTERN(MIN 500mA)
PLACE NEAR USB CONN



PLACE NEAR USB CONNECTOR
WIDE PATTERN(MIN 500mA)

Table 45-2

C1248, C1269, C1396, C395	1st NEC Tokin TEPSLB20J157M 2nd SANYO 6TPE150MAZB
---------------------------	--



Current Limit Target:
2.3A(2.10-2.45A)

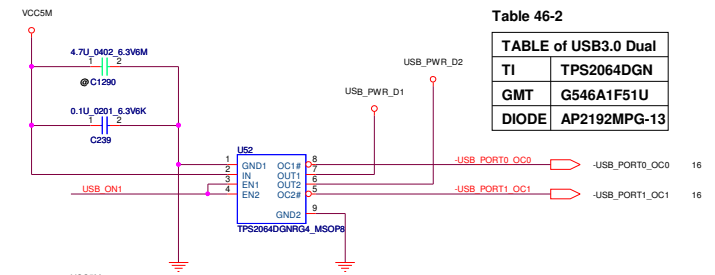


Table 46-2

TABLE of USB3.0 Dual	
TI	TPS2064DGN
GMT	G546A1F51U
DIODE	AP2192MPG-13

FOR ON BOARD DUAL USB 3.0 CONNECTOR

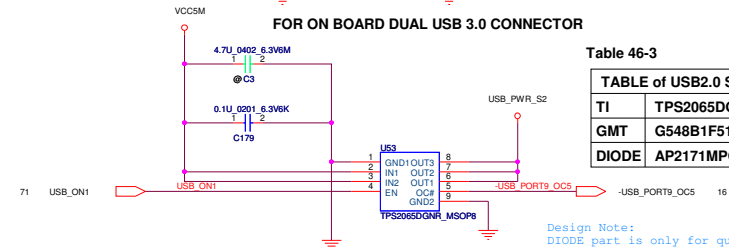
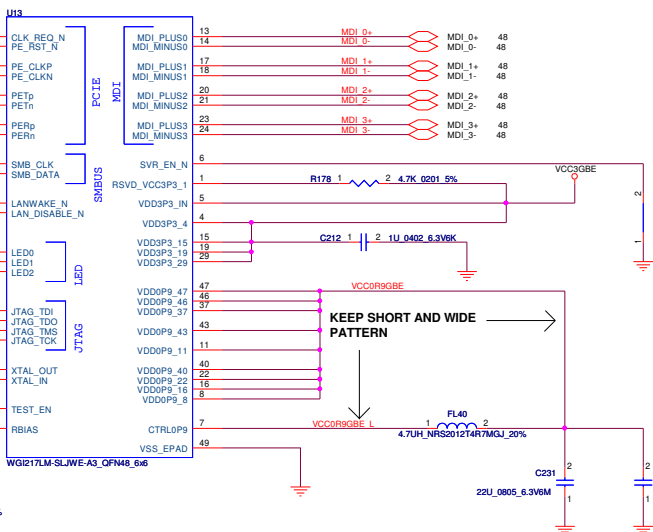
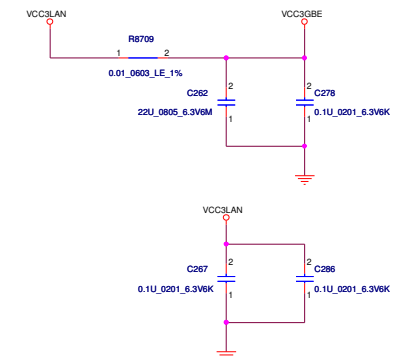
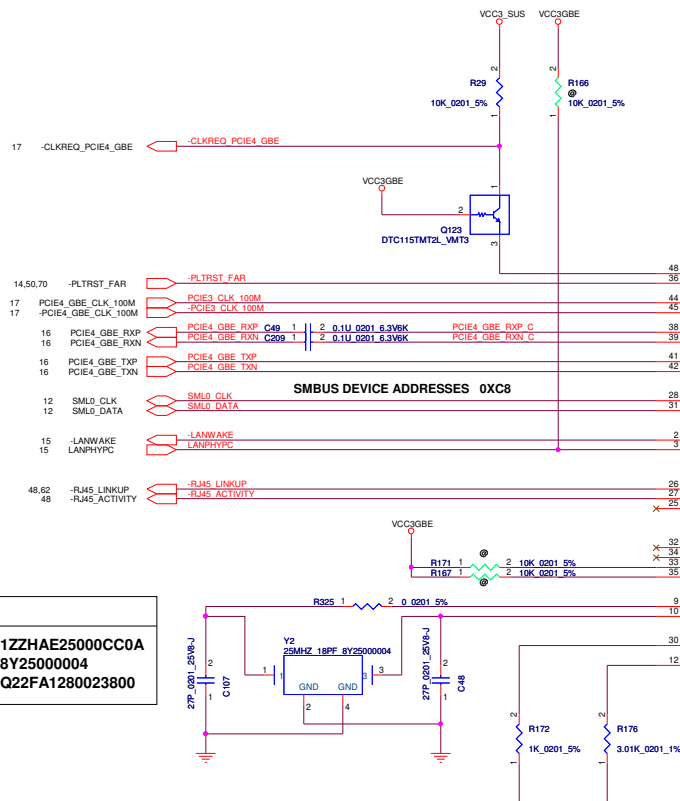


Table 46-3

TABLE of USB2.0 Single	
TI	TPS2065DGN
GMT	G548B1F51U
DIODE	AP2171MPG-13

FOR ON BOARD SINGLE USB 2.0 CONNECTOR

Design Note:
DIODE part is only for qualification purpose.
It will be dropped before SVT if GCM does not approve.



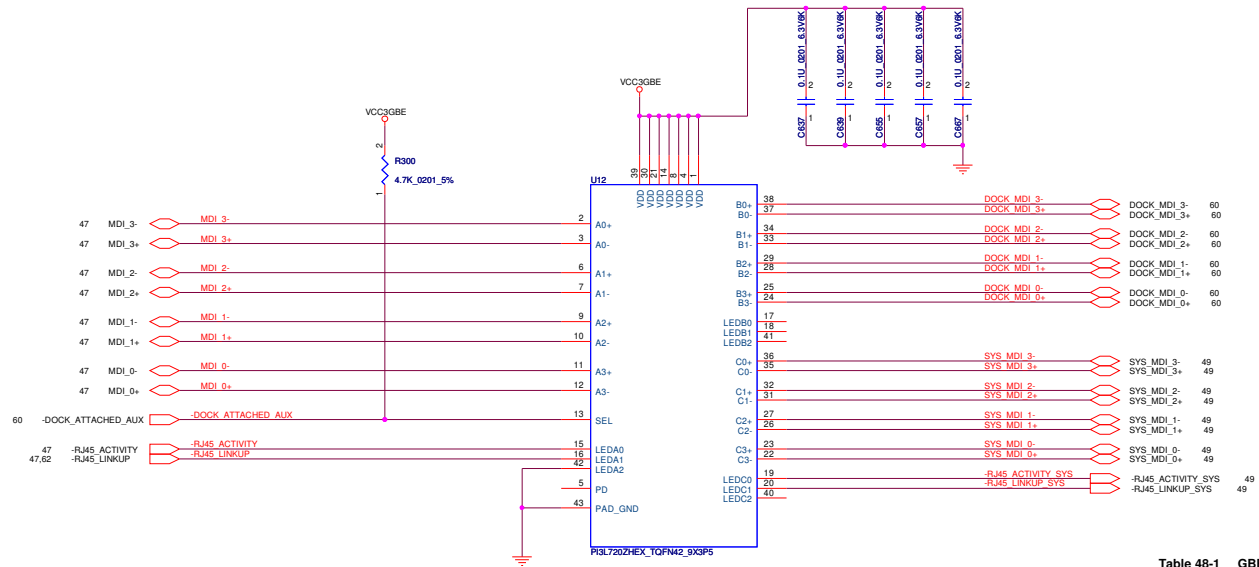
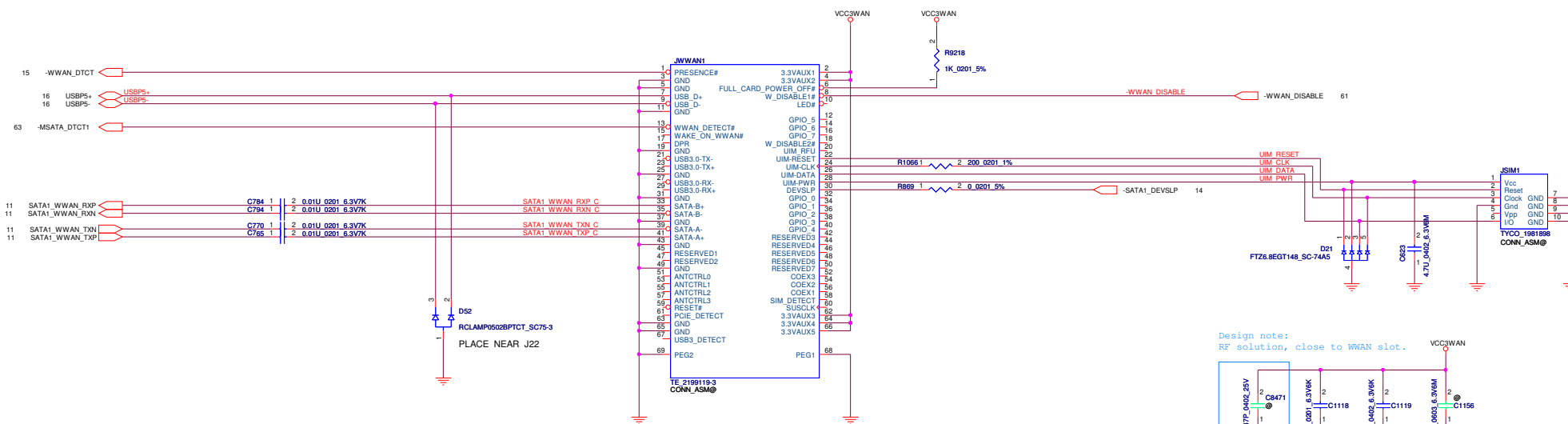


Table 48-1 GBE LAN SWITCH

Pericom	PI3L720ZHE
STmicro	STMUX1800E
Onsemi	NCN7201

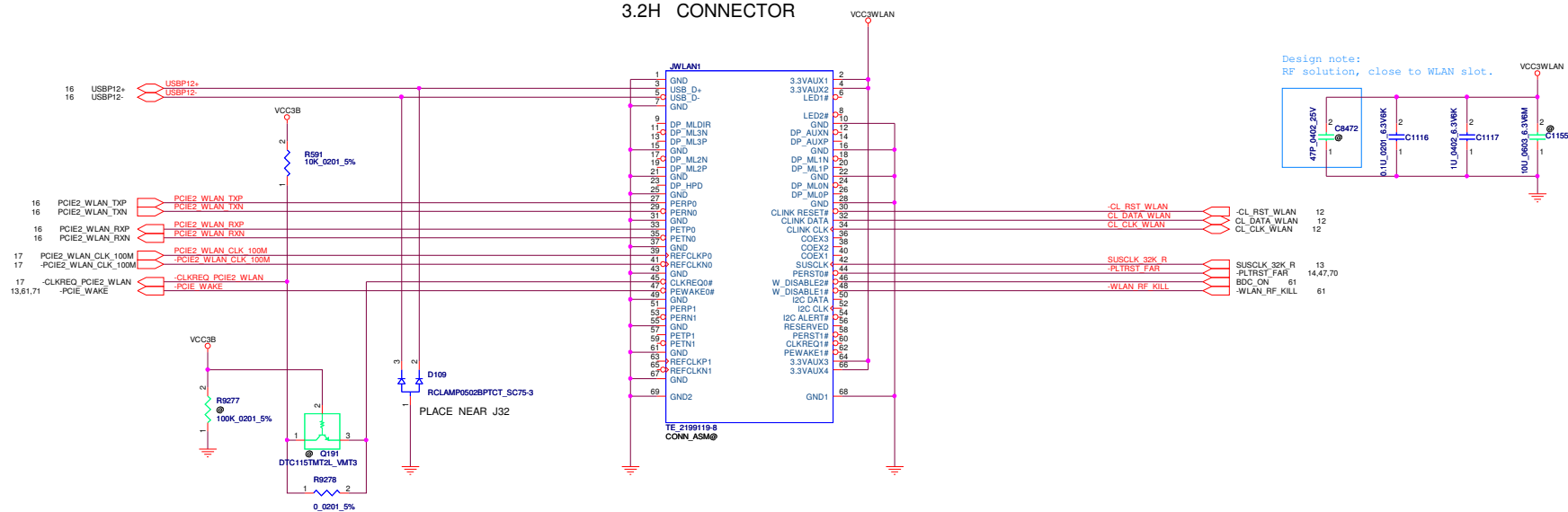
TYPE-B NGFF CARD FOR WWAN/SSD

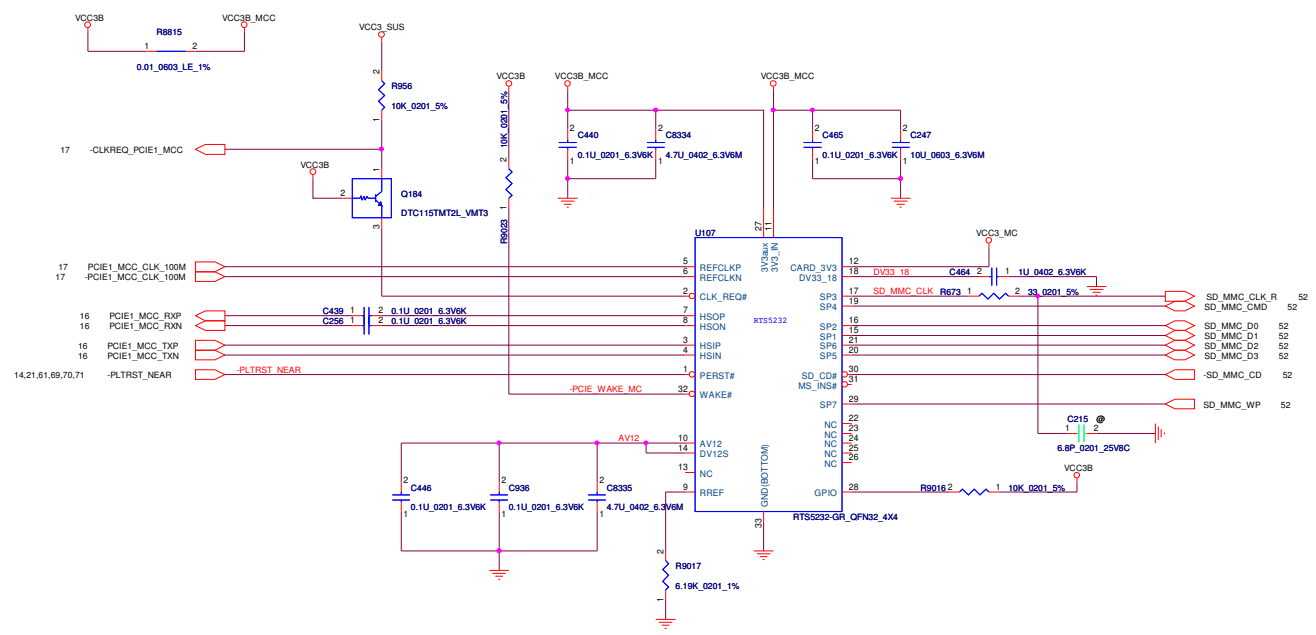
3.2H CONNECTOR

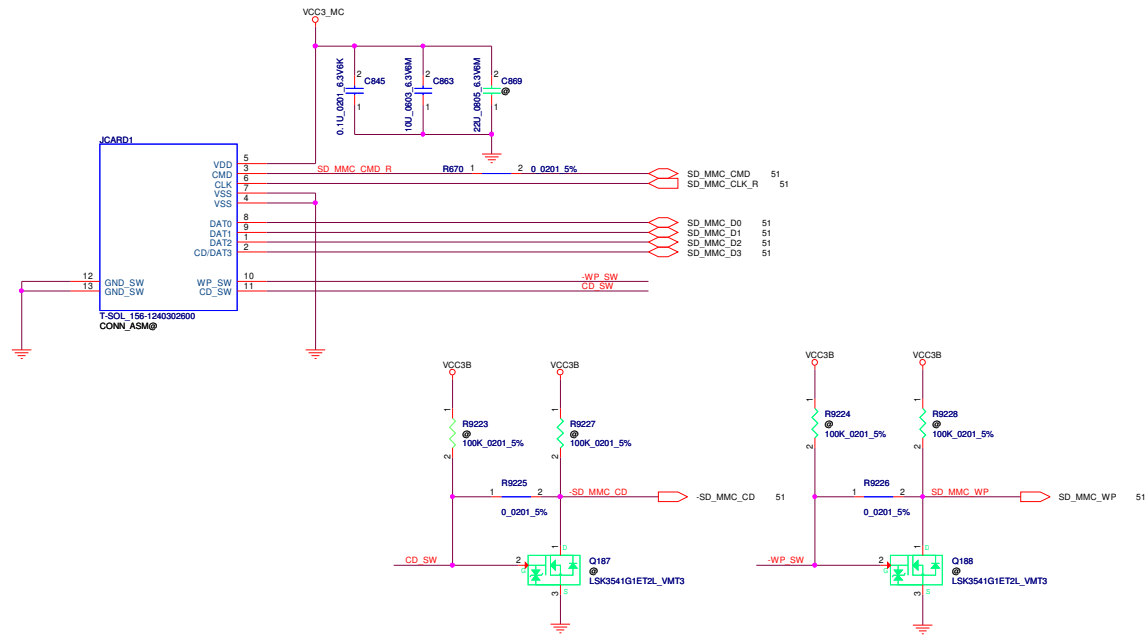


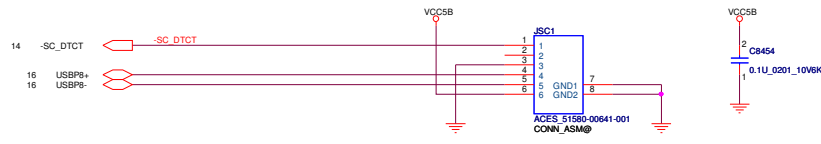
TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR



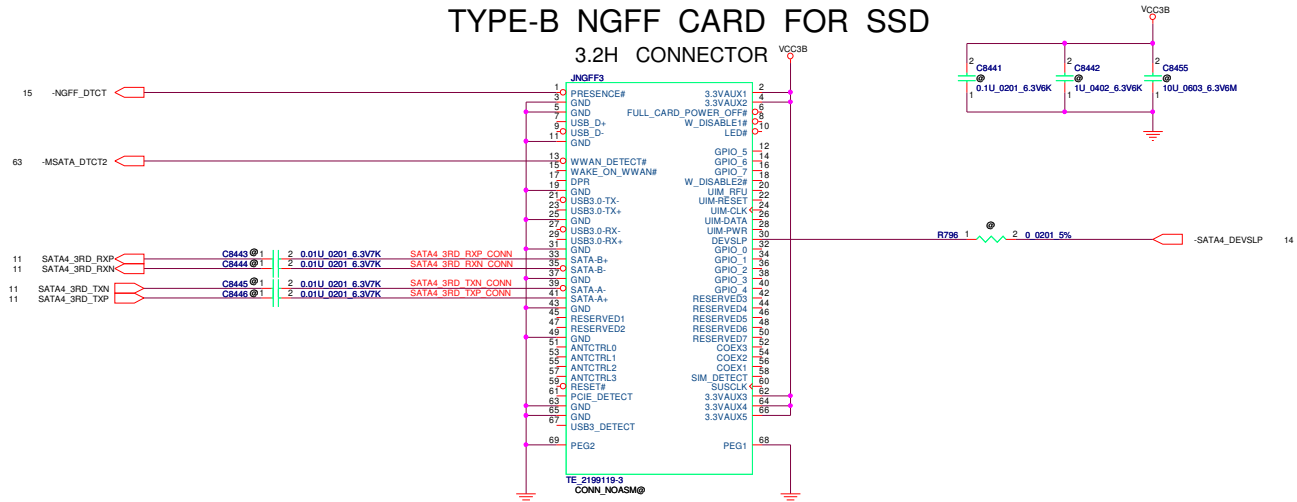


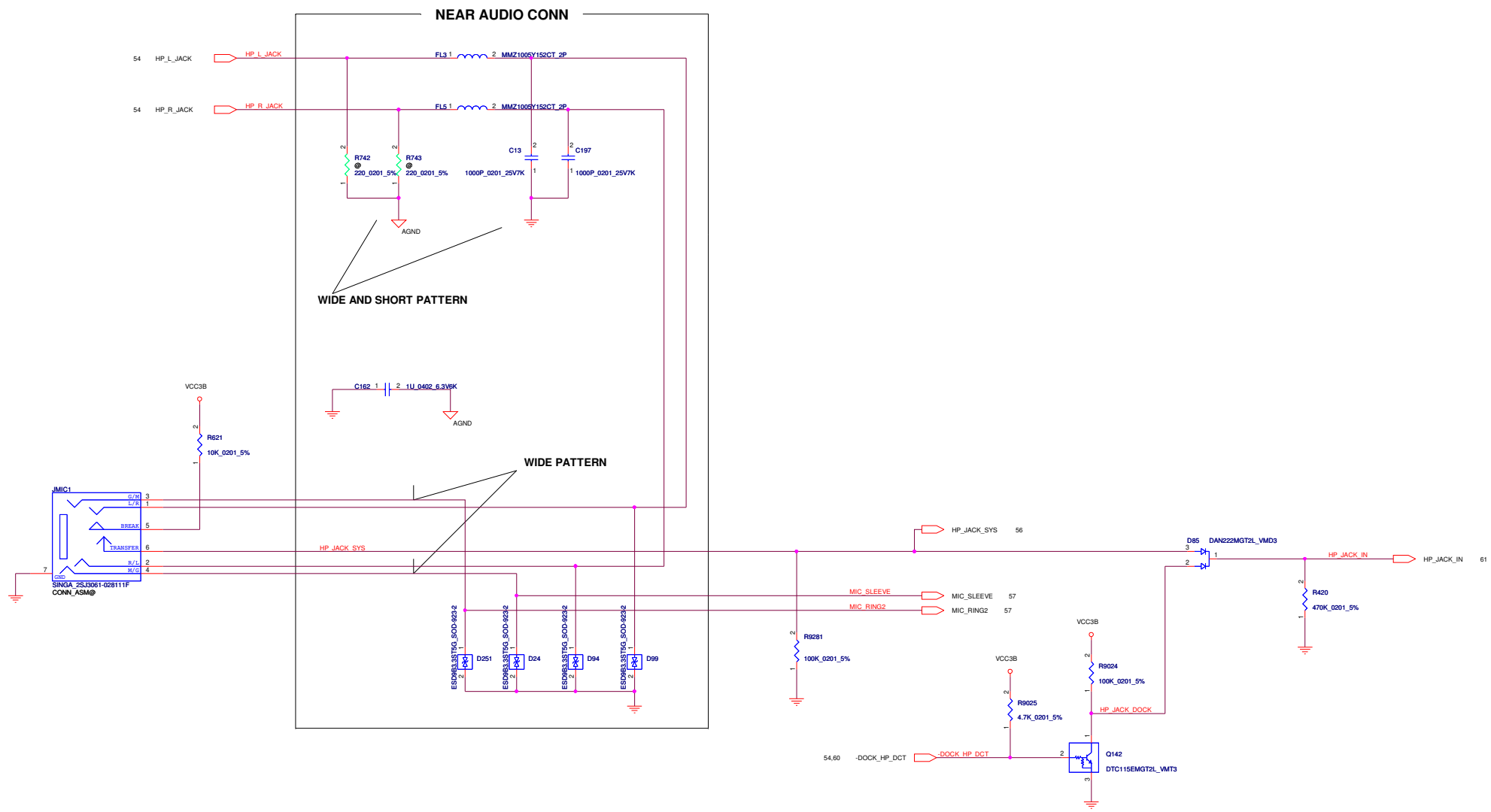




TYPE-B NGFF CARD FOR SSD

3.2H CONNECTOR





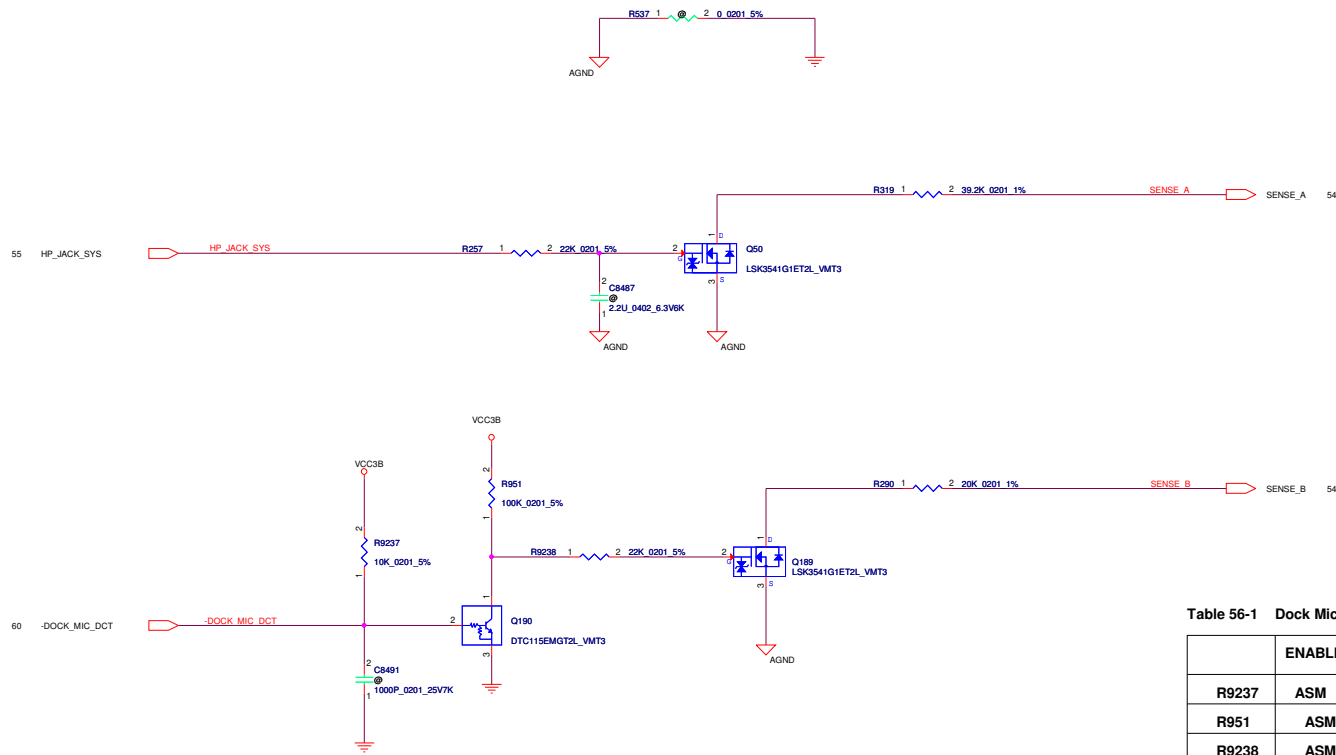
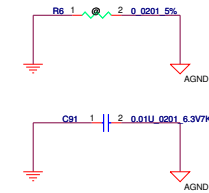
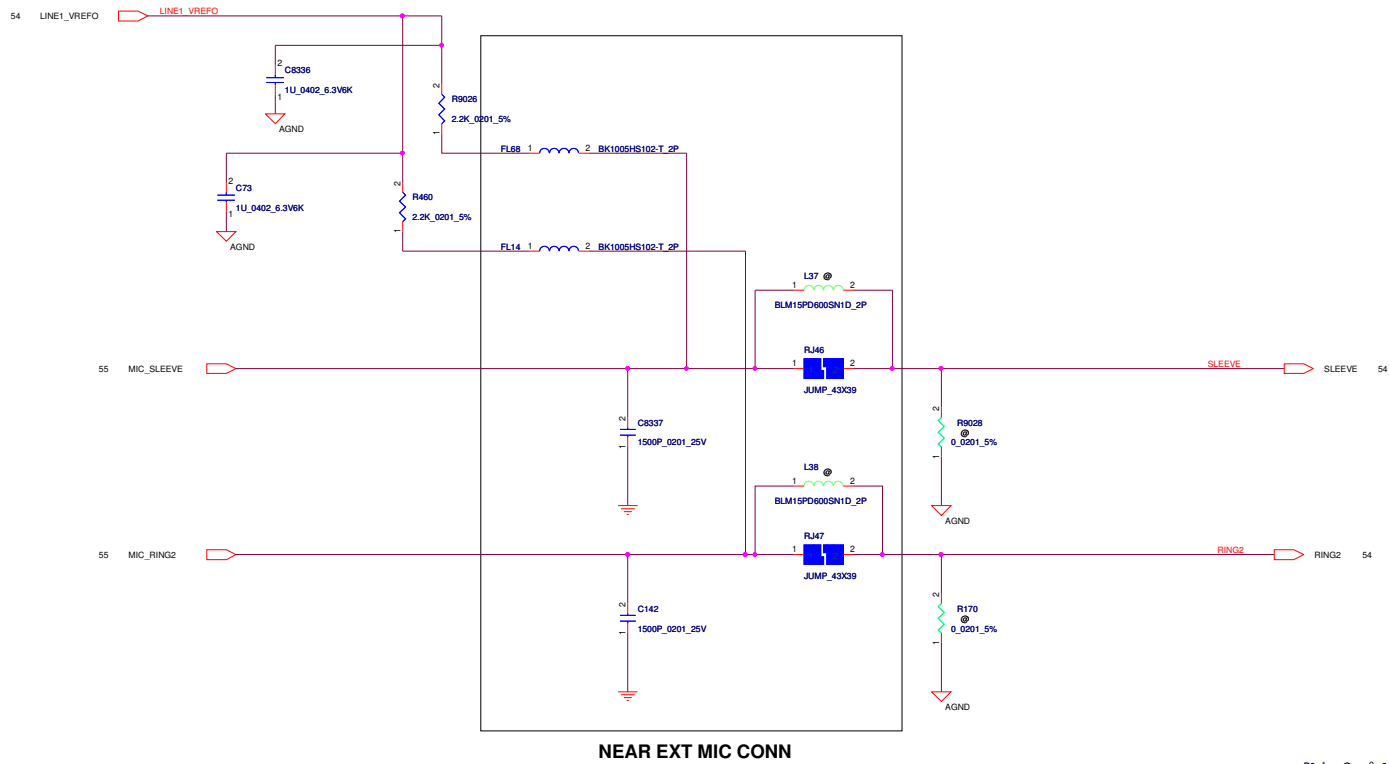


Table 56-1 Dock Mic HW Enable/Disable

	ENABLE	DISABLE
R9237	ASM	NO ASM
R951	ASM	NO ASM
R9238	ASM	NO ASM
R290	ASM	NO ASM
Q190	ASM	NO ASM
Q189	ASM	NO ASM

↑
Logic



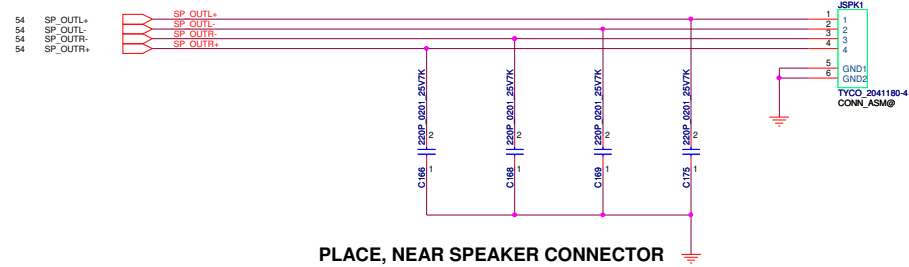
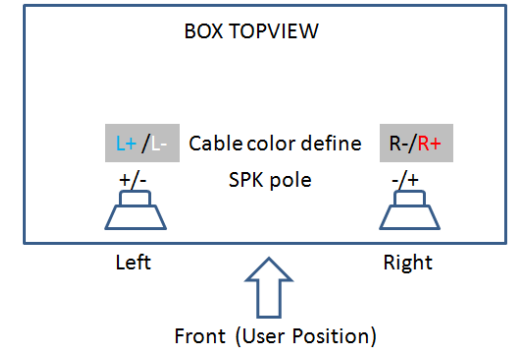
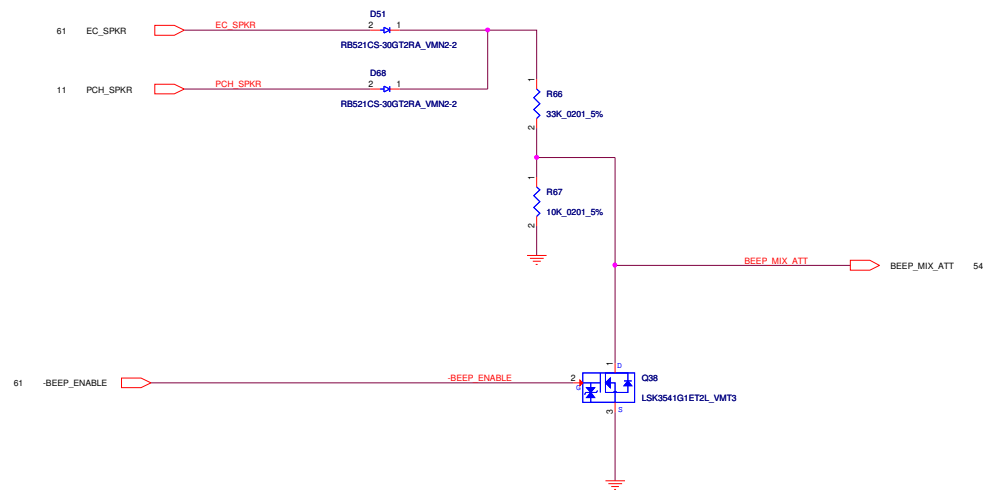


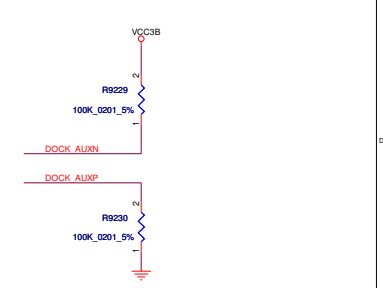
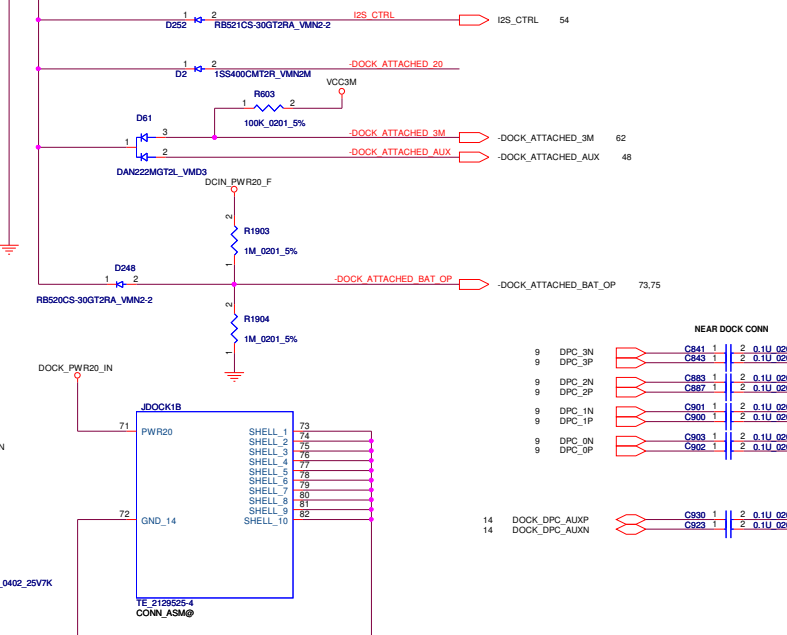
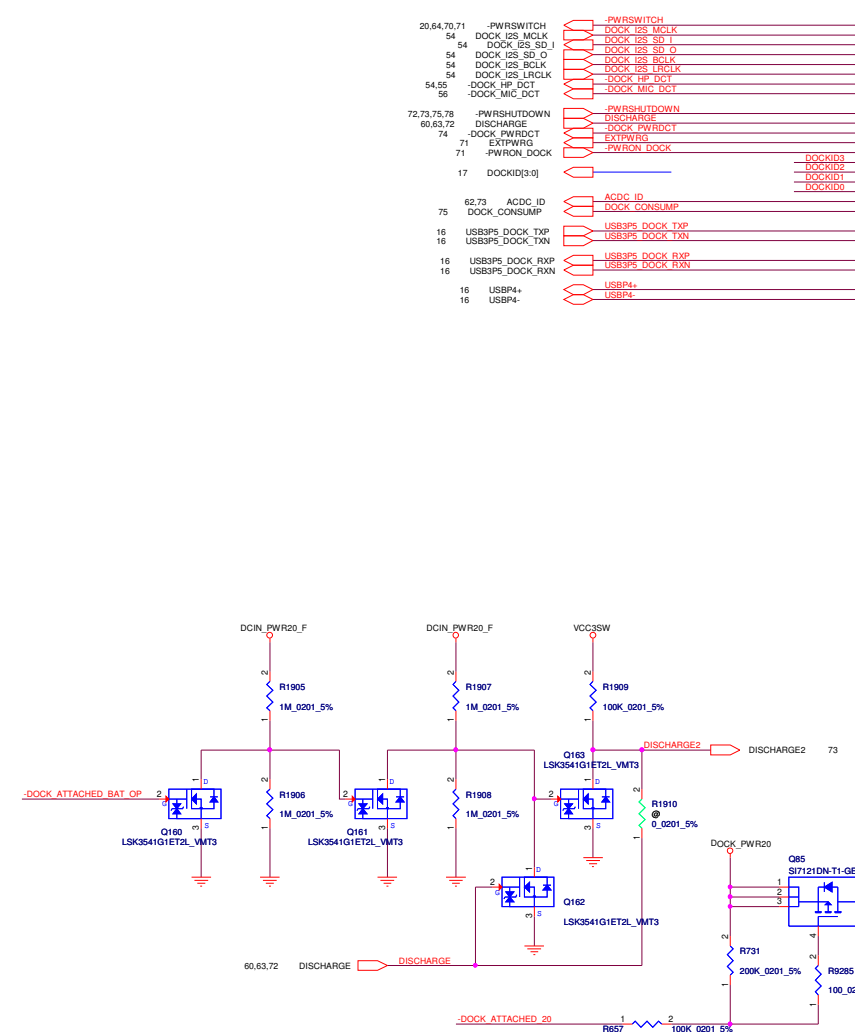
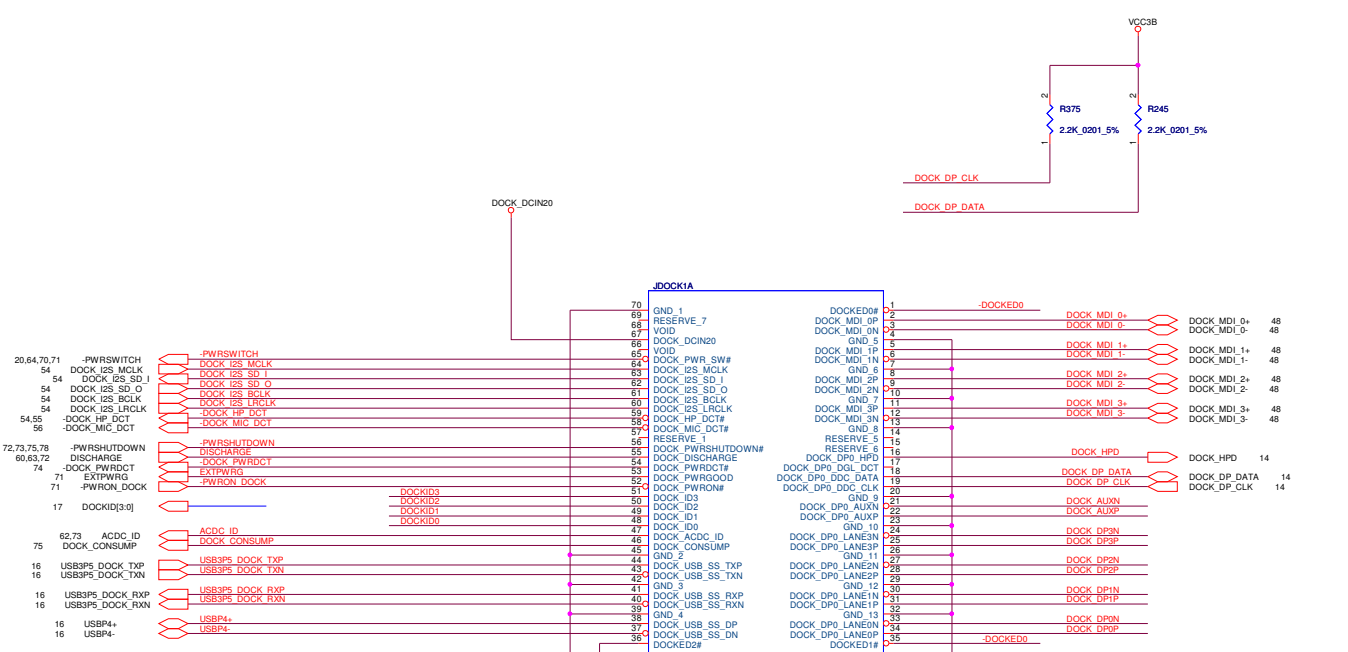
Table 58-1

Assign	Netname	Cable Color
Pin 1	SP_OUTL+	Blue
Pin 2	SP_OUTL-	White
Pin 3	SP_OUTR-	Black
Pin 4	SP_OUTR+	Red

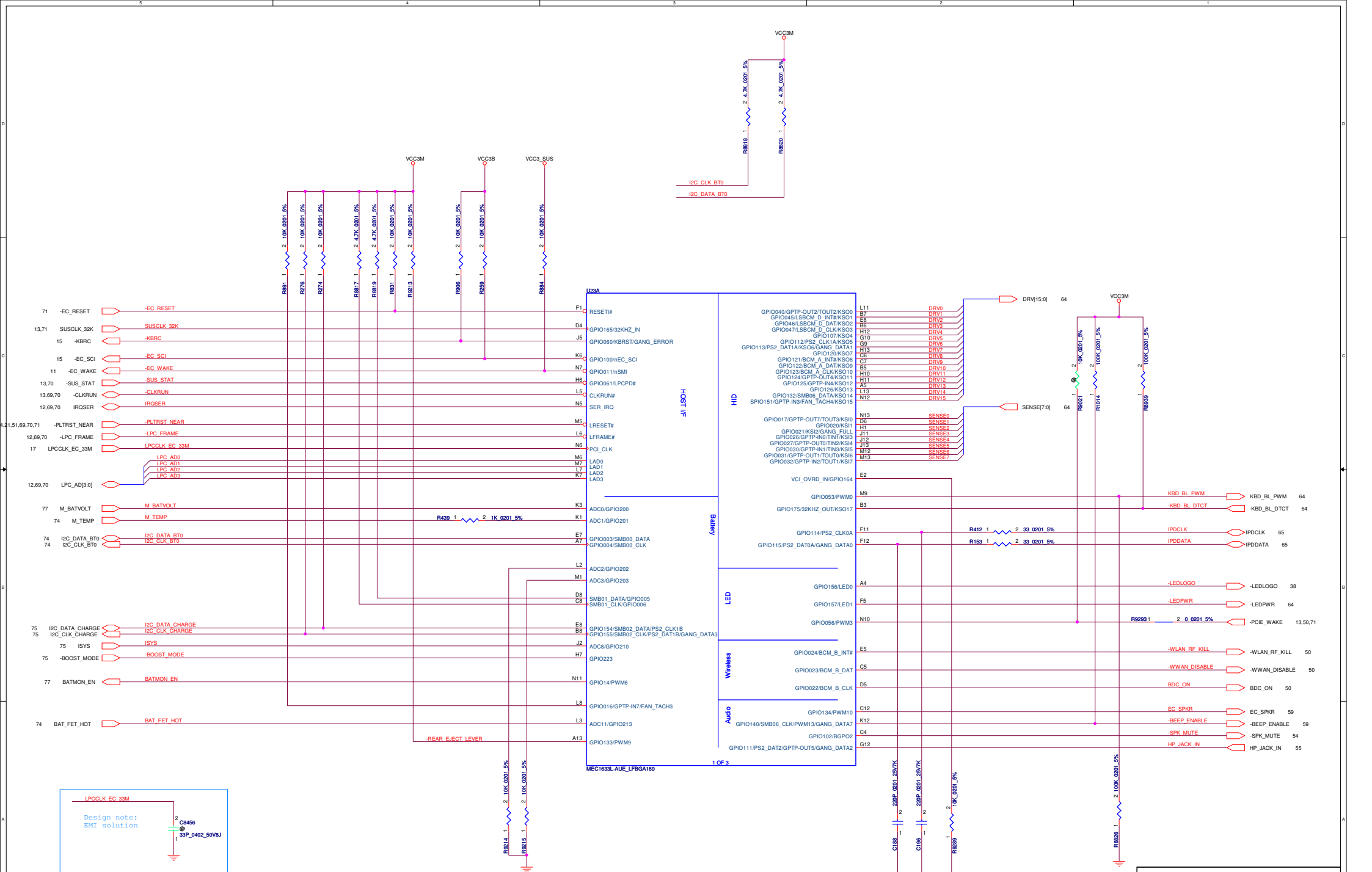
Figure 58-1



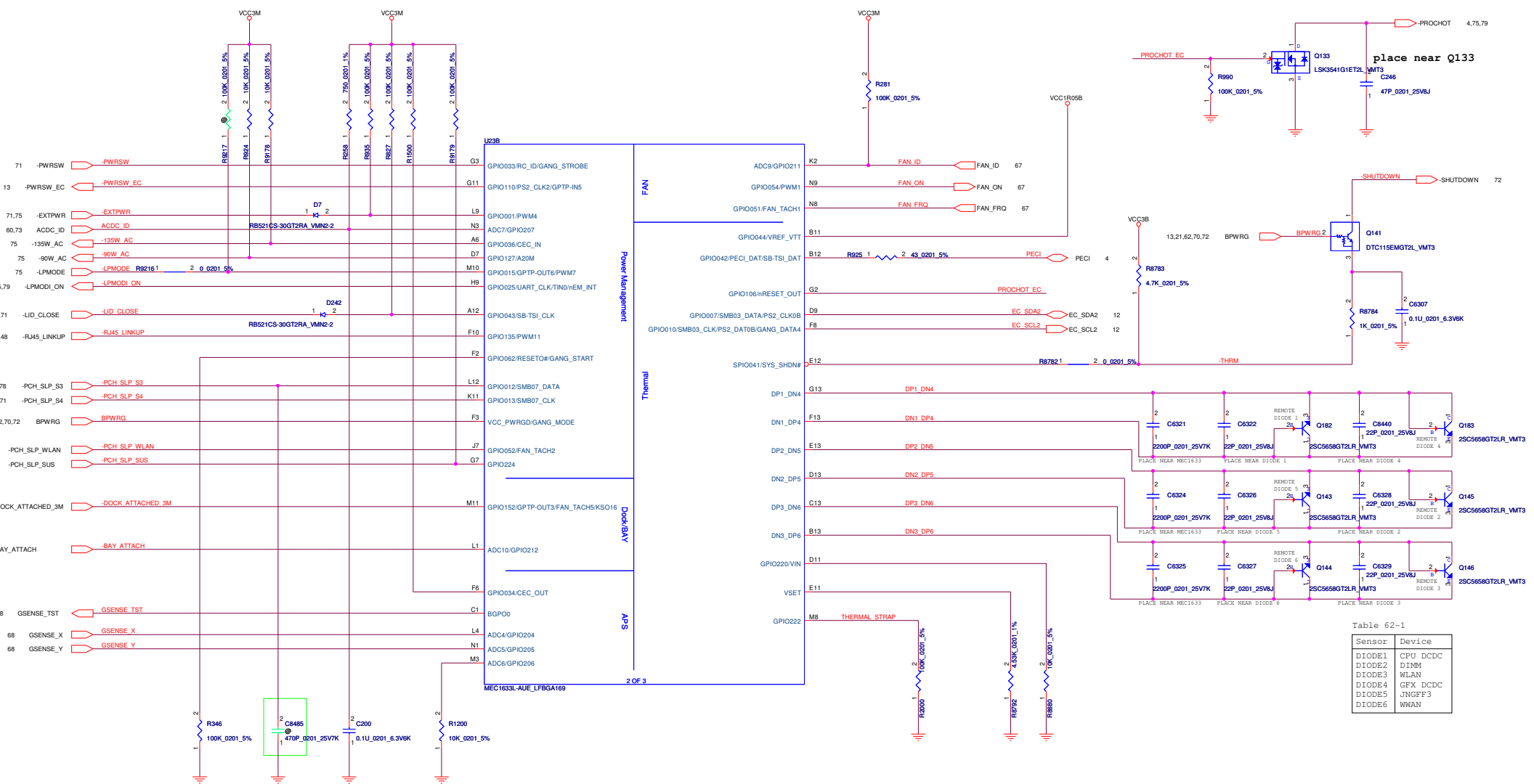




NEAR DOCK CONN			
9	DPC_3N	C841 1	2 0.1U 0201 6.3V8K DOCK_DP3N
9	DPC_3P	C843 1	2 0.1U 0201 6.3V8K DOCK_DP3P
9	DPC_2N	C883 1	2 0.1U 0201 6.3V8K DOCK_DP2N
9	DPC_2P	C887 1	2 0.1U 0201 6.3V8K DOCK_DP2P
9	DPC_1N	C901 1	2 0.1U 0201 6.3V8K DOCK_DP1N
9	DPC_1P	C900 1	2 0.1U 0201 6.3V8K DOCK_DP1P
9	DPC_0N	C903 1	2 0.1U 0201 6.3V8K DOCK_DP0N
9	DPC_0P	C902 1	2 0.1U 0201 6.3V8K DOCK_DP0P
14	DOCK_DPC_AUXN	C930 1	2 0.1U 0201 6.3V8K DOCK_AUXN
14	DOCK_DPC_AUXP	C929 1	2 0.1U 0201 6.3V8K DOCK_AUXP



Design note:
EMI solution



Layout note:
Put C8485 near EC (U23).

Table 62-1

Sensor	Device
DIODE1	CPU DCDC
DIODE2	DIMM
DIODE3	WLAN
DIODE4	GFX DCDC
DIODE5	JNGFF3
DIODE6	WWAN

Table 63-5

CPU SKU	47W_GAIN_EN
Dual Core CPU	Low
Quad Core CPU	High

Design Note :
47W_GAIN_EN should be driven HIGH even if QC is clipped at 3.7W

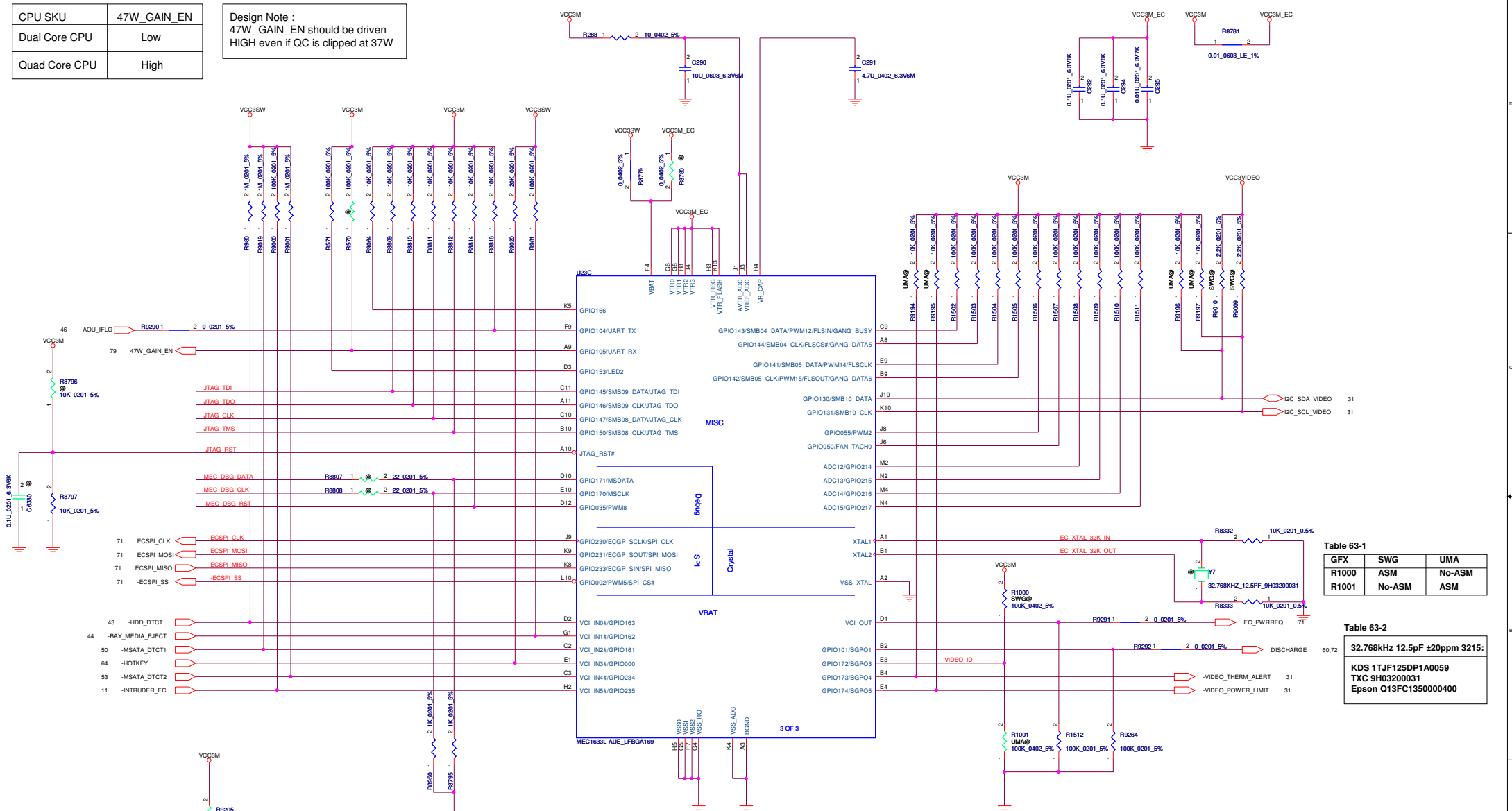


Table 63-3

JTAG debug port		
	Enable	Disable
R8796	ASM	NO-ASM
R8797	NO-ASM	ASM
R9205	ASM	NO-ASM

↑
LOGIC

Table 63-4

trace FIFO debug port		
	Enable	Disable
R8807	ASM	NO-ASM
R8808	ASM	NO-ASM
R8950	NO-ASM	ASM

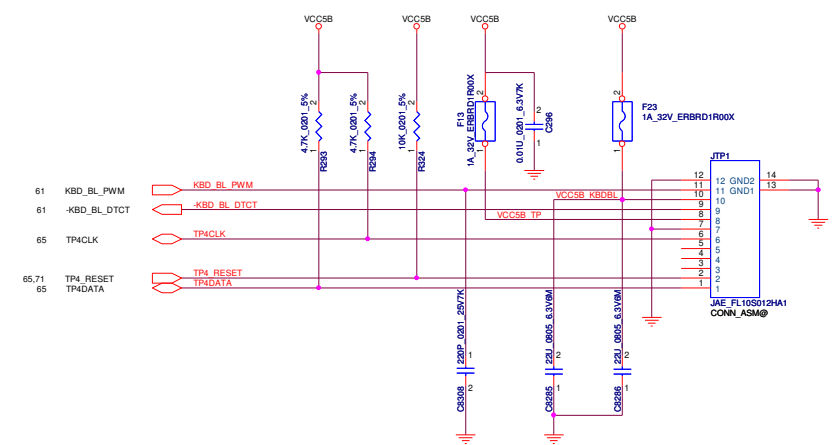
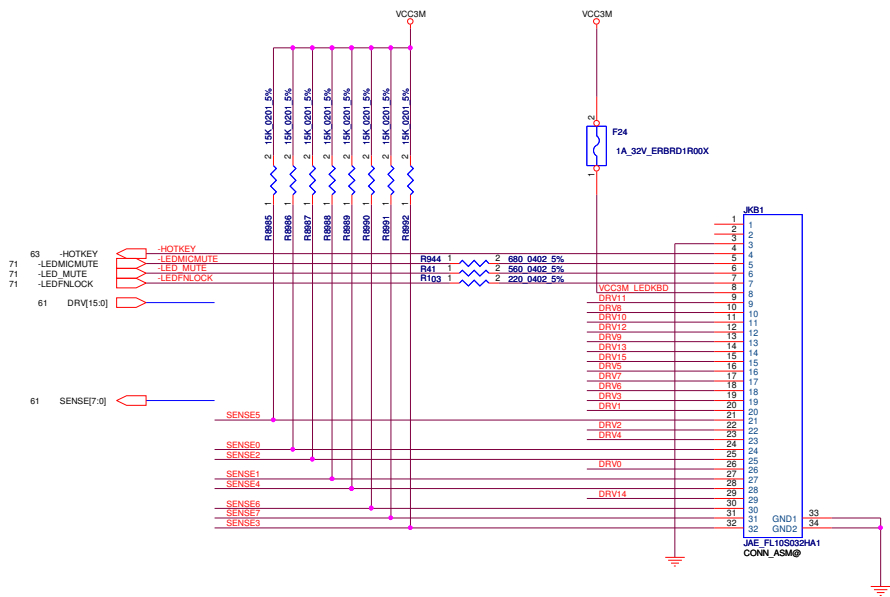
↑
LOGIC

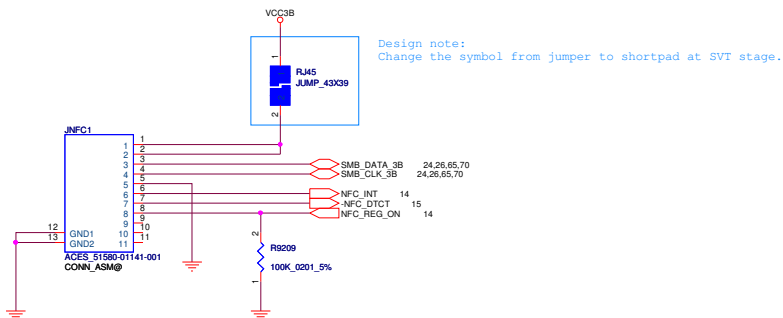
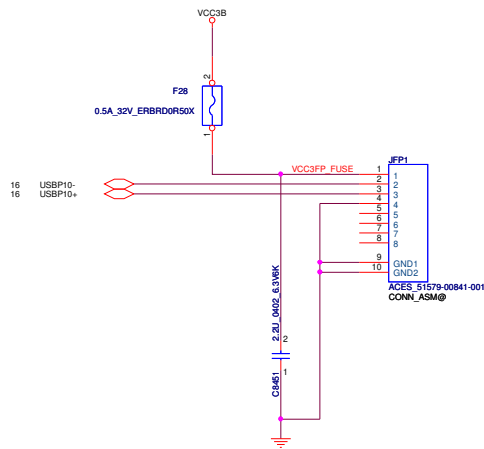
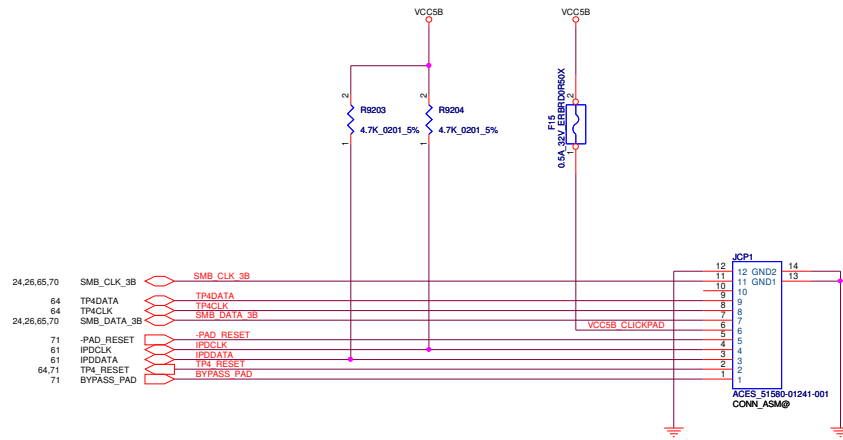
Table 63-1

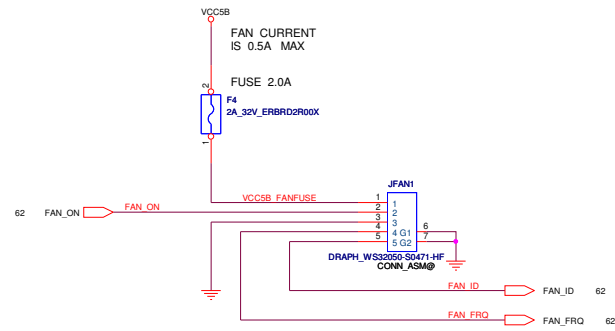
GFX	SWG	UMA
R1000	ASM	No-ASM
R1001	No-ASM	ASM

Table 63-2

32.768KHz 12.5pF ±20ppm 3215:
KDS 1TJF125DP1A0059
TXC 9H03200031
Epson Q13FC135000400







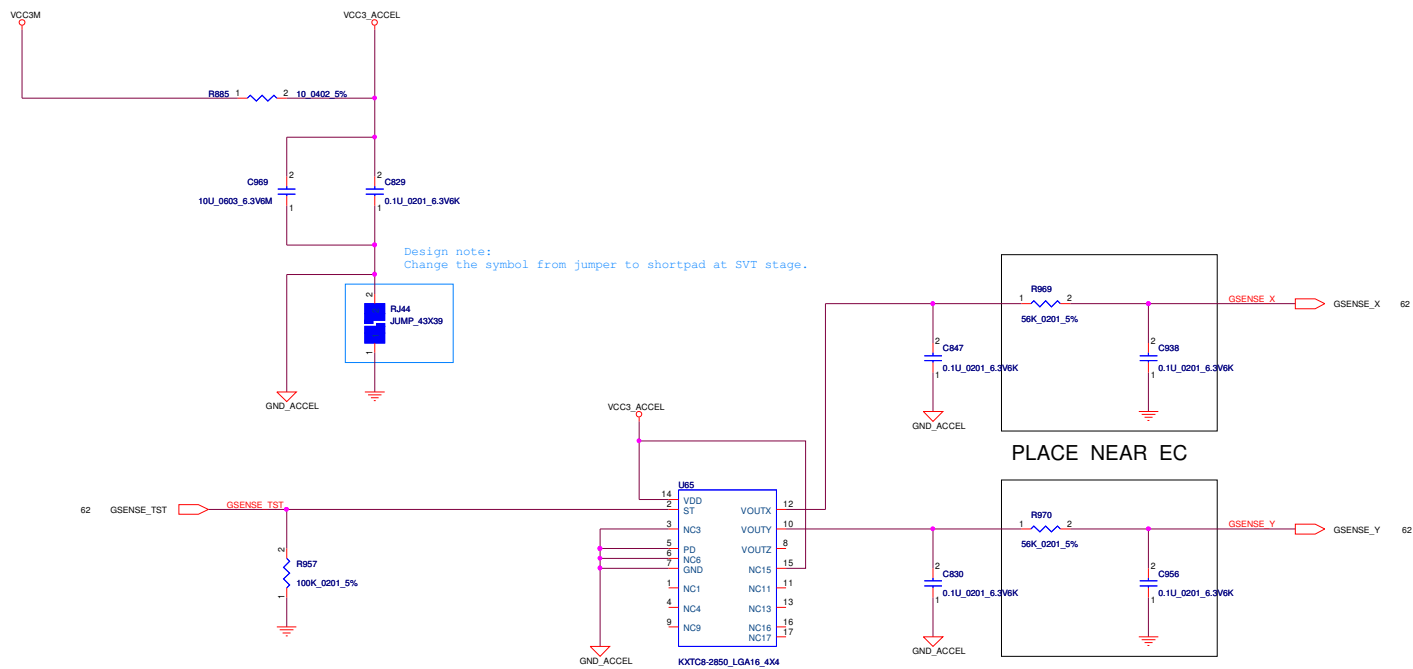


Table 68-1

	LIS34AL KXTC8-2850	NO_ACC.
R957	ASM	ASM
U65	ASM	NO_ASM
R885 C829 C969	10-OHM ASM ASM	NO_ASM NO_ASM NO_ASM
C830 C847	ASM ASM	NO_ASM NO_ASM
R969 C938 R970 C956	56K ASM 56K ASM	NO_ASM NO_ASM NO_ASM NO_ASM
C704 R344 C703	NO_ASM NO_ASM NO_ASM	NO_ASM NO_ASM NO_ASM
R125	ASM	ASM

Table 68-2

G-Sensor Table (U65)	
Kionix	KXTC8-2850
STMicro	LIS34ALTR

LOGIC
↓

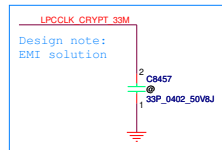
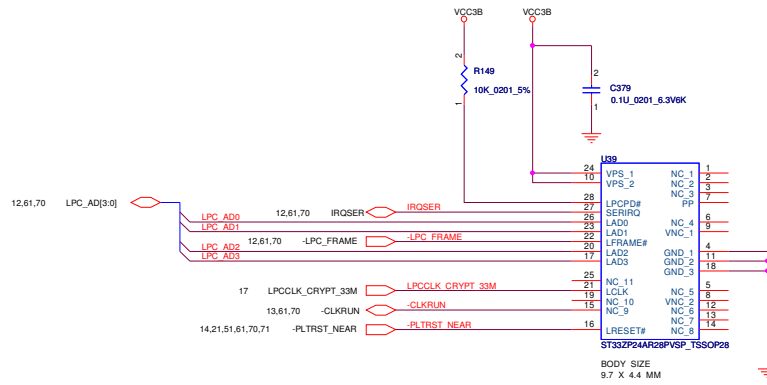


Table 70-1

EEPROM	U22	U23
U22	ASM	NO_ASM
C1005	ASM	NO_ASM
R577	ASM	NO_ASM
Q97	ASM	NO_ASM

LOGIC

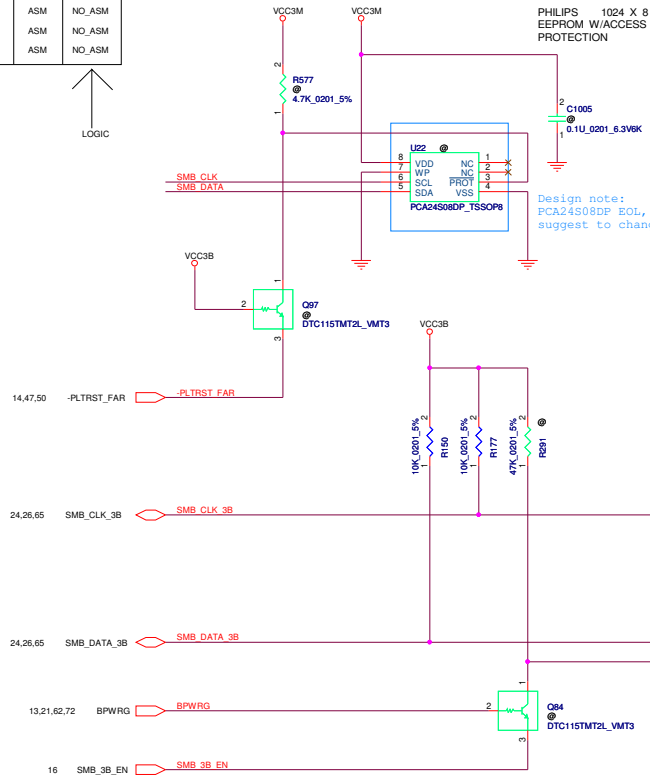


Table 70-2

REF	DES	ENABLE	DISABLE
JDB1	ASM	NO_ASM	
R220	ASM	NO_ASM	

LOGIC

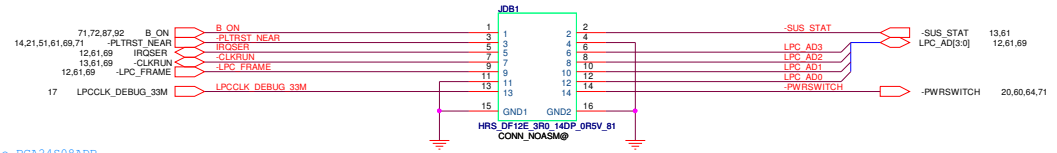
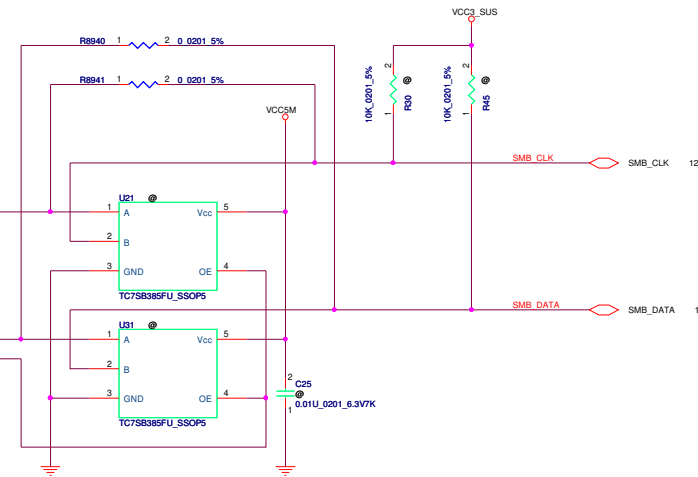


Table 70-3

EEPROM	U22	U23
U21	ASM	NO_ASM
U31	ASM	NO_ASM
C25	ASM	NO_ASM
R291	ASM	NO_ASM
Q84	ASM	NO_ASM
R8941	NO_ASM	ASM
R8940	NO_ASM	ASM
R30	ASM	NO_ASM
R45	ASM	NO_ASM

LOGIC



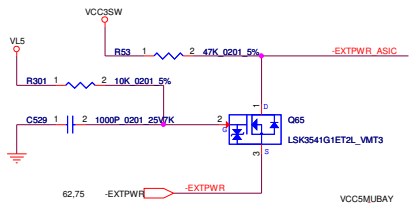
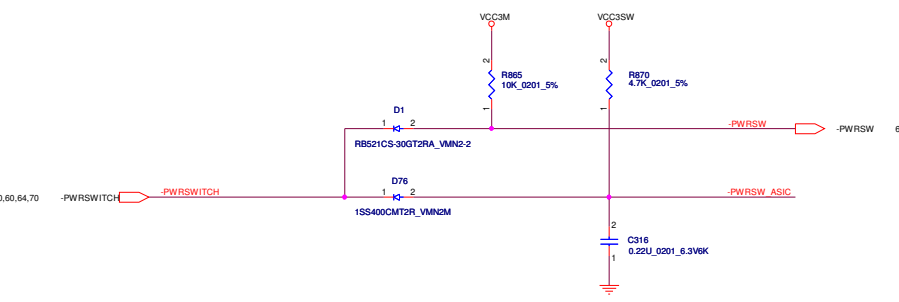
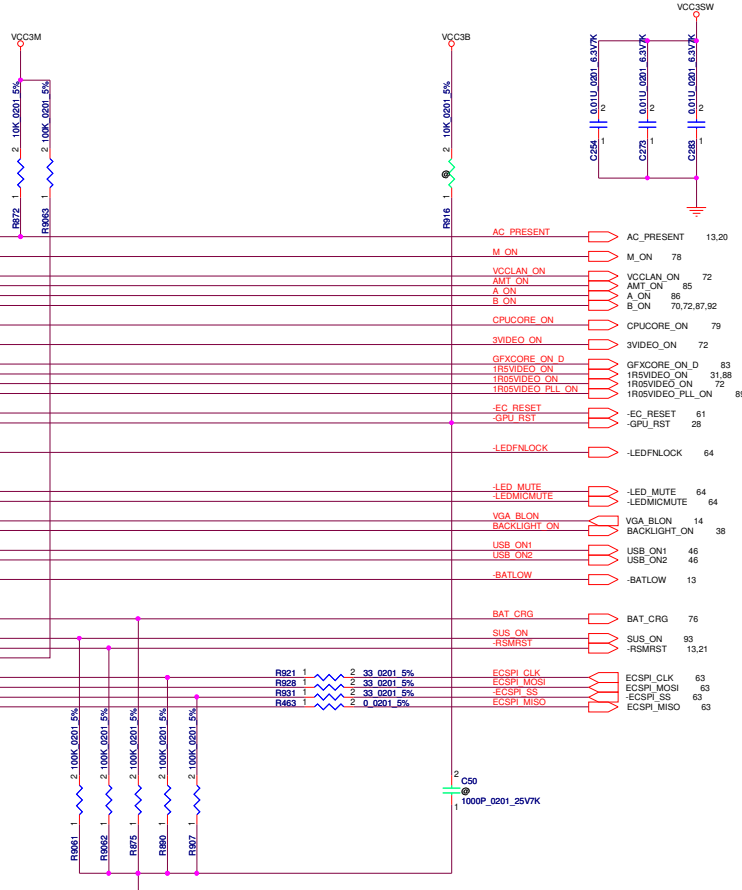
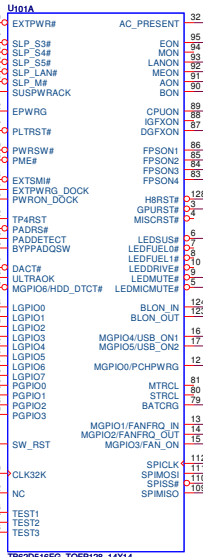
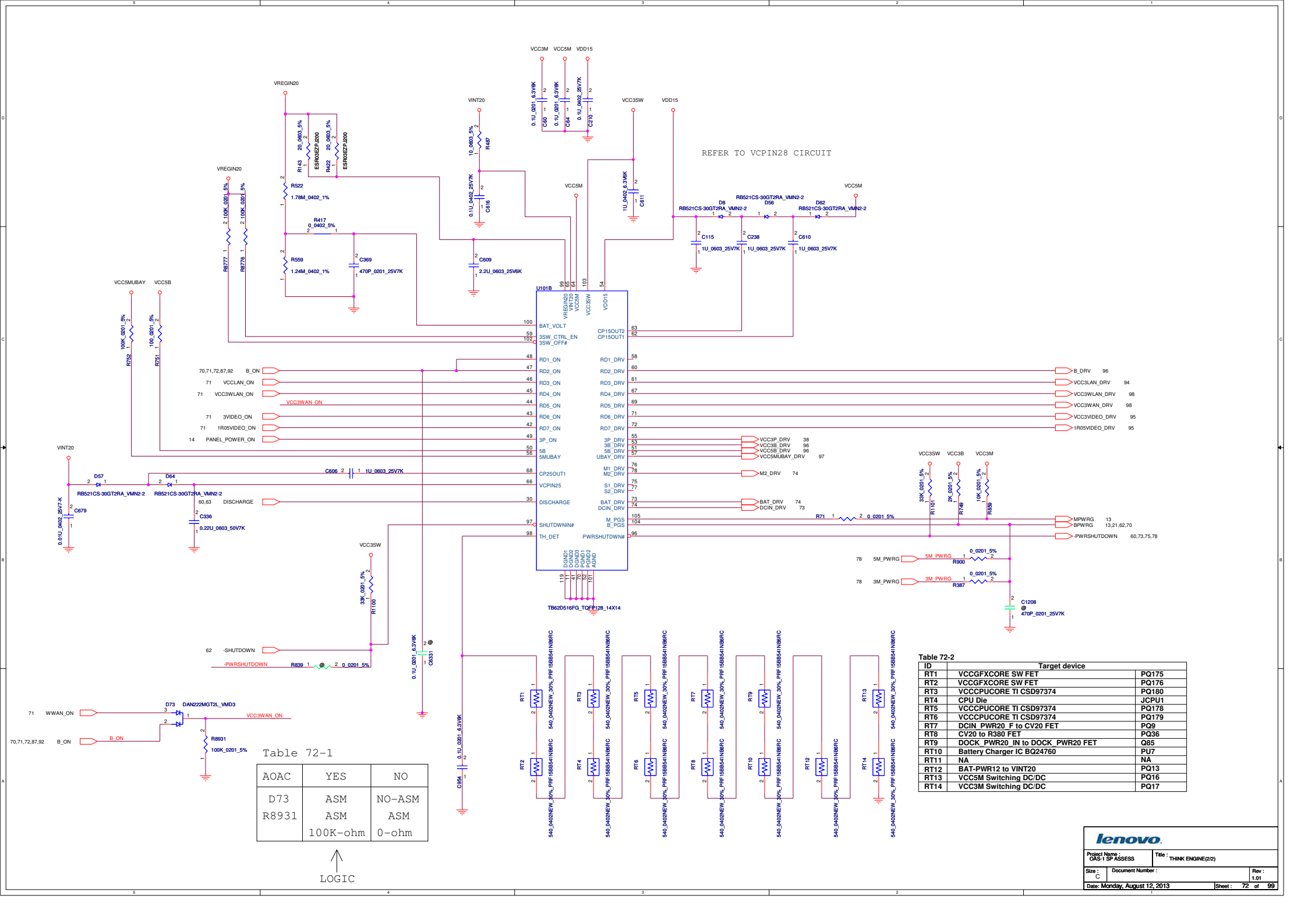


Table 71-1

ThinkEngine (U101)	
Toshiba	TB62D516FG
Rohm	BD4177KUT





REFER TO VCPIN28 CIRCUIT

Table 72-1

AOAC	YES	NO
D73	ASM	NO-ASM
R8931	ASM	ASM
	100K-ohm	0-ohm

LOGIC

Table 72-2

ID	Target device	
RT1	VCCGFXCORE SW FET	PQ175
RT2	VCCGFXCORE SW FET	PQ176
RT3	VCCCPUORE TI CSD97374	PQ180
RT4	CPU Die	JCPU1
RT5	VCCCPUORE TI CSD97374	PQ178
RT6	VCCCPUORE TI CSD97374	PQ179
RT7	DCIN PWR20 F to CV20 FET	PQ9
RT8	CV20 to R380 FET	PQ36
RT9	DOCK_PWR20_IN to DOCK_PWR20 FET	Q85
RT10	Battery Charger IC BQ24760	PU7
RT11	NA	NA
RT12	BAT-PWR12 to VINT20	PQ13
RT13	VCC5M Switching DC/DC	PQ16
RT14	VCC3M Switching DC/DC	PQ17

TABLE 73-1

Fuse (PF2)	
Littlefuse	0429007.WRMLHF
Cooper	3216FF7-R
AEM	F1206HI7000V024TM

Design Note:
 AEM part is only for qualification purpose.
 It will be dropped before SVT if GCM is not approved.

DCIN

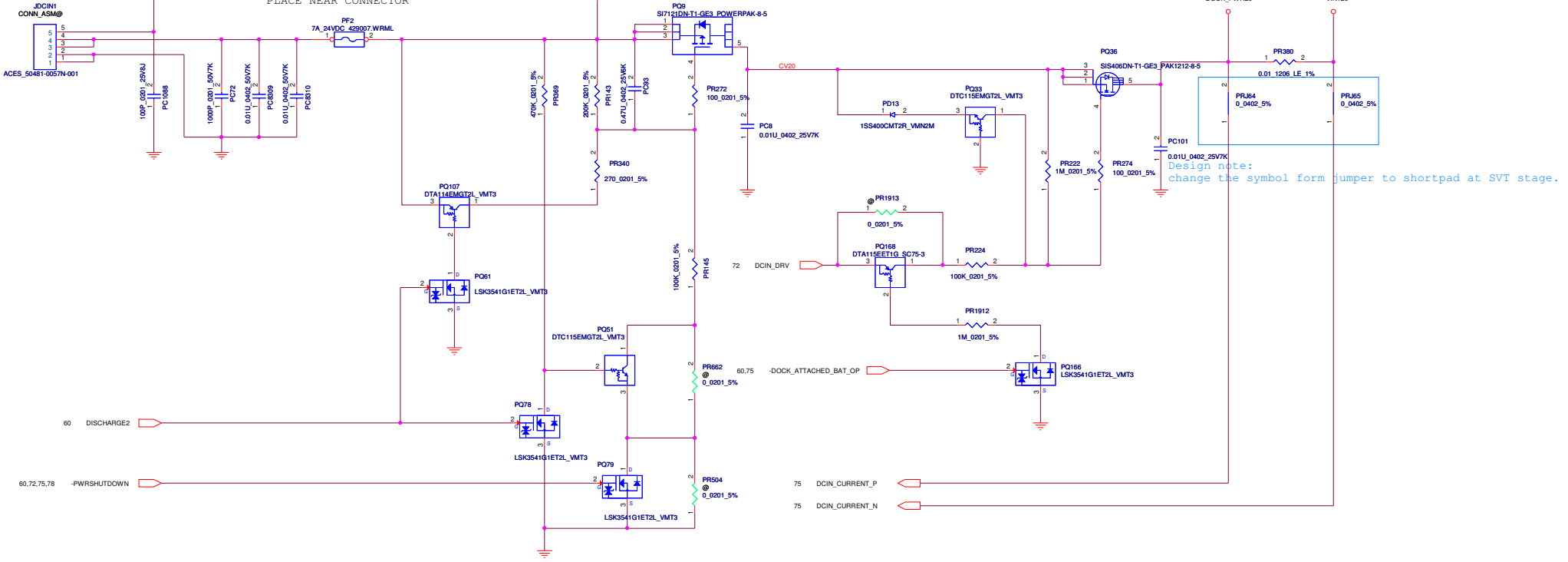


TABLE 73-1

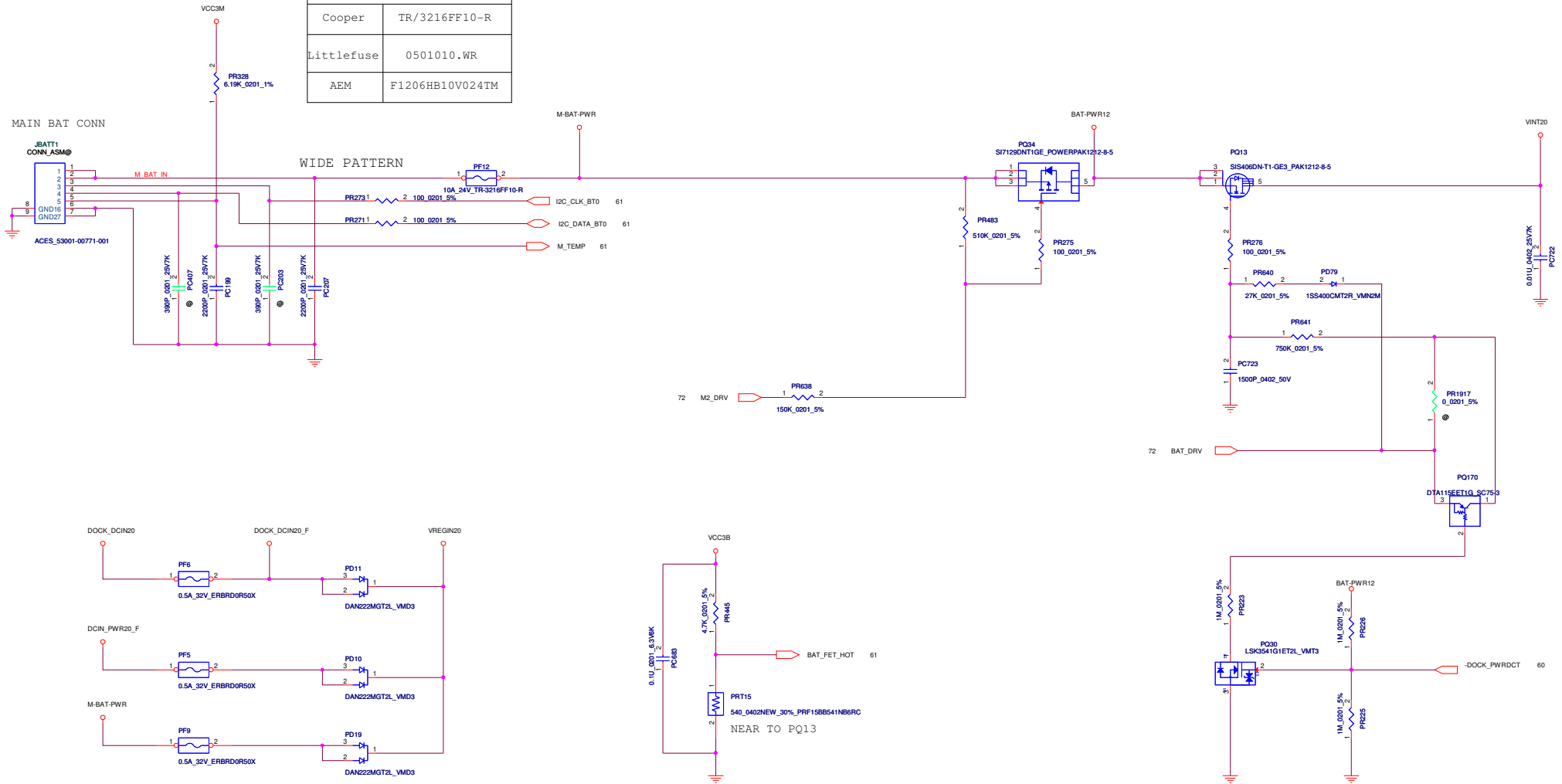
PEAK SHIFT	YES	NO
PR662	NO-ASM	ASM
PR369	ASM	NO-ASM
PQ78	ASM	NO-ASM
PQ51	ASM	NO-ASM

↑
LOGIC

Design Note:
 AEM part is only for qualification purpose.
 It will be dropped before SVT if GCM is not approved.

TABLE 74-1

Fuse (PF12)	
Cooper	TR/3216FF10-R
Littlefuse	0501010.WR
AEM	F1206HB10V024TM



BOM note:
Virtual symbol for BOM control.

CAD note:
According to MFVT EC006,
show part description when
new symbol announce.

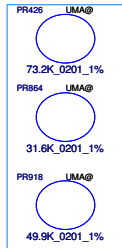
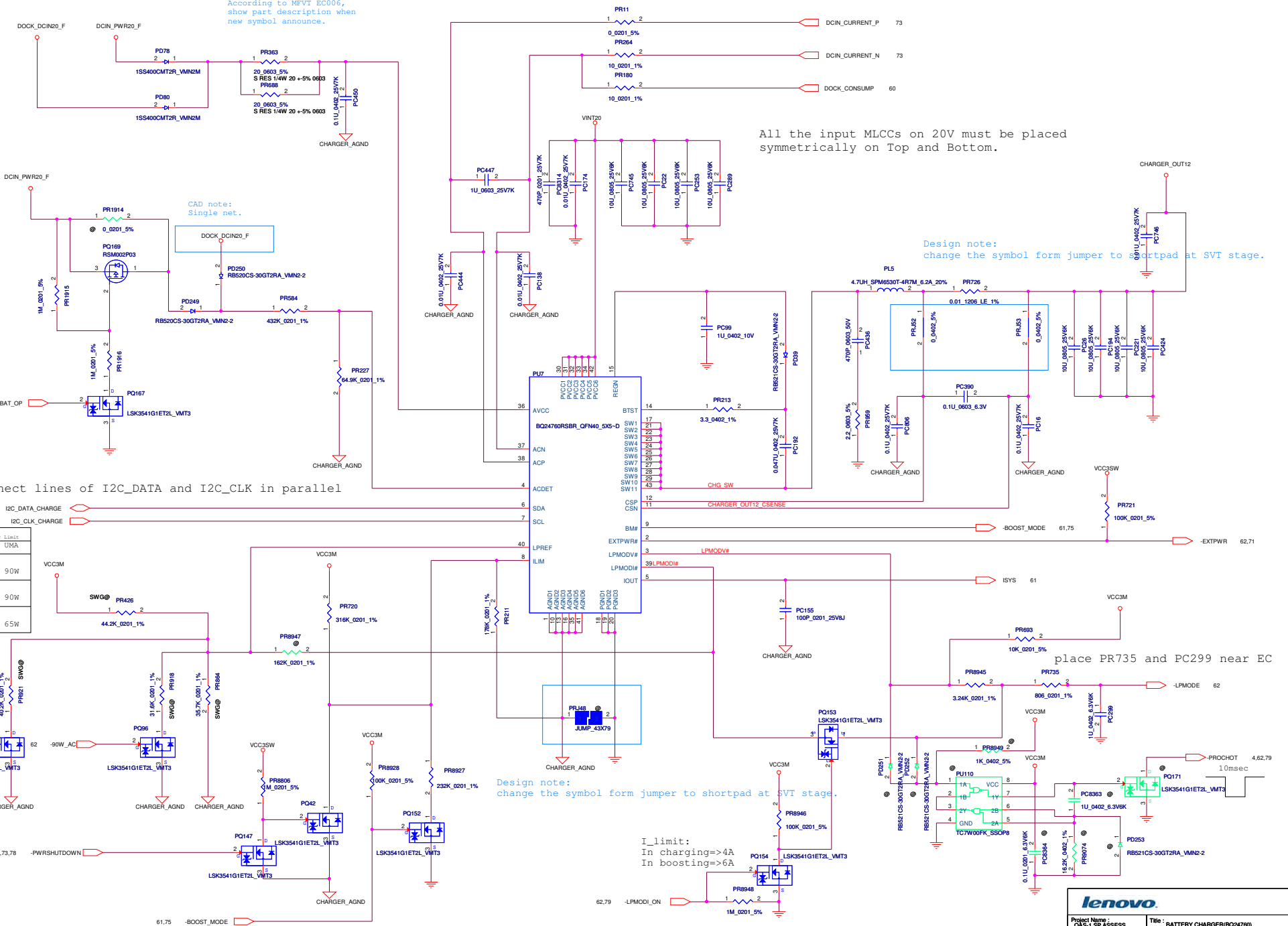


TABLE 75-1

	SWG	UMA
PR426	44.2K	73.2K
PR864	35.7K	31.6K
PR918	31.6K	49.9K
PR921	40.2K	DY
PQ97	ASM	DY

TABLE 75-2

AC Adapter	-135W_AC		-90W_AC		System Power Limit	
	SWG	UMA	SWG	UMA	SWG	UMA
135W	L	L	L	L	135W	90W
90W	H	L	L	L	90W	90W
65W	H	H	L	L	65W	65W



All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

Design note:
change the symbol form jumper to shortpad at SVT stage.

to connect lines of I2C_DATA and I2C_CLK in parallel

place PR735 and PC299 near EC

Design note:
change the symbol form jumper to shortpad at SVT stage.

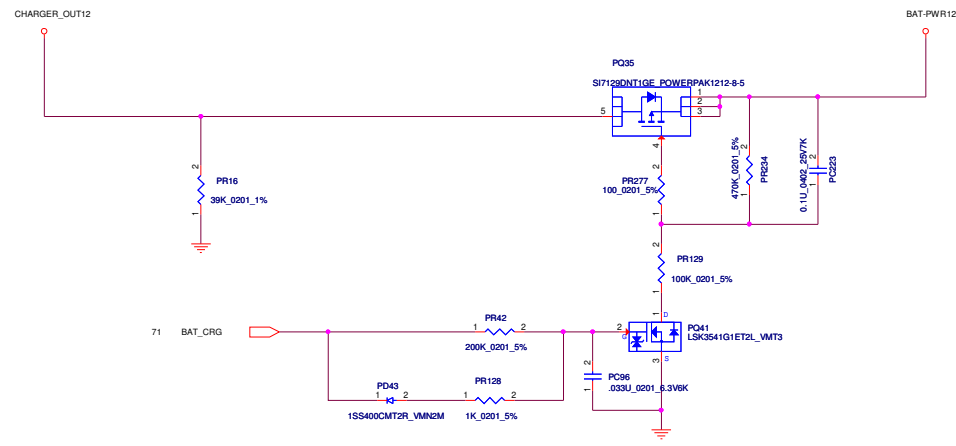
I_{limit}:
In charging=>4A
In boosting=>6A

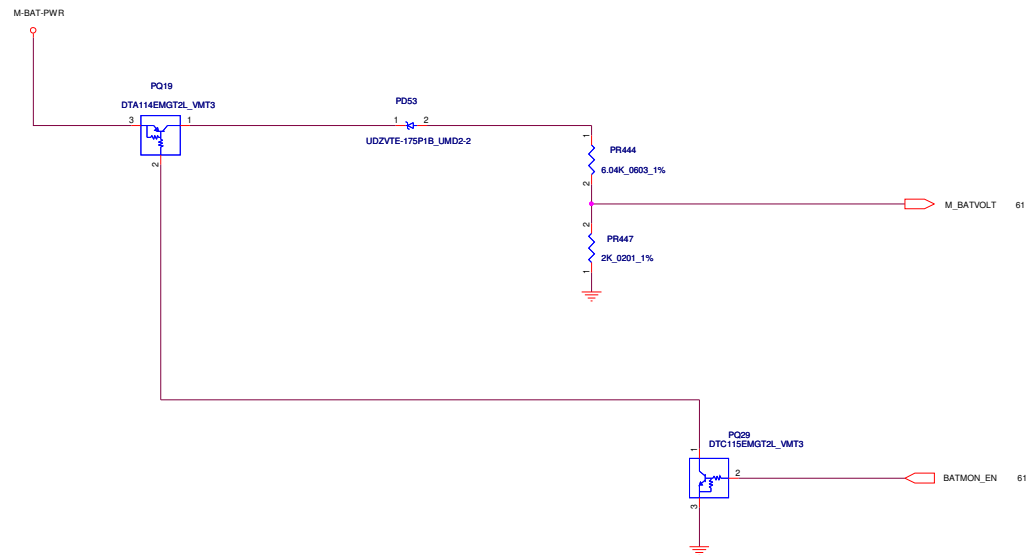
lenovo

Project Name : CAS-1 SP ASSESS Title : BATTERY CHARGER(BQ24760)

Size : Document Number : Rev : 1.01

Date : Monday, August 12, 2013 Sheet : 75 of 99



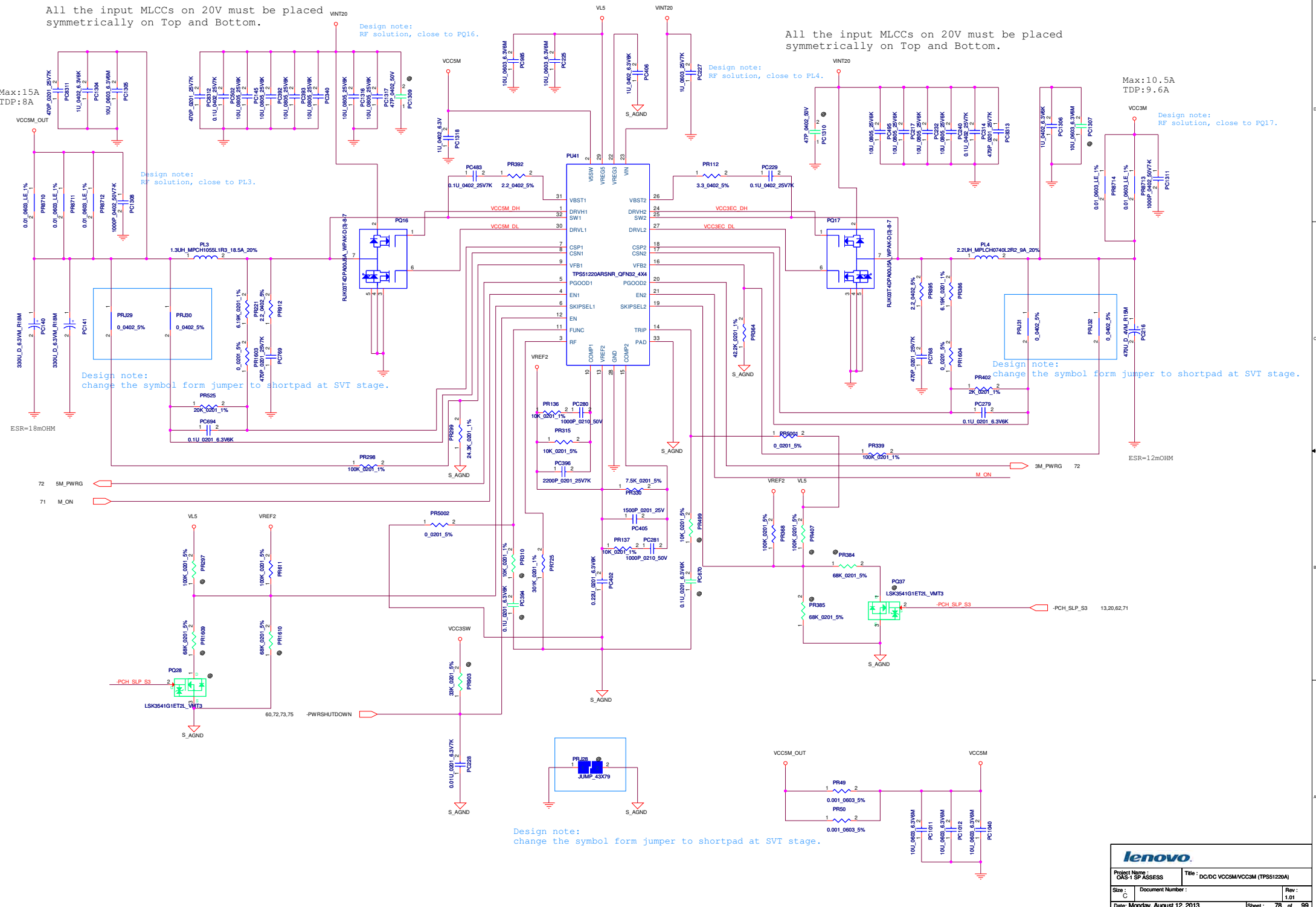


All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

Max:10.5A
TDP:9.6A

Max:15A
TDP:8A



Design note:
RF solution, close to PL3.

Design note:
RF solution, close to PQ16.

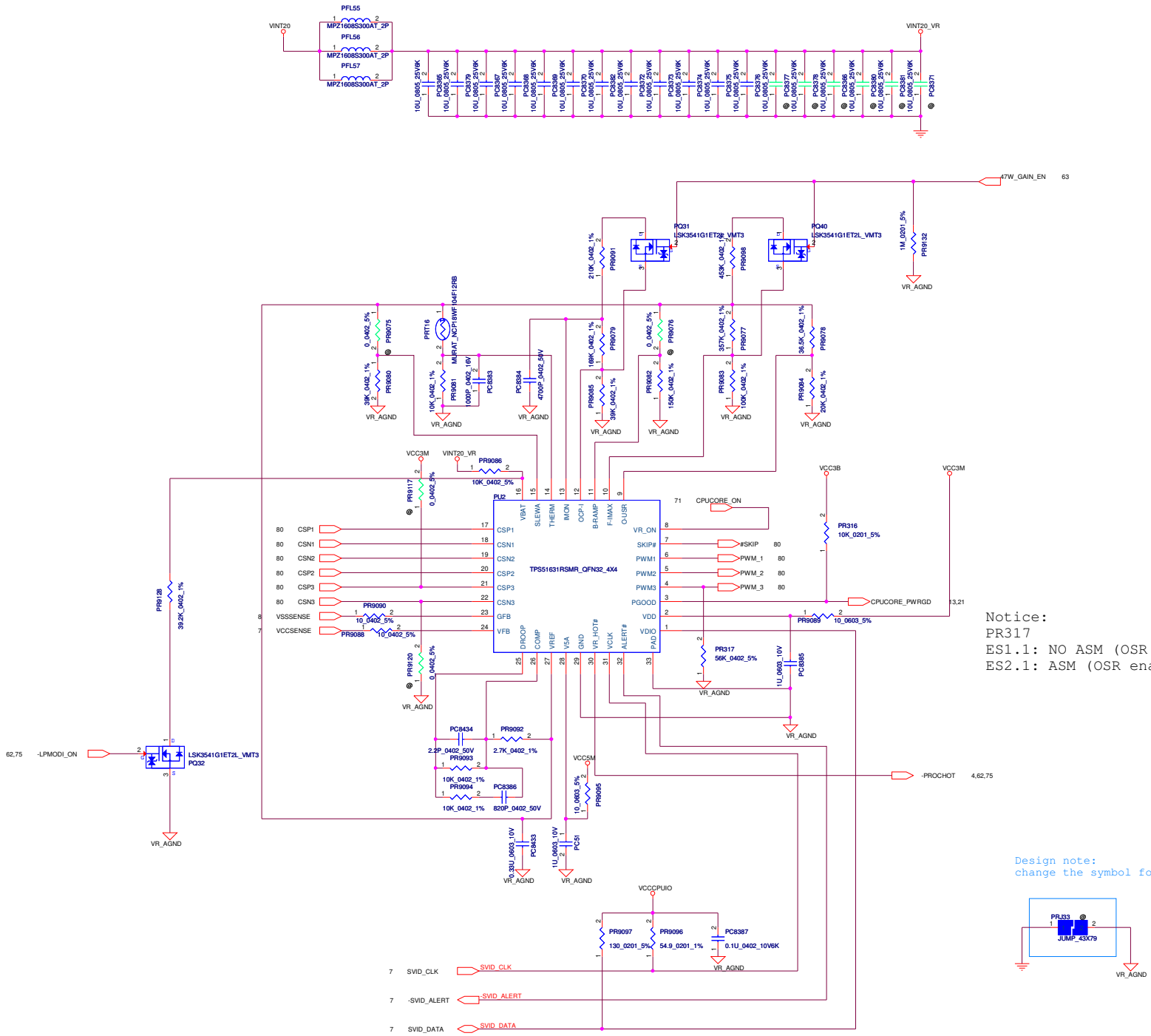
Design note:
RF solution, close to PL4.

Design note:
RF solution, close to PQ17.

Design note:
change the symbol form jumper to shortpad at SVT stage.

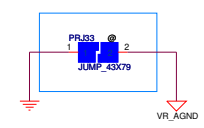
Design note:
change the symbol form jumper to shortpad at SVT stage.

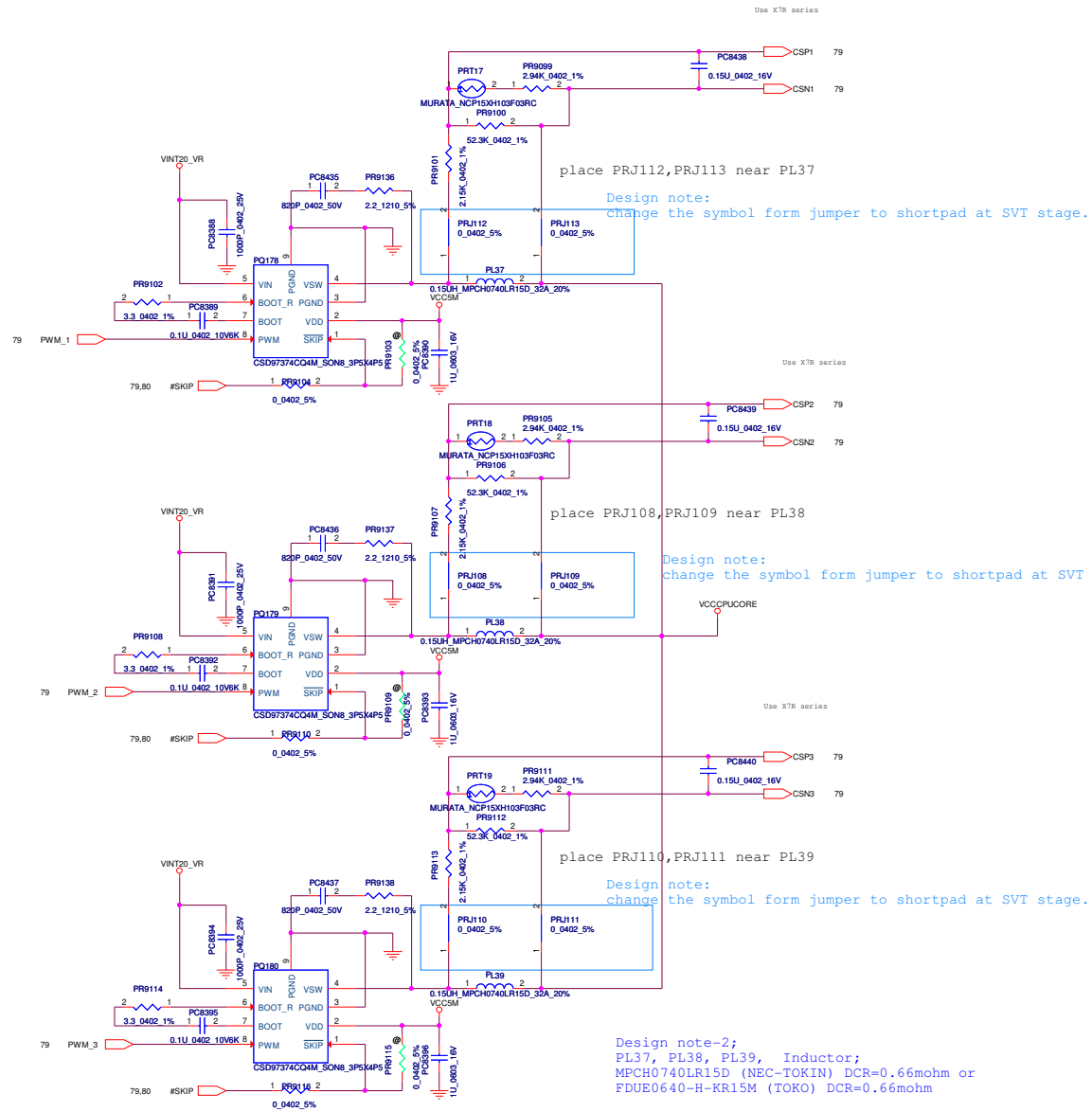
Design note:
change the symbol form jumper to shortpad at SVT stage.



Notice:
 PR317
 ES1.1: NO ASM (OSR disable)
 ES2.1: ASM (OSR enable)

Design note:
 change the symbol form jumper to shortpad at SVT stage.

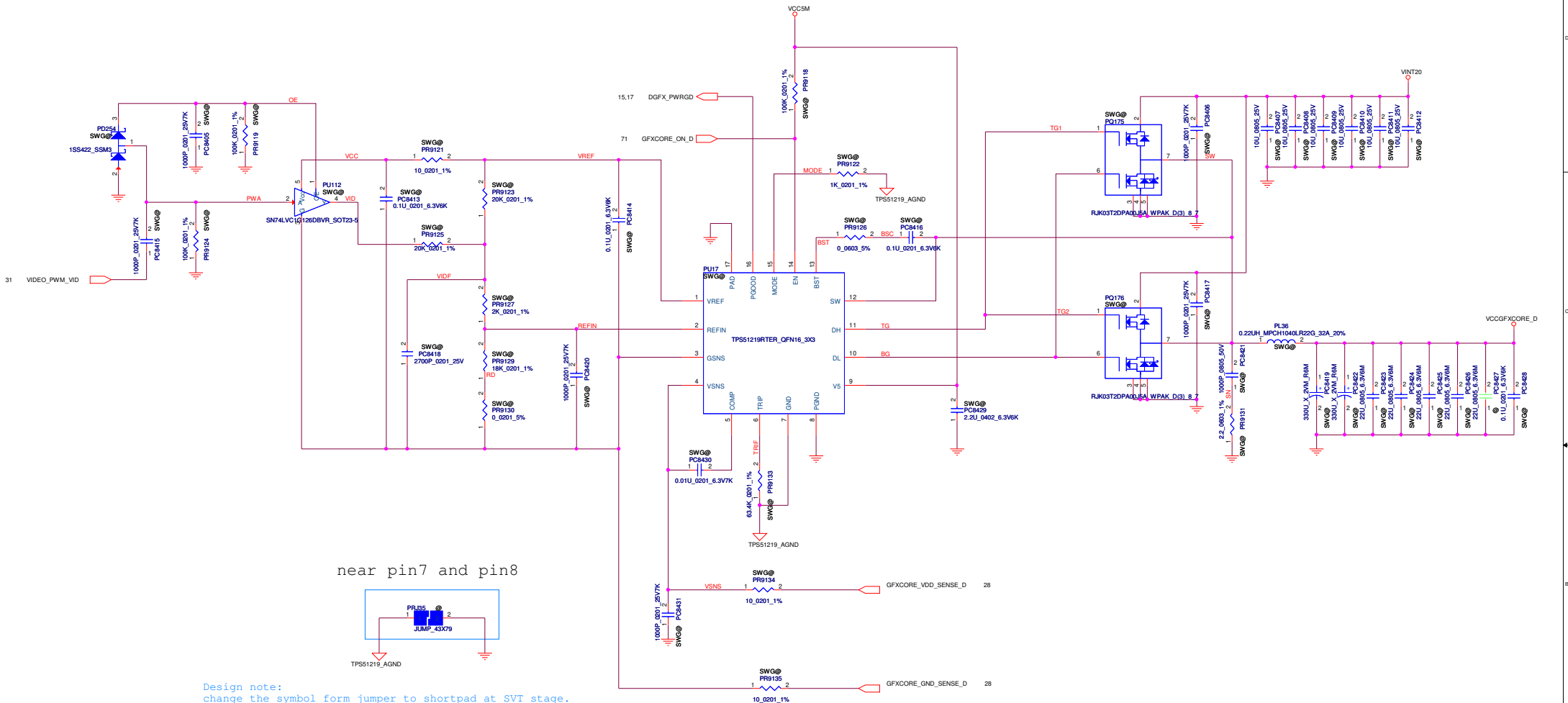




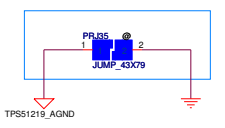
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Project Name: CDS-1307-ASSESS		Title: BLANK	
Size: C	Document Number:	Rev: 1.01	
Date: Monday, August 12, 2013		Sheet: 81	of 99



near pin7 and pin8

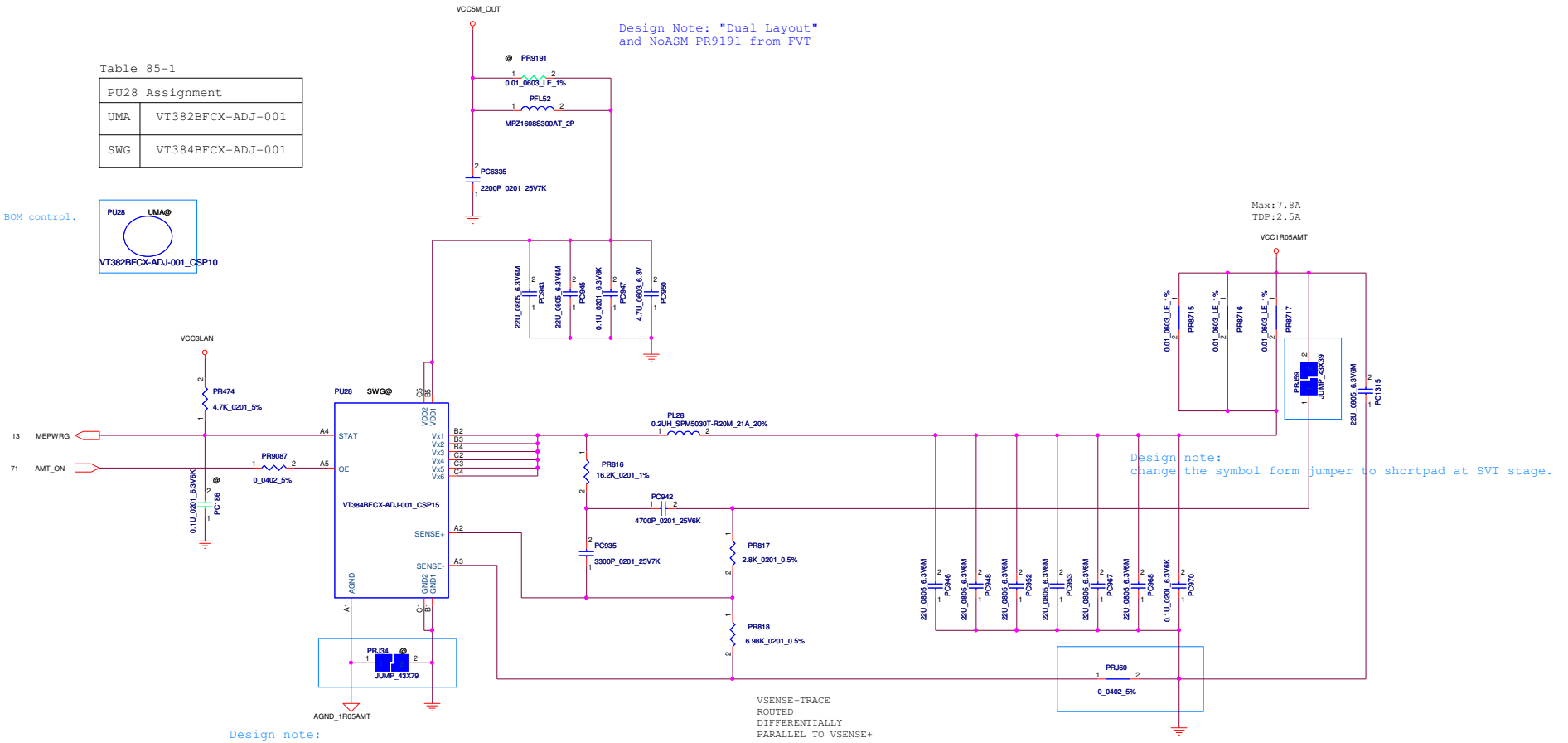
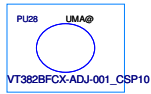


Design note:
change the symbol form jumper to shortpad at SVT stage.

Table 85-1

PU28 Assignment	
UMA	VT382BFCX-ADJ-001
SWG	VT384BFCX-ADJ-001

BOM note:
Virtual symbol for BOM control.



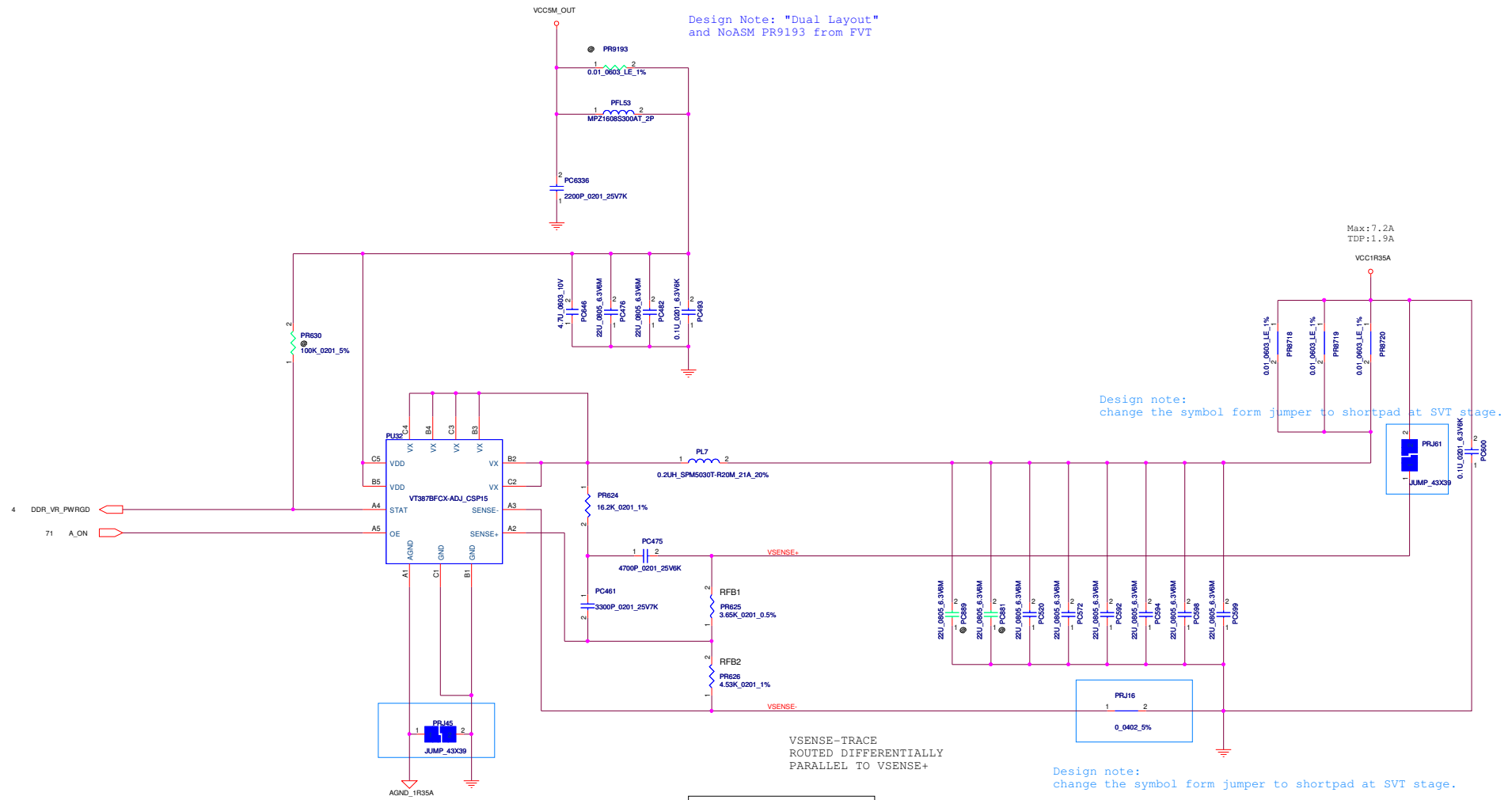
Design Note: "Dual Layout"
and NoASM PR9191 from FVT

Design note:
change the symbol form jumper to shortpad at SVT stage.

Design note:
change the symbol form jumper to shortpad at SVT stage.

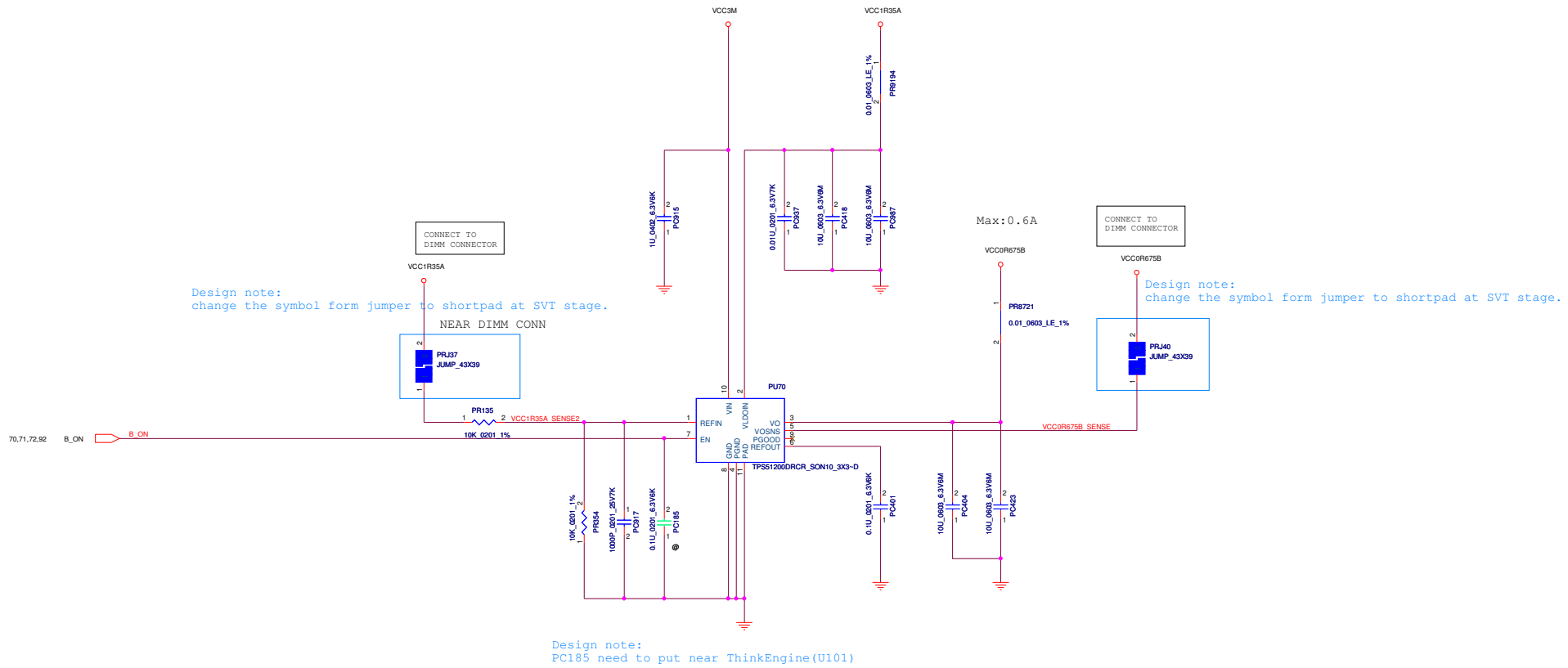
Design note:
change the symbol form jumper to shortpad at SVT stage.

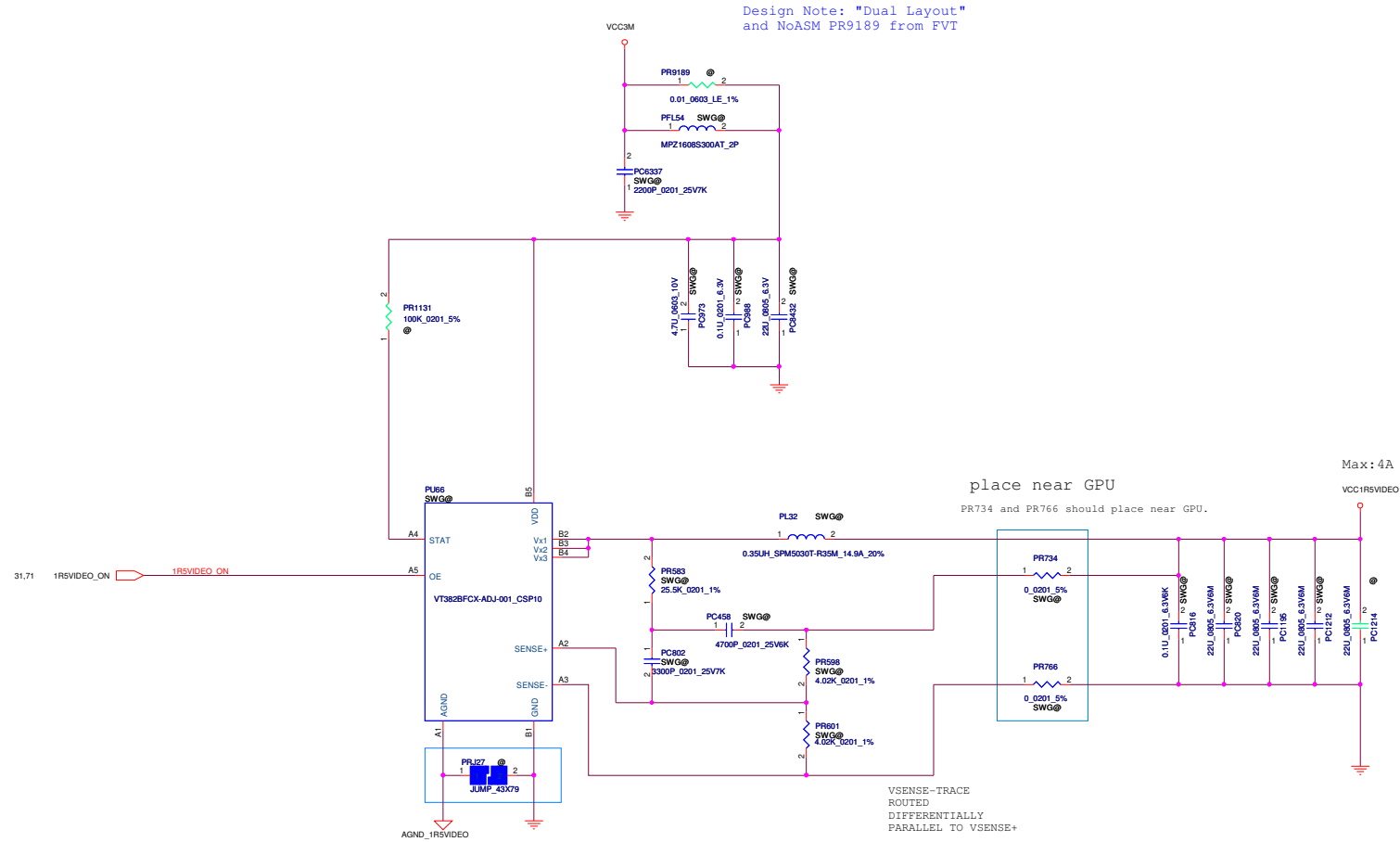
$$V_{out} = 0.75 \times (1 + PR817/PR818)$$



$$V_{out} = 0.75 \times (1 + (R_{FB1} / R_{FB2}))$$

RFB1	RFB2
PR625	PR626
3.65K	4.53K for 1.35V
4.02K	4.02K for 1.50V

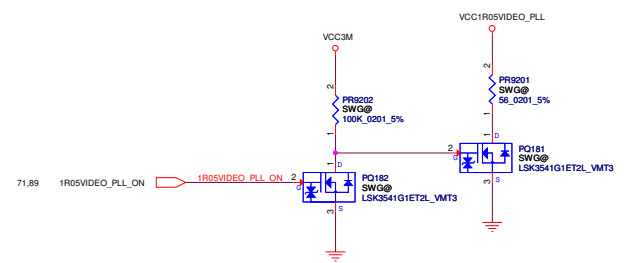
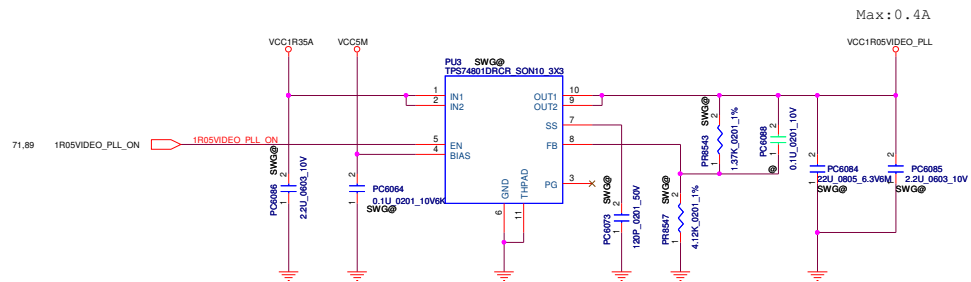





Design Note: "Dual Layout" and NoASM PR9189 from FVT

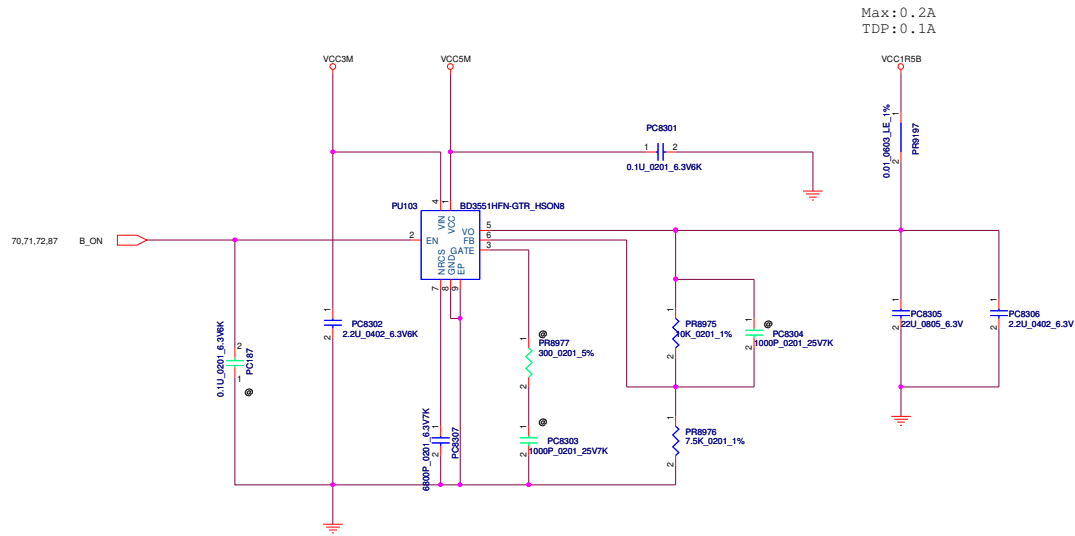
Design note:
change the symbol form jumper to shortpad at SVT stage.

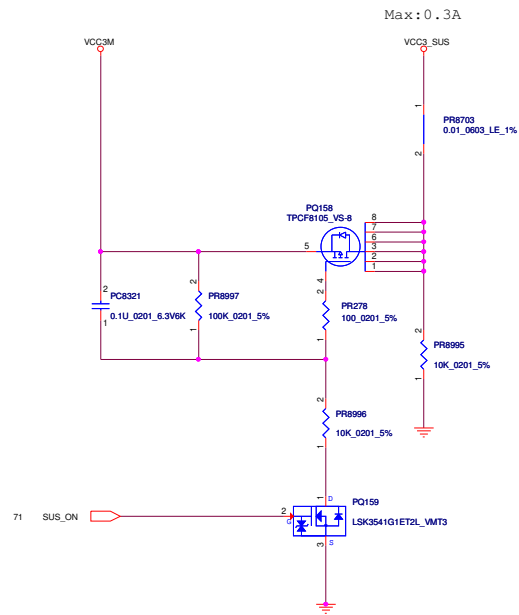
$$V_{out} = 0.75 \times (1 + PR598/PR601)$$

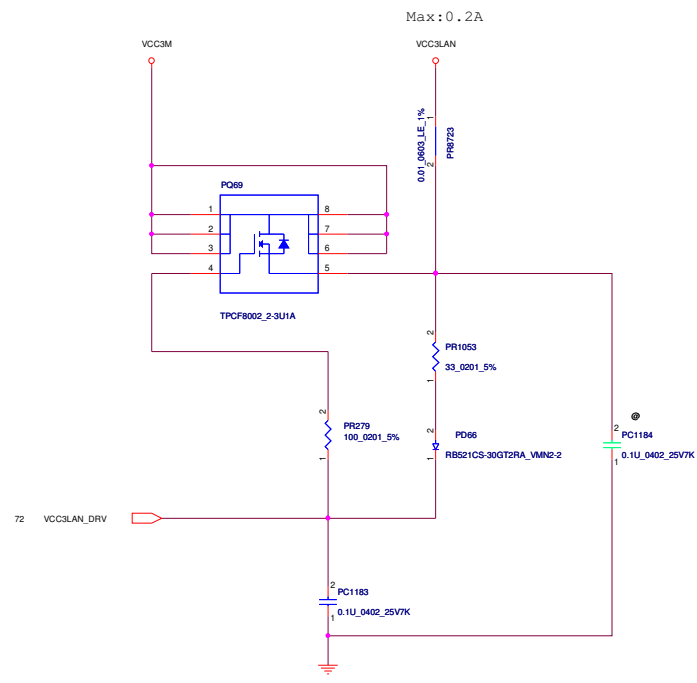


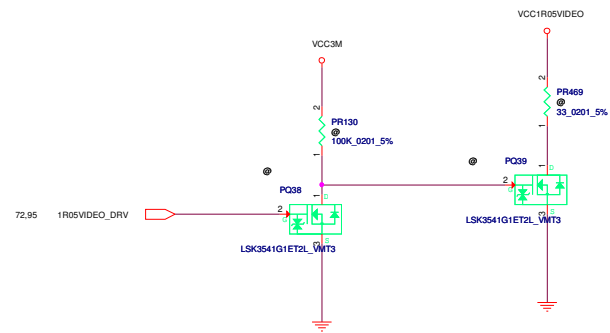
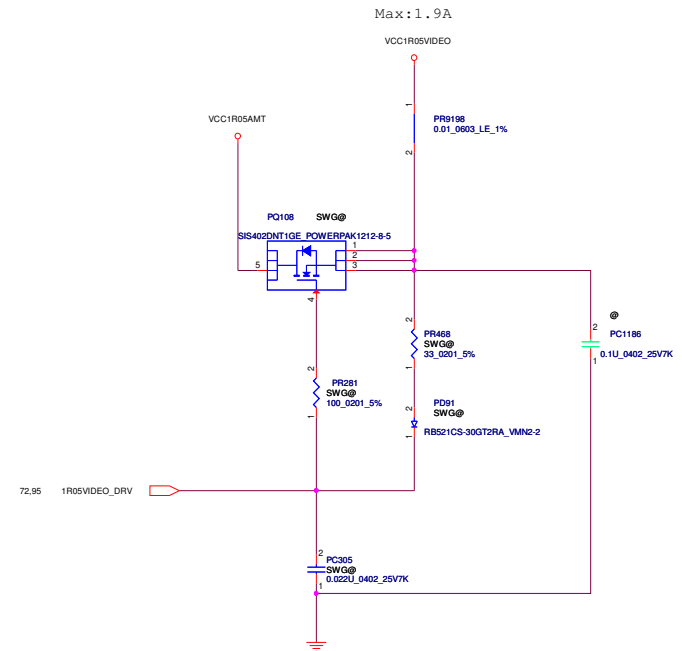
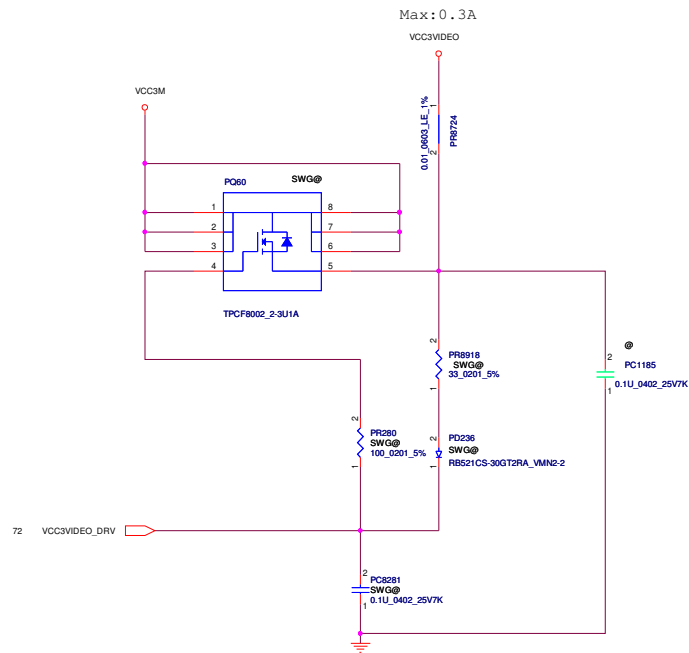
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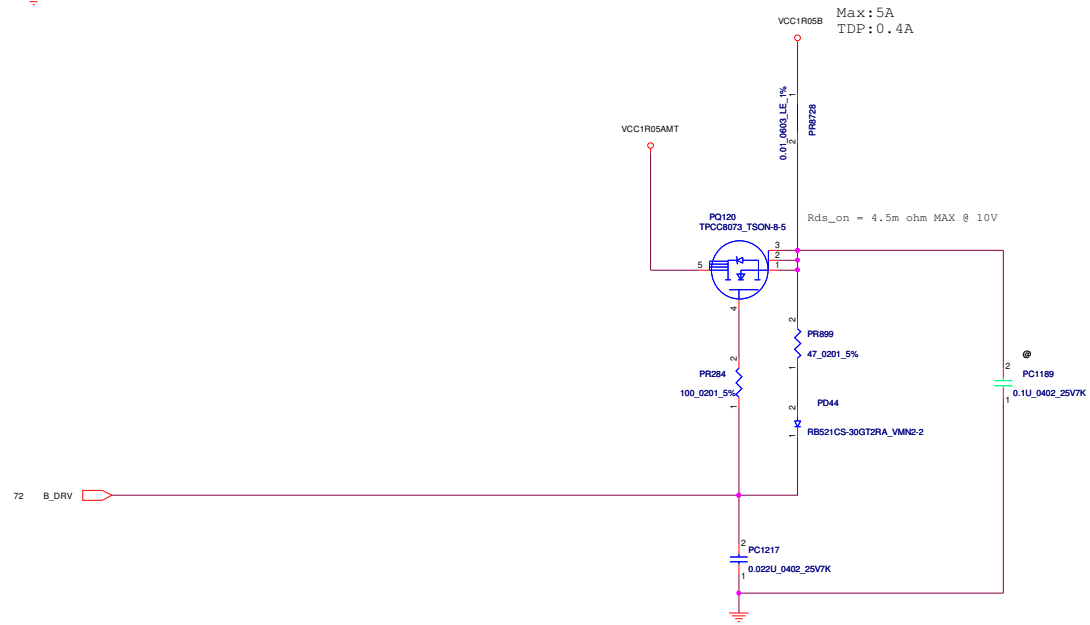
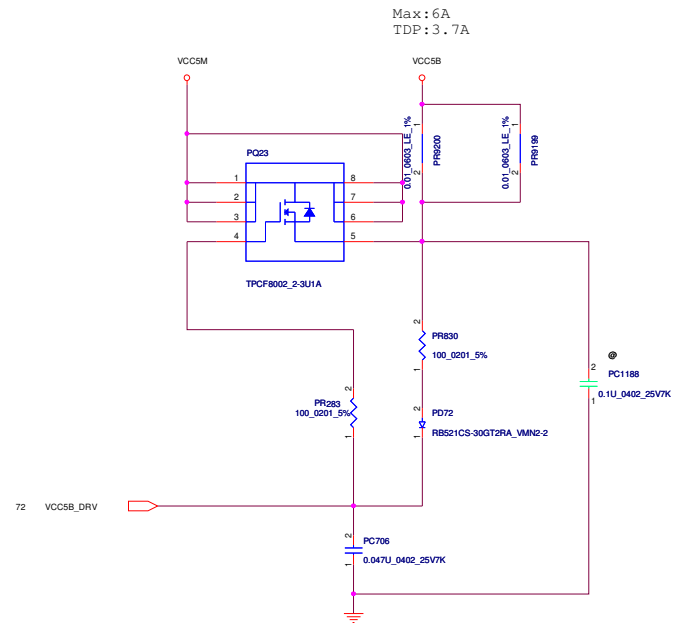
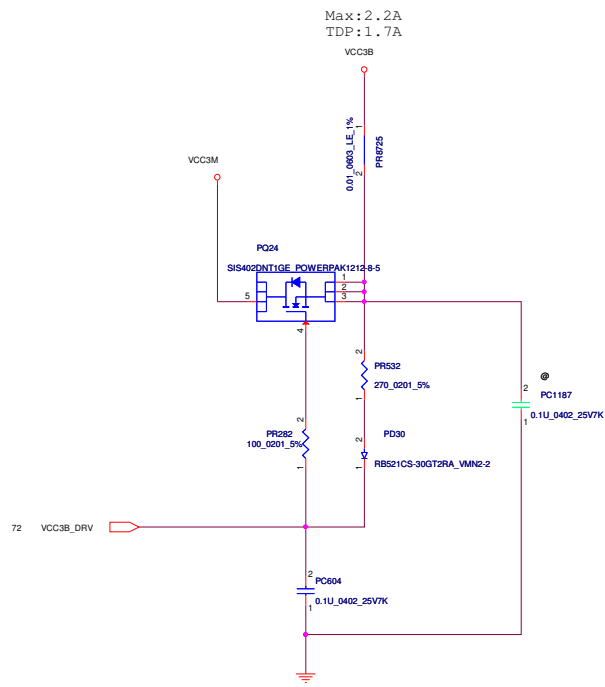
		
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Date: Monday, August 12, 2013	Sheet: 90	of 99

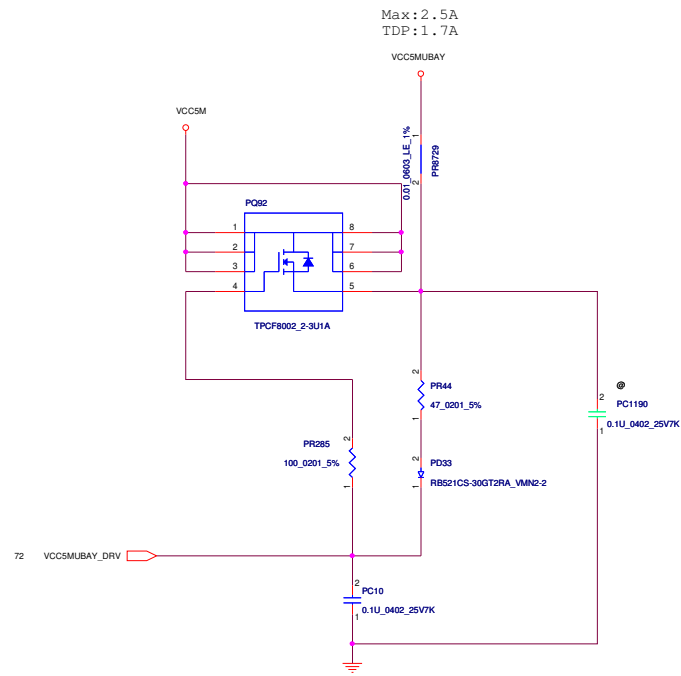












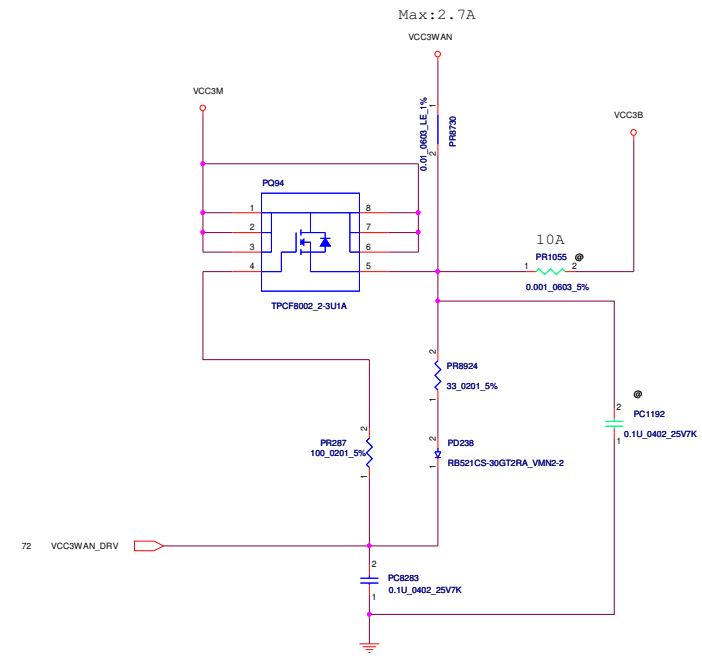
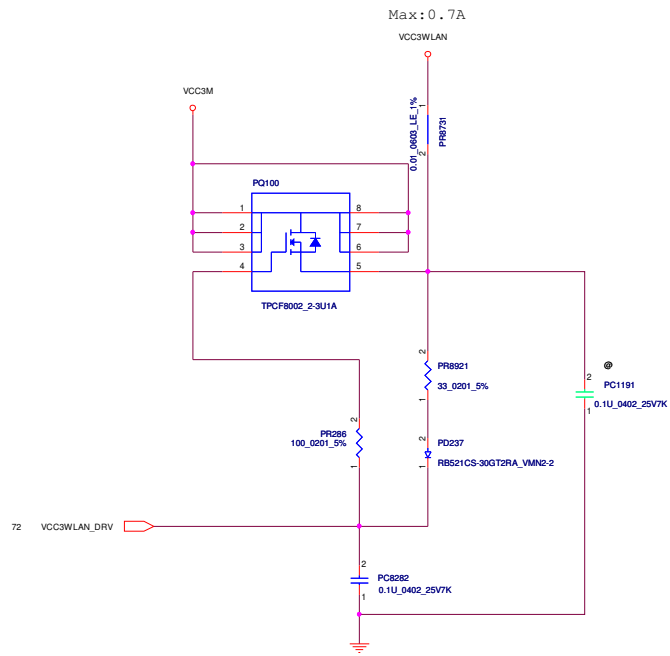
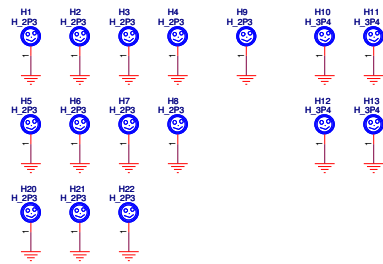


TABLE 98-1

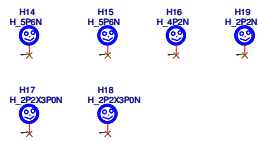
AOAC	YES	NO
PR1055	NO-ASM	ASM
PQ94	ASM	NO-ASM
PR8924	ASM	NO-ASM
PC8283	ASM	NO-ASM
PD238	ASM	NO-ASM

↑
LOGIC

PTH FOR SCREW HOLE



NPTH



FID
Board Area

- FD1 NC, NO CONNECT TO ANY.
- FD2 NC, NO CONNECT TO ANY.
- FD3 NC, NO CONNECT TO ANY.
- FD4 NC, NO CONNECT TO ANY.
- FD5 NC, NO CONNECT TO ANY.
- FD6 NC, NO CONNECT TO ANY.

FID
Component Area