

***LCFC Confidential***

***DL470***

***(L470)***


***NM-B021 Rev0.1 Schematic***

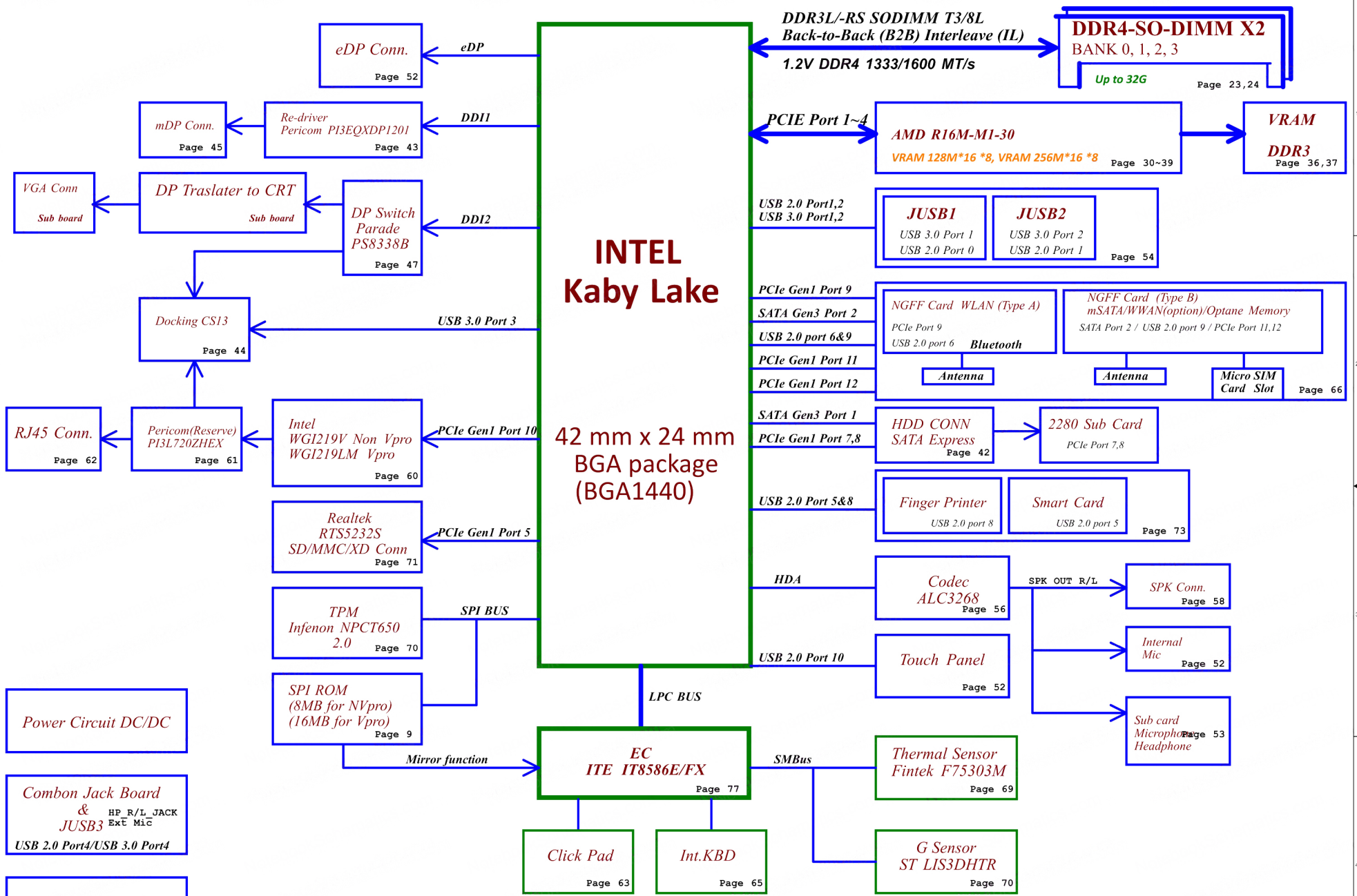
***Intel KabyLake Processor with DDR4 + PCH***

***AMD R16M-M1-30***

***2016-02-25 Rev0.1***

Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12
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Title		
COVER PAGE		
Size	Document Number	Rev
Custom	DL470_NM-B021	0.2
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# Voltage Rails

O --> Means ON  
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL						
	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

## SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

## HSIO Port

Port	Device
1	USB3.0 port (On Board)
2	USB3.0 port (On Board)
3	USB3.0 port (Docking)
4	USB3.0 port (Sub Board)
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	PCIE (LAN)
10	PCIE (Card Reader)
11	SATA express (PCIE)
12	SATA express (SATA)
13	PCIE (WLAN)
14	N/A
15	M.2 (PCIE)
16	M.2 (SATA)

## USB2.0 Port

Port	Device
1	USB port (On Board)
2	USB port (On bBoard)
3	USB port (Docking)
4	USB port (Sub Board)
5	Smart Card
6	BT
7	Camera
8	Finger Printer
9	WWAN
10	Touch Panel

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# Voltage Rails

O --> Means ON  
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.2V +0.6VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL						
	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

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	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

## HSIO Port

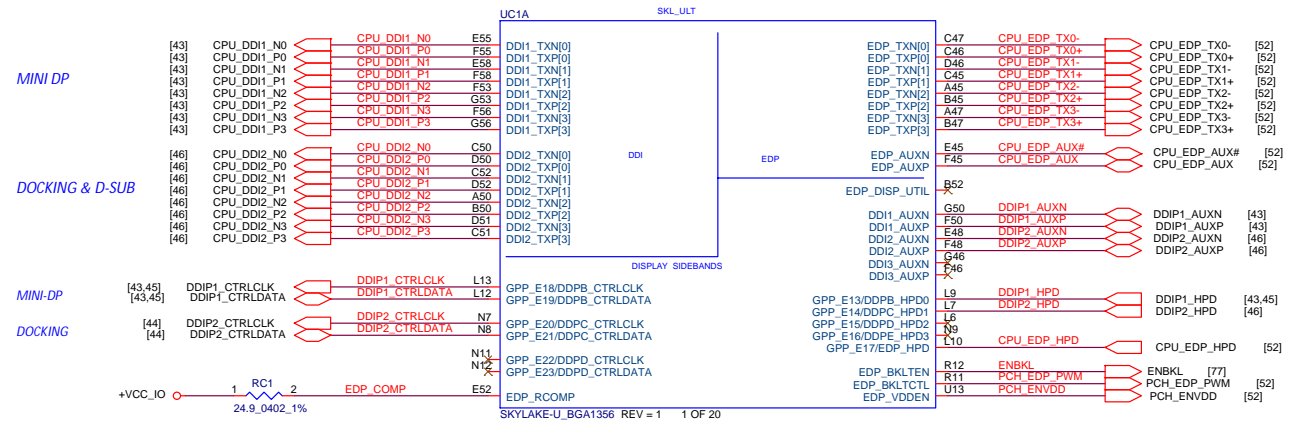
Port	Device
1	USB3.0 port (On Board)
2	USB3.0 port (On Board)
3	USB3.0 port (Docking)
4	USB3.0 port (Sub Board)
5	PCIE (GPU)
6	PCIE (GPU)
7	PCIE (GPU)
8	PCIE (GPU)
9	PCIE (LAN)
10	PCIE (Card Reader)
11	SATA express (PCIE)
12	SATA express (SATA)
13	PCIE (WLAN)
14	N/A
15	M.2 (PCIE)
16	M.2 (SATA)

## USB2.0 Port

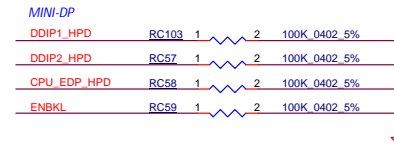
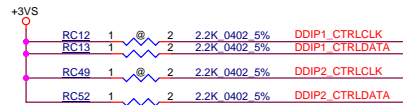
Port	Device
1	USB port (On Board)
2	USB port (On bBoard)
3	USB port (Docking)
4	USB port (Sub Board)
5	Smart Card
6	BT
7	Camera
8	Finger Printer
9	WWAN
10	Touch Panel

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**EDP\_RCOMP**  
 1. Trace width=20 mils, Spacing=25mil, Max length=100mils  
 2. RC1 close to MCP  
 Trace Width=20mil, Spacing=25mil, Max length=100mil



DDIP2\_HPD : PS8338B has Int.PD 150K

DP port	Enable	Disable
DDPB_CTRLDATA	pull-high	no connect
DDPC_CTRLDATA	pull-high	no connect

TABLE	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL8	DDR0_DQ[1]	DDR0_DQ[1]
	AN88	DDR0_DQ[2]	DDR0_DQ[2]
	AN89	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL89	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AN72	DDR0_DQ[8]	DDR0_DQ[8]
	AR88	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU69	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR89	DDR0_DQ[13]	DDR0_DQ[13]
AU70	DDR0_DQ[14]	DDR0_DQ[14]	
AU89	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB55	DDR0_DQ[16]	DDR0_DQ[16]
	AW65	DDR0_DQ[17]	DDR0_DQ[17]
	AW63	DDR0_DQ[18]	DDR0_DQ[18]
	A180	DDR0_DQ[19]	DDR0_DQ[19]
	AY66	DDR0_DQ[20]	DDR0_DQ[20]
	AY66	DDR0_DQ[21]	DDR0_DQ[21]
	BA83	DDR0_DQ[22]	DDR0_DQ[22]
	BB55	DDR0_DQ[23]	DDR0_DQ[23]
	BA81	DDR0_DQ[24]	DDR0_DQ[24]
	AW61	DDR0_DQ[25]	DDR0_DQ[25]
	BB58	DDR0_DQ[26]	DDR0_DQ[26]
	AW69	DDR0_DQ[27]	DDR0_DQ[27]
	BB81	DDR0_DQ[28]	DDR0_DQ[28]
	AY19	DDR0_DQ[29]	DDR0_DQ[29]
AY68	DDR0_DQ[31]	DDR0_DQ[31]	
Block 4	AY38	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY36	DDR0_DQ[40]	DDR1_DQ[8]
	AW36	DDR0_DQ[41]	DDR1_DQ[9]
	AY38	DDR0_DQ[42]	DDR1_DQ[10]
	AW39	DDR0_DQ[43]	DDR1_DQ[11]
	BB38	DDR0_DQ[44]	DDR1_DQ[12]
	BA36	DDR0_DQ[45]	DDR1_DQ[13]
BA33	DDR0_DQ[46]	DDR1_DQ[14]	
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY19	DDR0_DQ[48]	DDR1_DQ[16]
	AW19	DDR0_DQ[49]	DDR1_DQ[17]
	AY28	DDR0_DQ[50]	DDR1_DQ[18]
	AW28	DDR0_DQ[51]	DDR1_DQ[19]
	BB31	DDR0_DQ[52]	DDR1_DQ[20]
	BA31	DDR0_DQ[53]	DDR1_DQ[21]
	BA29	DDR0_DQ[54]	DDR1_DQ[22]
	BB29	DDR0_DQ[55]	DDR1_DQ[23]
	AY27	DDR0_DQ[56]	DDR1_DQ[24]
	AW27	DDR0_DQ[57]	DDR1_DQ[25]
	AY26	DDR0_DQ[58]	DDR1_DQ[26]
	AW26	DDR0_DQ[59]	DDR1_DQ[27]
	BB27	DDR0_DQ[60]	DDR1_DQ[28]
	BA27	DDR0_DQ[61]	DDR1_DQ[29]
BA26	DDR0_DQ[62]	DDR1_DQ[30]	
BB26	DDR0_DQ[63]	DDR1_DQ[31]	

[23] DDR\_A\_D[63..0]

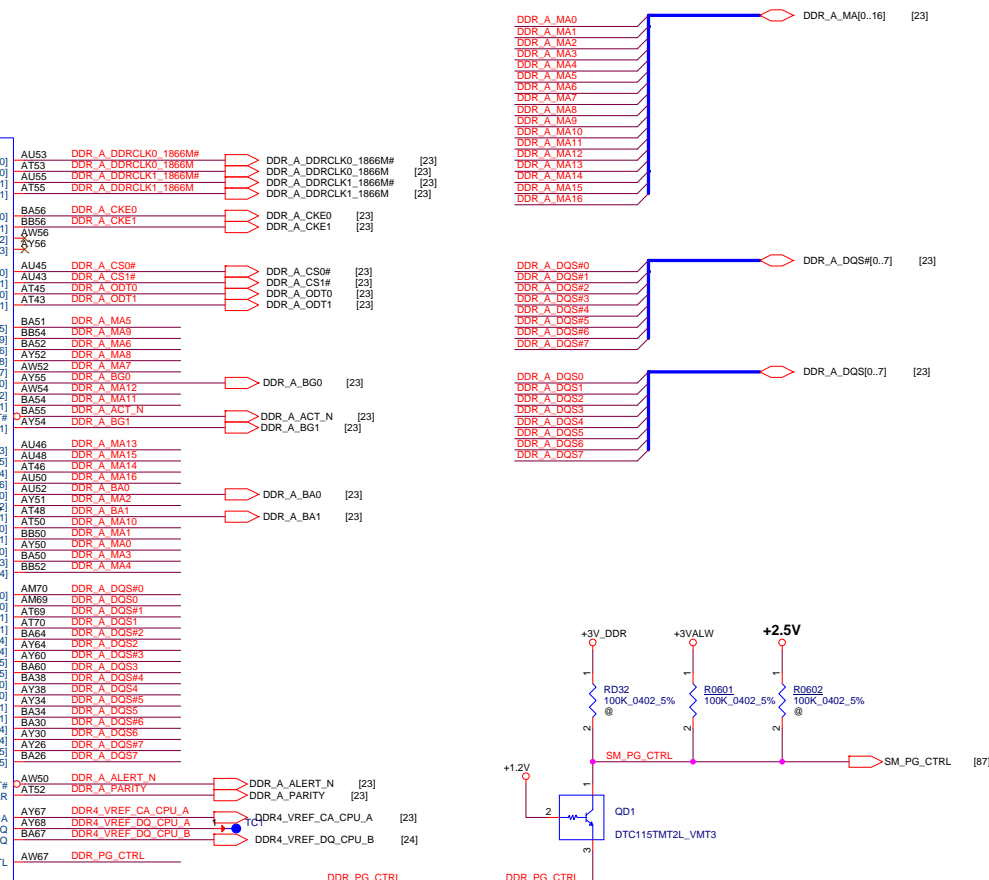
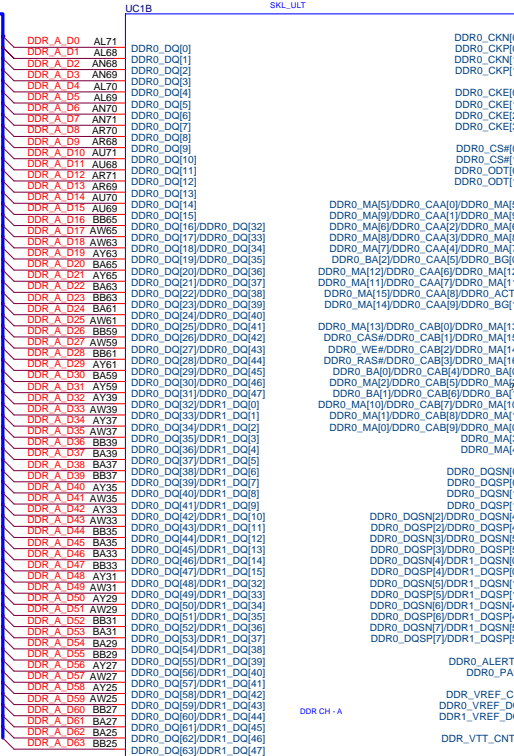


TABLE	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[2]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[2]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[3]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[4]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[4]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[5]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[6]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[6]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[7]

TABLE	Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]	
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]	
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]	
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]	
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]	
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]	
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]	
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]	
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#	
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]	
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]	
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]	
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]	
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]	
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]	
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]	
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]	
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]	
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]	
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]	
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]	
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]	

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Size	Document Number	Rev		0.2
Cushtm	<b>DL470_NM-B021</b>	Date:		Friday, November 04, 2016   Sheet 6 of 99

TABLE	Pin	Interleave	Non-Interleave
Block 1	AF66	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK66	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF68	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK68	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
AH70	DDR1_DQ[14]	DDR0_DQ[30]	
AH69	DDR1_DQ[15]	DDR0_DQ[31]	
Block 3	AT68	DDR1_DQ[16]	DDR0_DQ[48]
	AU68	DDR1_DQ[17]	DDR0_DQ[49]
	AF66	DDR1_DQ[18]	DDR0_DQ[50]
	AN66	DDR1_DQ[19]	DDR0_DQ[51]
	AN68	DDR1_DQ[20]	DDR0_DQ[52]
	AF68	DDR1_DQ[21]	DDR0_DQ[53]
	AT66	DDR1_DQ[22]	DDR0_DQ[54]
	AU66	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AF60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AF61	DDR1_DQ[29]	DDR0_DQ[61]
AT60	DDR1_DQ[30]	DDR0_DQ[62]	
AU60	DDR1_DQ[31]	DDR0_DQ[63]	
Block 6	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AF40	DDR1_DQ[37]	DDR1_DQ[21]
	AF37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU39	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AF33	DDR1_DQ[45]	DDR1_DQ[29]
AR30	DDR1_DQ[46]	DDR1_DQ[30]	
AF30	DDR1_DQ[47]	DDR1_DQ[31]	
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT26	DDR1_DQ[50]	DDR1_DQ[50]
	AU26	DDR1_DQ[51]	DDR1_DQ[51]
	AF27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN26	DDR1_DQ[54]	DDR1_DQ[54]
	AF26	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AF22	DDR1_DQ[61]	DDR1_DQ[61]
AF21	DDR1_DQ[62]	DDR1_DQ[62]	
AN21	DDR1_DQ[63]	DDR1_DQ[63]	

[24] DDR\_B\_D[0..63]

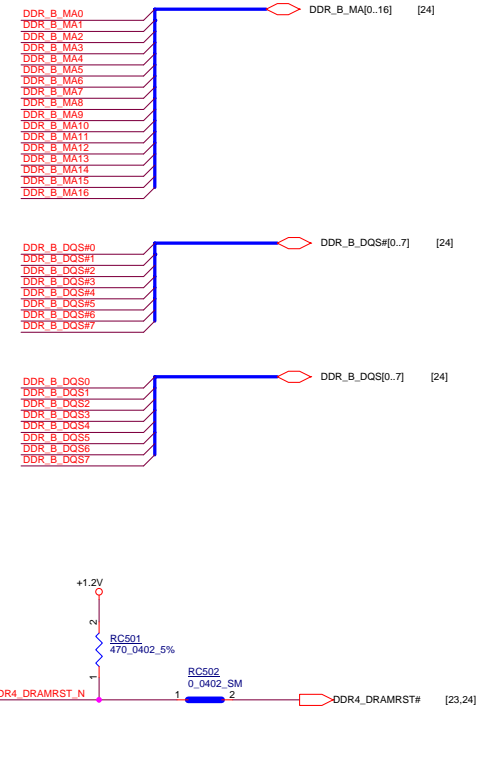
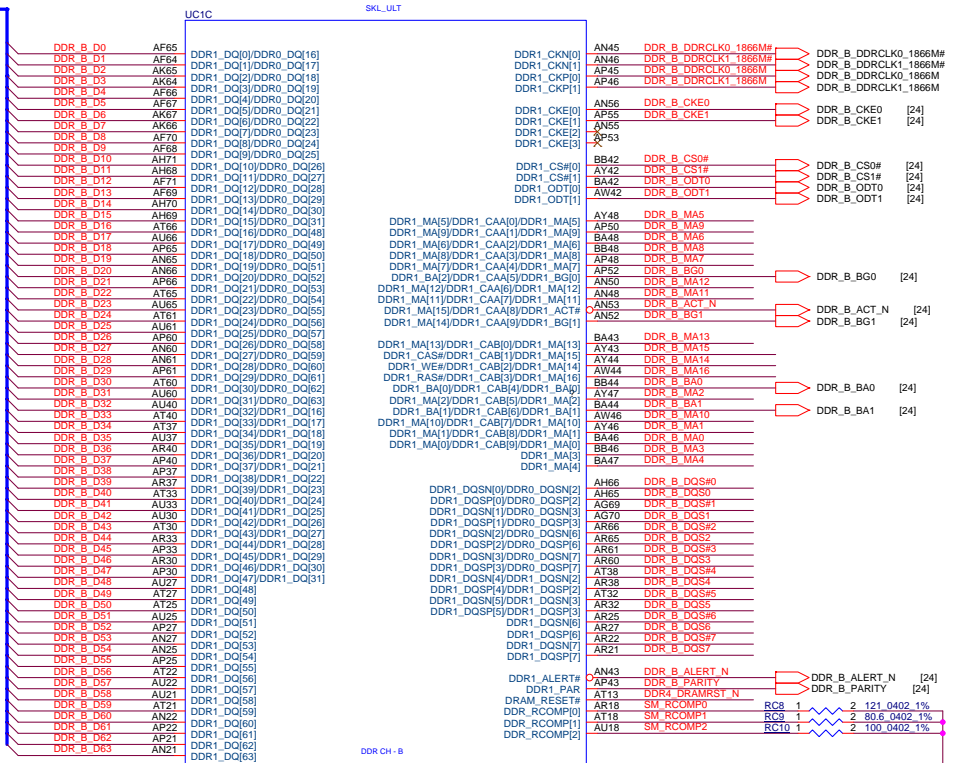
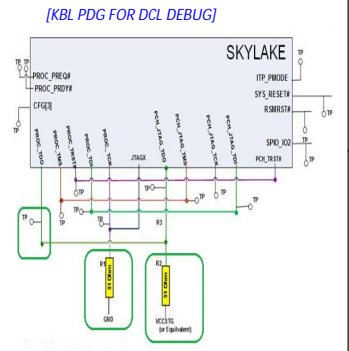
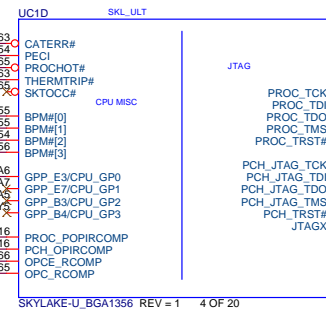
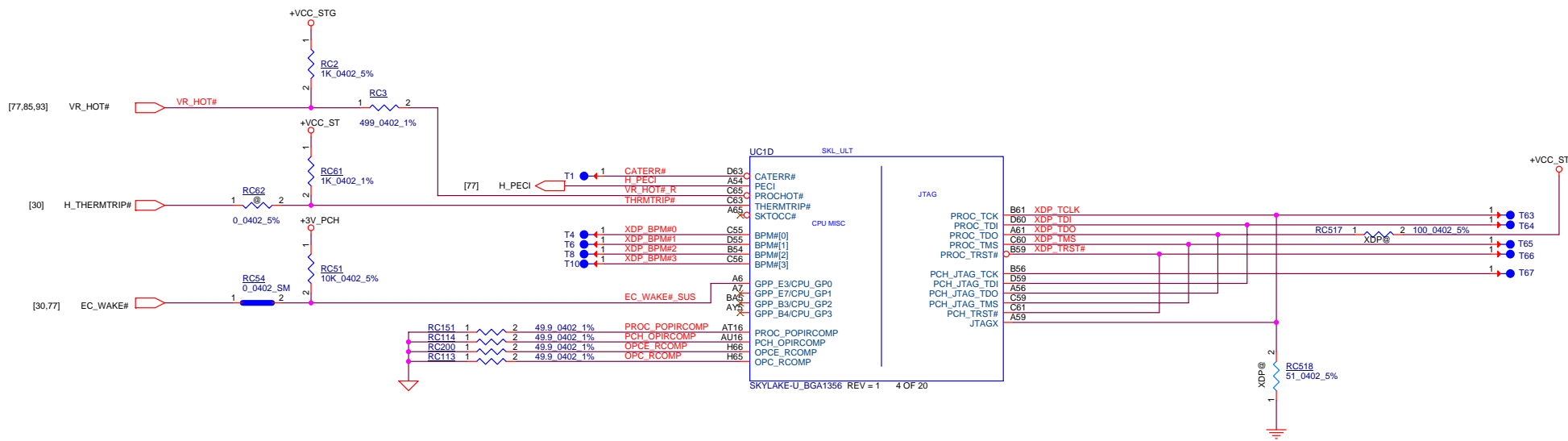



TABLE	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE	Pin	DDR3L	LPDDR3	DDR4
Block 1	AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
	AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
	BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
	BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
	AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
	AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BA[2]
	AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
	AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
	AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
	AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
Block 2	BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
	AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
	AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
	AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
	BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_MA[10]
	AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
	BB44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_MA[11]
	AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
	AY46	DDR1_MA[11]	DDR1_CAB[8]	DDR1_MA[11]
	BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BB47	DDR1_MA[4]	Not Used	DDR1_MA[4]	

[KBL PDG] for DDR4 COMPENSATION  
 DDR\_RCOMP[0] Pull down 121 ohm resistor  
 DDR\_RCOMP[1] Pull down 80.6 ohm resistor  
 DDR\_RCOMP[2] Pull down 100 ohm resistor

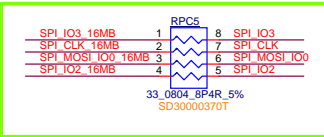
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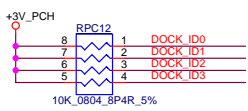
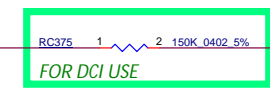
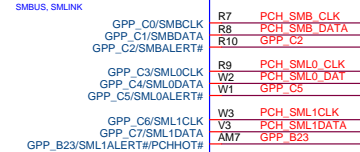
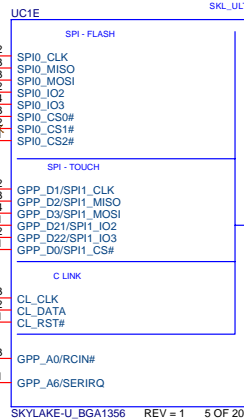
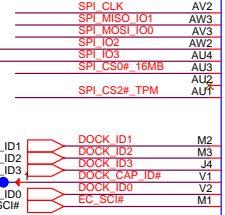
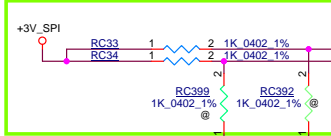
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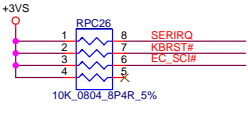
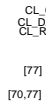
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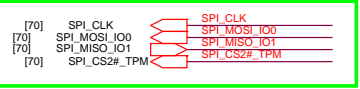
Reverse internal 1K PU high



C-LINK

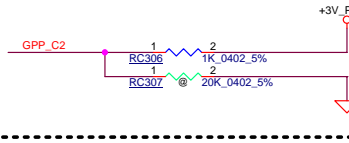


To TPM IC

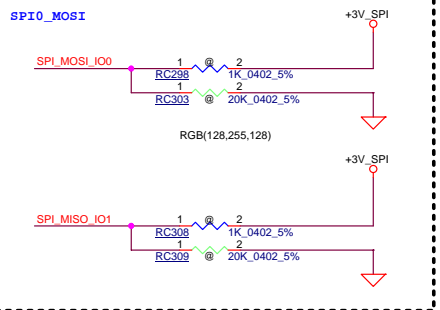


Functional Strap Definitions

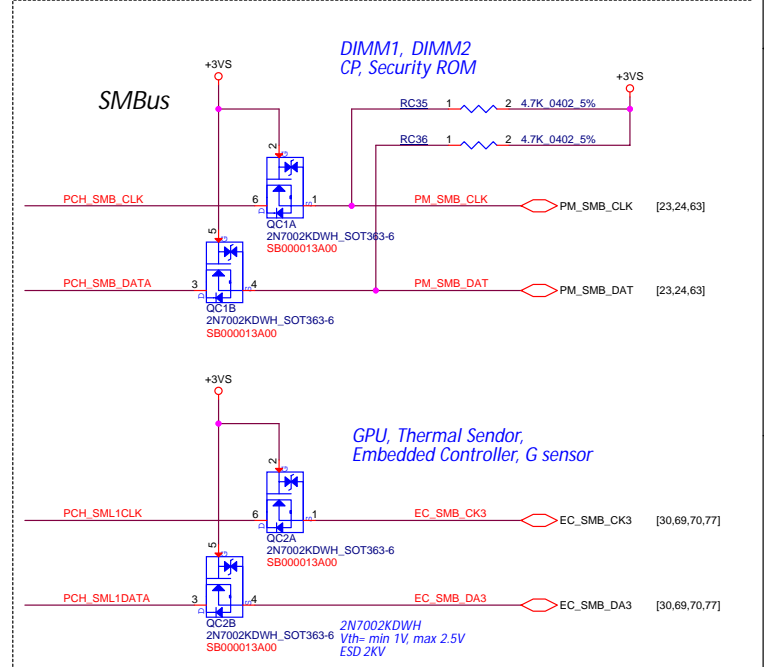
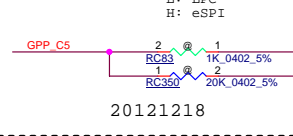
L: Disable Intel ME Crypto TLS cipher suite (no confidentiality).  
 \*H: Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.  
**GPP\_C2, Internal PD 20K**



JTAG ODT

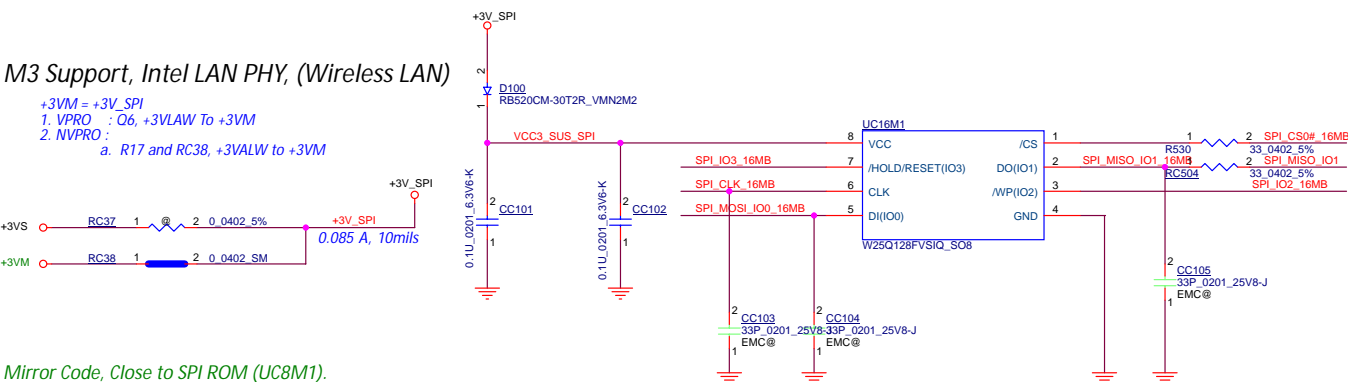


GPP\_C5, Internal PD 20K

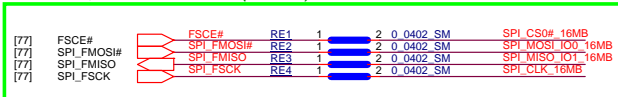


M3 Support, Intel LAN PHY, (Wireless LAN)

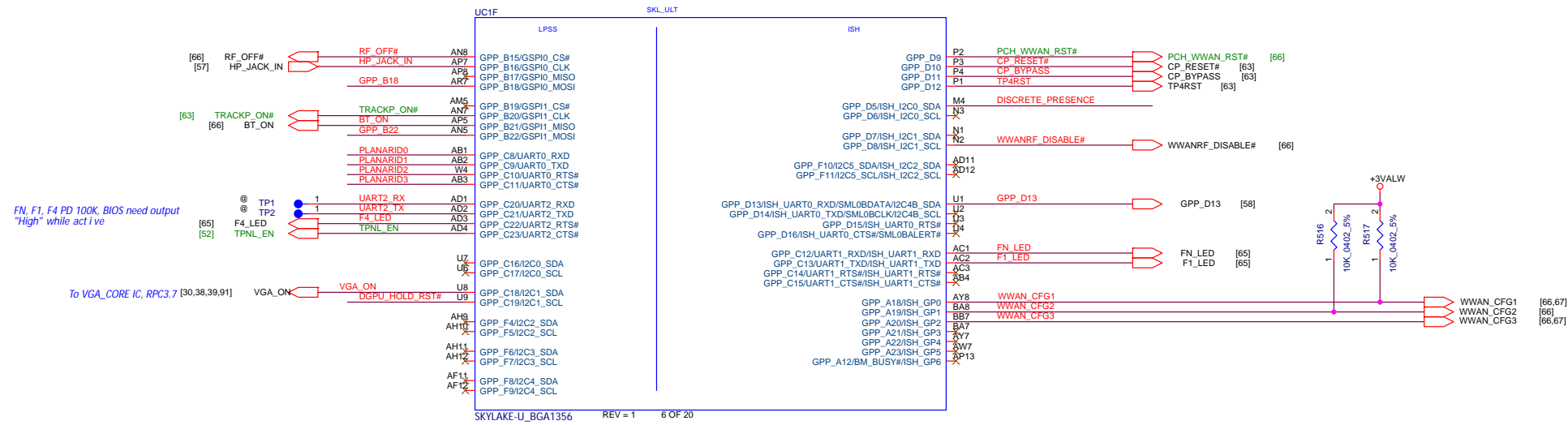
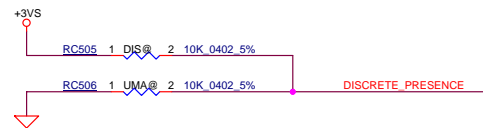
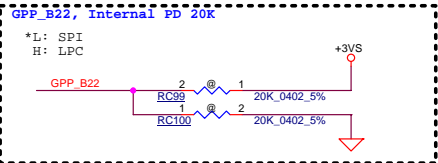
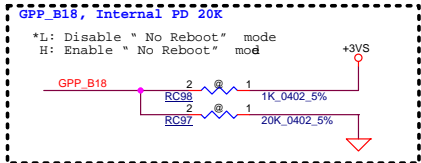
+3VM = +3V\_SPI  
 1. VPRO : Q6, +3VALW To +3VM  
 2. NVPRO : a. R17 and RC38, +3VALW to +3VM



Mirror Code, Close to SPI ROM (UC8M1).



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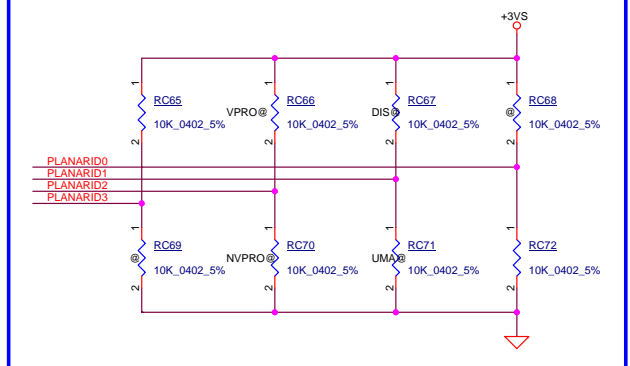
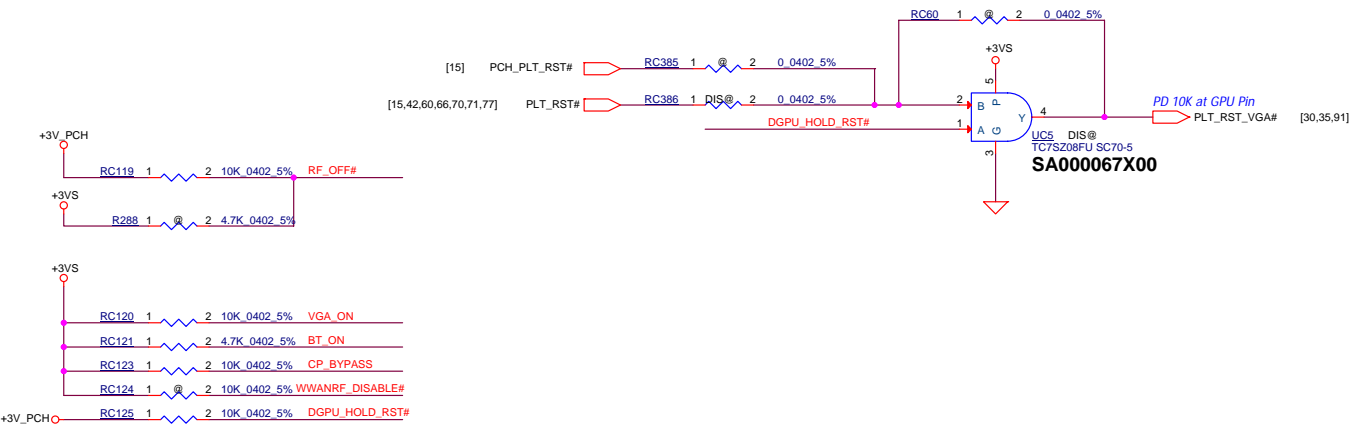
FN, F1, F4 PD 100K, BIOS need output "High" while active

To VGA\_CORE IC, RPC3.7 [30.38,39.91]

SKYLAKE-U\_BGA1356 REV = 1 6 OF 20

Project/SKU ID

	PLANARID3 (GPP_C11)	PLANARID2 (GPP_C10)	PLANARID1 (GPP_C9)	PLANARID0 (GPP_C8)
1	1(RC65)	VPRO SKU (RC66)	DIS (RC67)	15" (RC68)
0	X	NVPRO SKU (RC70)	UMA (RC71)	14" (RC72)

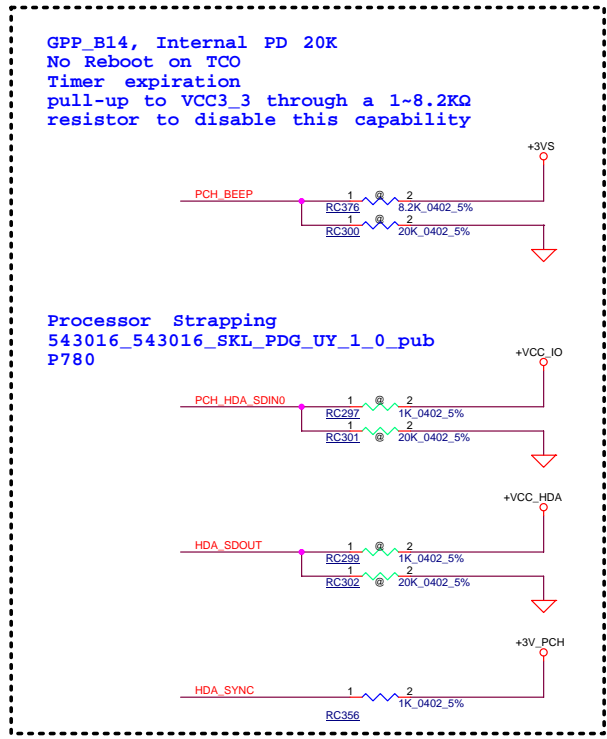
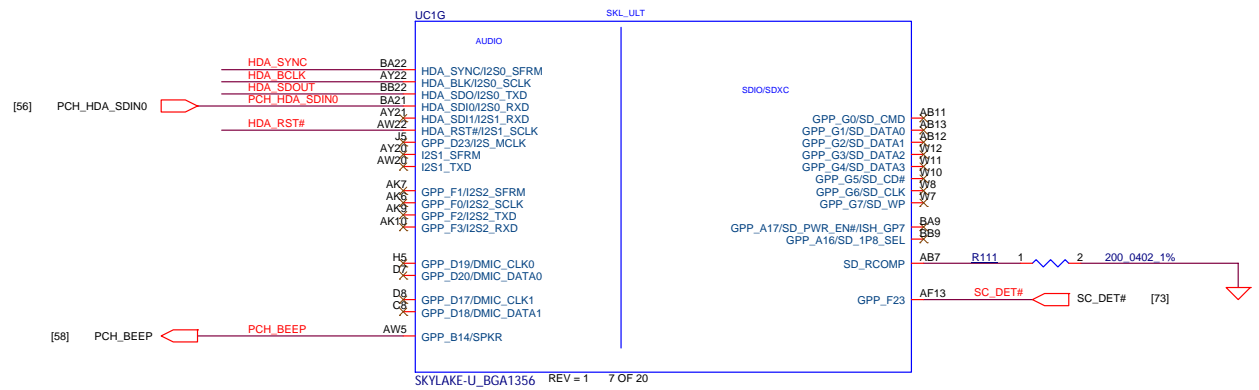
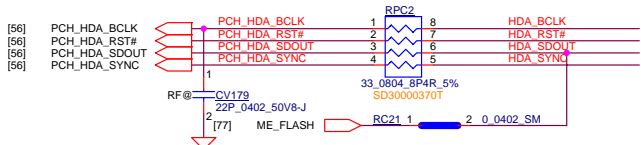


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**SKL\_GPIO**

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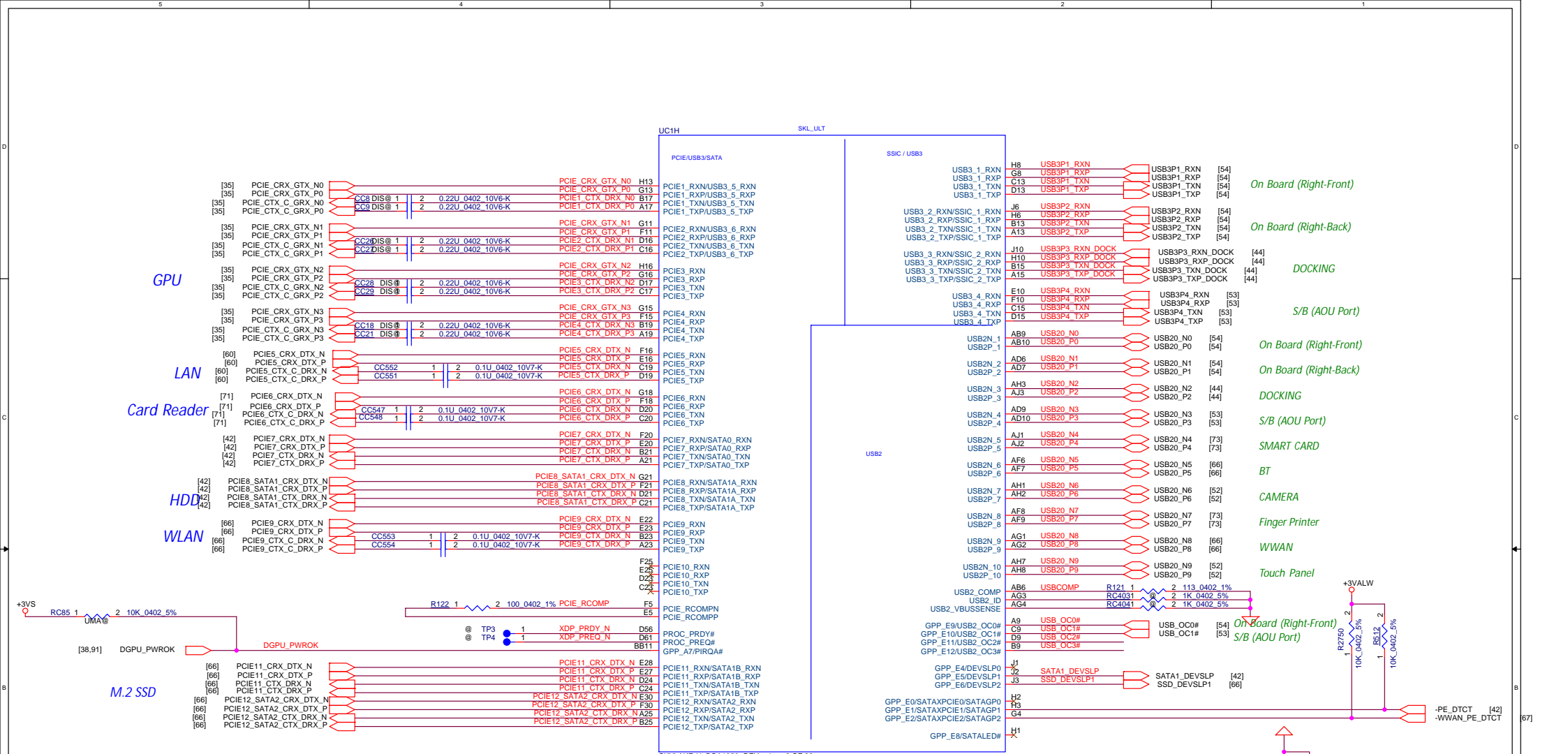


Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

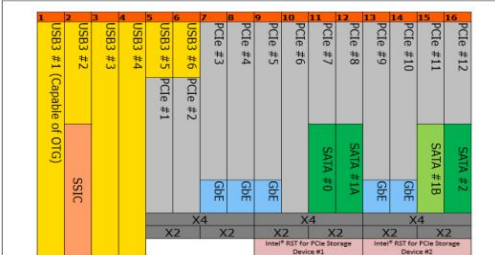
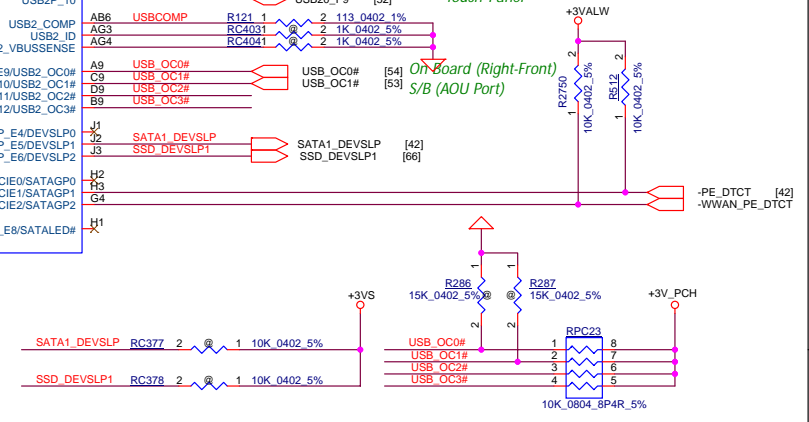
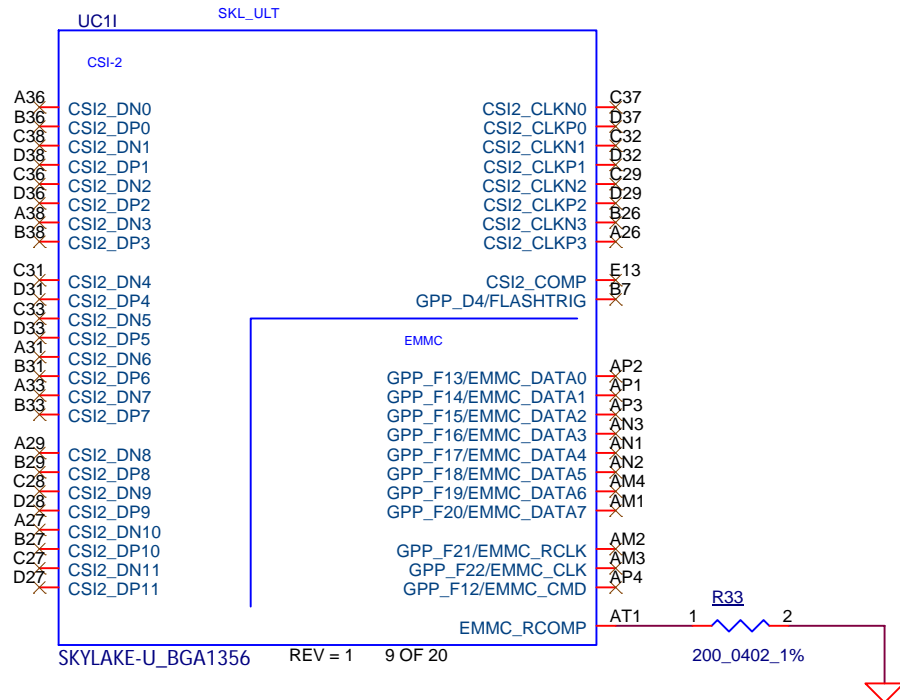


Table 12-1. PCI Express\* Link Configurations Supported by the Guidelines in this Chapter (Sheet 1 of 2)

SKL PCH	Max Device Ports	Max Lanes	PCIe Link Config	Flexible HSIO Lanes													
				PCIe Controller 1				PCIe Controller 2				PCIe Controller 3					
				5	6	7	8	9	10	11	12	13	14	15	16		
				PCI Express* Lanes													
				1	2	3	4	5	6	7	8	9	10	11	12		
				P1			P5			P9			P11				
				2x2+2x1		P1	P3	P5	P7	P9	P11	P12					
				2x1+1x2		P4	P3	P1	P8	P7	P5	P12	P11	P9			
				4x1		P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12




Pin.	USB3.0 Port NO.	USB2.0 Port NO.	Default Port Mapping
USB_OCO#	Port 1, 2	Port 0, 1	Port 0, 1
USB_OCI#	Port 4	Port 3	Port 2, 3
USB_OC2#	Unused.	Unused.	Port 4, 5
USB_OC3#	Unused.	Unused.	Port 6, 7

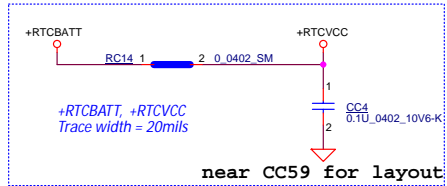


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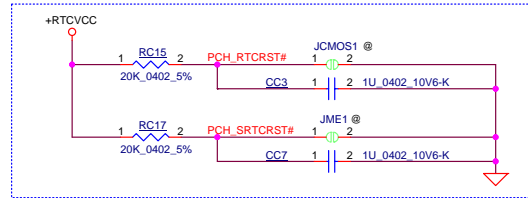
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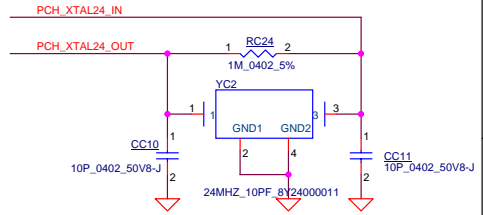
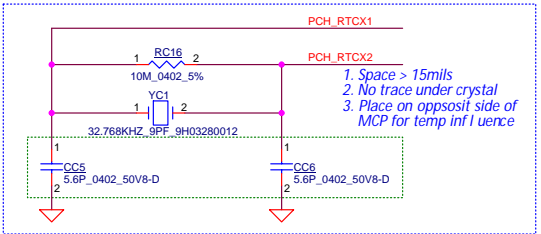
RTC External Circuit



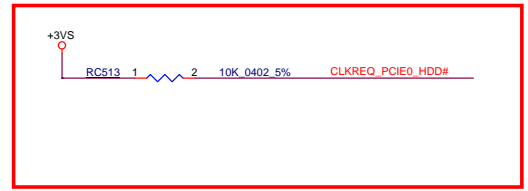
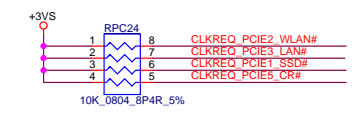
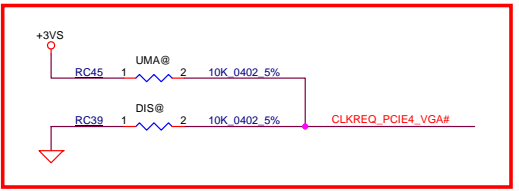
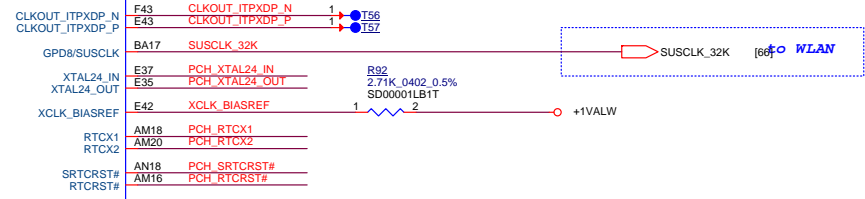
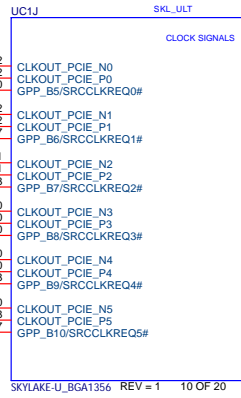
JCMOS, JME Set ting Near Undr DIR Dao

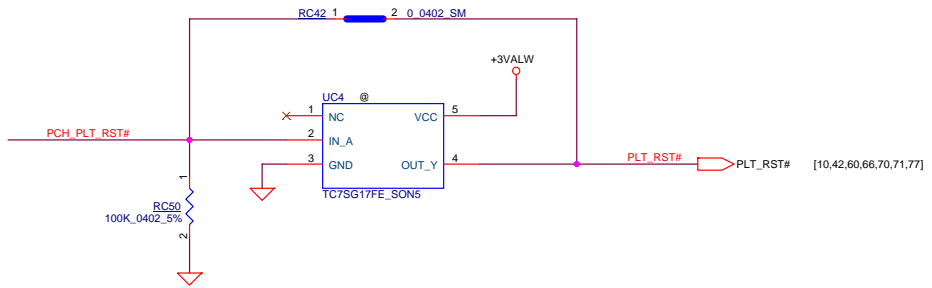
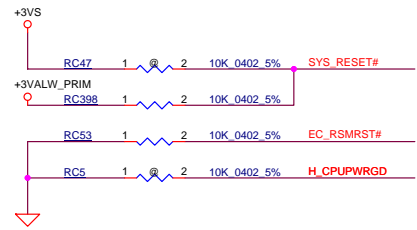
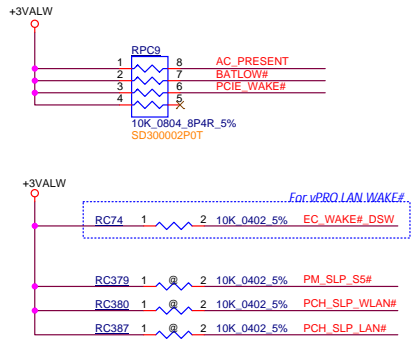
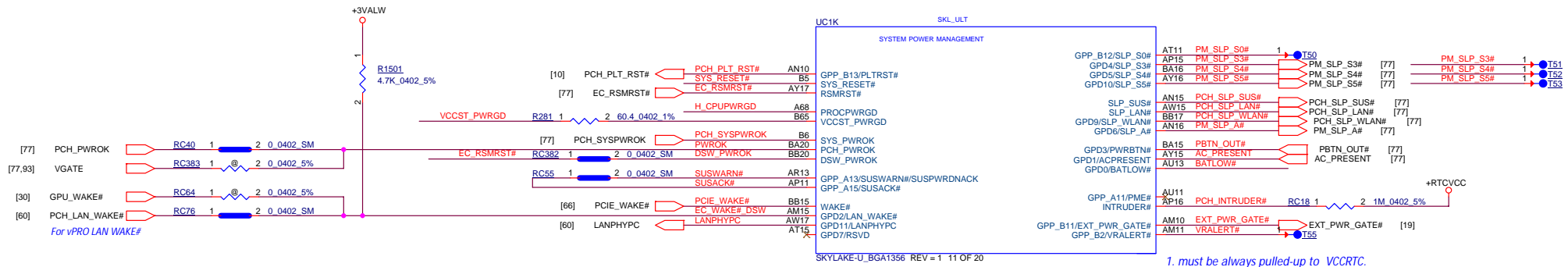


RTC Crystal

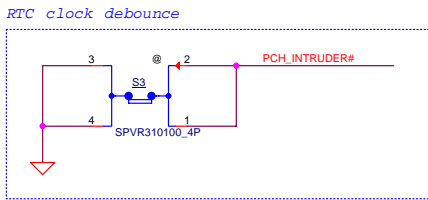
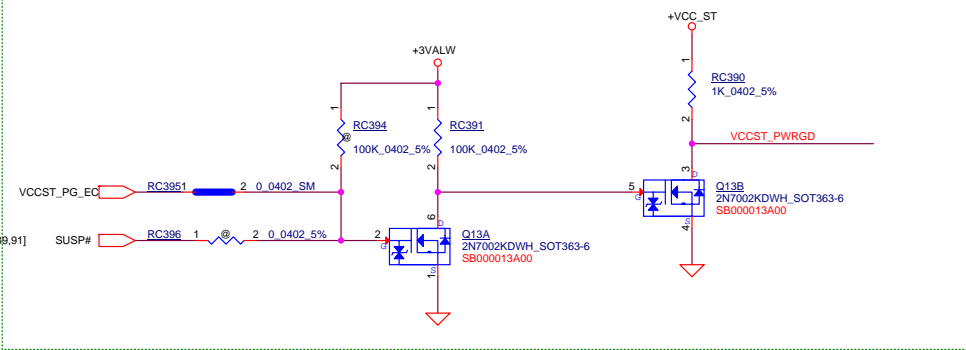


Component	Pin	Signal	Pin	Signal
HDD	[42]	CLK_PCIE_HDD#	D42	CLKOUT_PCIE_N0
	[42]	CLK_PCIE_HDD	C42	CLKOUT_PCIE_P0
	[42]	CLKREQ_PCIE0_HDD#	AR10	GPP_B5/SRCLKREQ0#
M.2 SSD	[66]	CLK_PCIE_SSD#	B42	CLKOUT_PCIE_N1
	[66]	CLK_PCIE_SSD	A42	CLKOUT_PCIE_P1
	[66]	CLKREQ_PCIE1_SSD#	AT7	GPP_B9/SRCLKREQ1#
WLAN	[66]	CLK_PCIE_WLAN#	D41	CLKOUT_PCIE_N2
	[66]	CLK_PCIE_WLAN	C41	CLKOUT_PCIE_P2
	[66]	CLKREQ_PCIE2_WLAN#	AT8	GPP_B7/SRCLKREQ2#
LAN	[60]	CLK_PCIE_LAN#	D40	CLKOUT_PCIE_N3
	[60]	CLK_PCIE_LAN	C40	CLKOUT_PCIE_P3
	[60]	CLKREQ_PCIE3_LAN#	AT10	GPP_B8/SRCLKREQ3#
VGA	[35]	CLK_PCIE_VGA#	B40	CLKOUT_PCIE_N4
	[35]	CLK_PCIE_VGA	A40	CLKOUT_PCIE_P4
	[30]	CLKREQ_PCIE4_VGA#	AU8	GPP_B9/SRCLKREQ4#
CR	[71]	CLK_PCIE_CR#	E40	CLKOUT_PCIE_N5
	[71]	CLK_PCIE_CR	E38	CLKOUT_PCIE_P5
	[71]	CLKREQ_PCIE5_CR#	AU7	GPP_B10/SRCLKREQ5#

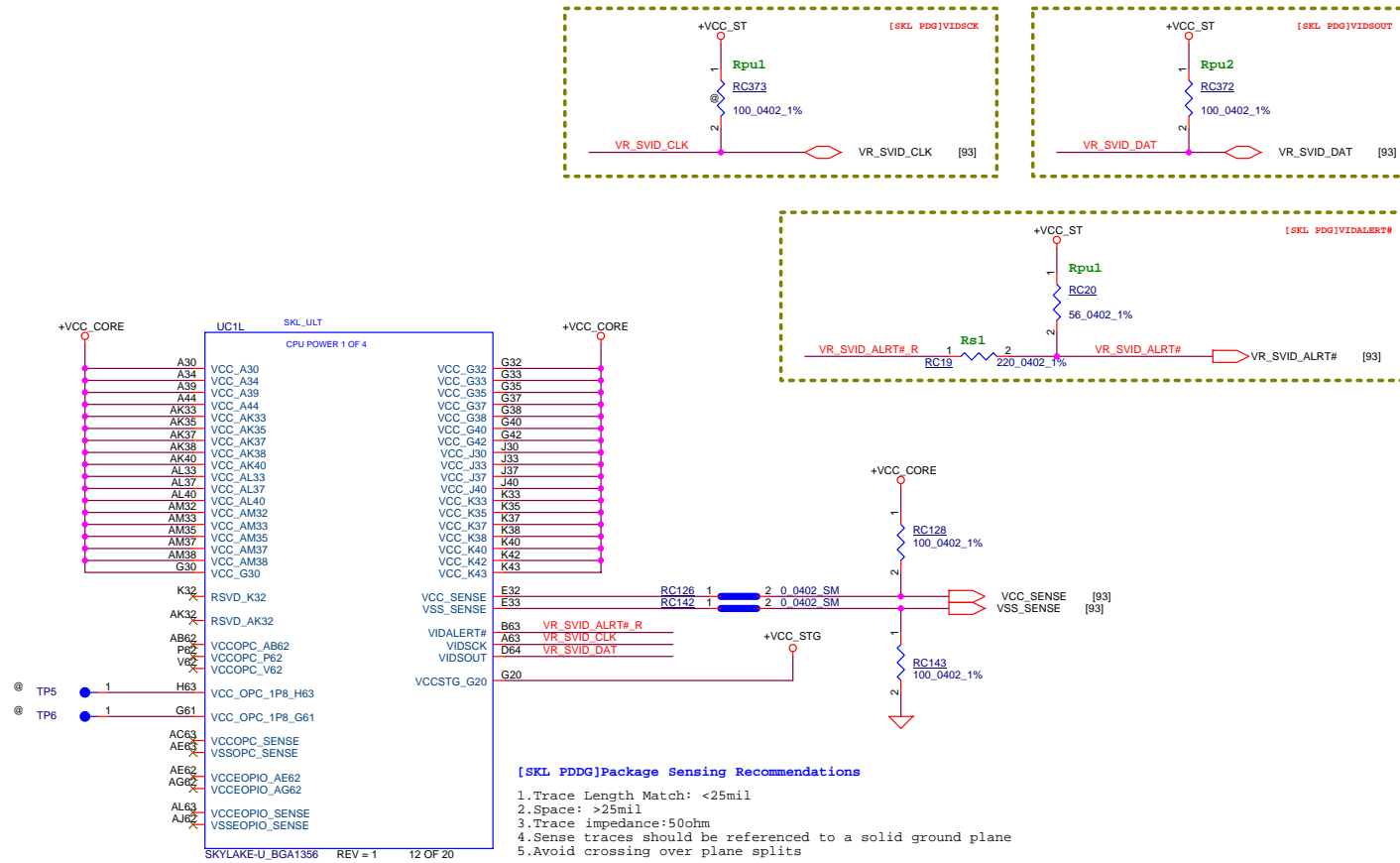




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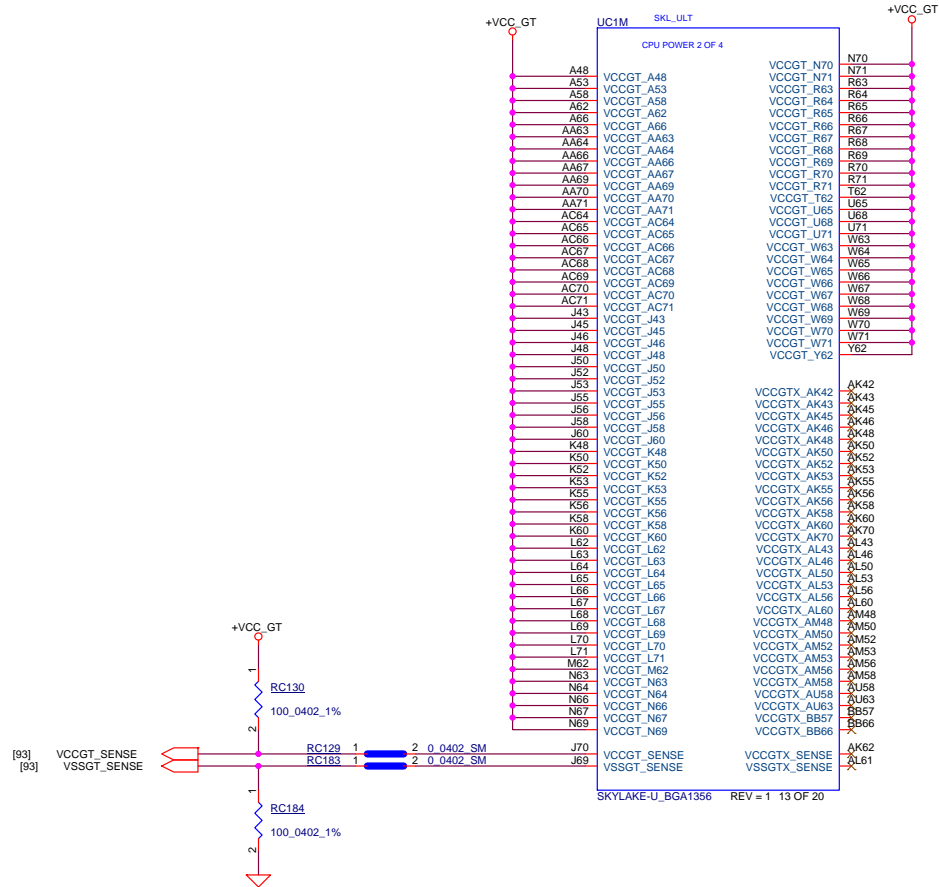


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Custom			0.2
Date:	Friday, November 04, 2016	Sheet	16 of 99

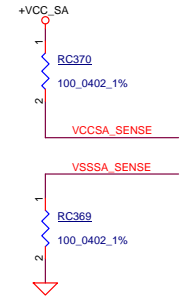
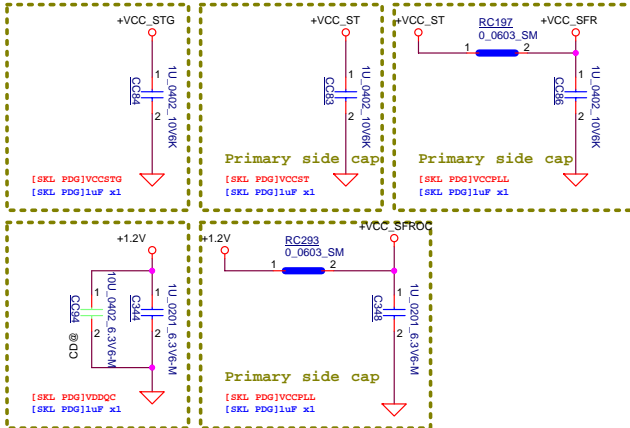
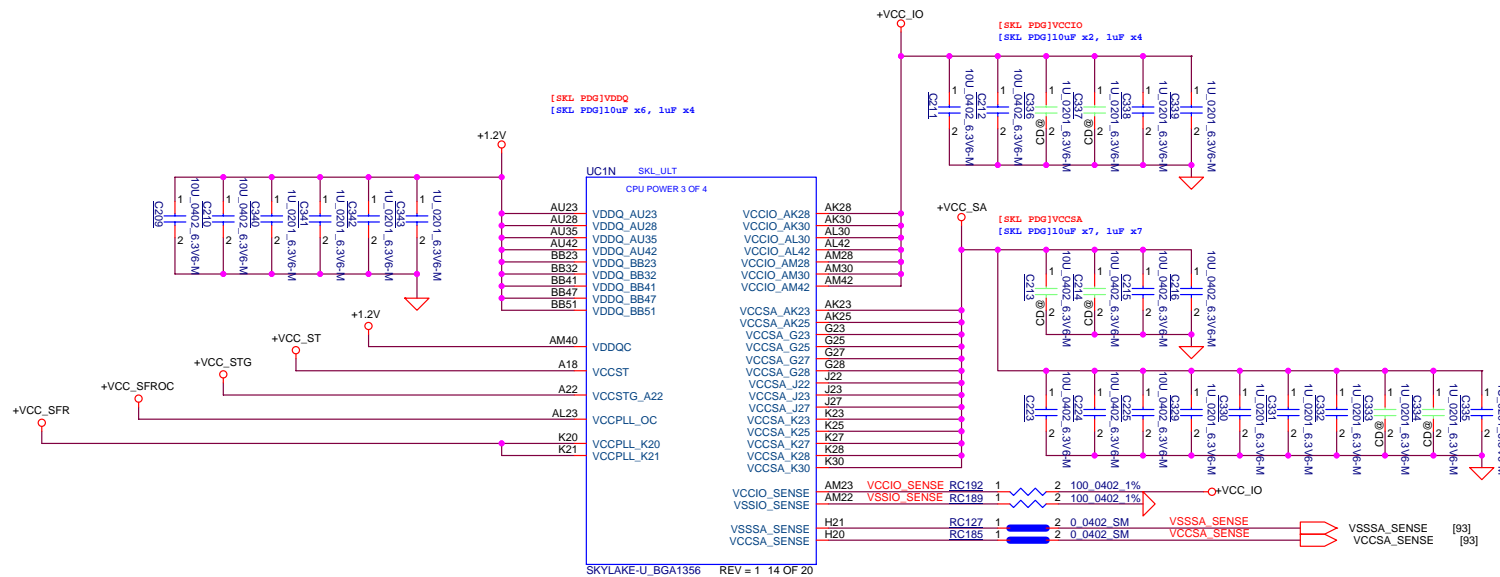






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Title		
KBL_POWER_VCCGT		
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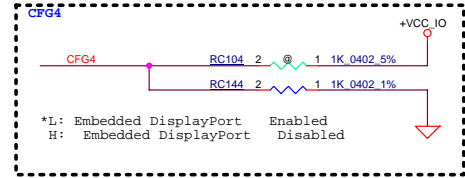
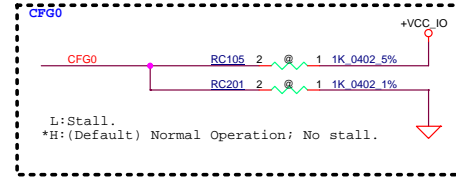


Power Rail	Description	Control
VCC	Processor IA Cores Power Rail	SVID
VccGT	Processor Graphics Power Rails	SVID
VccGTX	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VccSA	System Agent Power Rail	SVID
VccIO	IO Power Rail	Fixed
VccST	Sustain Power Rail	Fixed
VccPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed
VccOPC	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccOPC_1P8	Processor OPC power rail (available only in SKU' s with OPC)	Fixed
VccEOPIO	Processor OPC power rail (available only in SKU' s with OPC)	Fixed



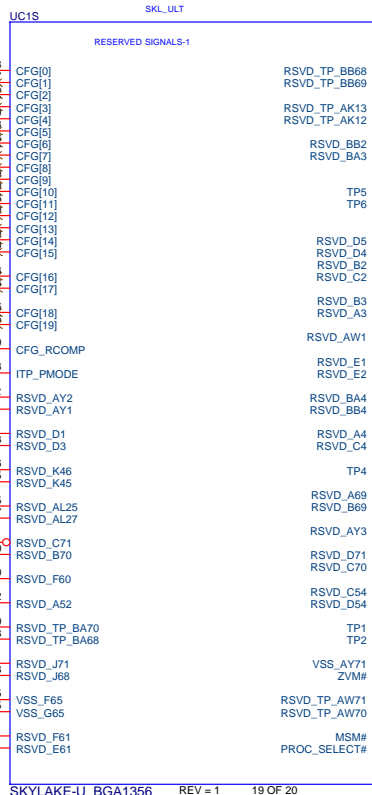


[SKL\_EDS]



L: Stall.  
\*H: (Default) Normal Operation; No stall.

\*L: Embedded DisplayPort Enabled  
H: Embedded DisplayPort Disabled



[SKL\_CRB]  
RC152 2 1 49.9 0402 1%  
RC371 2 1 1.5K 0402 5%  
+1VALW\_PCH

[SKL\_PDG]Route HOOK[6] to Skylake ITP\_PMODE. Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH\_V1.0A Rail.

**TABLE**

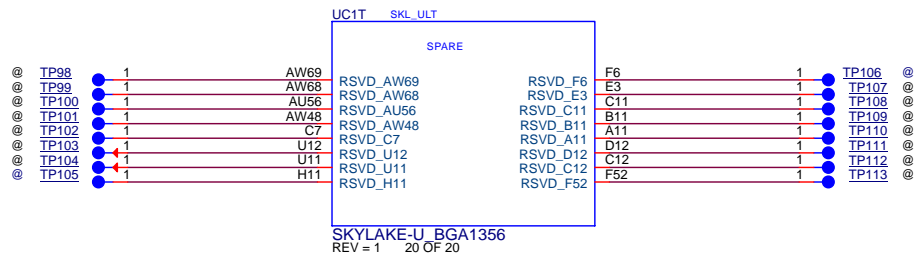
<p><b>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted</b> 1 : No Stall 0 : Stall</p>
<p><b>CFG4 : eDP Enable</b> 1 : Disabled 0 : Enabled</p>
<p><b>CFG9 : SVID Bus Communication</b> 1 : Enabled 0 : Disabled</p>

[SKL\_EDS]Zero Voltage Mode:VCCOCP is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM# state	VCCOCP
0V	0V
1V	1V

[SKL\_EDS]Minimum Speed Mode: VCCEPIO can be connected to OPC VR in this case VCCEPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal . In order to achieve better power/performance it is recommended to use a separate VR for VCCEPIO in this case VCCEPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EPIO interface as shown below:

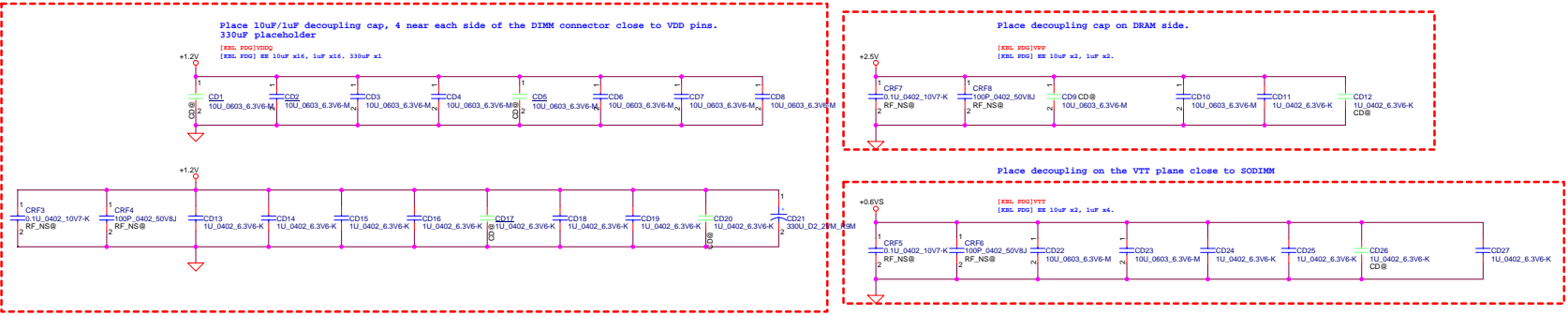
ZVM# state	MSM# state	VCCEPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V



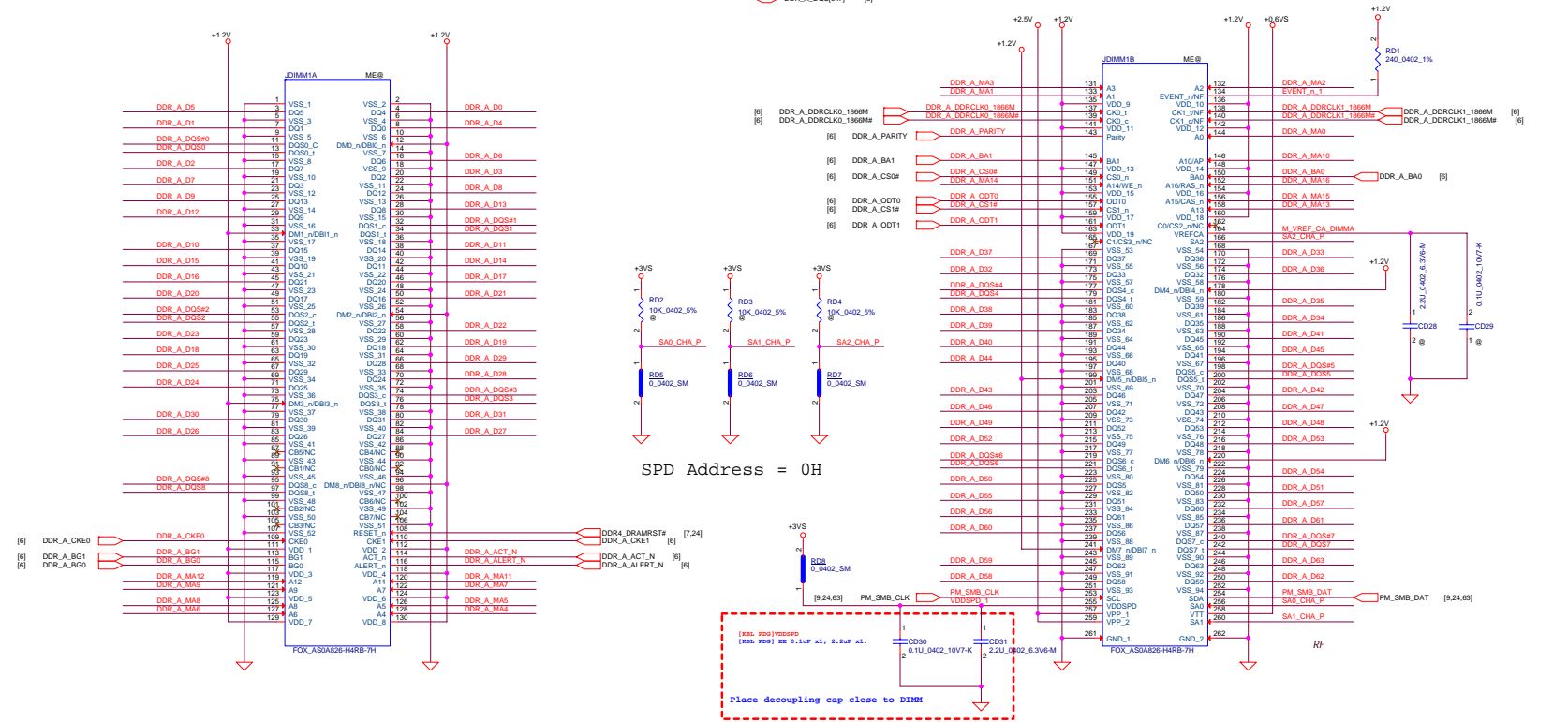
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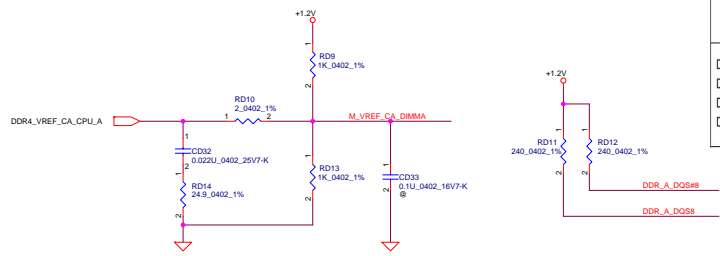
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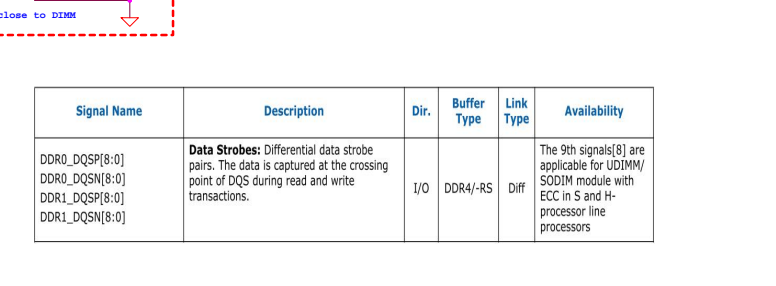
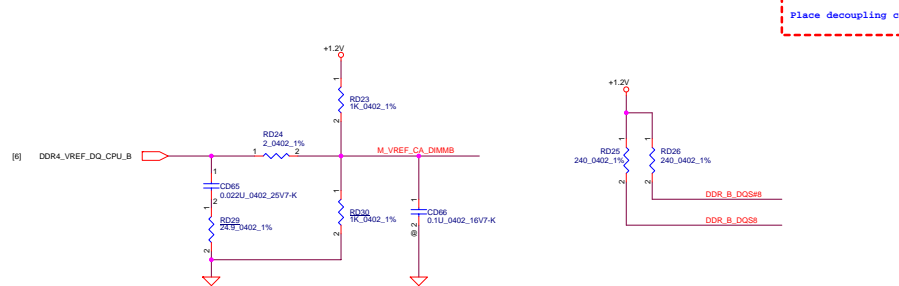
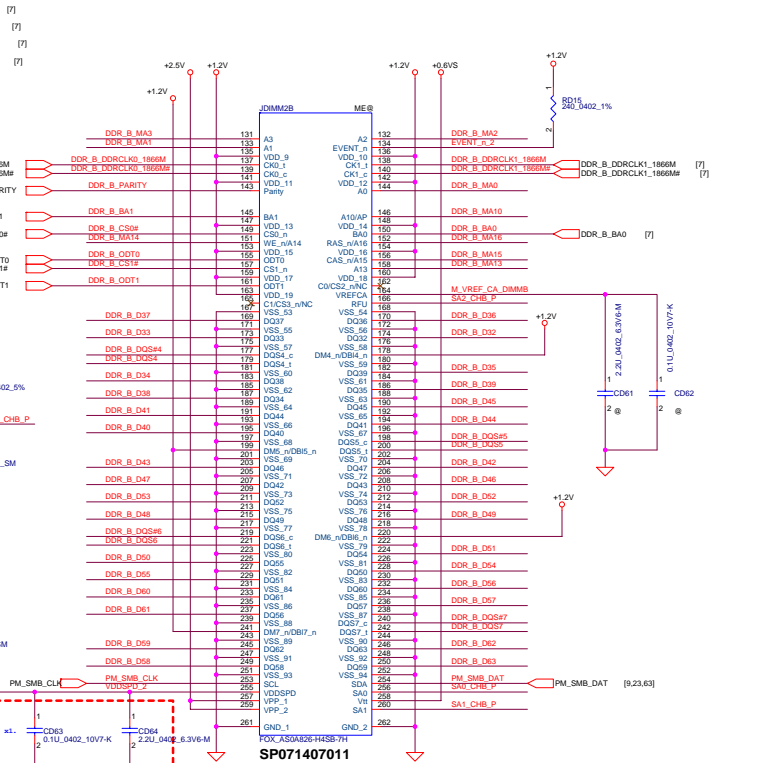
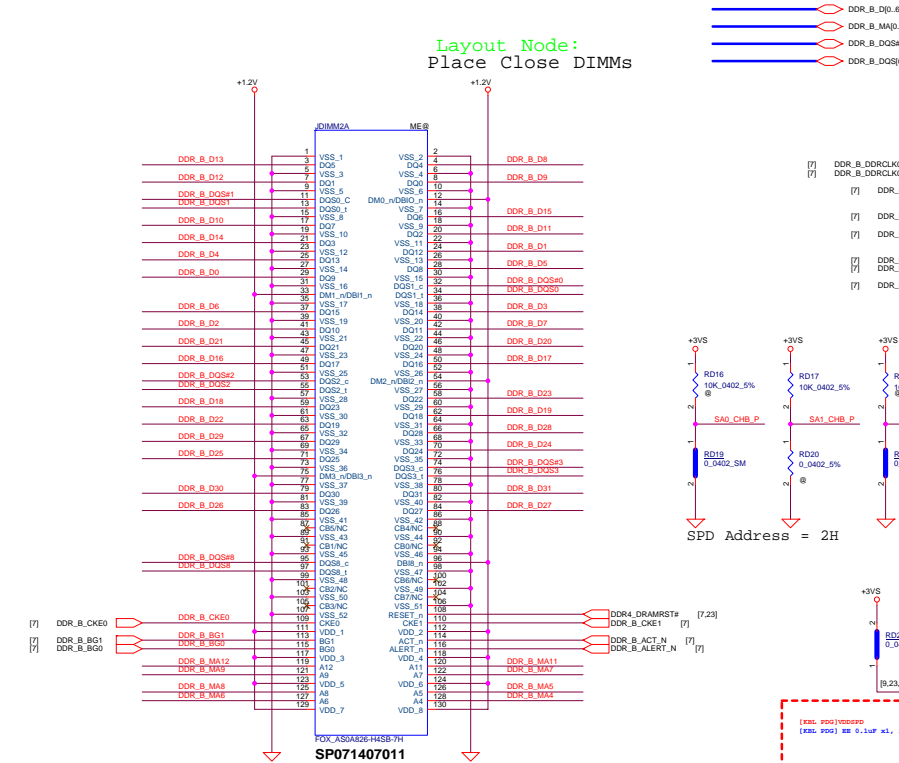
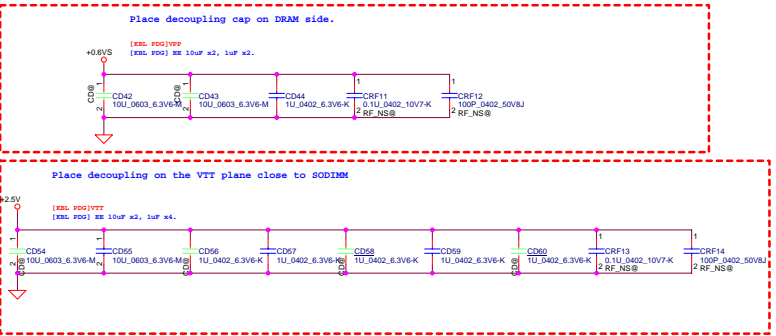
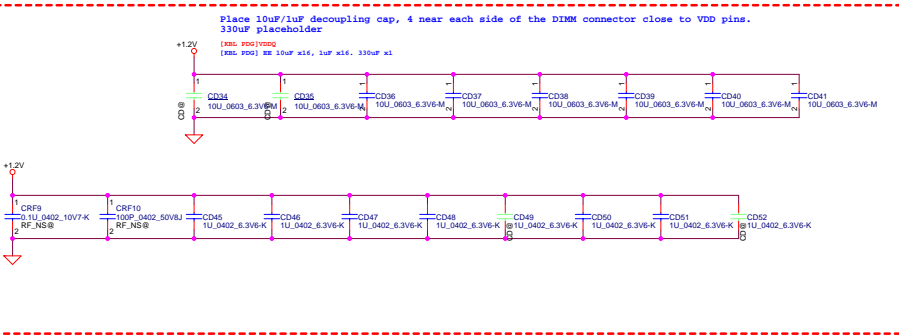


- DDR\_A\_D0[0..63] [8]
- DDR\_A\_MA0[0..16] [6]
- DDR\_A\_DQS0[0..7] [8]
- DDR\_A\_DQS0[0..7] [8]



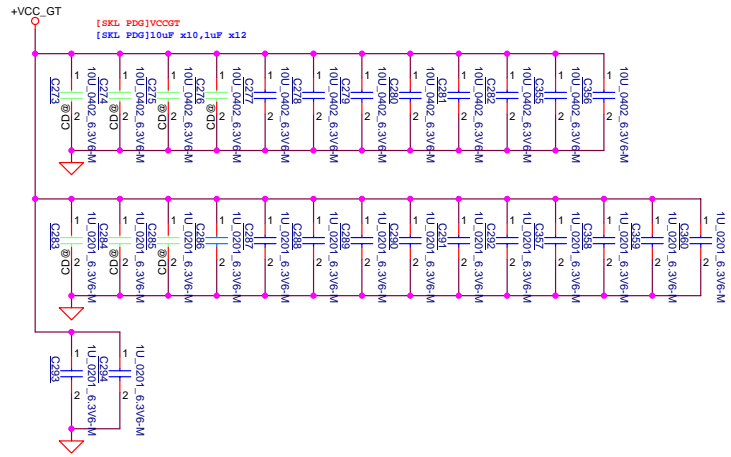
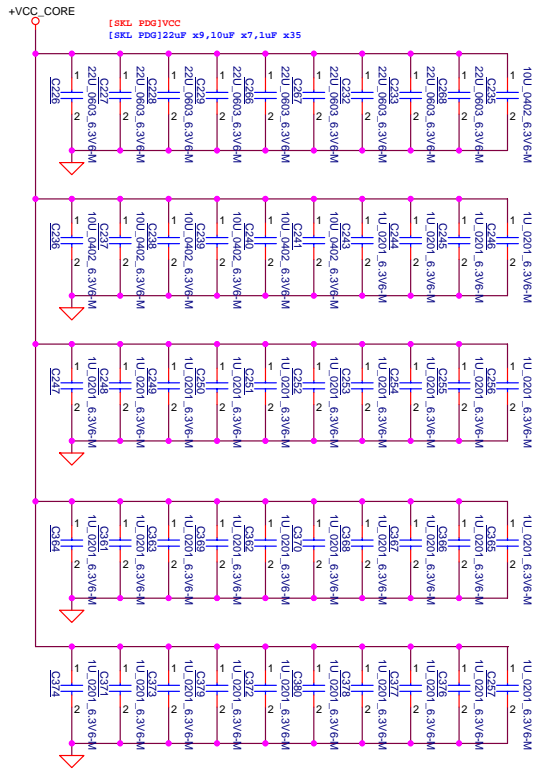
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-RS	Diff.	The 9th signals[8] are applicable for UDIMM/SODIM module with ECC in S and H-processor line processors
DDR0_DQSN[8:0]					
DDR1_DQSP[8:0]					
DDR1_DQSN[8:0]					



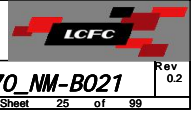


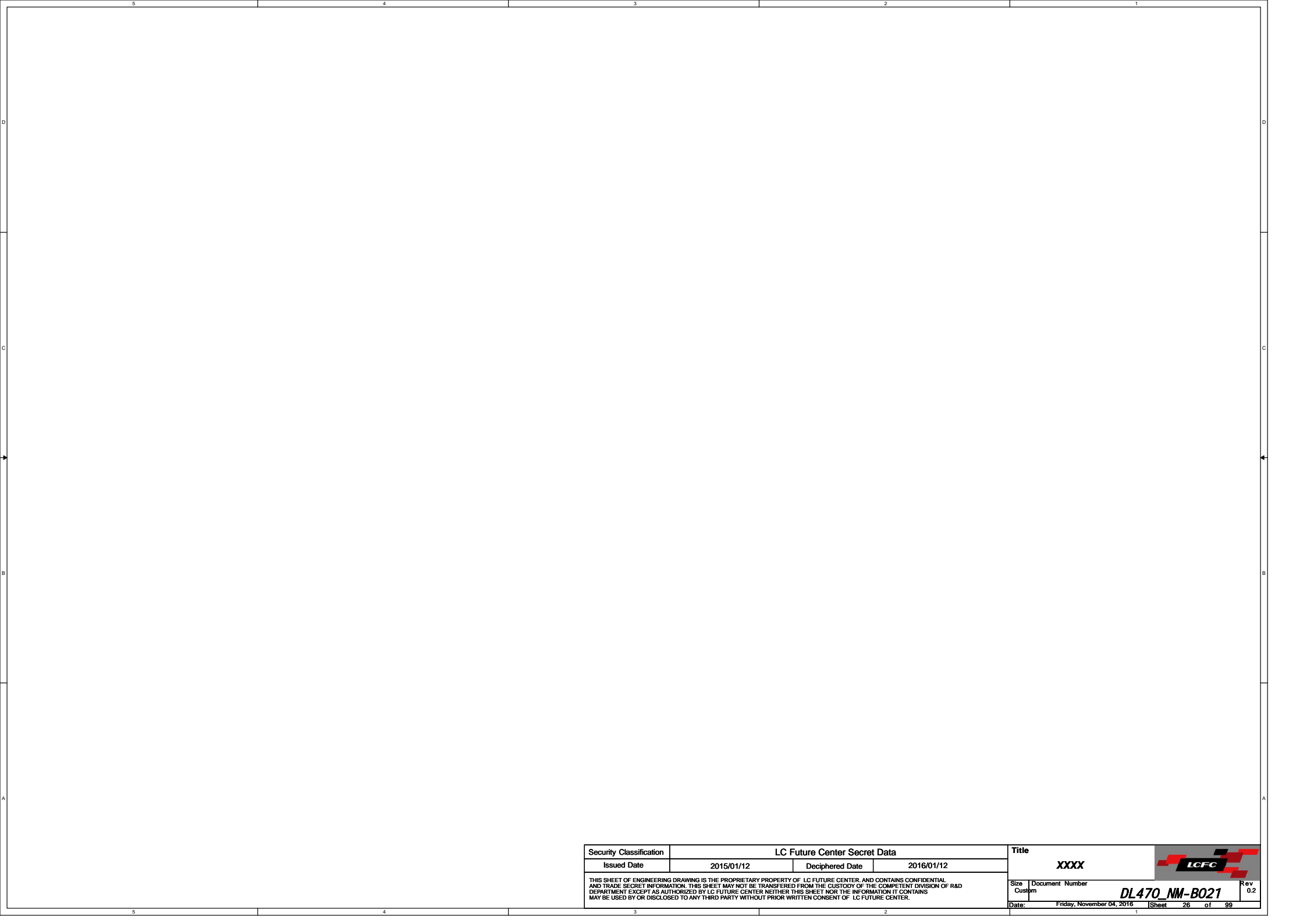
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0]	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4-RS	Diff	The 9th signals[8] are applicable for UDIMM/SODIM module with ECC in S and H-processor line processors
DDR0_DQS[8:0]					
DDR1_DQSP[8:0]					




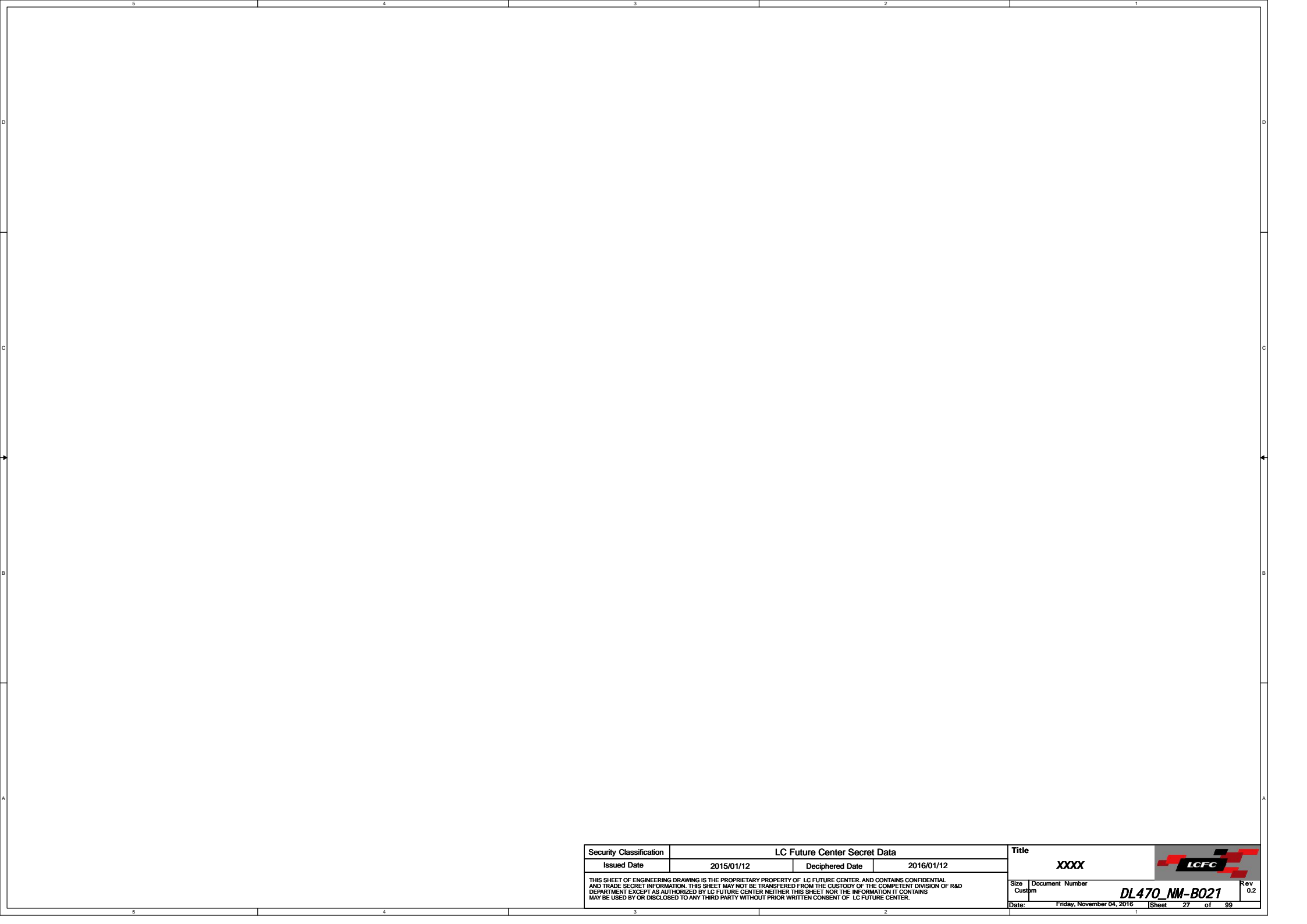



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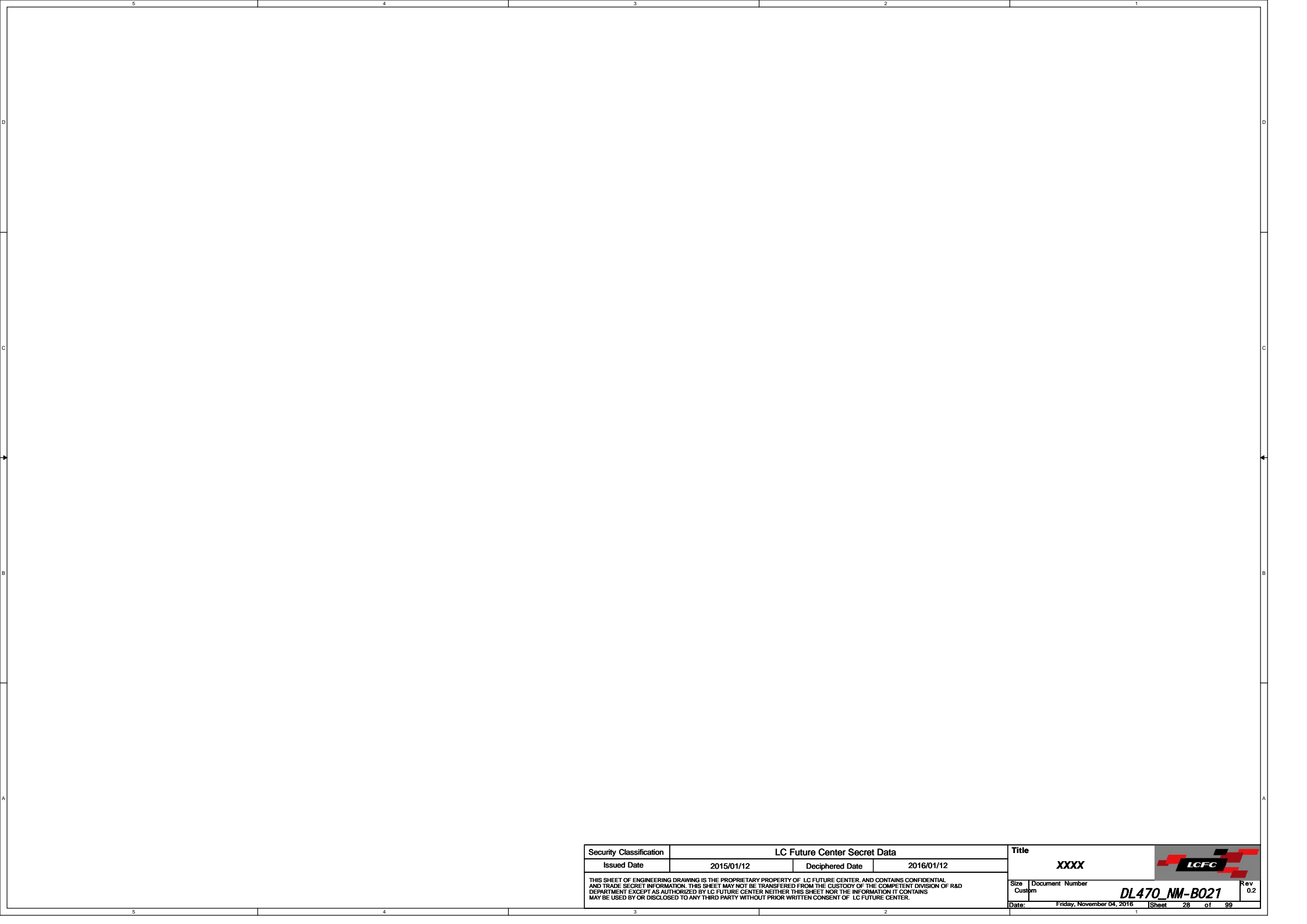





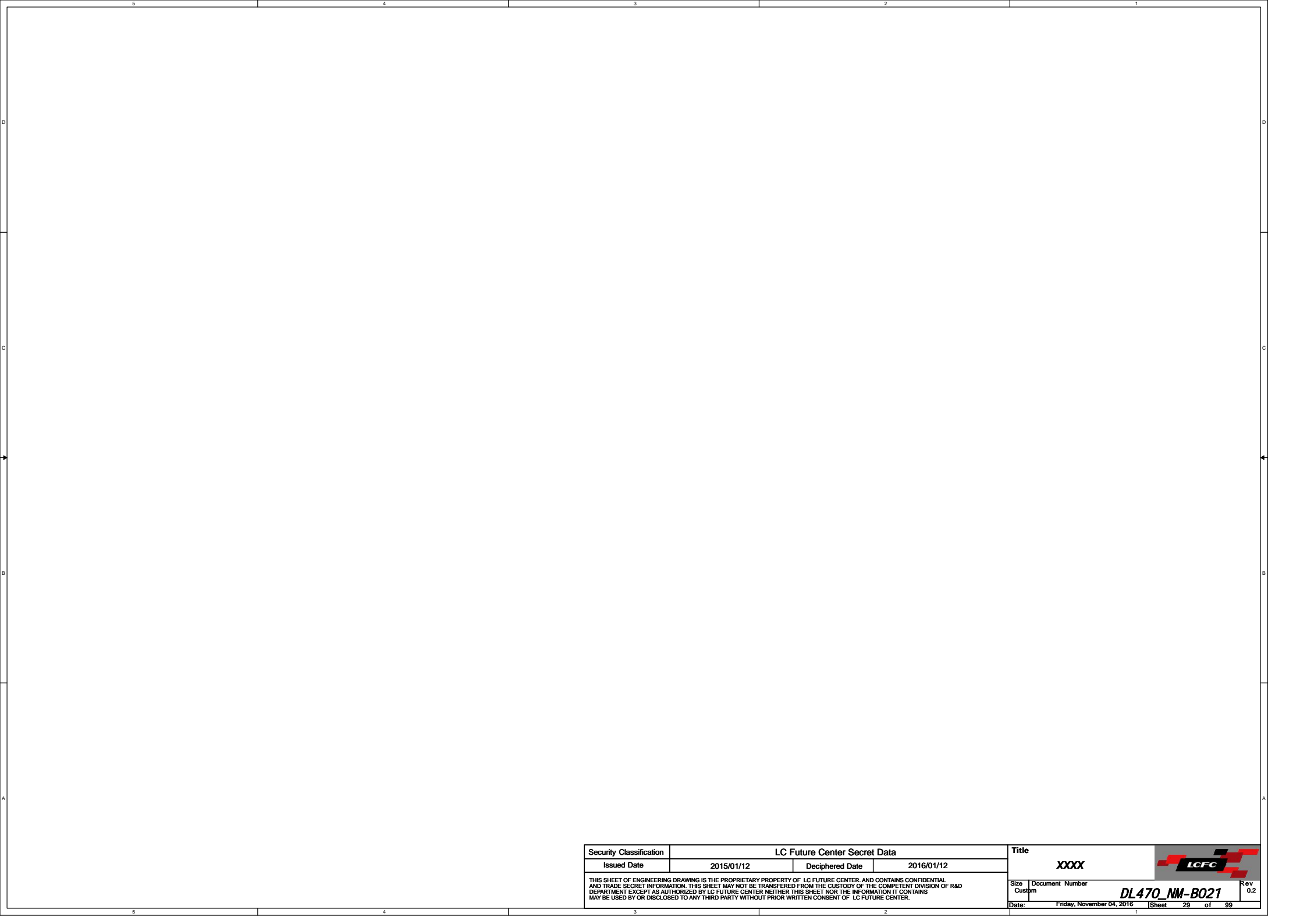
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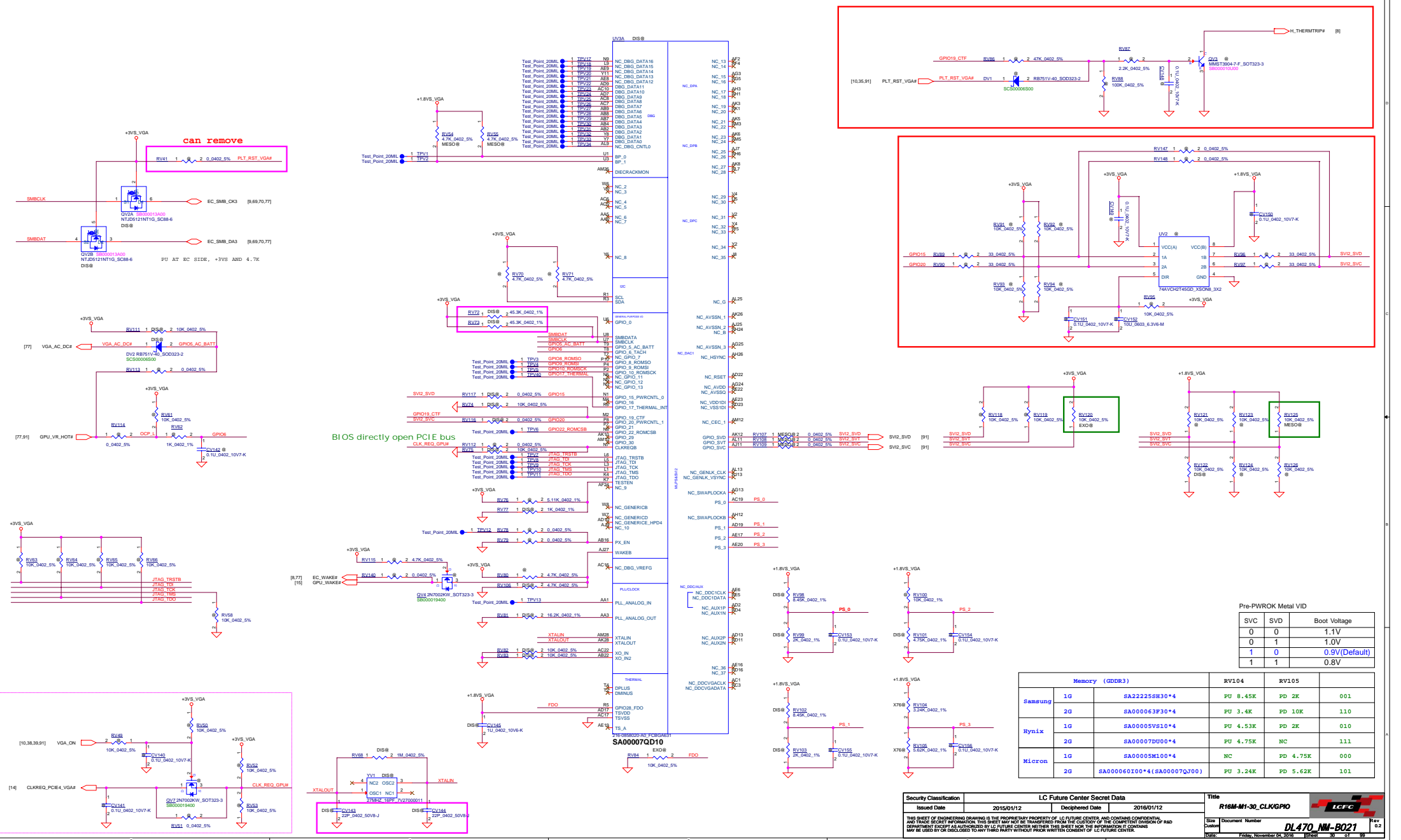
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Pre-PWRC Metal VID

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

Memory (GDDR3)

		RV104	RV105	
Samsung	1G	SA2225SH30*4	PU 8.45K	PD 2K 001
	2G	SA000063P30*4	PU 3.4K	PD 10K 110
Hynix	1G	SA00005V810*4	PU 4.53K	PD 2K 010
	2G	SA00007D000*4	PU 4.75K	NC 111
Micron	1G	SA00005M100*4	NC	PD 4.75K 000
	2G	SA000060I00*4(SA00007Q700)	PU 3.24K	PD 5.62K 101

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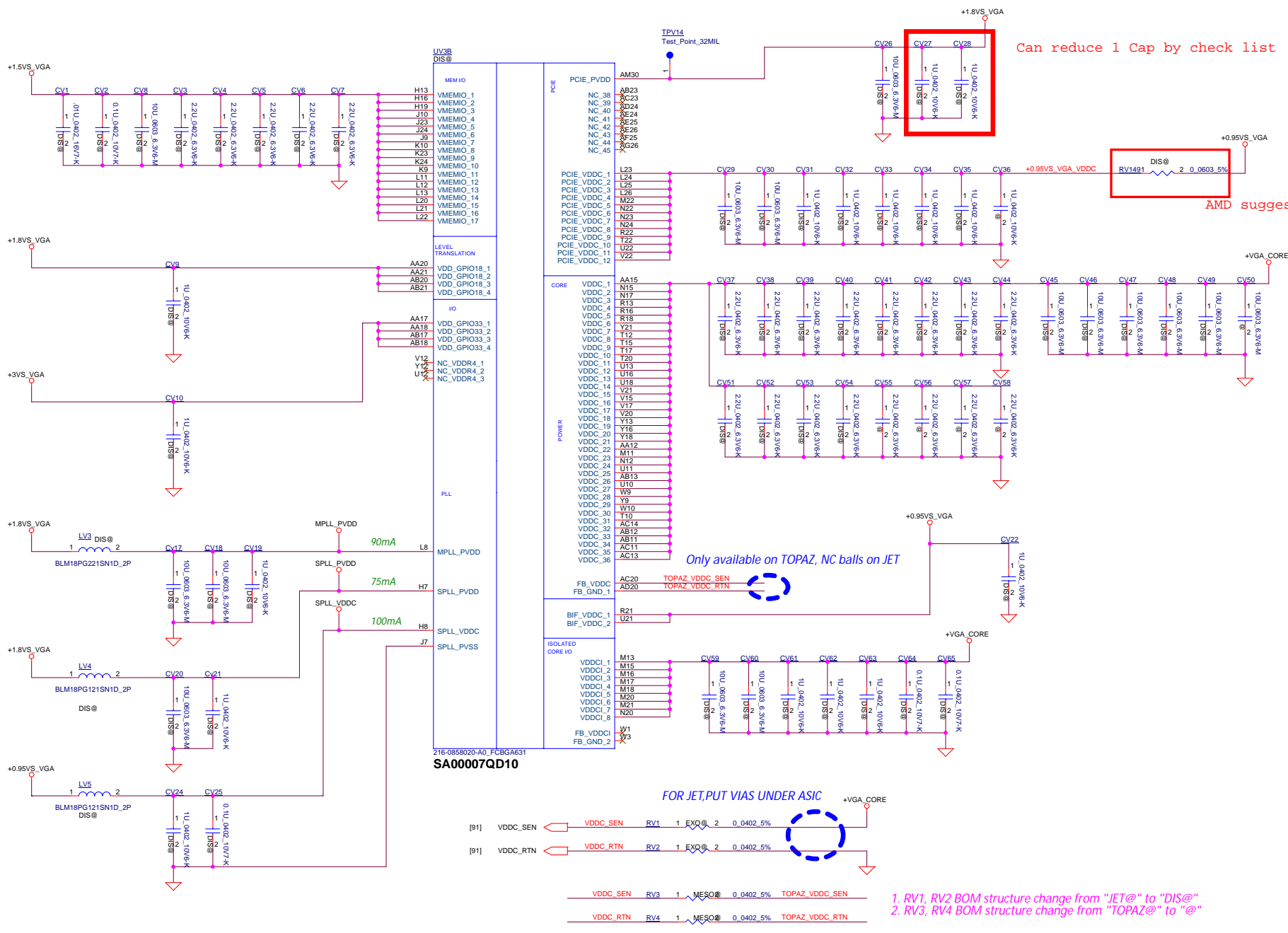
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Can reduce 1 Cap by check list

RV1491 DIS@ 2 0 0603 5%  
AMD suggest

Only available on TOPAZ, NC balls on JET

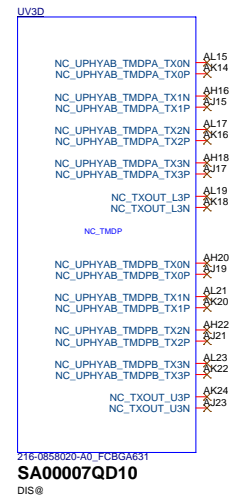
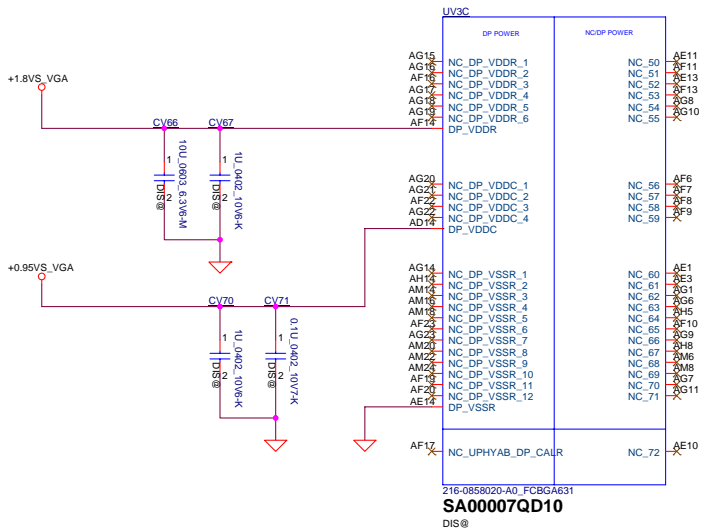
FOR JET, PUT VIAS UNDER ASIC

- [B1] VDDC\_SEN VDDC\_SEN RV1 1 EXQ@ 2 0.0402 5%
- [B1] VDDC\_RTN VDDC\_RTN RV2 1 EXQ@ 2 0.0402 5%

- VDDC\_SEN RV3 1 MESO@ 0.0402 5% TOPAZ\_VDDC\_SEN
- VDDC\_RTN RV4 1 MESO@ 0.0402 5% TOPAZ\_VDDC\_RTN

1. RV1, RV2 BOM structure change from "JET@" to "DIS@"  
2. RV3, RV4 BOM structure change from "TOPAZ@" to "@"

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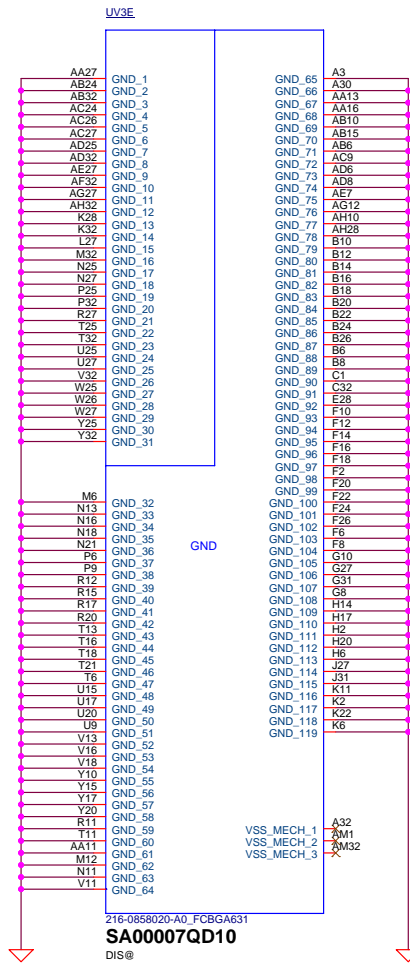
ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?

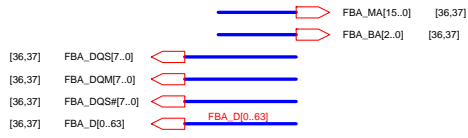
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UV3F

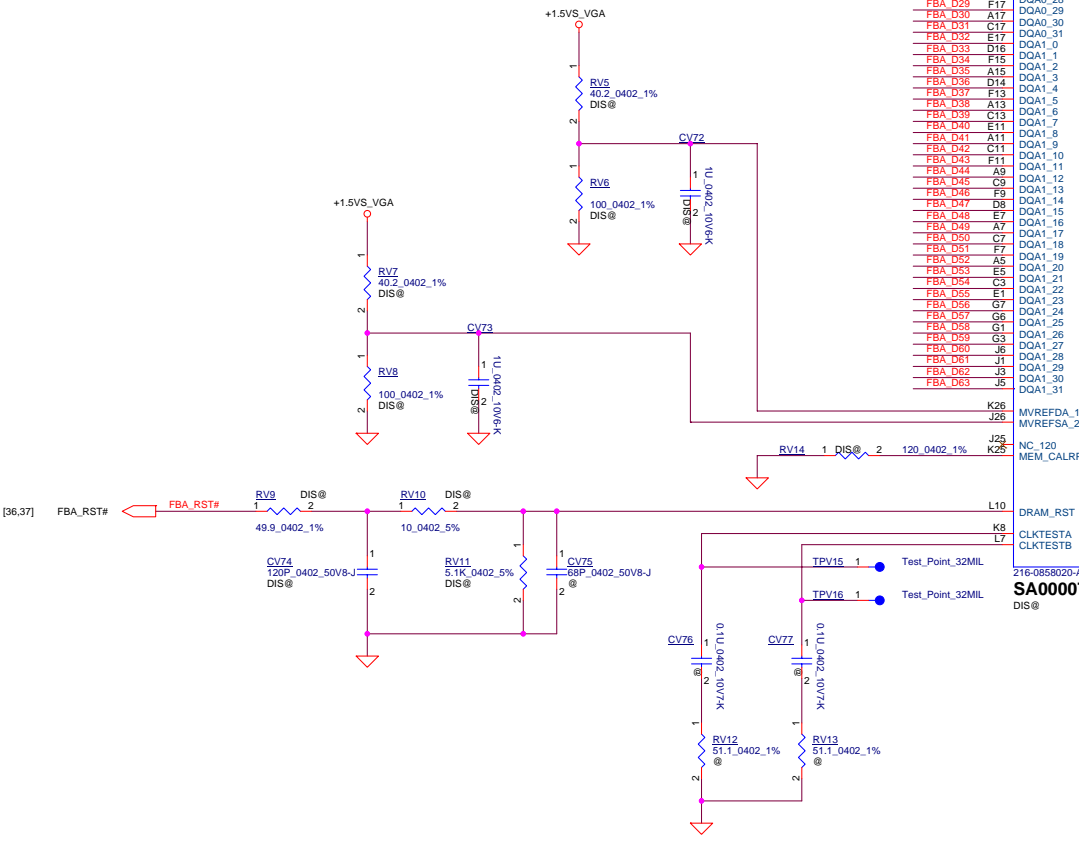
Pin	Signal	Bank
FBA D0	K27	DDA0_0
FBA D1	H31	DDA0_1
FBA D2	H30	DDA0_2
FBA D3	H32	DDA0_3
FBA D4	G29	DDA0_4
FBA D5	F28	DDA0_5
FBA D6	F32	DDA0_6
FBA D7	F30	DDA0_7
FBA D8	C30	DDA0_8
FBA D9	F27	DDA0_9
FBA D10	A28	DDA0_10
FBA D11	E29	DDA0_11
FBA D12	E27	DDA0_12
FBA D13	G26	DDA0_13
FBA D14	D26	DDA0_14
FBA D15	F25	DDA0_15
FBA D16	A25	DDA0_16
FBA D17	C25	DDA0_17
FBA D18	E25	DDA0_18
FBA D19	D24	DDA0_19
FBA D20	E23	DDA0_20
FBA D21	F23	DDA0_21
FBA D22	D22	DDA0_22
FBA D23	F21	DDA0_23
FBA D24	E21	DDA0_24
FBA D25	D20	DDA0_25
FBA D26	F19	DDA0_26
FBA D27	A19	DDA0_27
FBA D28	D18	DDA0_28
FBA D29	F17	DDA0_29
FBA D30	A17	DDA0_30
FBA D31	C17	DDA0_31
FBA D32	E17	DDA0_32
FBA D33	D16	DDA1_0
FBA D34	F15	DDA1_1
FBA D35	A15	DDA1_2
FBA D36	D14	DDA1_3
FBA D37	F13	DDA1_4
FBA D38	A13	DDA1_5
FBA D39	C13	DDA1_6
FBA D40	E11	DDA1_7
FBA D41	A11	DDA1_8
FBA D42	C11	DDA1_9
FBA D43	F11	DDA1_10
FBA D44	A9	DDA1_11
FBA D45	C9	DDA1_12
FBA D46	F9	DDA1_13
FBA D47	D8	DDA1_14
FBA D48	E7	DDA1_15
FBA D49	A7	DDA1_16
FBA D50	C7	DDA1_17
FBA D51	F7	DDA1_18
FBA D52	A5	DDA1_19
FBA D53	E5	DDA1_20
FBA D54	C3	DDA1_21
FBA D55	F3	DDA1_22
FBA D56	A3	DDA1_23
FBA D57	E3	DDA1_24
FBA D58	C3	DDA1_25
FBA D59	F3	DDA1_26
FBA D60	A3	DDA1_27
FBA D61	E3	DDA1_28
FBA D62	C3	DDA1_29
FBA D63	F3	DDA1_30
FBA D63	J5	DDA1_31

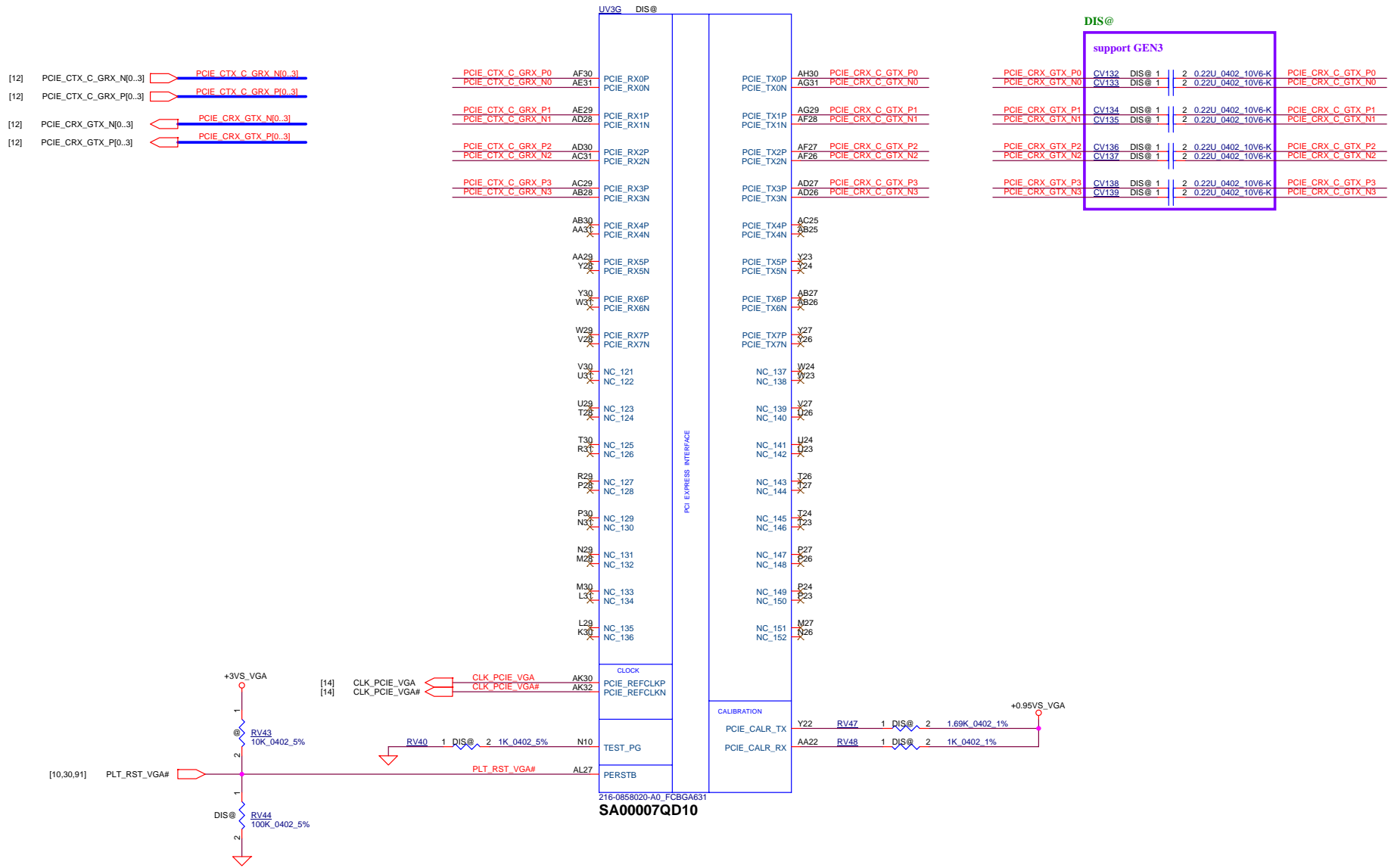
Pin	Signal	Bank
MAA0_0	K17	FBA MA0
MAA0_1	J20	FBA MA1
MAA0_2	H03	FBA MA2
MAA0_3	G23	FBA MA3
MAA0_4	H24	FBA MA4
MAA0_5	G24	FBA MA5
MAA0_6	H24	FBA MA6
MAA0_7	J19	FBA MA7
MAA0_8	G20	FBA MA8
MAA0_9	L17	FBA MA9
MAA1_0	J14	FBA MA10
MAA1_1	K14	FBA MA11
MAA1_2	J11	FBA MA12
MAA1_3	J13	FBA MA13
MAA1_4	H11	FBA MA14
MAA1_5	G11	FBA MA15
MAA1_6	J16	FBA MA16
MAA1_7	L15	FBA MA17
MAA1_8	G14	FBA MA18
MAA1_9	L16	FBA MA19

Pin	Signal	Bank
WCKA0_0	E32	FBA DOM0
WCKA0_1	E30	FBA DOM1
WCKA0_2	A21	FBA DOM2
WCKA0_3	C21	FBA DOM3
WCKA0B_1	E13	FBA DOM4
WCKA1_0	D12	FBA DOM5
WCKA1B_0	E3	FBA DOM6
WCKA1_1	F4	FBA DOM7
WCKA1B_1	K	FBA DOM8

Pin	Signal	Bank
EDCA0_0	H28	FBA DOS0
EDCA0_1	C27	FBA DOS1
EDCA0_2	A23	FBA DOS2
EDCA0_3	E19	FBA DOS3
EDCA1_0	E15	FBA DOS4
EDCA1_1	D10	FBA DOS5
EDCA1_2	D6	FBA DOS6
EDCA1_3	G5	FBA DOS7
EDCA1_4	H7	FBA DOS8
EDCA1_5	A27	FBA DOS9
EDCA1_6	C23	FBA DOS10
EDCA1_7	C19	FBA DOS11
EDCA1_8	C15	FBA DOS12
EDCA1_9	E9	FBA DOS13
EDCA1_10	C5	FBA DOS14
EDCA1_11	H4	FBA DOS15

Pin	Signal	Bank
ADBA0	L18	FBA ODTA0
ADBA1	K16	FBA ODTA1
ADBA2	H26	FBA CLKA0
ADBA3	H25	FBA CLKA0#
ADBA4	G9	FBA CLKA1
ADBA5	H9	FBA CLKA1#
ADBA6	G22	FBA RASA0
ADBA7	G17	FBA RASA1
ADBA8	G19	FBA CASA0
ADBA9	G16	FBA CASA1
ADBA10	H22	FBA CSA0
ADBA11	K2	FBA CSA1
ADBA12	G13	FBA CSA0#
ADBA13	K13	FBA CSA1#
ADBA14	K20	FBA CKEA0
ADBA15	J17	FBA CKEA1
ADBA16	G25	FBA WEA0
ADBA17	H10	FBA WEA1



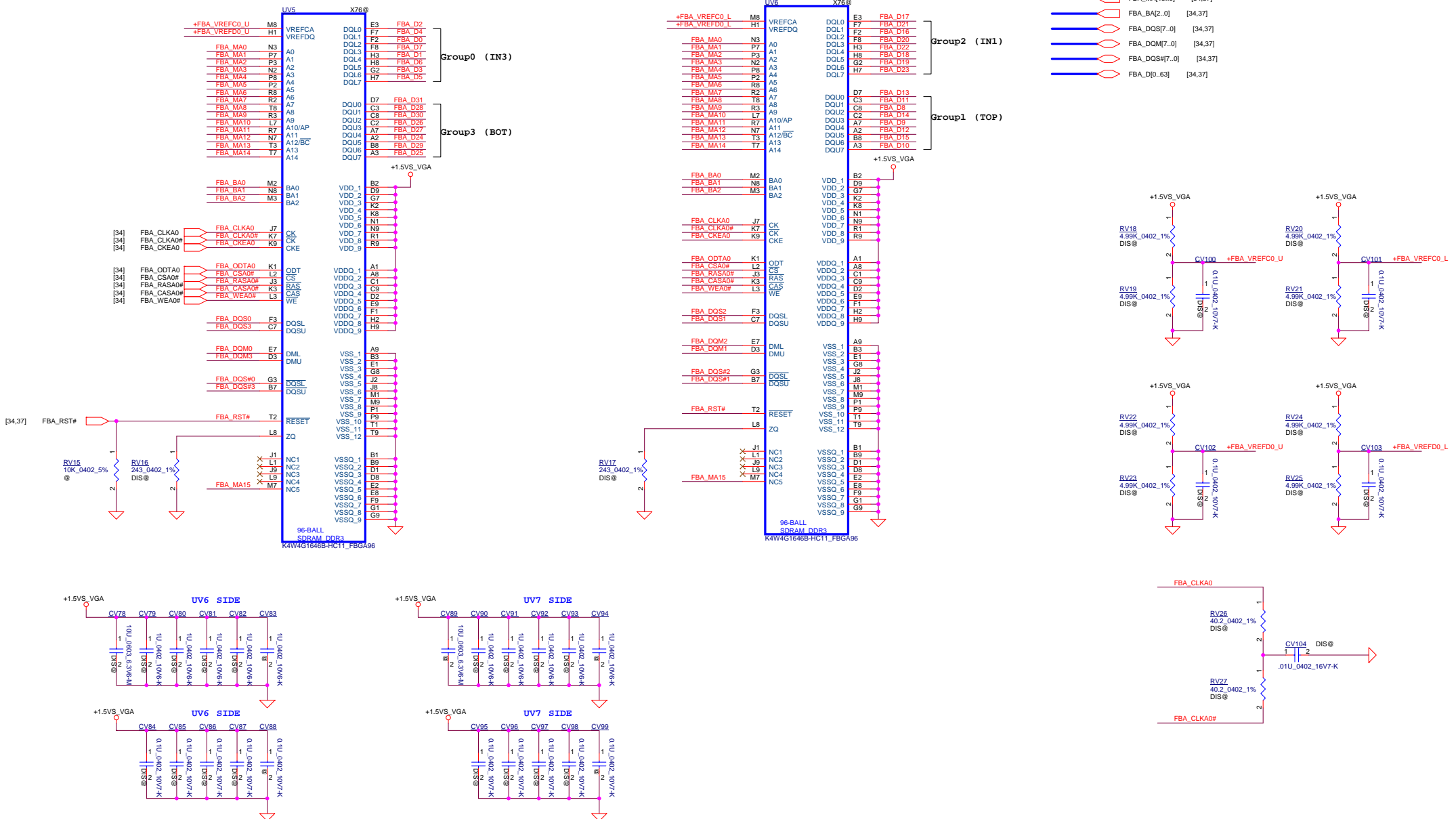


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Title	R16M-M1-30_PCIE	
Size	Document Number	Rev
Custom	DL470_NM-B021	0.2
Date:	Friday, November 04, 2016	Sheet 35 of 99

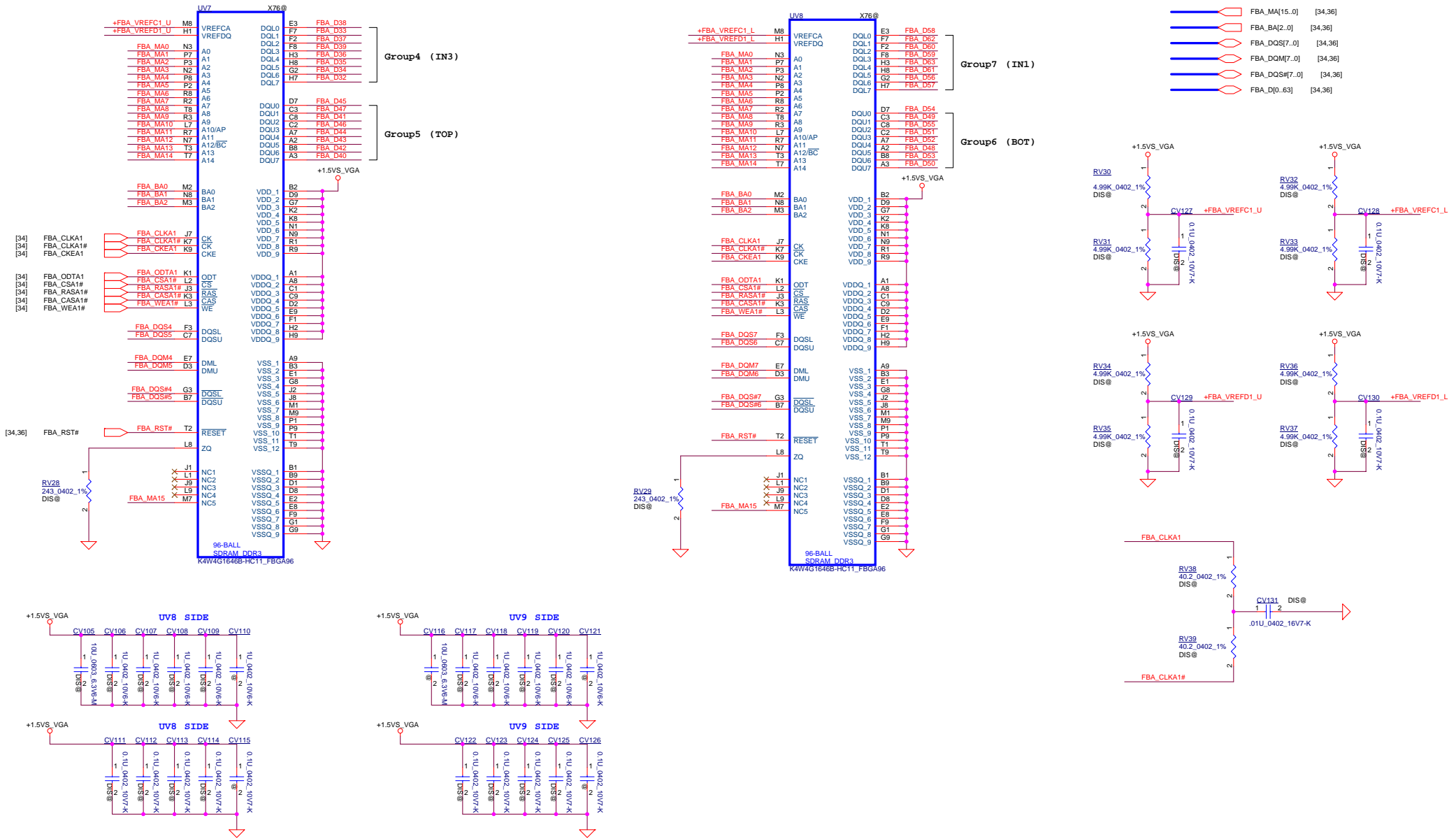


# Memory Partition A - Lower 32 bits



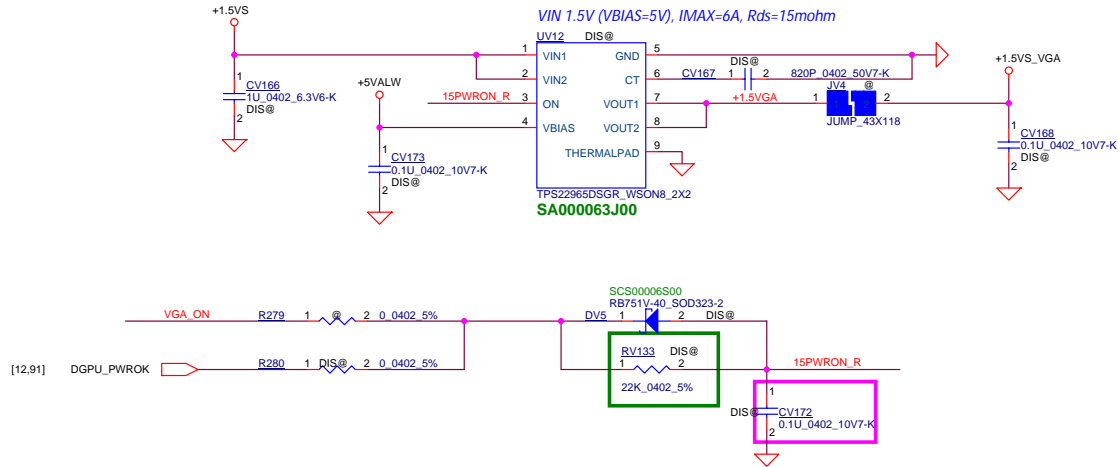
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	R16M-M1-30_VRAM1	
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# Memory Partition A - Upper 32 bits

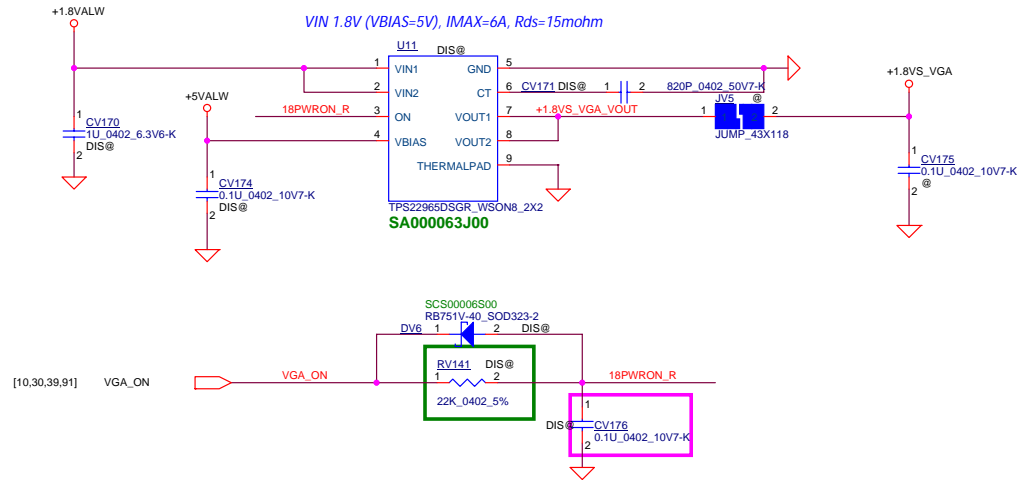


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**+1.5VS to +1.5VS\_VGA**



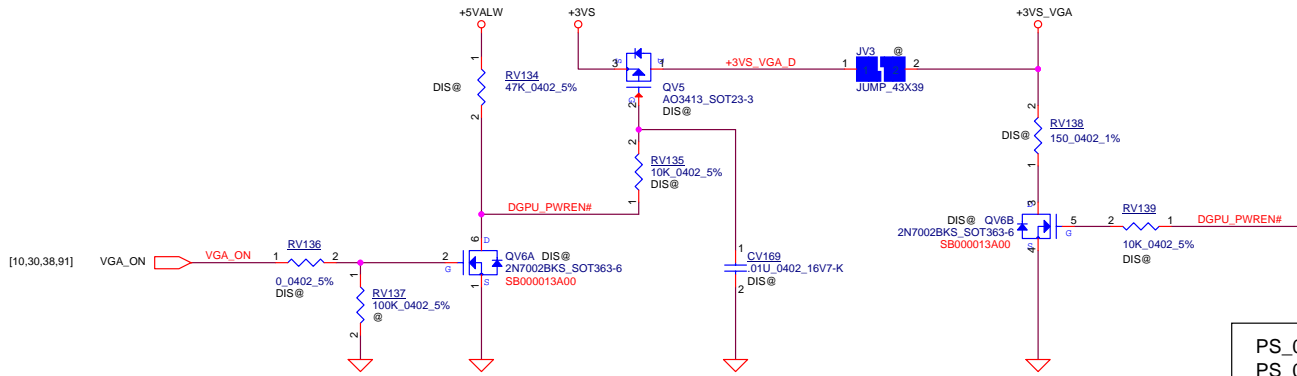
**+1.8VALW to +1.8VS\_VGA**



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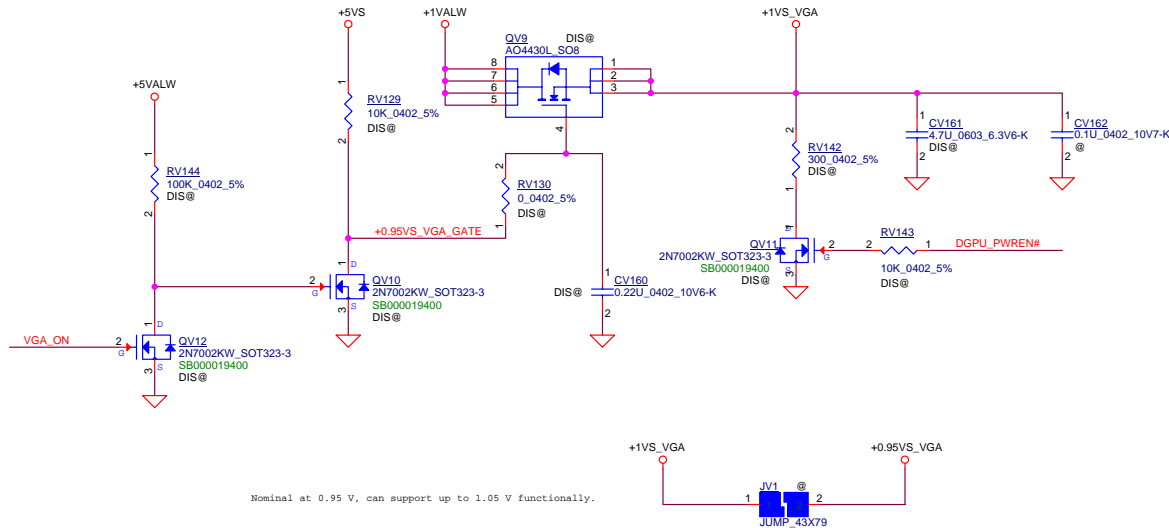
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R16M-M1-30_PW SWITCH		
Size	Document Number	Rev
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**+3VS to +3VS\_VGA**



MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

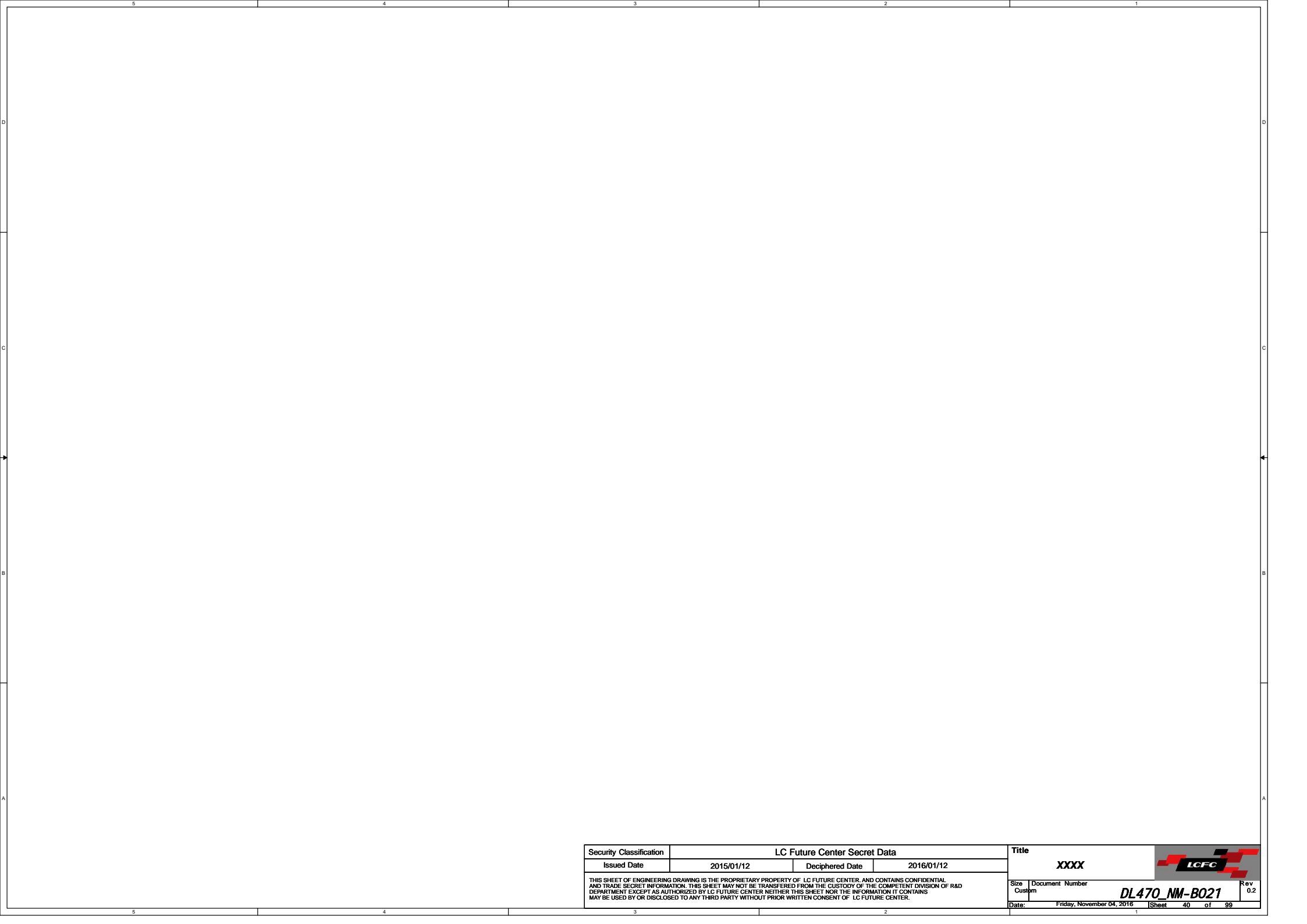
**+1VALW to +1VS\_VGA**




PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

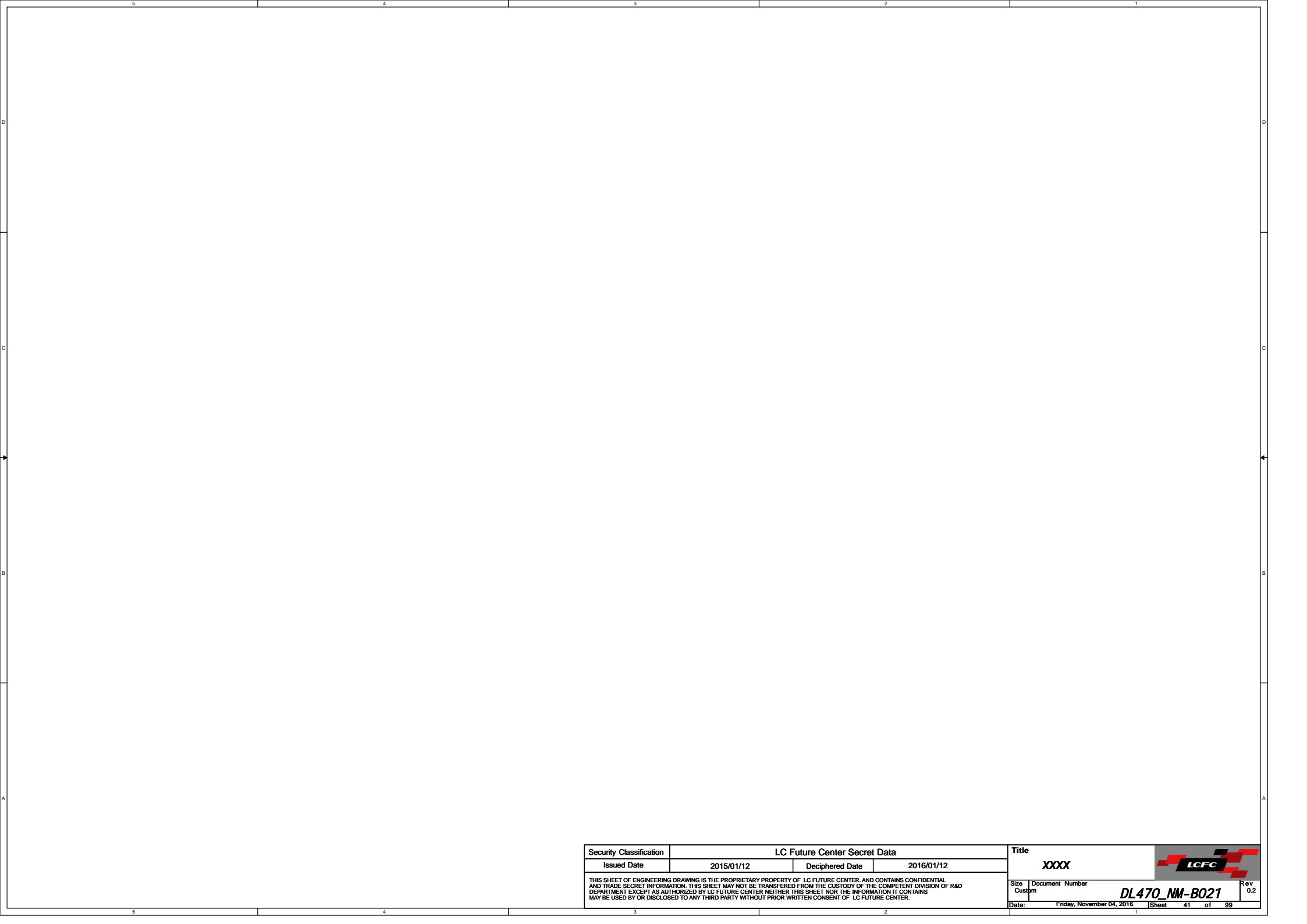
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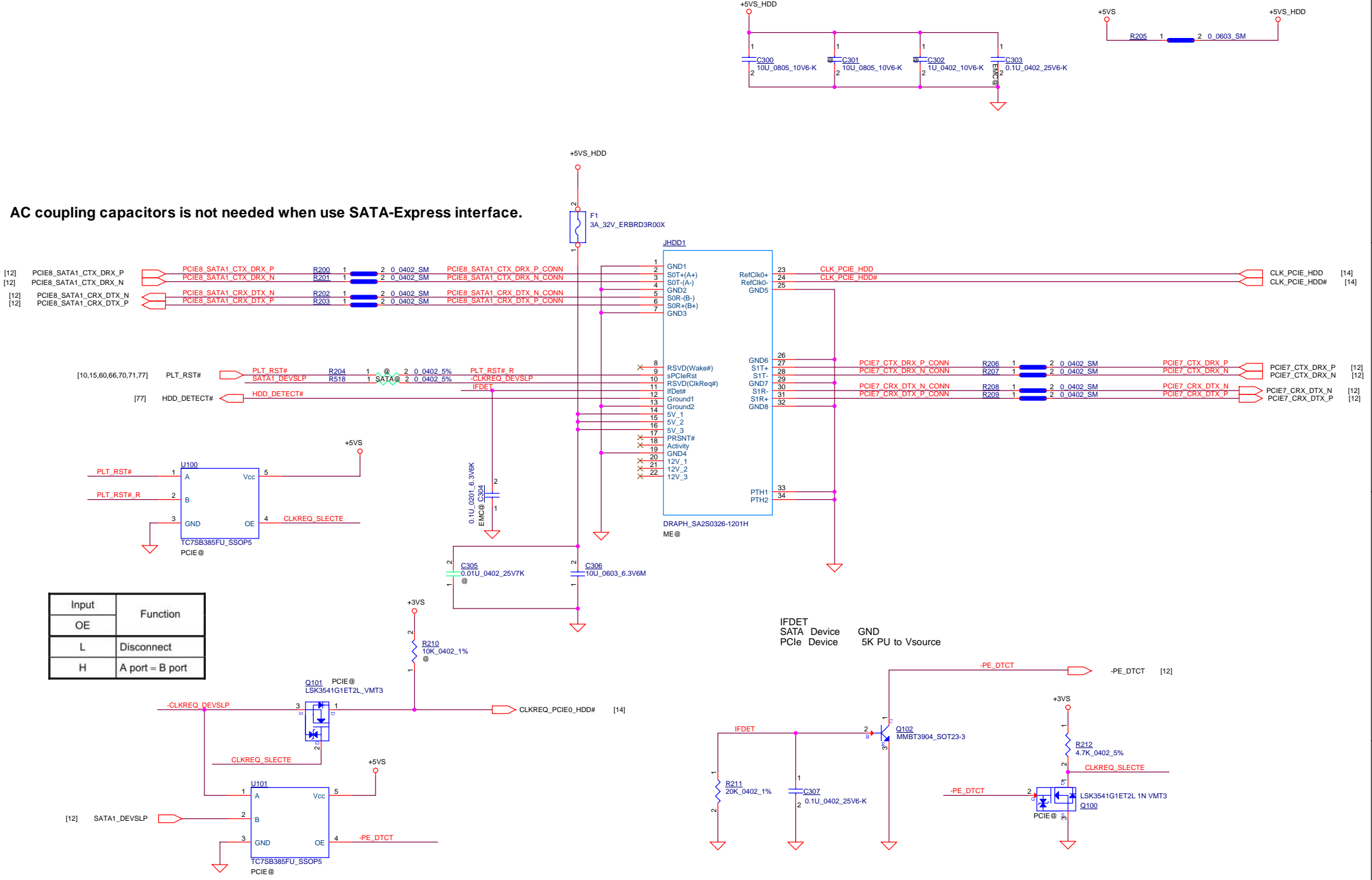
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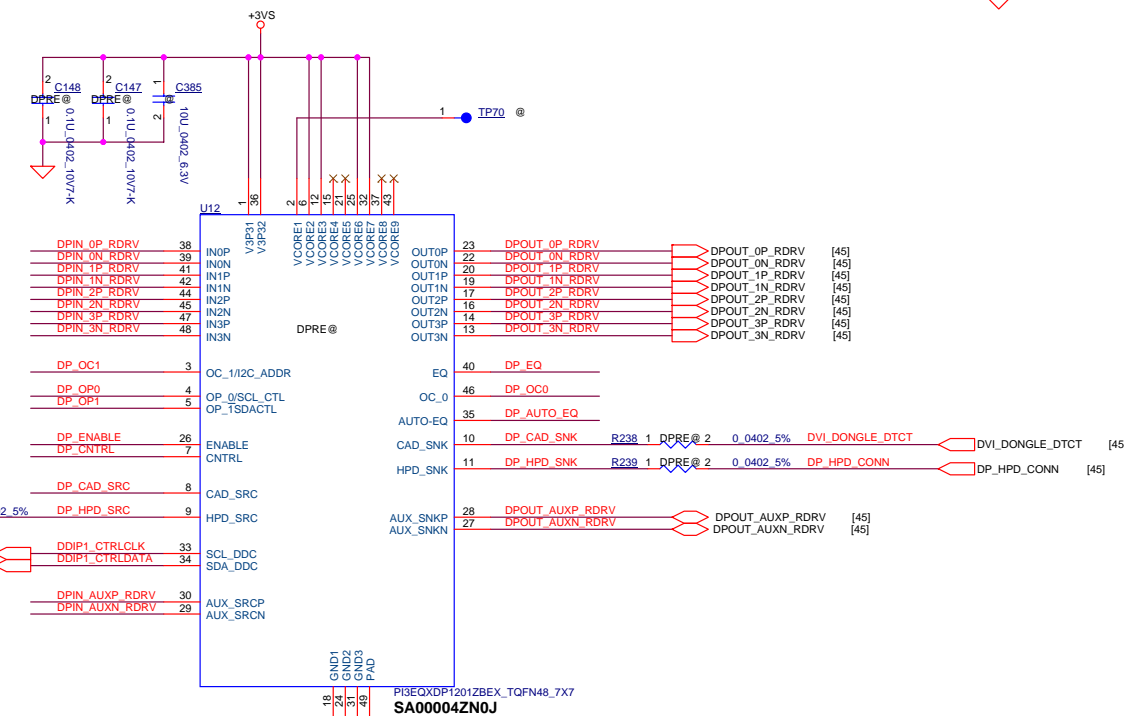
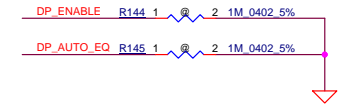
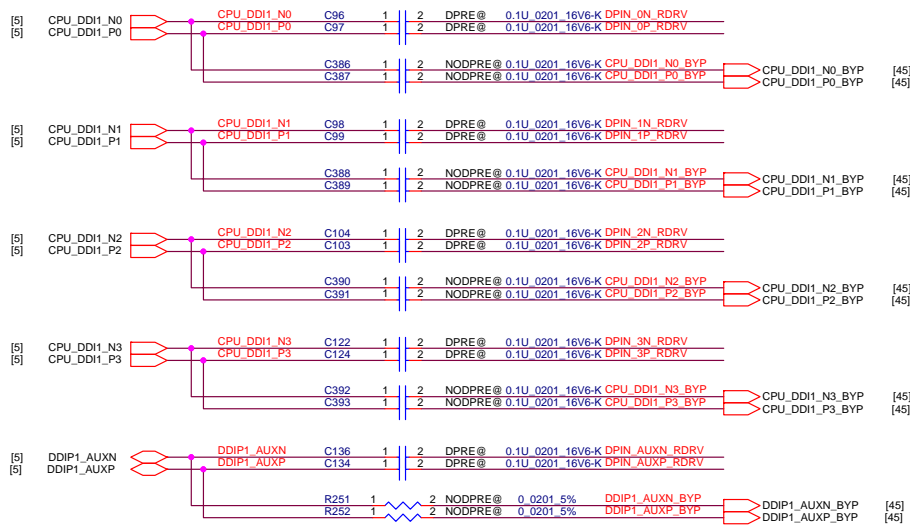
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AC coupling capacitors is not needed when use SATA-Express interface.



Input	Function
OE	
L	Disconnect
H	A port = B port

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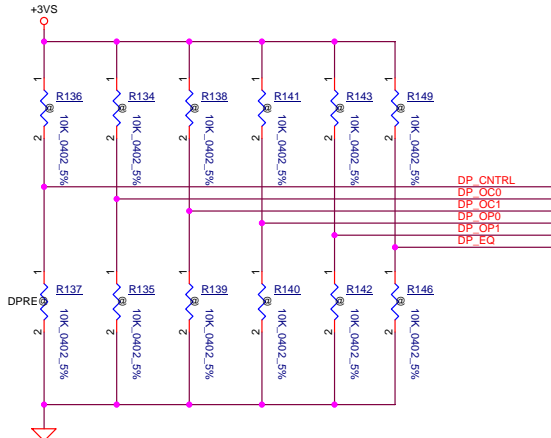


Follow mini DP SA00005V10J U1 design

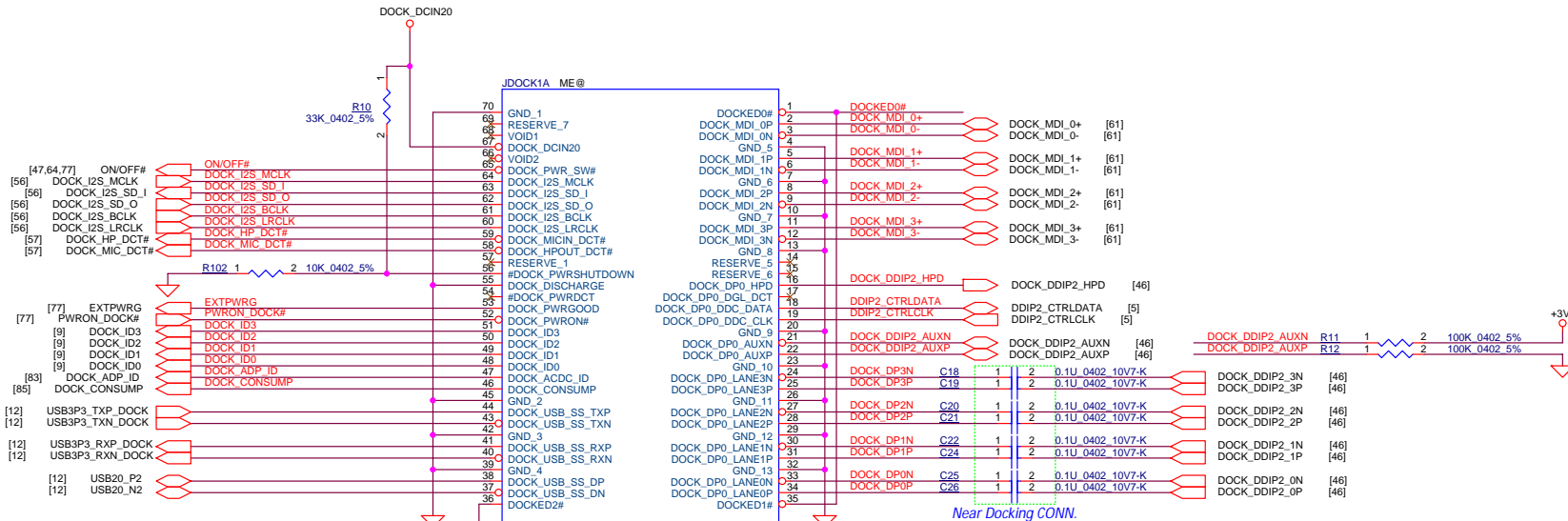
DP\_HPDC\_SRC 1 R150 2 DP\_CAD\_SRC  
0.0402 5%

[5,45] DDIP1\_HPDC DDIP1\_HPDC R237 1 DP\_RE@ 2 0.0402 5% DP\_HPDC\_SRC

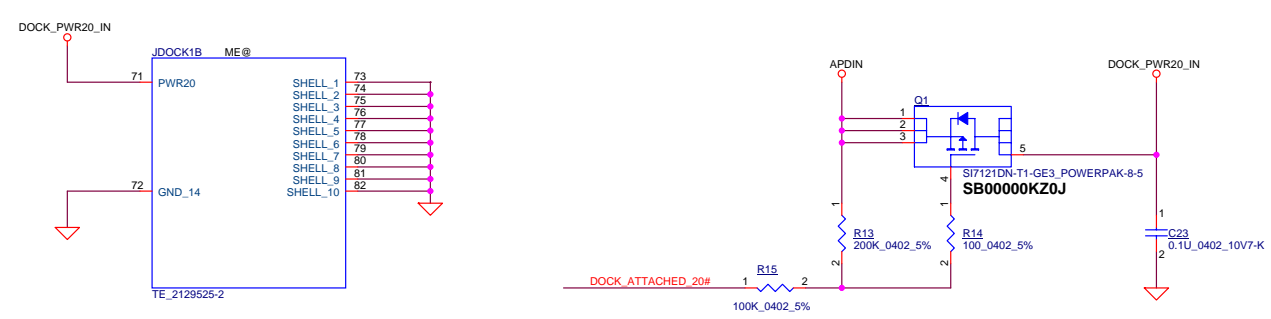
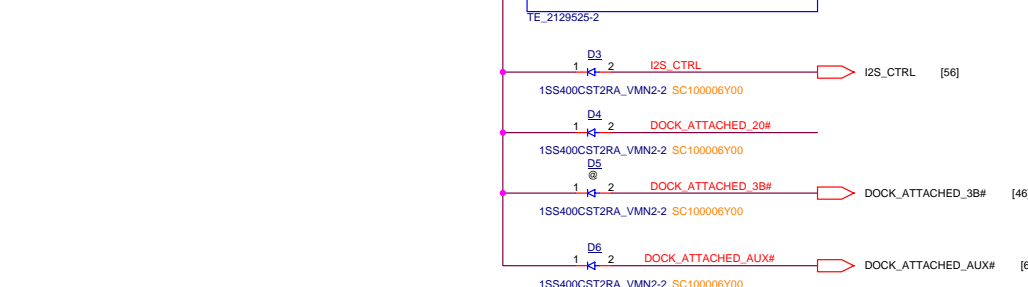
[5,45] DDIP1\_CNTRLCLK DDIP1\_CNTRLCLK DDIP1\_CNTRLDATA DDIP1\_CNTRLDATA



CNTRL	CAD_SNK	Mode
0	0	Normal Mode for AUX
0	1	Normal Mode for DDC
1	X	Test Mode




Near Docking CONN.



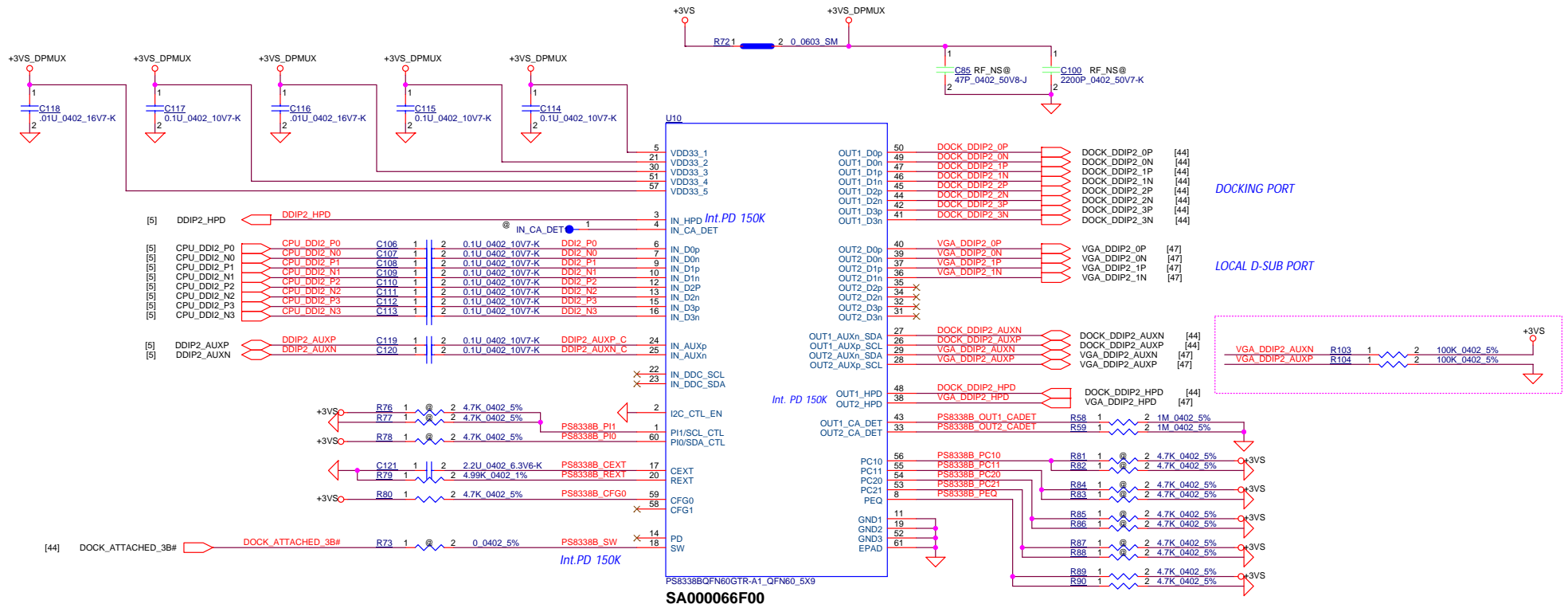
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	2015/01/12	2016/01/12	<b>DOCKING CONN.</b>

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**DL470\_NM-B021**
  
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**PS8338B\_P11**

Auto test enable: Internal pull down at -150KOhm, 3.3V I/O.  
 \*L: Auto test disable & input of fset cancel at i on enable (def aut)  
 H: Auto test enable & input of fset cancel at i on enable  
 M: Auto test disable & input of fset cancel at i on d sã

**PS8338B\_PC10/PC20**

AUX intercept i on dsã e f or Port y (y = 1, 2). I r t e r nã pull down at -150K Oh m 3.3V I/O  
 \*L: AUX intercept i on enable & di ver confi gur at ion i s set by I i r k t rã n i n g (def aut)  
 H: AUX intercept i on dsã e f di ver out put ù t h f i xã t 80 Oh m and 0B  
 M: AUX intercept i on dsã e f di ver out put ù t h f i xã t 40 Oh m and 0B

**DOCK\_ATTACHED\_3B#**

For Automatic S w i t c h i n g Mode (CFG0=H)  
 SW=L : Port1 has higher priority when both ports are plugged (docking side)  
 SW=H : Port2 has higher priority when both ports are plugged

**PS8338B\_P10**

Automatic EQ dsã e I r t e r nã pull down at -150K Oh m 3.3V I/O  
 \*L: Automatic EQ enable (def aut)  
 H: Automatic EQ dsã e

**PS8338B\_PC11/PC21**

Output swing adjustment for Port y (y = 1, 2). Internal pull down at -150KOhm, 3.3V I/O:  
 \*L: default  
 H: +20%  
 M: -16.7%

**CA\_DAT**

default CA\_DAT add 1M pull down (AUX enable), CA\_DAT check plug-in is DP or HDMI!! DP=L, HDMI dongle =H.

**PS8338B\_CFG0**

Chip operat ionã mode confi gur at ion I r t e r nã pull down at -150K Oh m 3.3V I/O  
 L: Control switching mode  
 \*H: Automatic s w i t c h i n g mode (def aut)

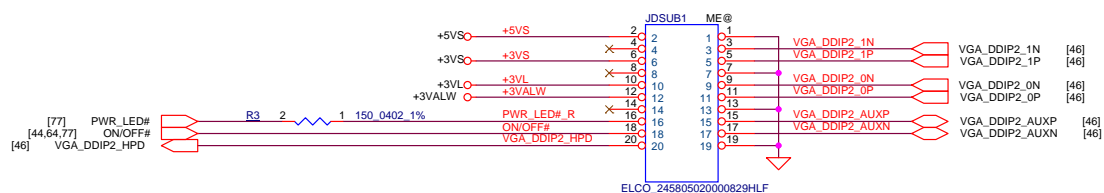
**PS8338B\_PEQ**

Programmable input equalizat ion e v d s I r t e r nã pull down at -150K Oh m 3.3V I/O  
 L: default, LEO, compensate channel loss up to 11.5dB @ HBR2  
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2  
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

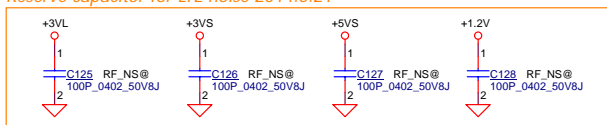
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PS8338B DP SW		
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### M/B TO D-SUB/B BTB CONN.



Reserve capacitor for LTE noise 2014.5.21



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D-SUB BTB CONN.		Size	Rev
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A

B

C

D

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A

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Custom	DL470_NM-B021	Friday, November 04, 2016		0.2	
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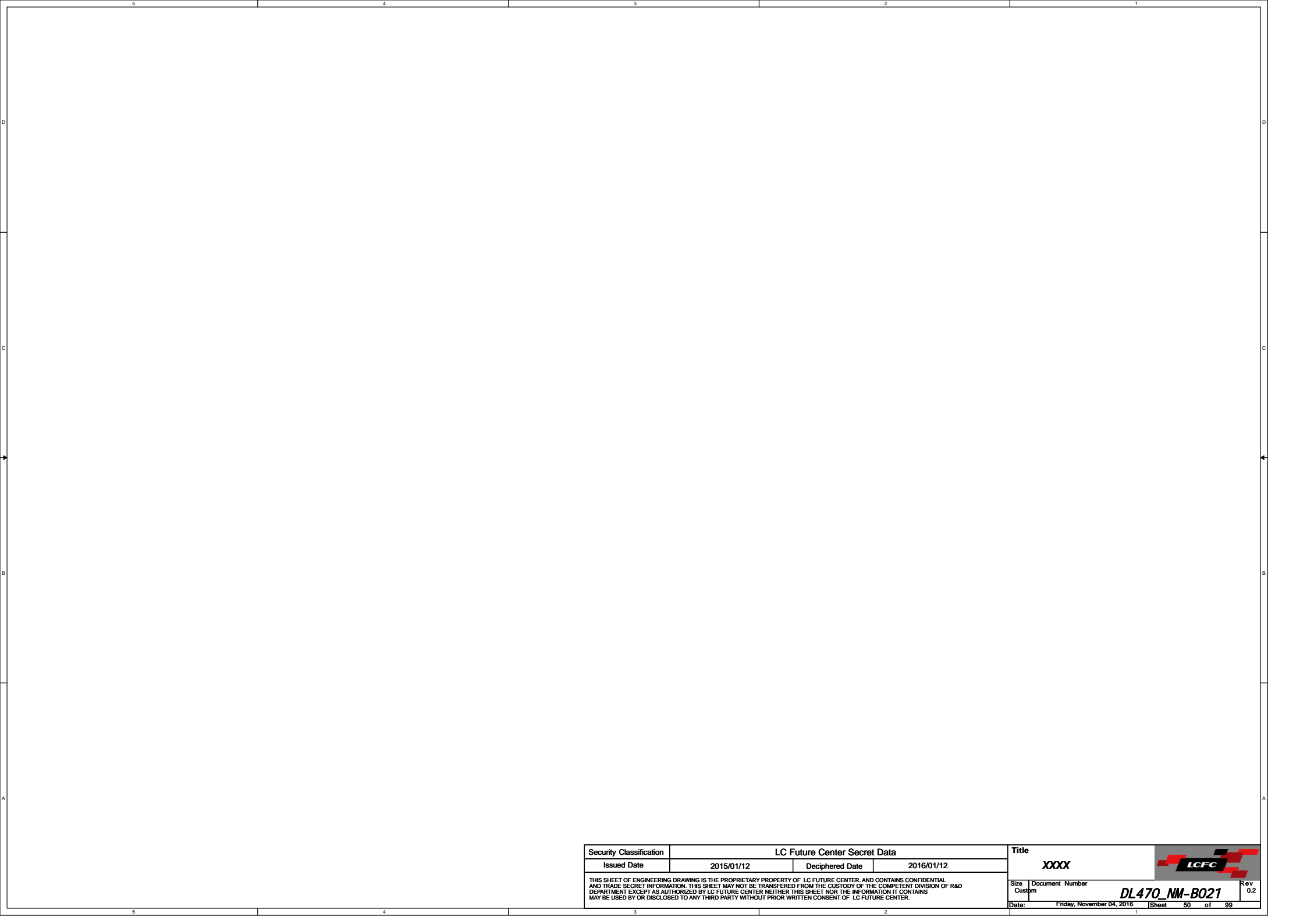
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B

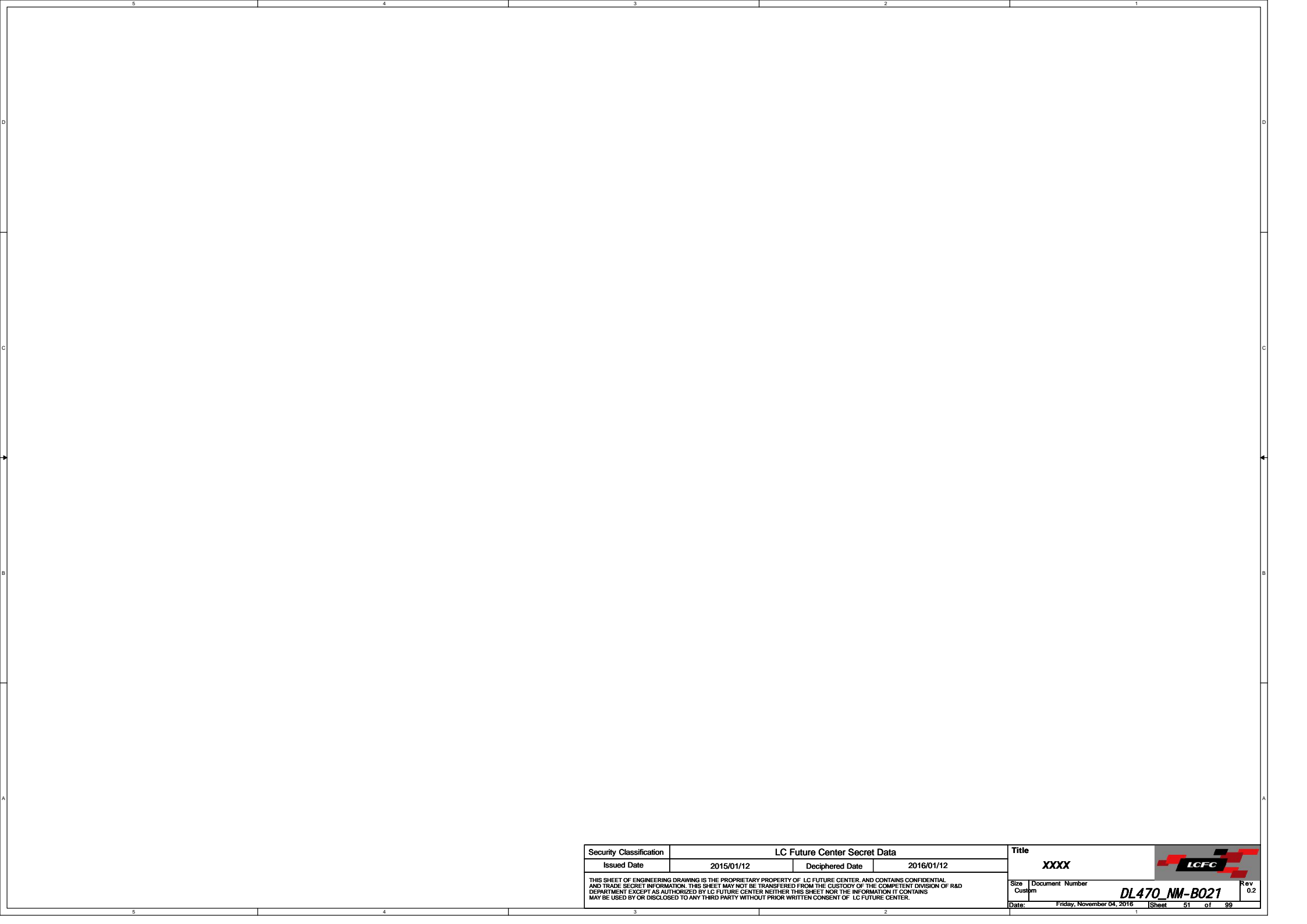
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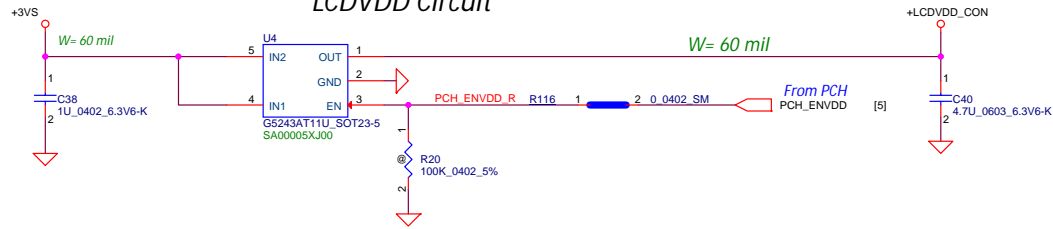


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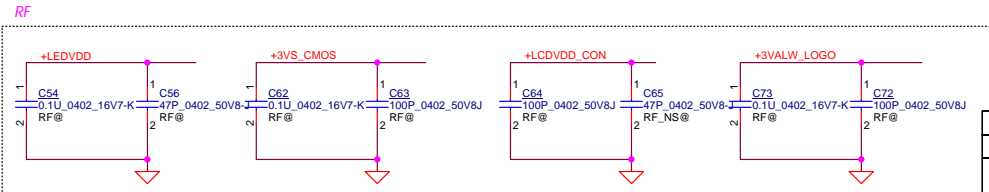
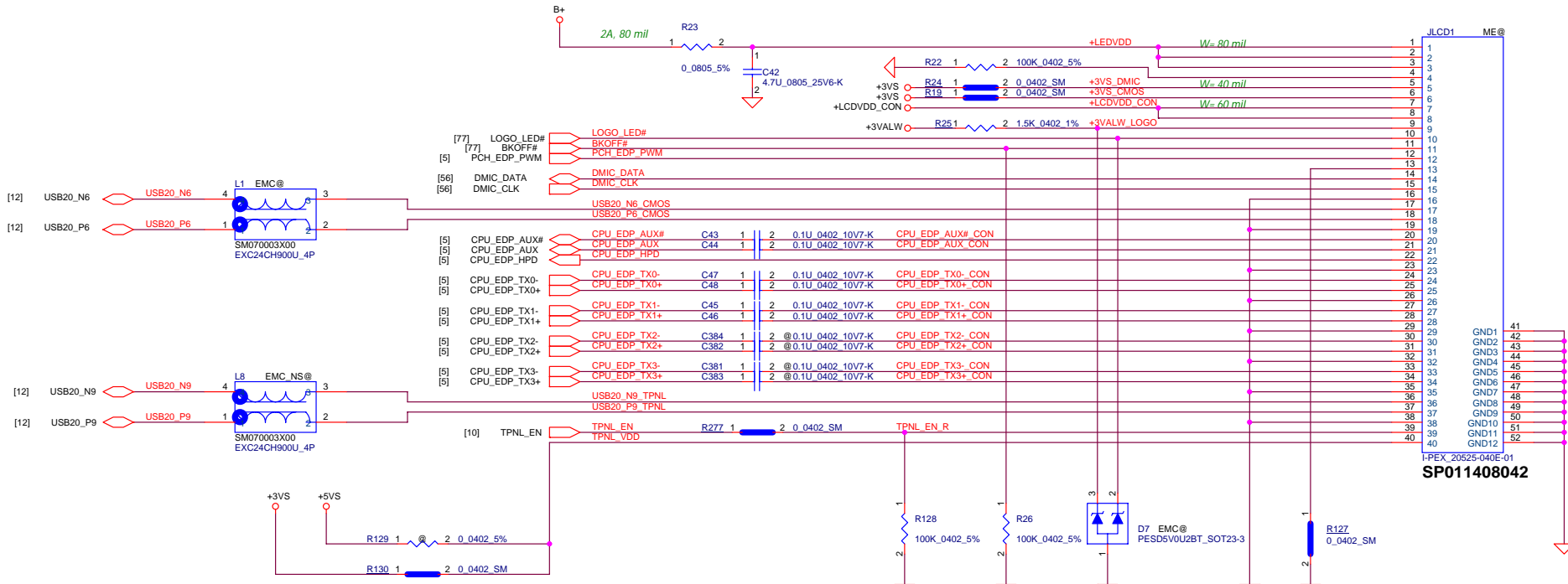


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### LCDVDD Circuit

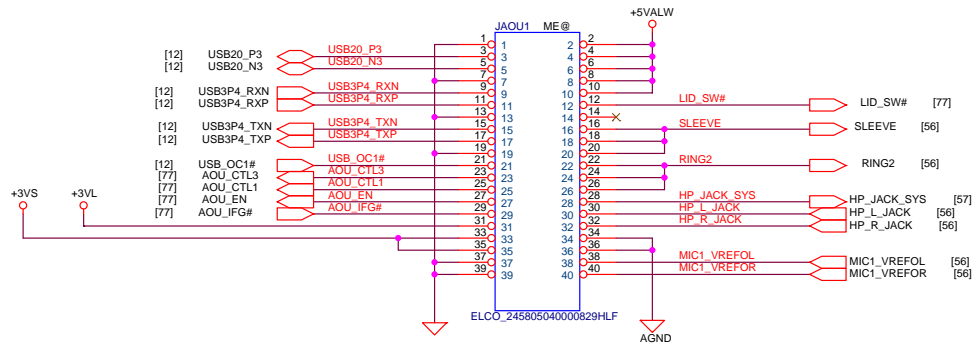


### eDP/CMOS/LOGO-LED CONN.




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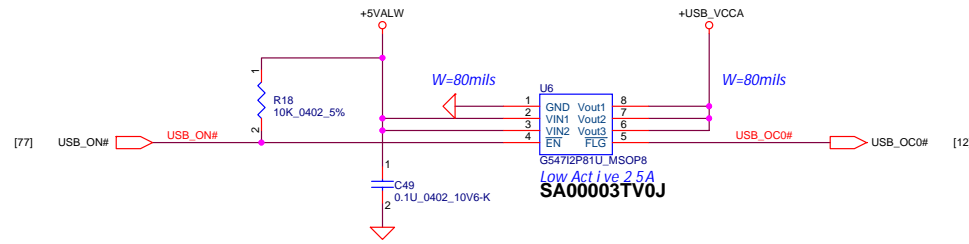
AOU/JACK/LID-SW BTB CONN.



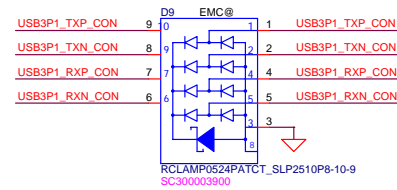
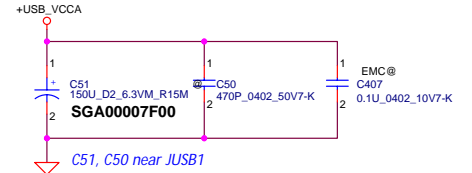
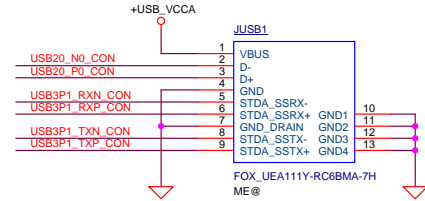
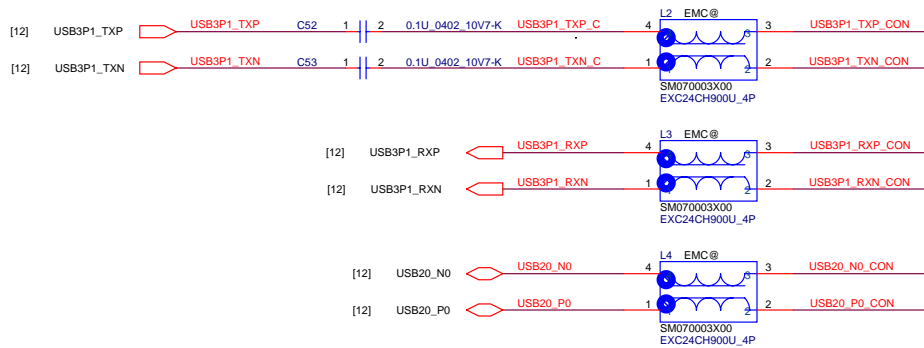
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AOU/JACK/LID-SW BTB CONN.		
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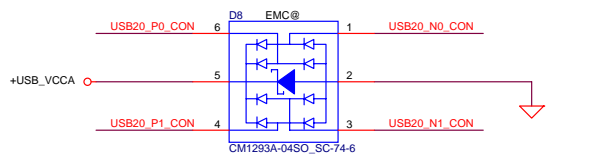
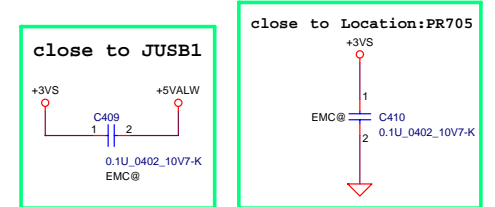
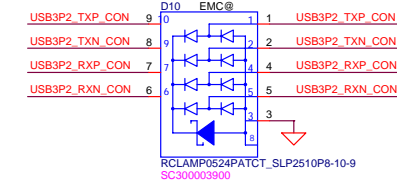
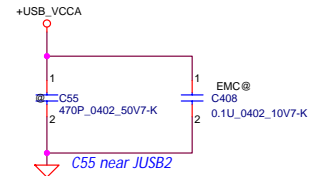
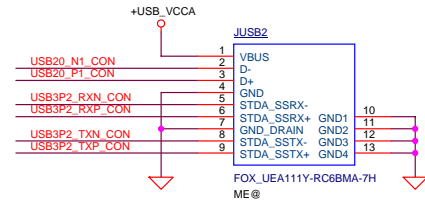
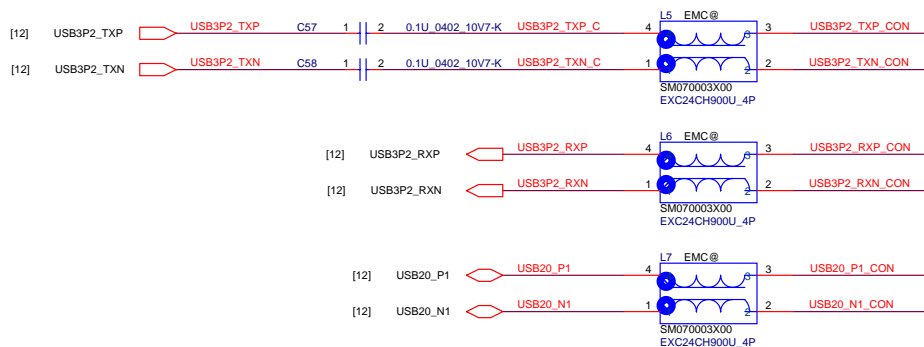
USB POWER SWITCH



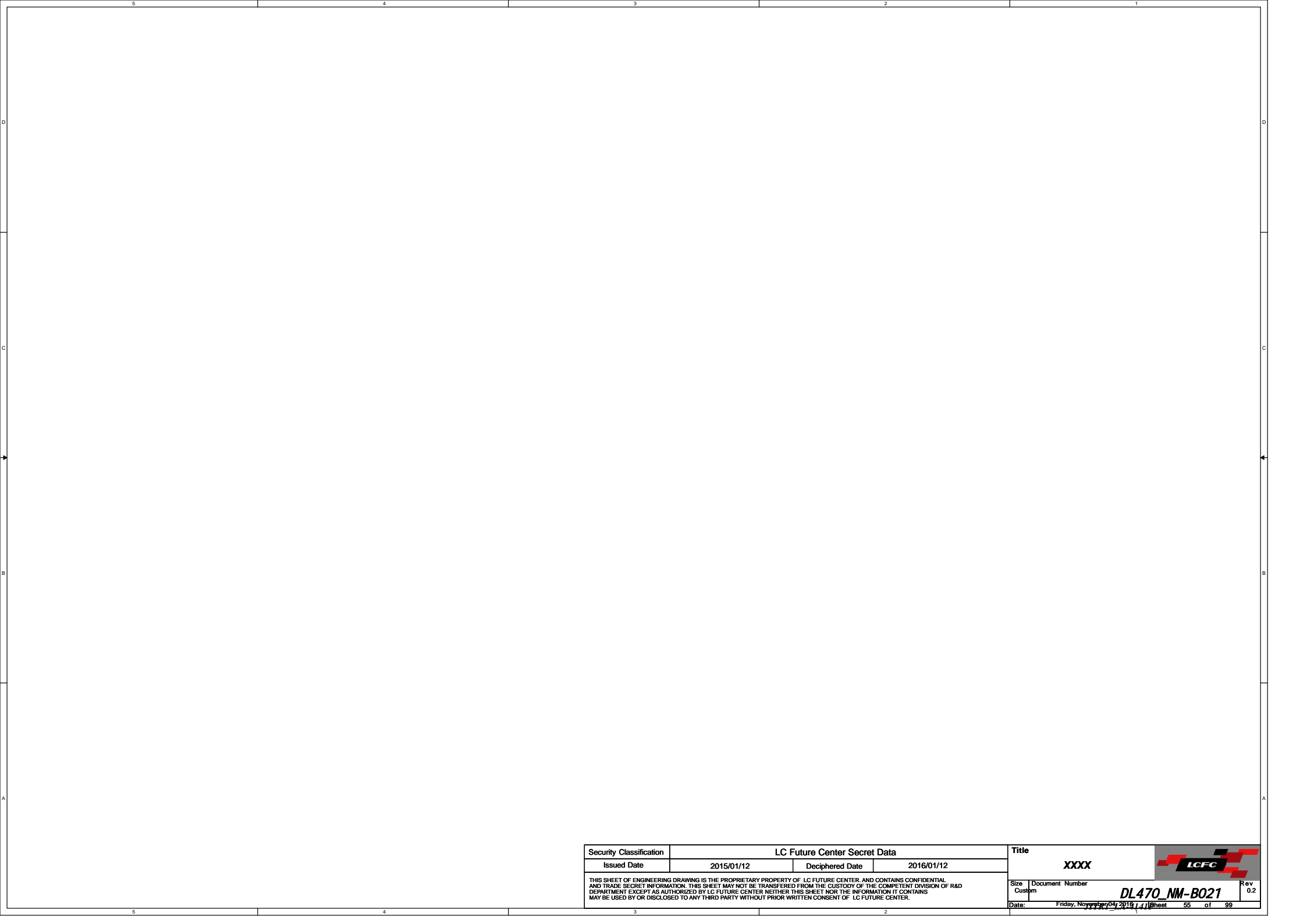
On Board (Right-Front)




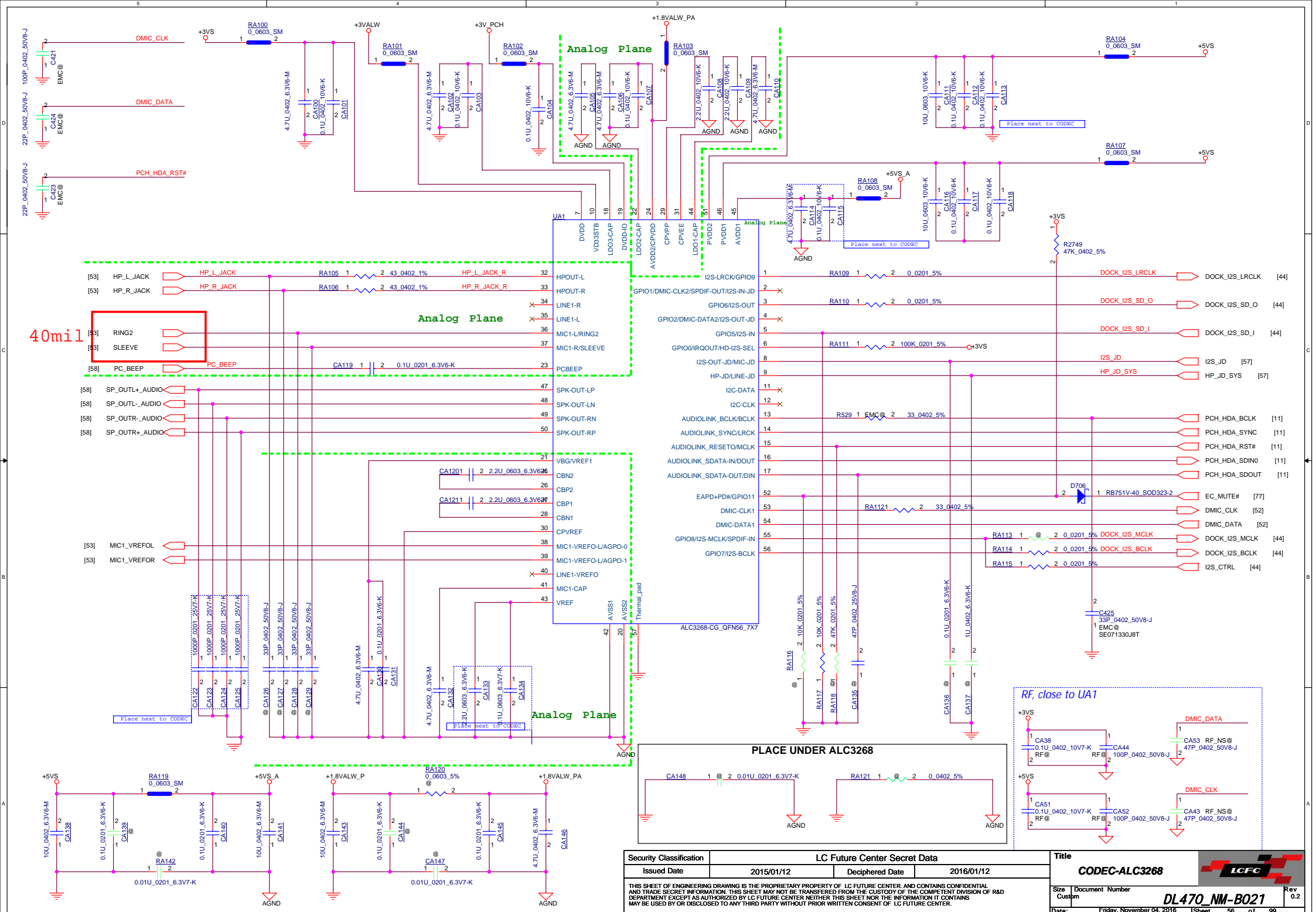
On Board (Right-Back)



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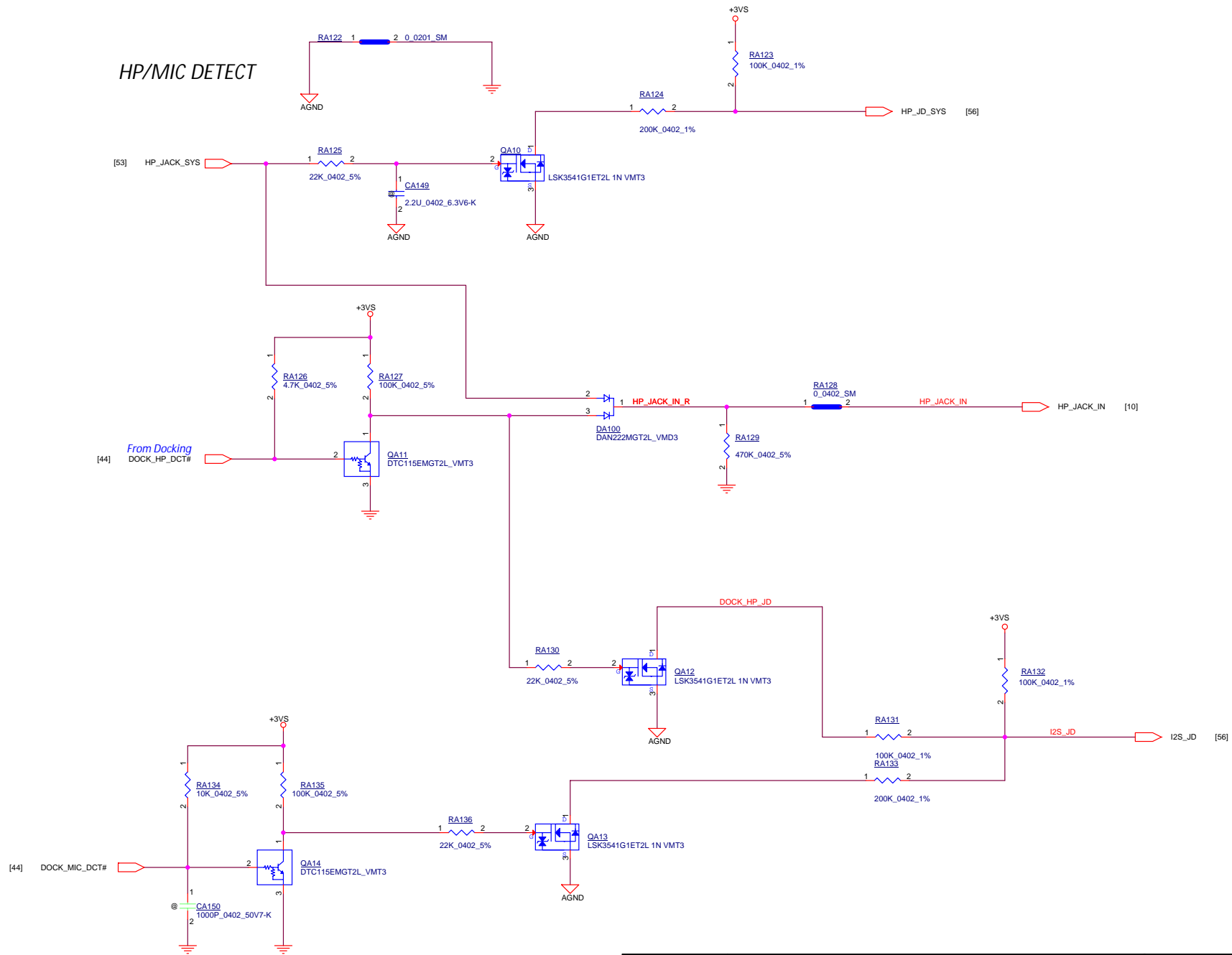
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Title		Rev	
CODEC-ALC3268		DL470_NM-B021	
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Custom		0.2	
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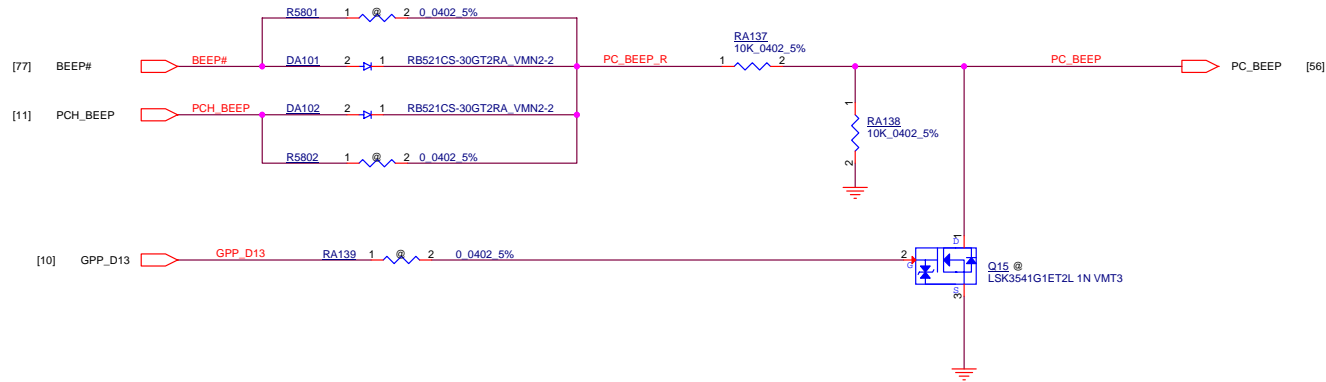
# HP/MIC DETECT



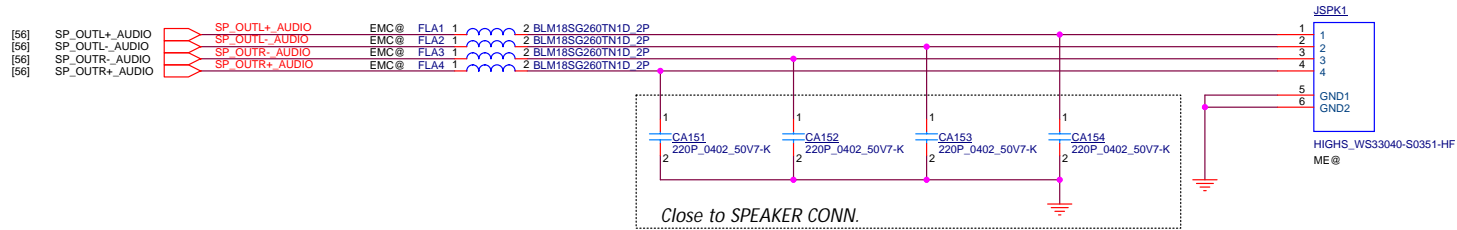
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Issued Date	2015/01/12	Deciphered Date	2016/01/12
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Title		ICFC
HP/MIC DETECT		
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Custom		
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### PC-BEEP



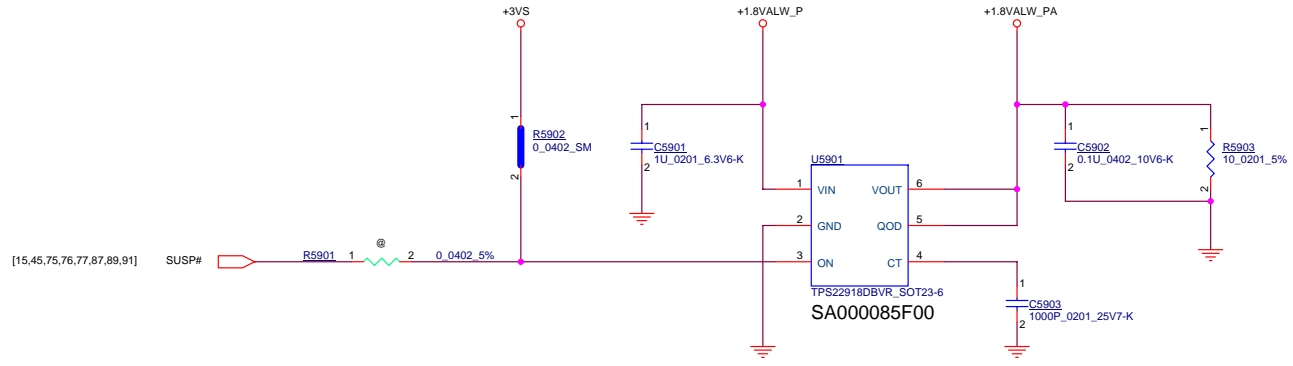
### SPEAKER CONN.



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		2016/01/12
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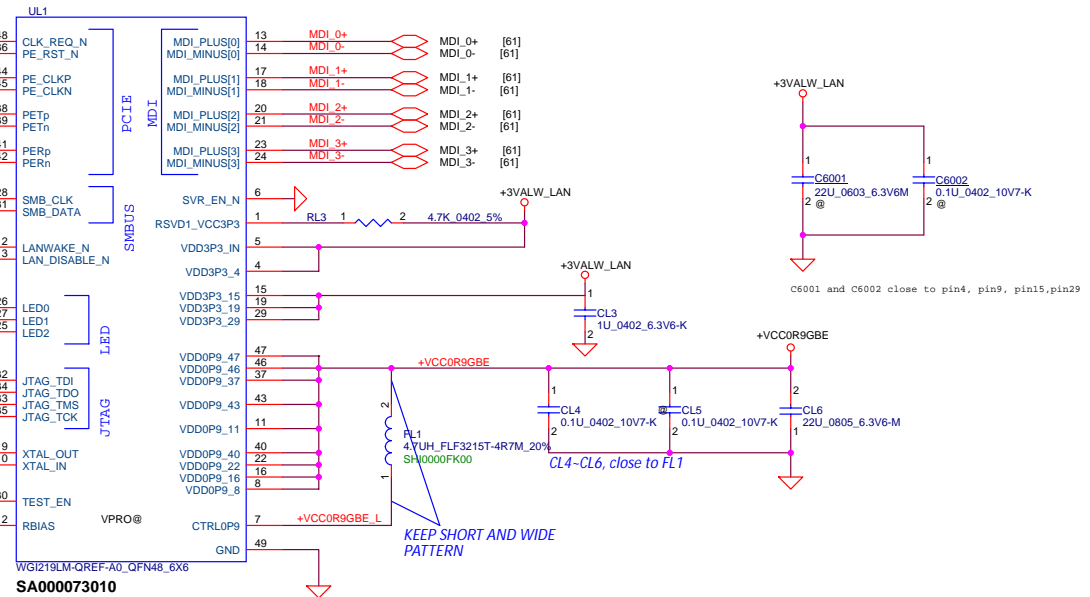
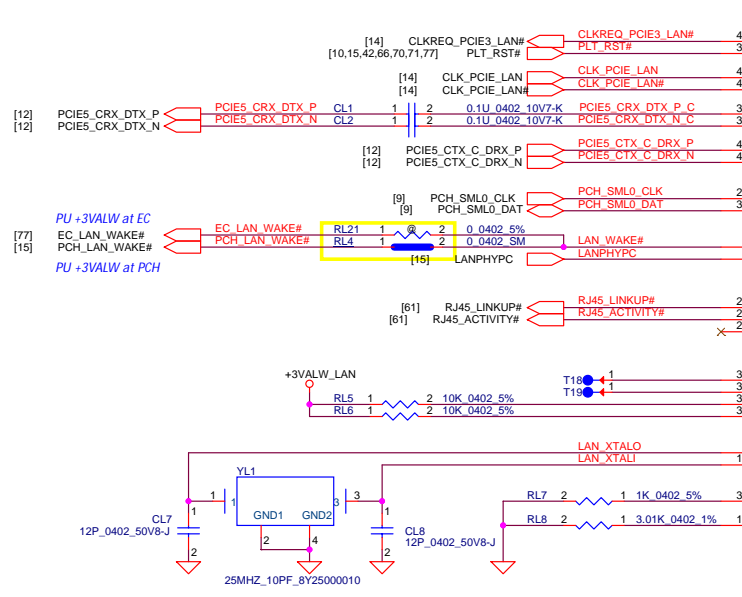
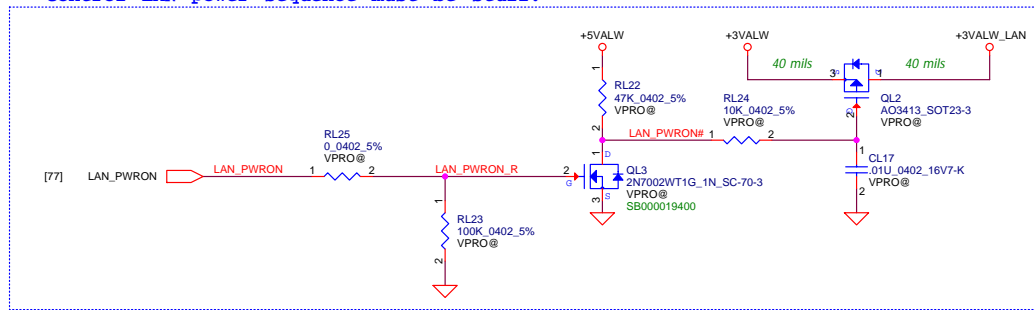
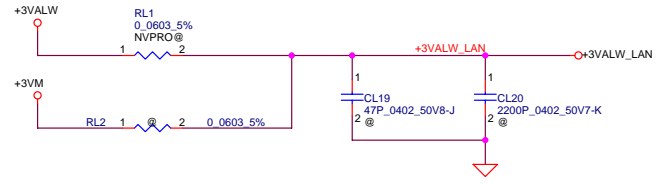




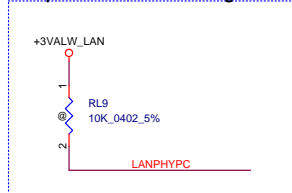
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				Sheet	59 of 99
				Rev	0.2



Due to solve G3 to S5 wake on lan issue  
 +3VALW must meet INTEL spec.  
 Control LAN power sequence must be stuff.

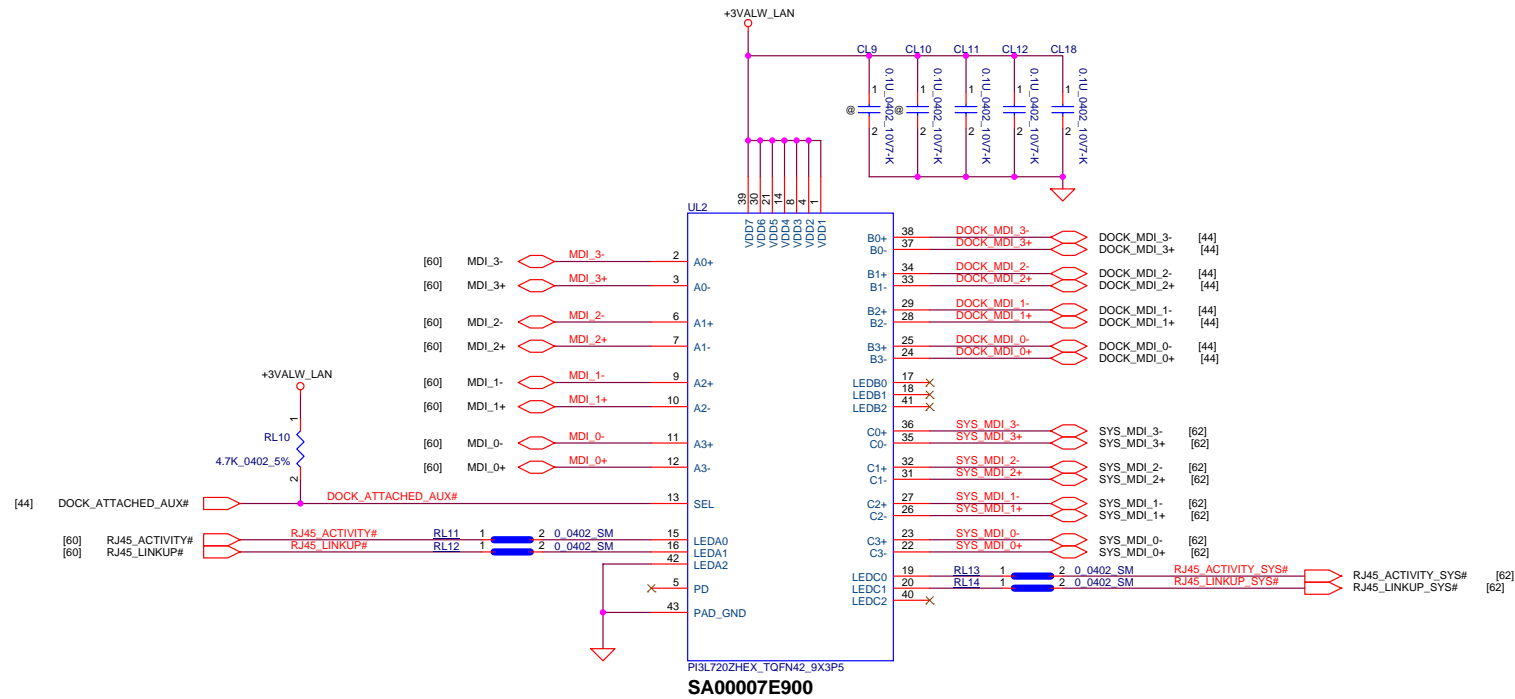


When use Native function, intel  
 recommend pull high 10K ohm.  
 This part is un-mount in Sting.



UL1 GBE PHY

	Model	P/N
vPro	WGI219LM	SA000073010
non-vPro	WGI219V	SA000072220



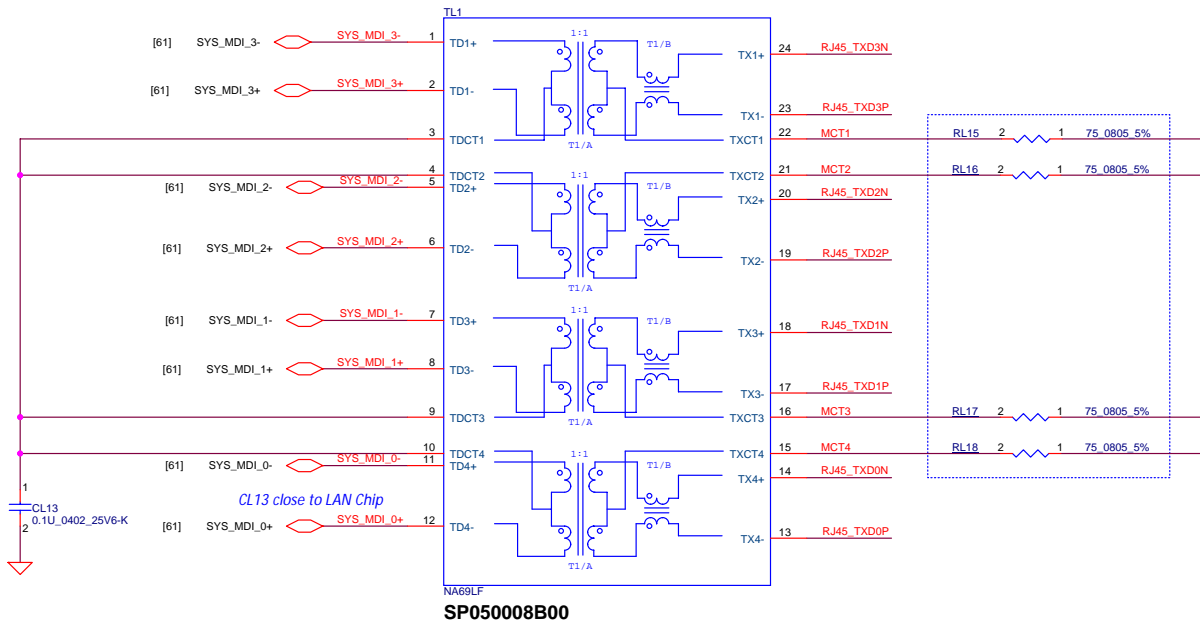
Vendor	P/N	NOTE
Pericom	PI3L720ZHE+CX, SA00007E900	Main Source
ONsemi	NCN7201, SA00005TF00	2nd Source (FVT)

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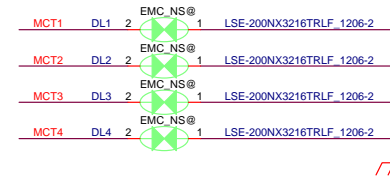
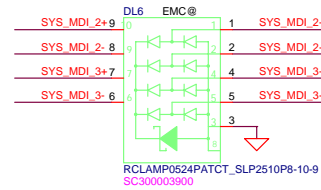
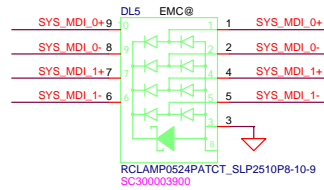
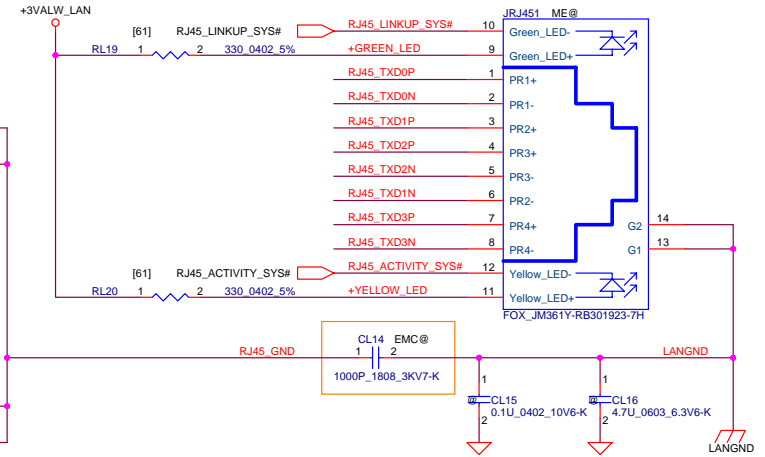


LAN X' FORM



NA69LF  
SP050008B00

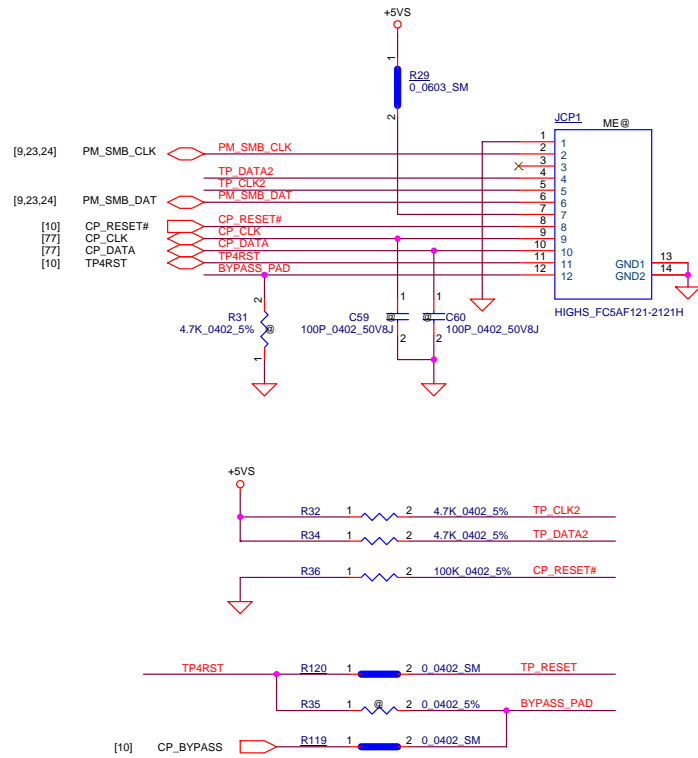
RJ45 Conn.



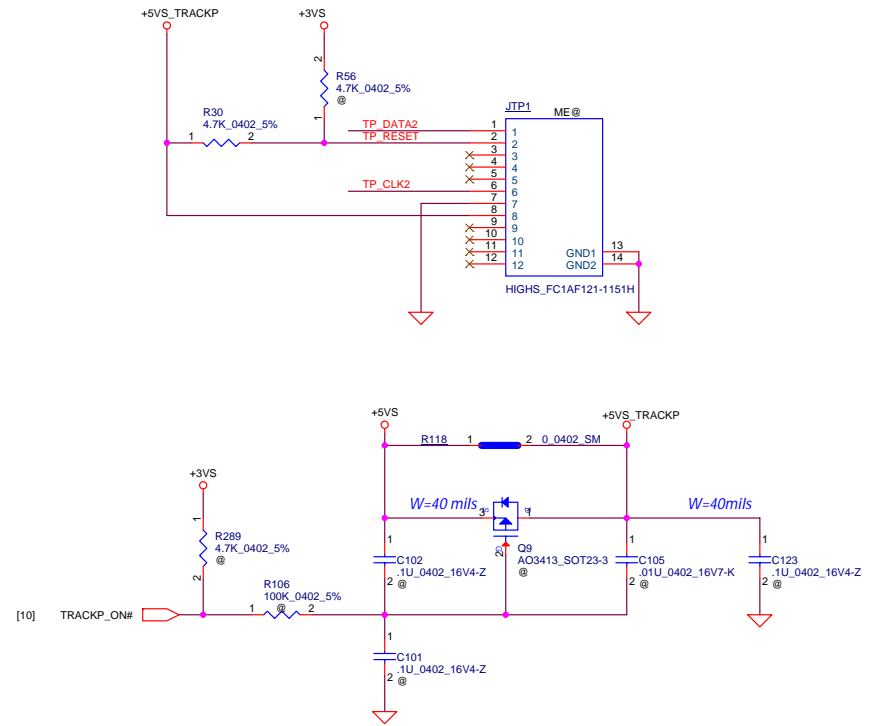
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Title		
RJ45 CONN.		
Size	Document Number	<b>DL470_NM-B021</b>
Custom		
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## 5-Button Click Pad

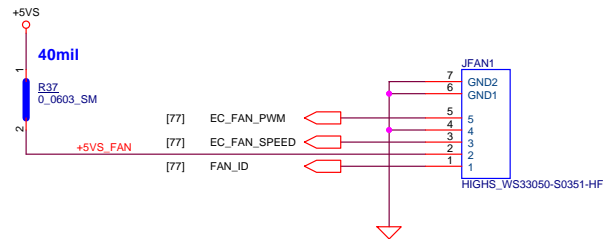


## Track Point

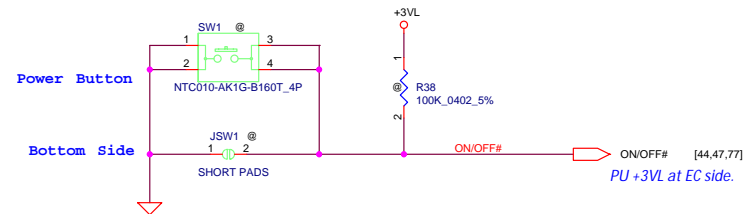



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### FAN CONN.

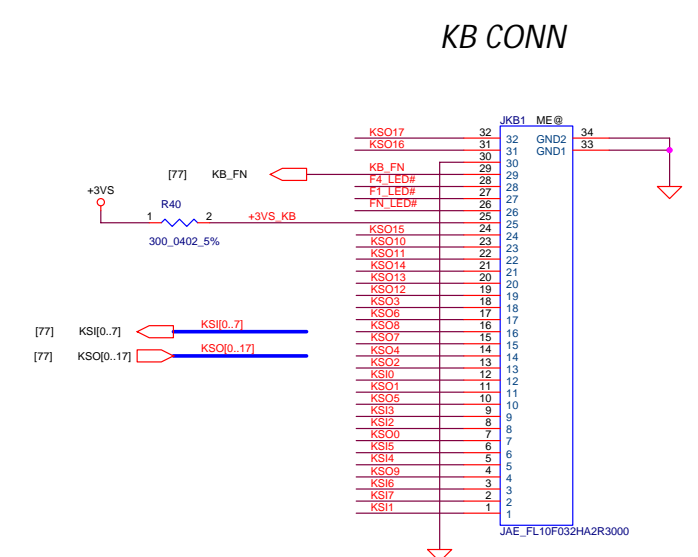
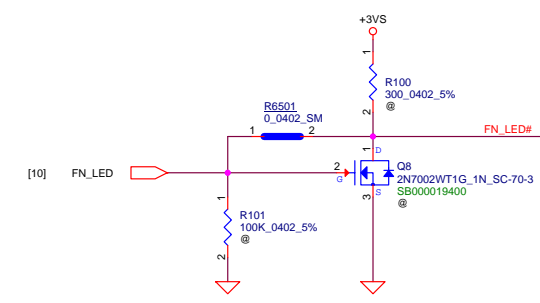
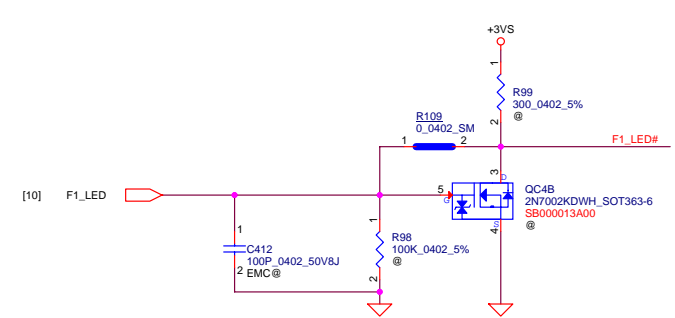
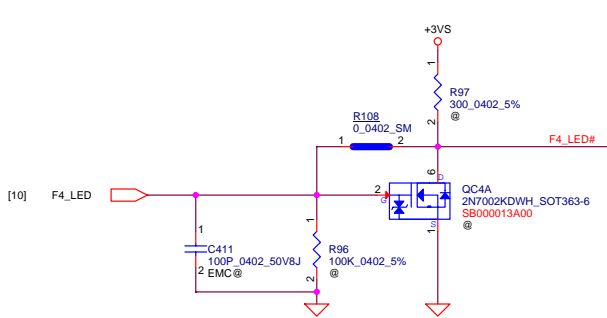


### PWRBTN FOR DENUG

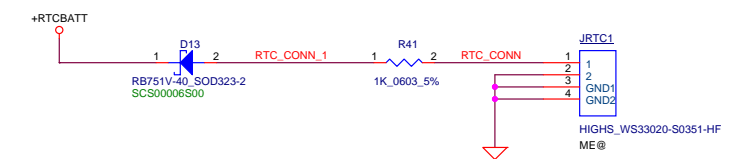


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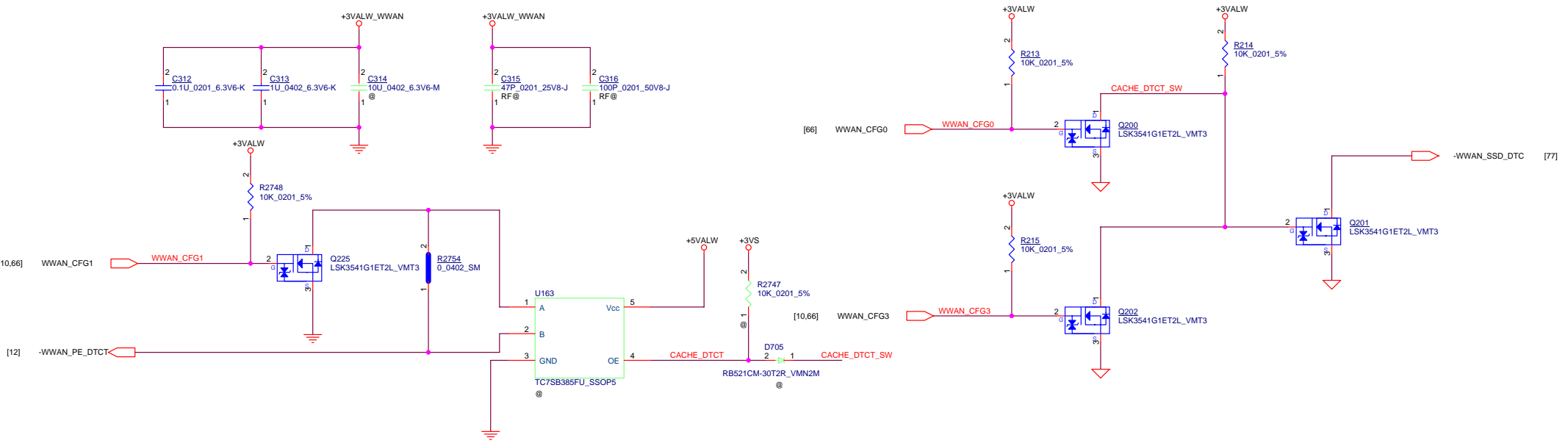
RTC CONN.



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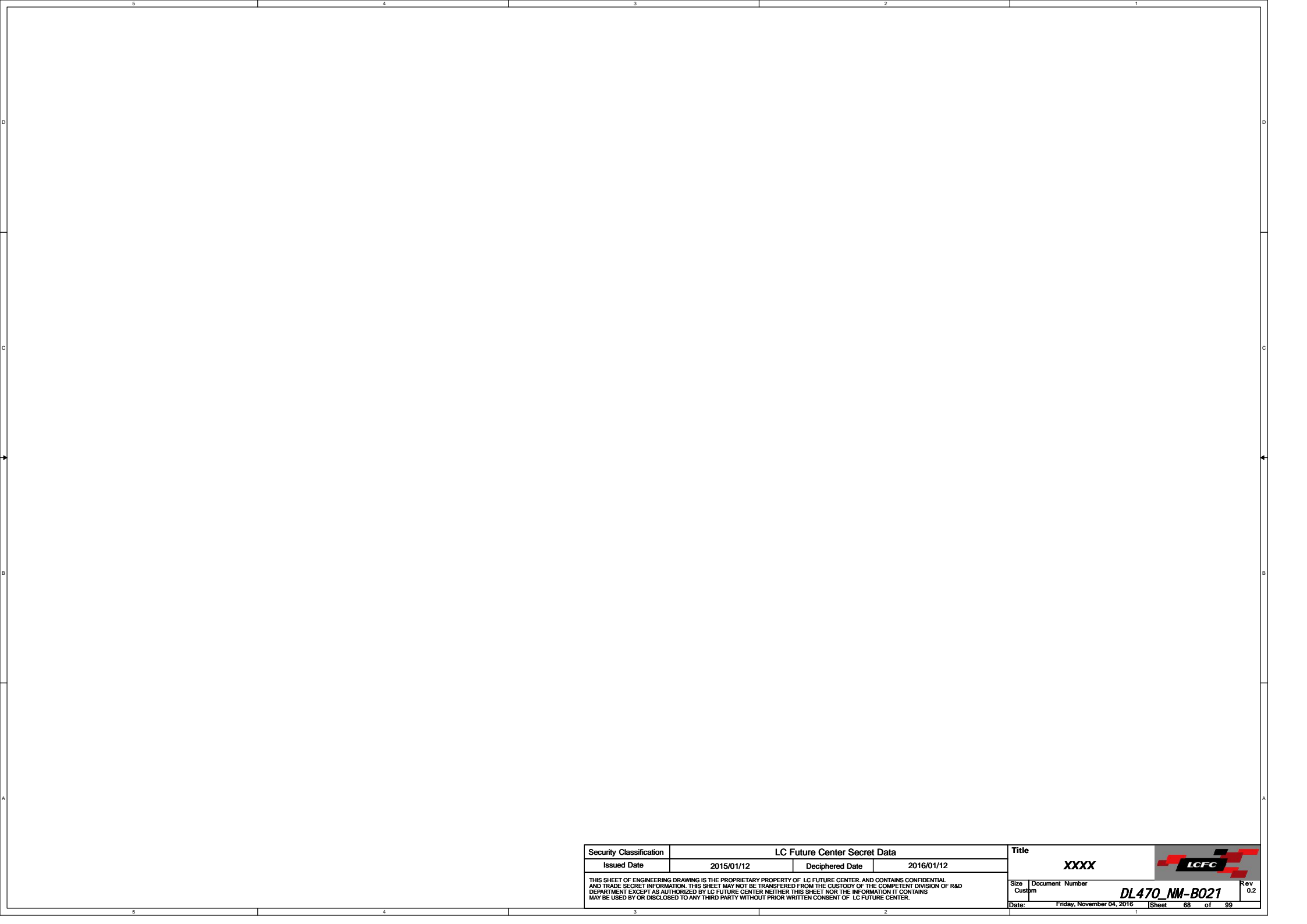



74	3.3V	CONFIG_2	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	CONFIG_1	69
66	SIM DETECT (O)	RESET# (O)(0/1.8V)	67
64	COEX1 (I/O)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX2 (I/O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	N/C	ANTCTLO (I)(0/1.8V)	59
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V)	REFCLKn	53
50	PERST# (O)(0/3.3V)	GND	51
48	GPIO_4 (I/O)(0/1.8V*)	PETp/SATA-A+	49
46	GPIO_3 (I/O)(0/1.8V*)	PETn/SATA-A-	47
44	GPIO_2 (I/O)(0/1.8V*)	GND	45
42	GPIO_1 (I/O)(0/1.8V*)	PERp/SATA-B-	43
40	GPIO_0 (I/O)(0/1.8V*)	PERn/SATA-B+	41
38	DEVSLP (O)	GND	39
36	UIM-PWR (I)	PETp1/USB3-D-Tx+/SSIC-TxP	37
34	UIM-DATA (I/O)	PETn1/USB3-D-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3-D-Rx+/SSIC-RxP	31
28	GPIO_8 (I/O) (0/1.8V)	PERn1/USB3-D-Rx-/SSIC-RxN	29
26	GPIO_10 (I/O) (0/1.8V)	GND	27
24	GPIO_7 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
22	GPIO_6 (I/O) (0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
20	GPIO_5 (I/O) (0/1.8V)	CONFIG_0	21
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
10	GPIO_9/SAS/D5# (I/O)/LED1B(I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	USB_D+	7
4	3.3V	GND	5
2	3.3V	CONFIG_3	3

TABLE:

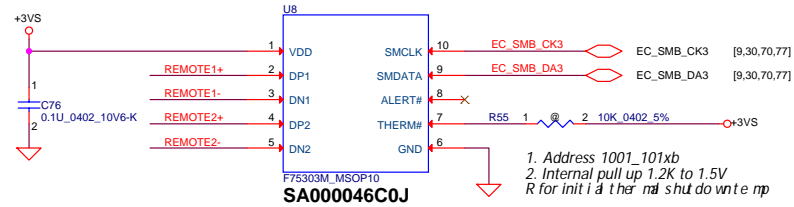
State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

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				DL470_NM-B021	
				Rev	0.2
				Date:	Friday, November 04, 2016
				Sheet	67 of 99

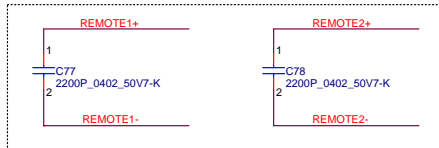


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Issued Date	2015/01/12	Deciphered Date	2016/01/12	XXXX		
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				Custom	DL470_NM-B021	0.2
				Date:	Friday, November 04, 2016	Sheet 68 of 99

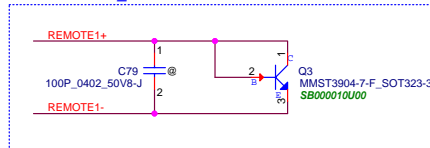
### Thermal Sensor



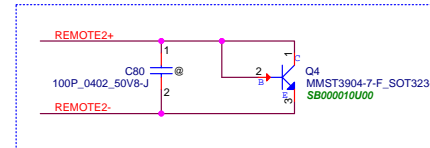
Close to U8



Close to +VCC\_CORE



Close JDIMM1&JDIMM2

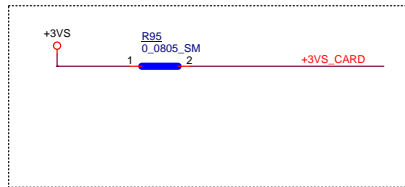


REMOTE2+/-:  
 Trace width/space:10/10 mil  
 Trace length:<8"

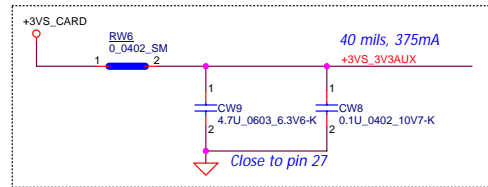
Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/01/12	Deciphered Date	2016/01/12
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Date:	Friday, November 04, 2016	Sheet	69 of 99



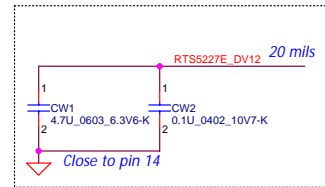
**+3VS TO +3VS\_CARD**



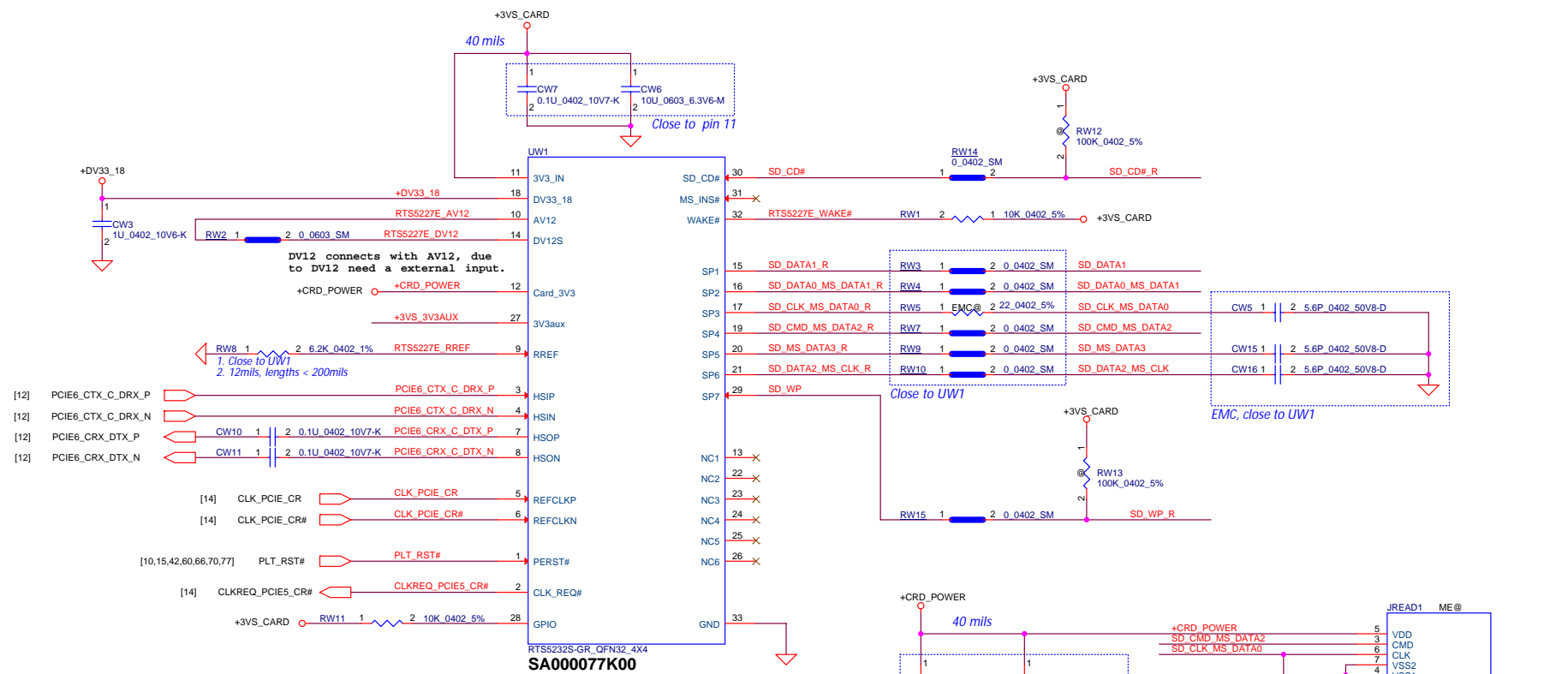
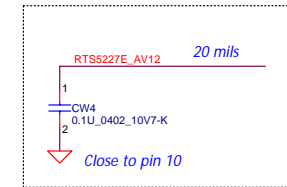
**+3VS\_3V3AUX**



**RTS5227E\_DV12**



**RTS5227E\_AV12**



- [12] PCIE6\_CTX\_C\_DRX\_P
- [12] PCIE6\_CTX\_C\_DRX\_N
- [12] PCIE6\_CRX\_DTX\_P
- [12] PCIE6\_CRX\_DTX\_N

- [14] CLK\_PCIE\_CR
- [14] CLK\_PCIE\_CR#
- [10,15,42,60,66,70,77] PLT\_RST#
- [14] CLKREQ\_PCIE5\_CR#

Connector side / IC side	WP		CD
	Lock	Unlock	
Card insertion	L	H	H
Card uninsertion	L	L	L

**Security Classification** LC Future Center Secret Data

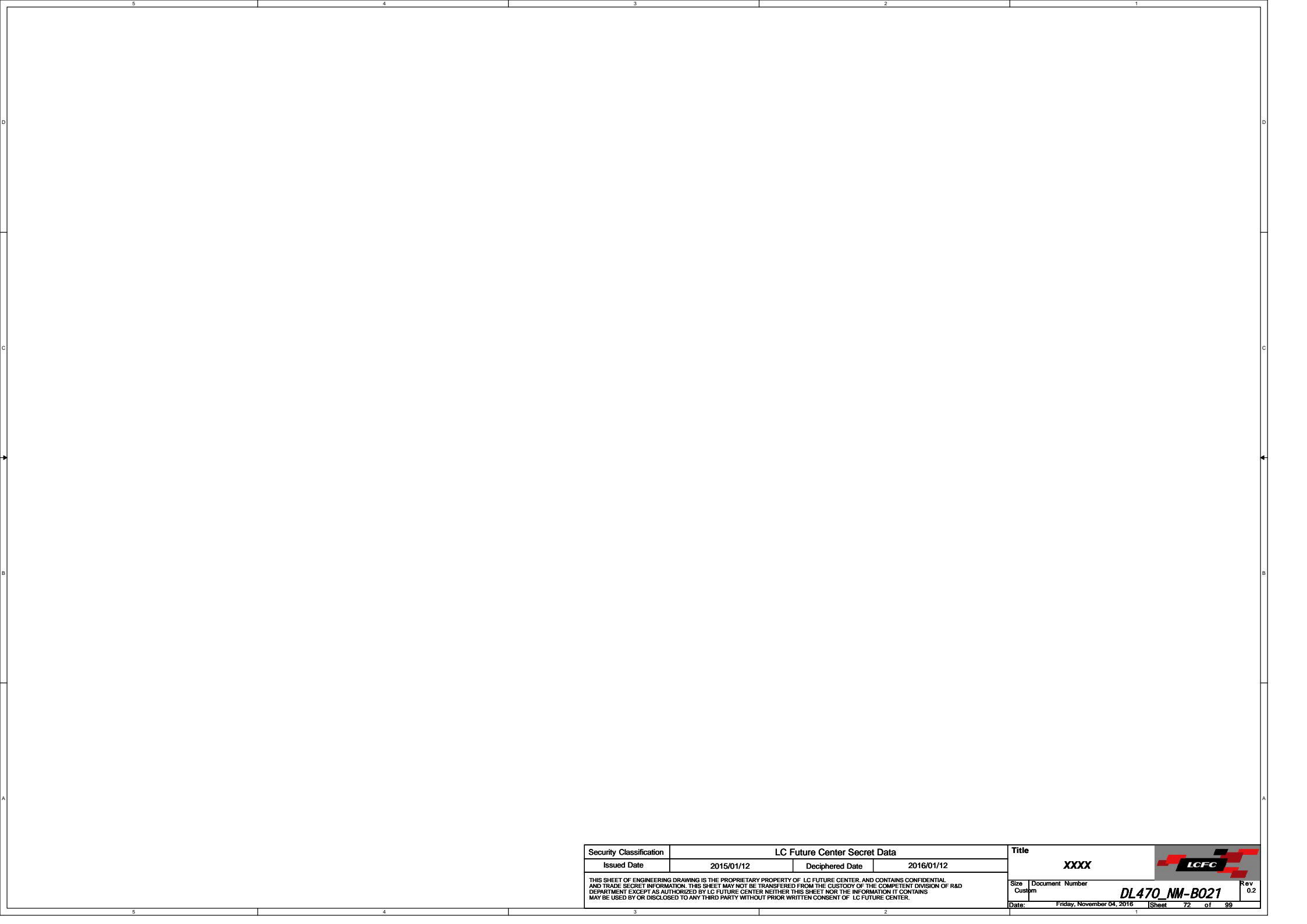
**Issued Date** 2015/01/12      **Deciphered Date** 2016/01/12

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**Title** RTS5232S CARDREADER/CO

**Size** Custom      **Document Number** DL470\_NM-B021

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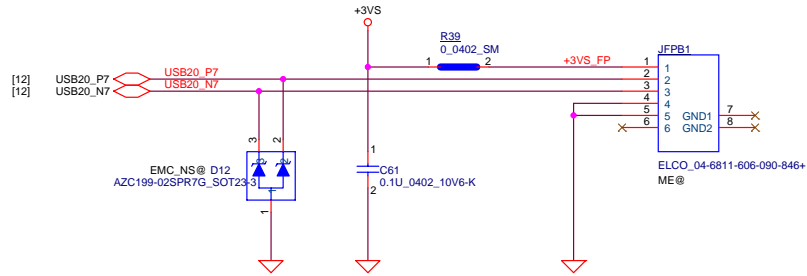


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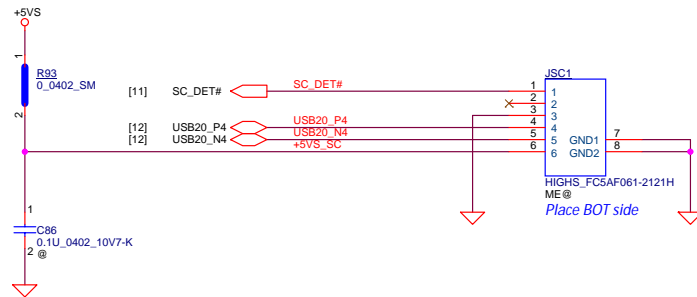
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Size	Custom	
Document Number	DL470_NM-B021	Rev 0.2
Date:	Friday, November 04, 2016	Sheet 72 of 99



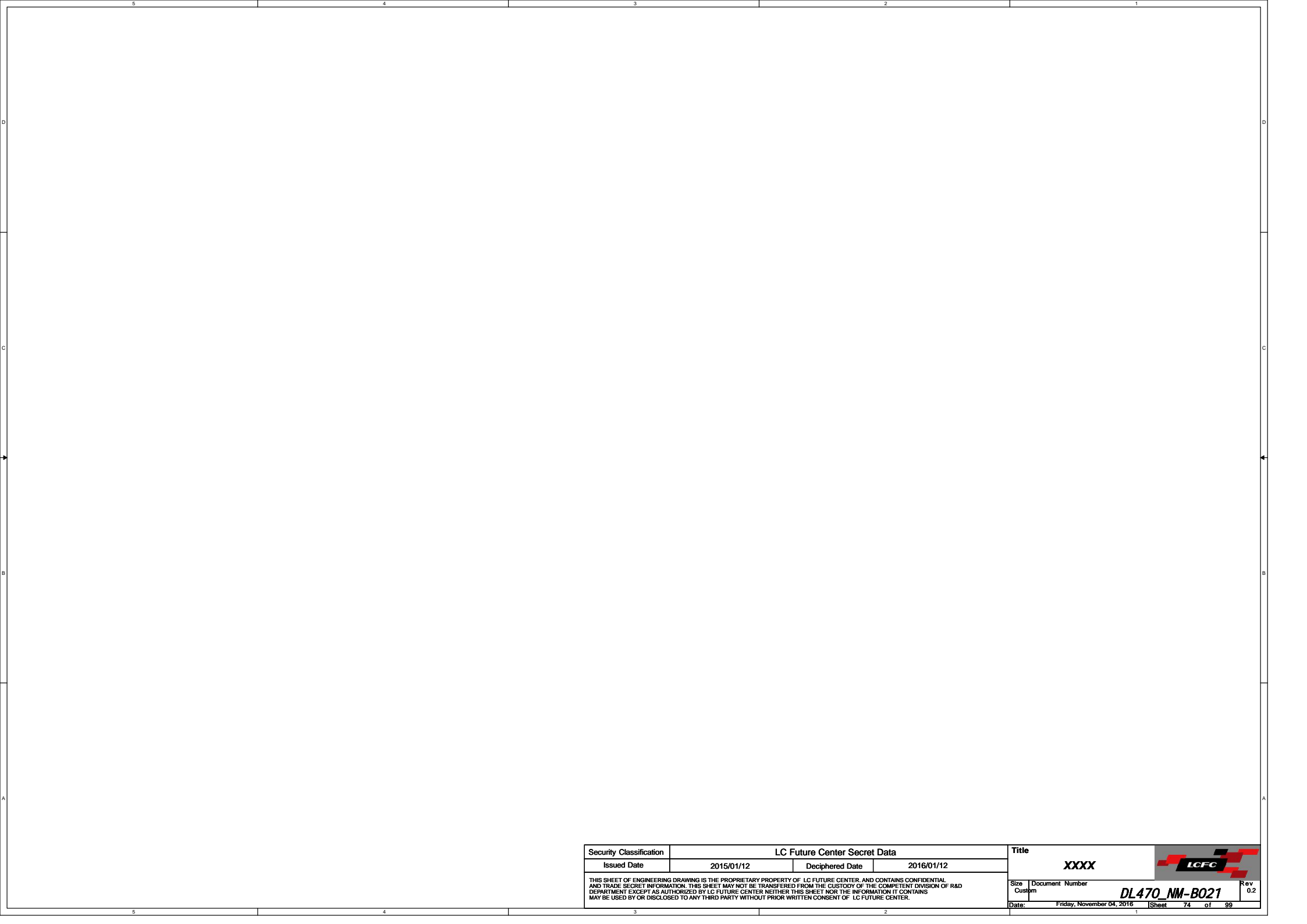
### FingerPrint CONN.




### SMART CARD CONN.

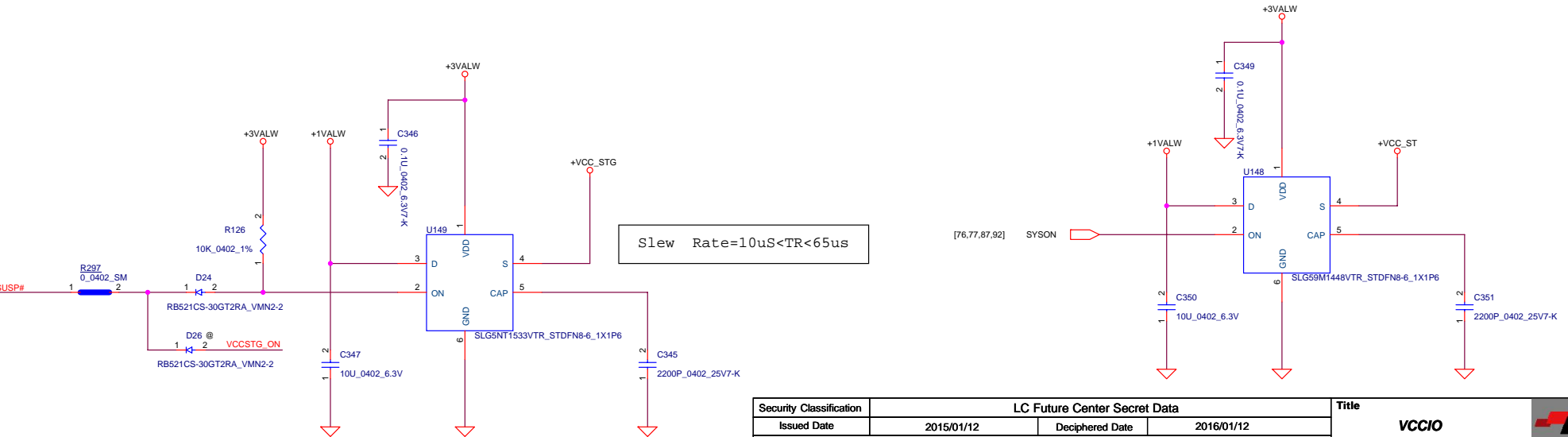
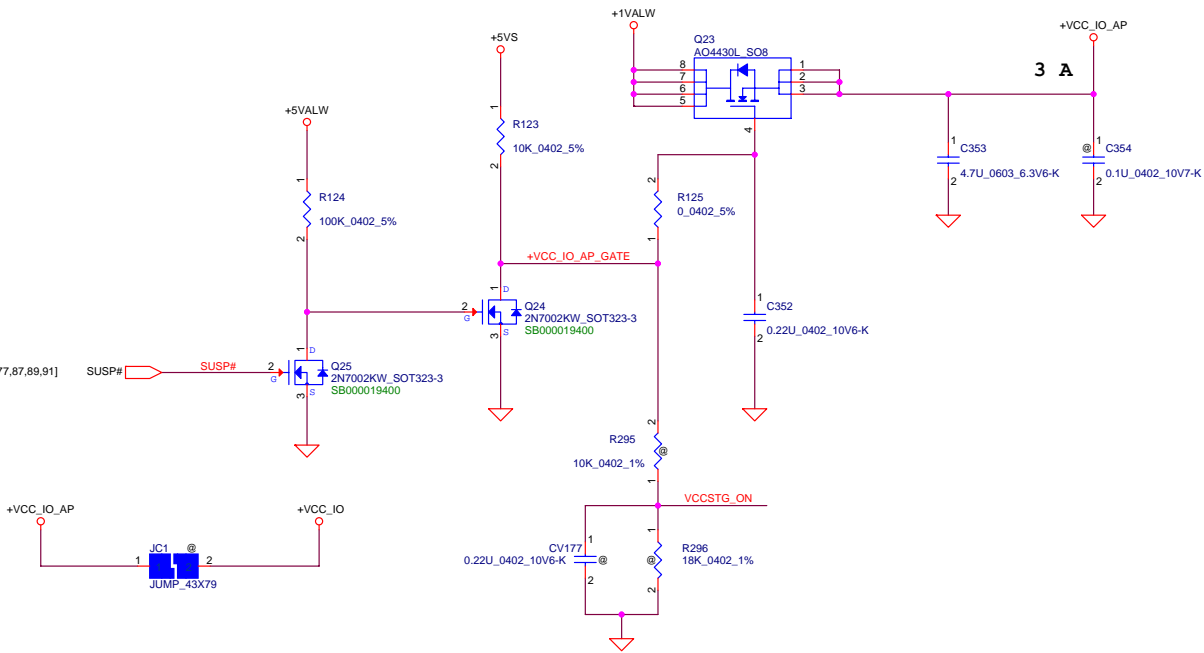


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			Rev 0.2
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+1VALW to +VCC\_IO\_AP



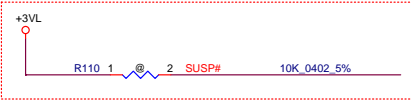
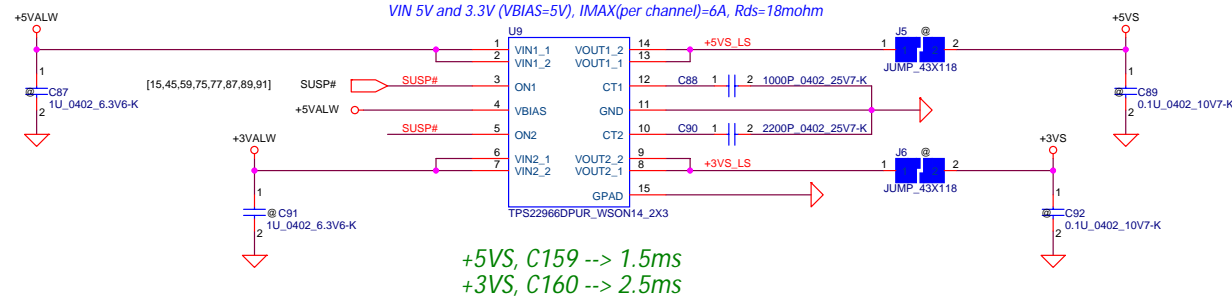
Security Classification			
LC Future Center Secret Data			
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Title	
VCCIO	
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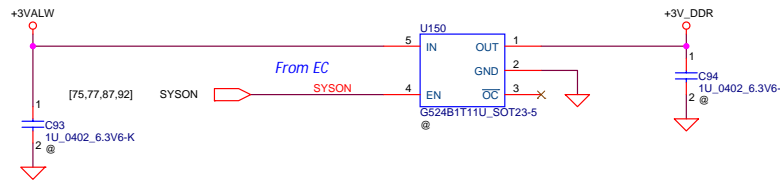
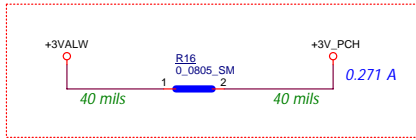
Rev 0.2

Smart Switch  
+5VALW To +5VS  
+3VALW To +3VS

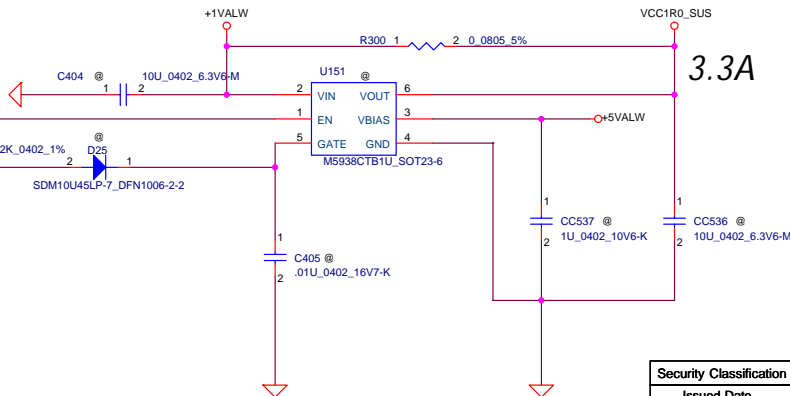


1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

+3VALW To +3V\_PCH : Short, Don't support Deep Sx

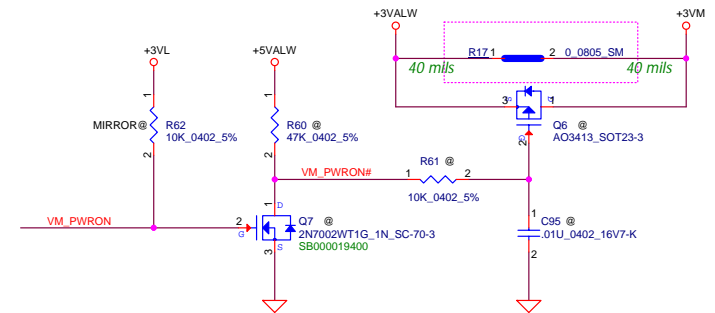


+1VALW to VCC1R0\_SUS

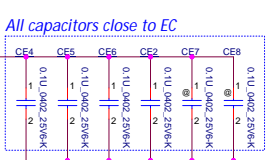
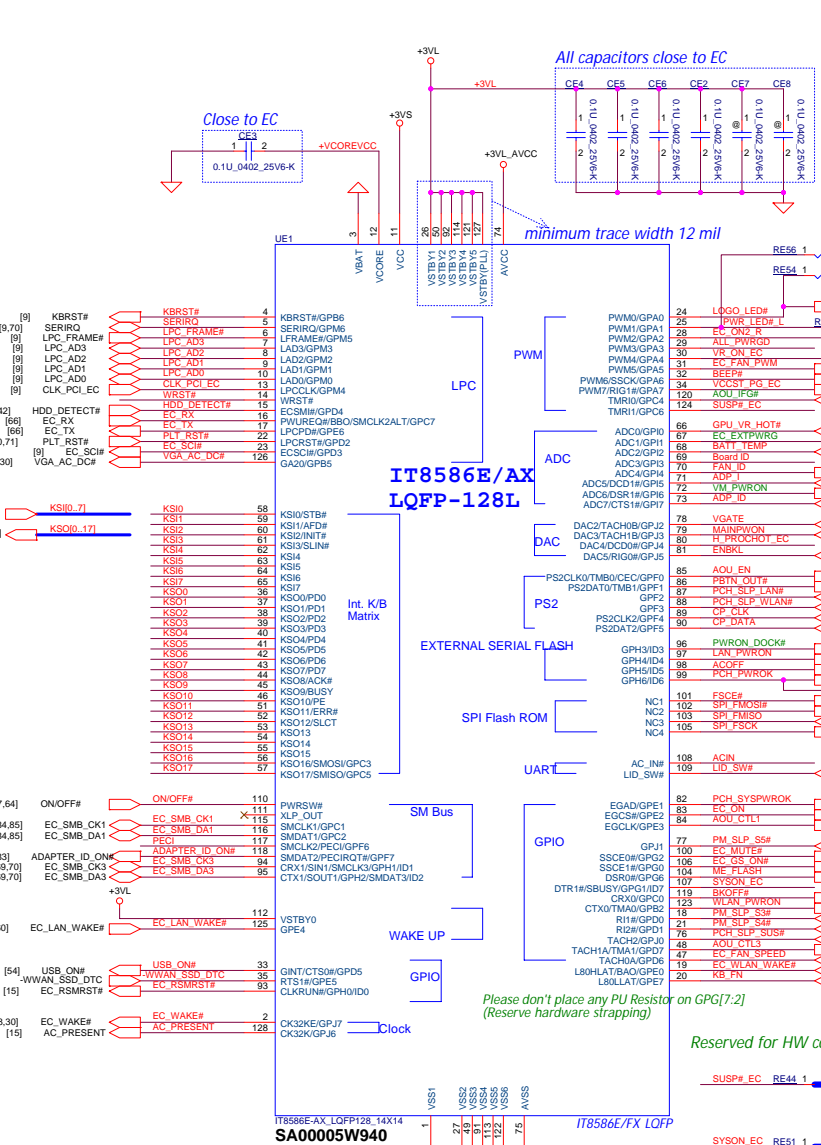
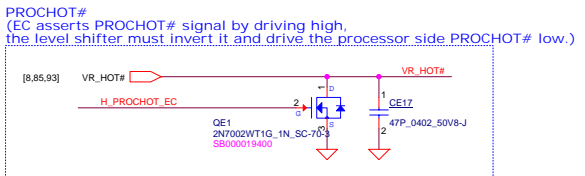
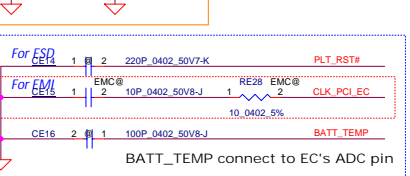
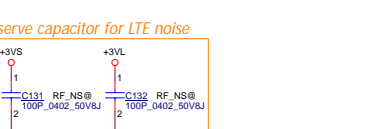
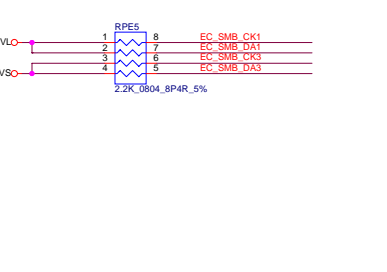
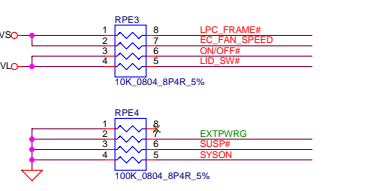
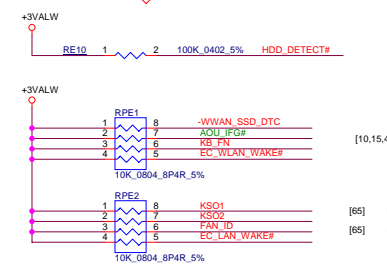
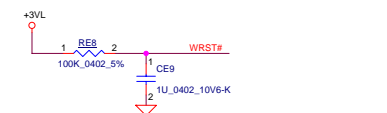
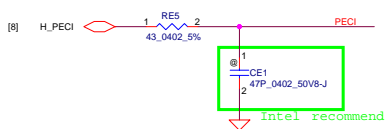


+3VALW to +3VM  
VPRO : SPI ROM

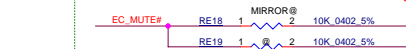
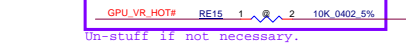
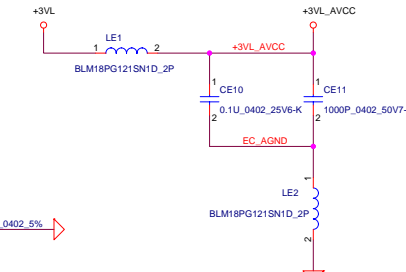
+3VM to SPI ROM.  
Reserve for LAN and WLAN.



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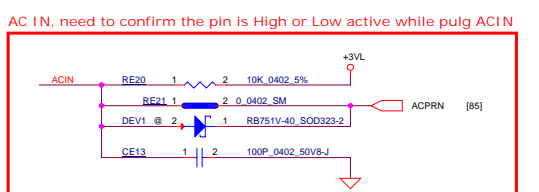
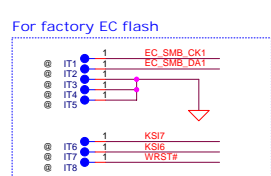


Vcc		3.3V +/- 5%			
Board ID	RE7	VAD_BID min	VAD_BID typ	VAD_BID max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



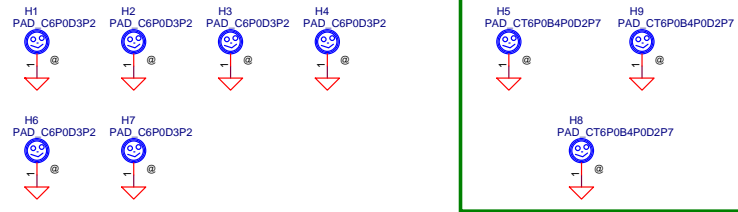
1. Version CX : Don't Support Mirror Code  
Version DX/EX/FX : Support Mirror Code  
2. For Mirror Code "H" --> Enable  
"L" --> Disable (Default)

Reserved for HW control

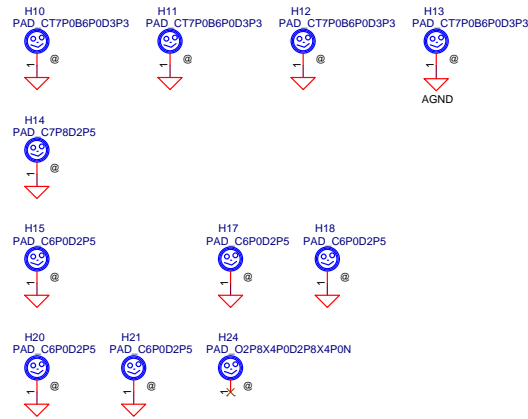


# Screw Hole

For CPU and GPU



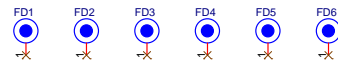
For ME GND hole




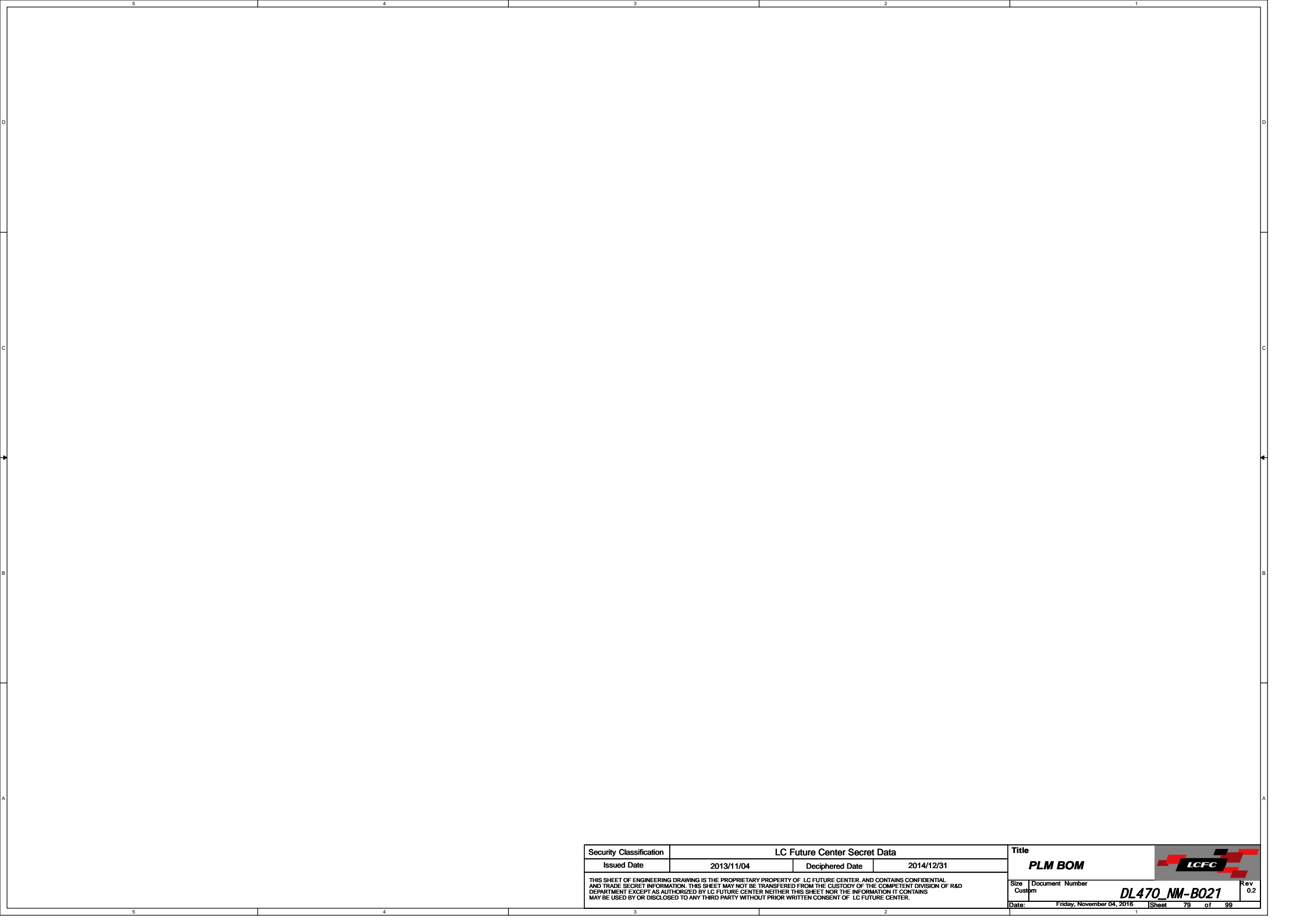
For ME hole




## PCB Fedical Mark PAD

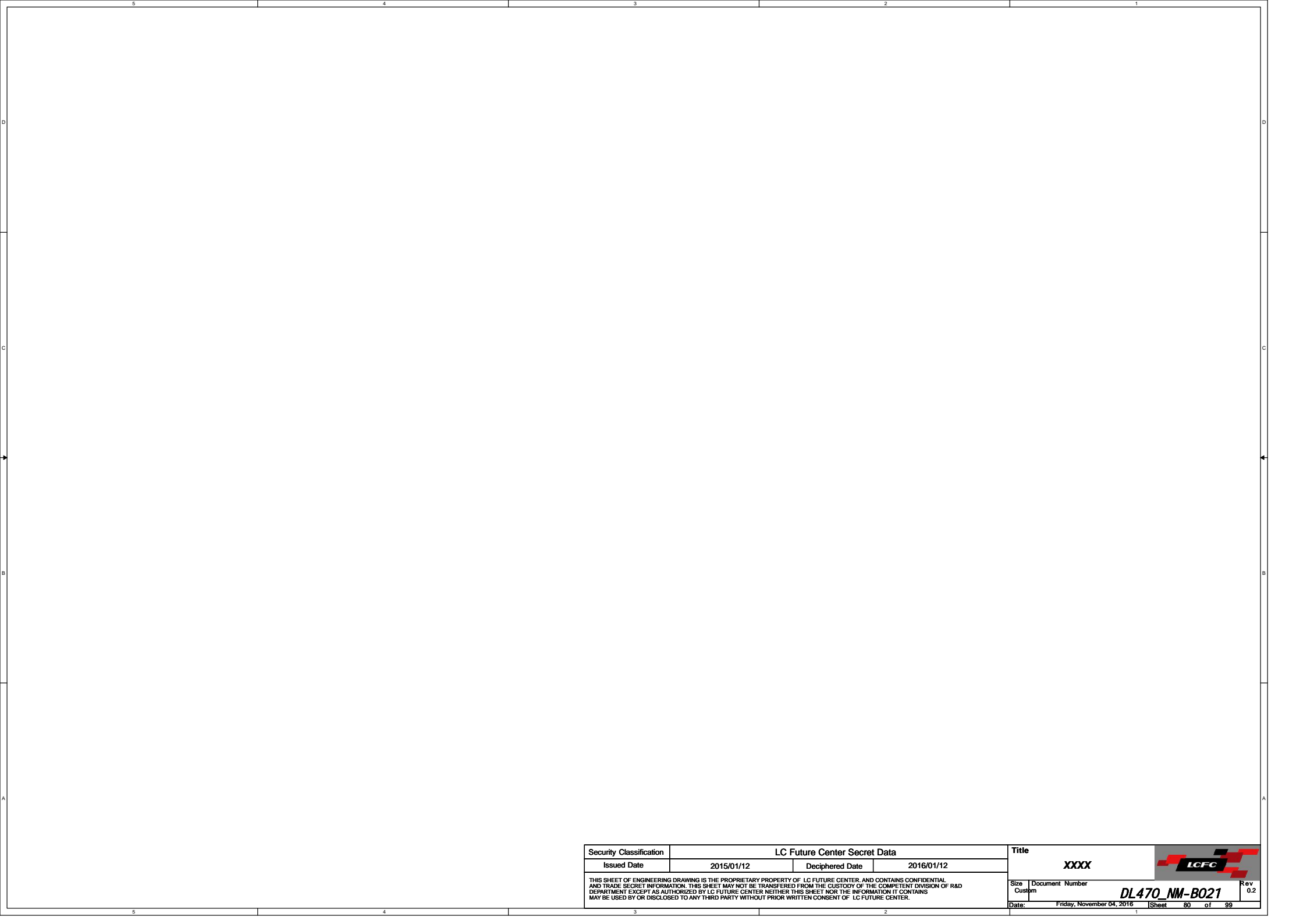



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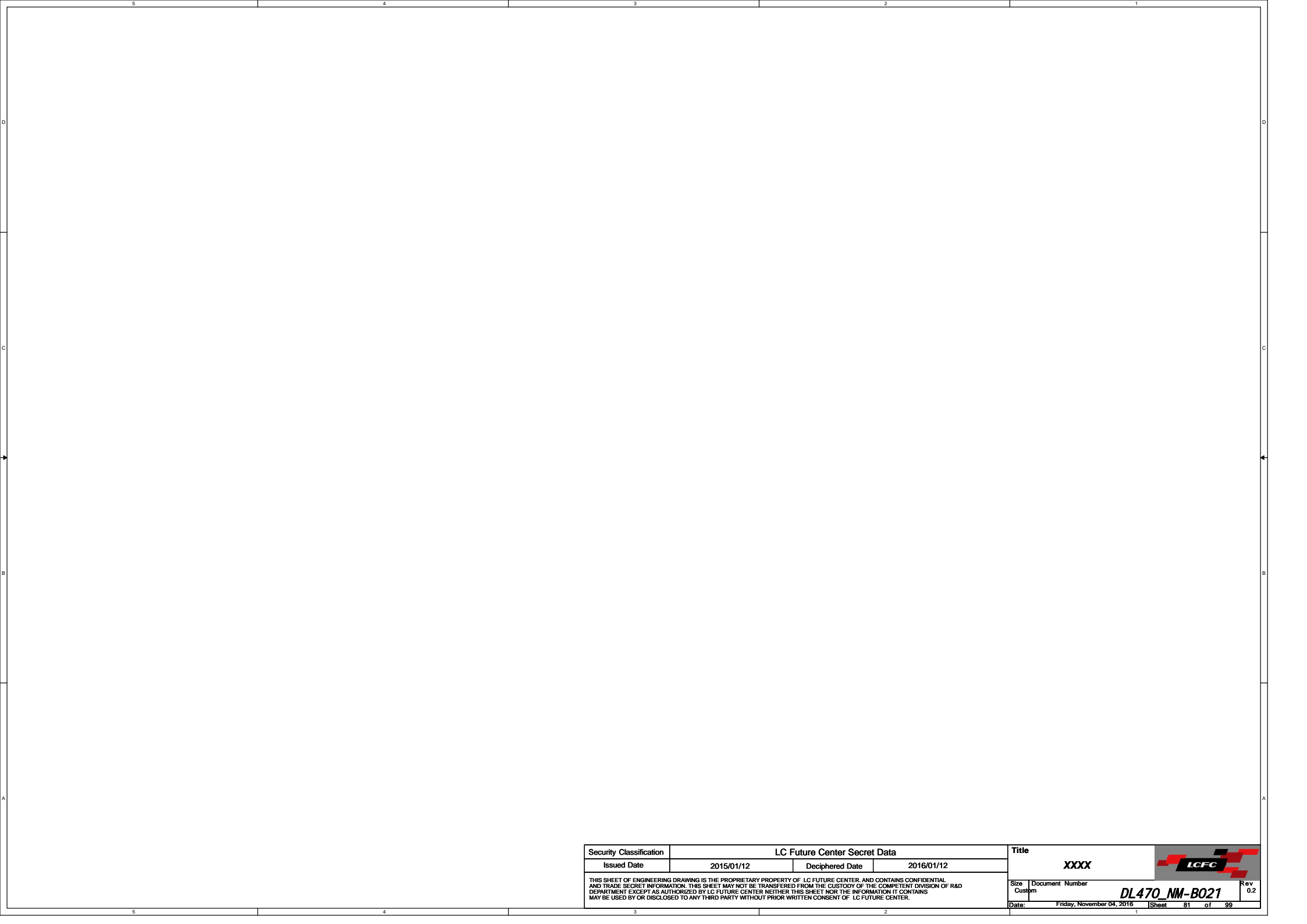
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Issued Date	2013/11/04	Deciphered Date	2014/12/31
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PLM BOM		
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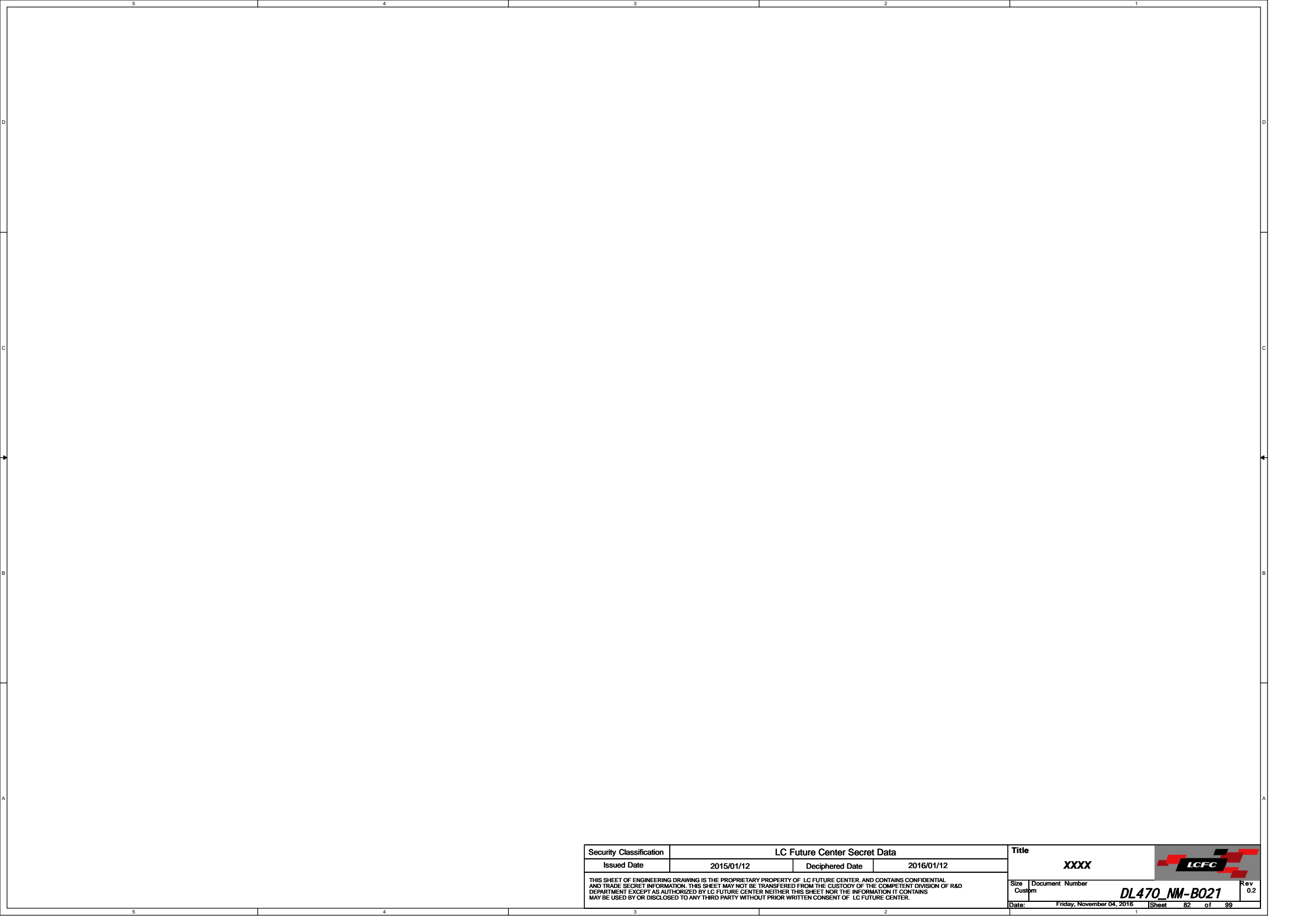
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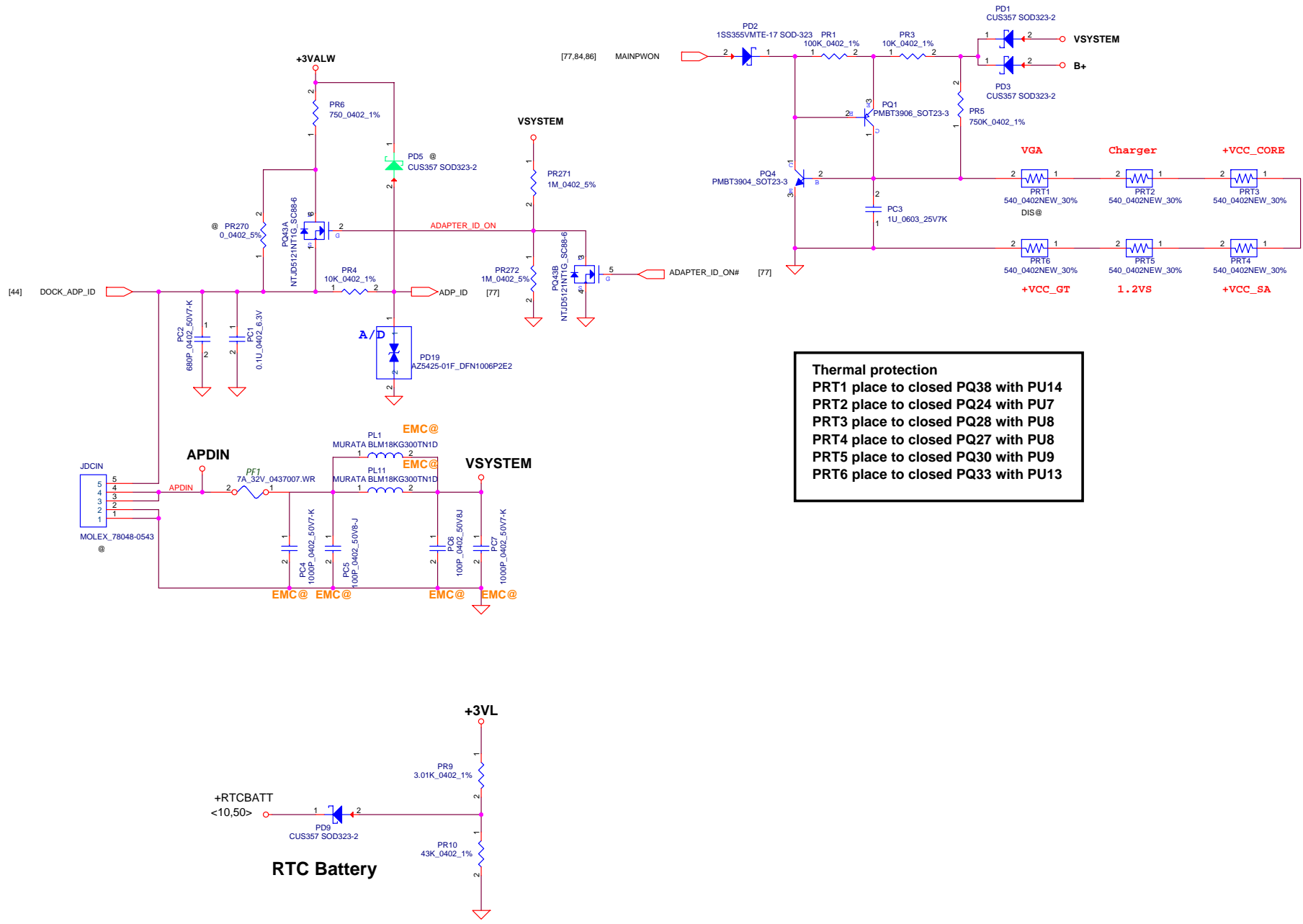
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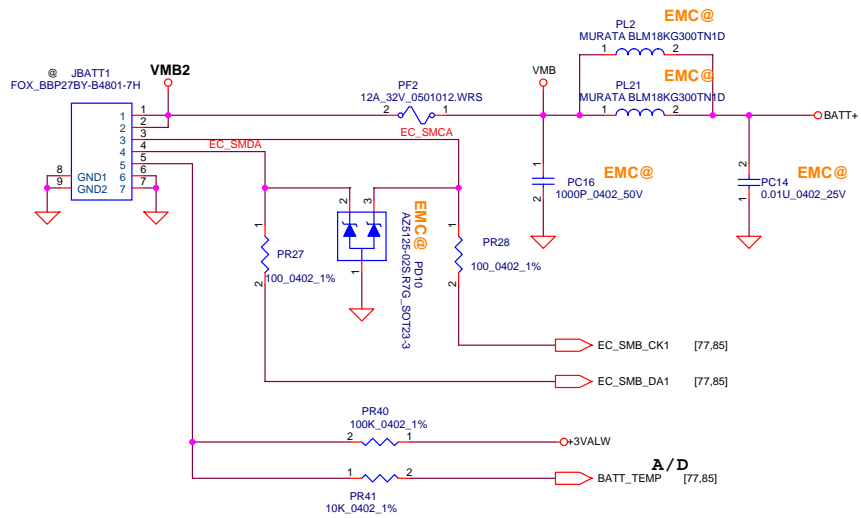
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		2016/01/12
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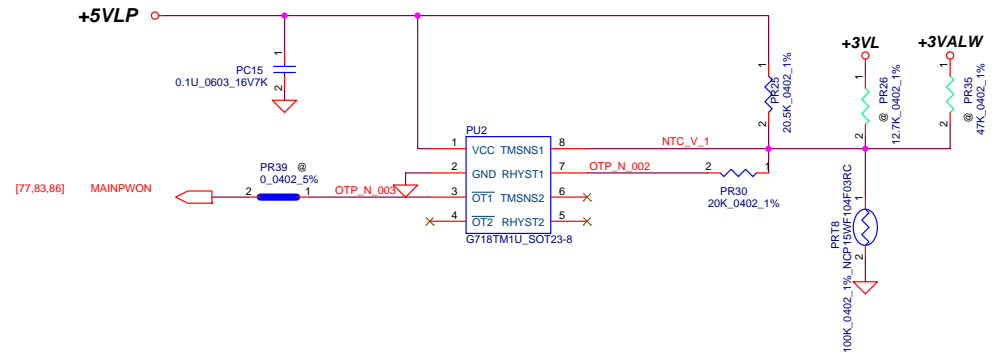



**Thermal protection**  
 PRT1 place to closed PQ38 with PU14  
 PRT2 place to closed PQ24 with PU7  
 PRT3 place to closed PQ28 with PU8  
 PRT4 place to closed PQ27 with PU8  
 PRT5 place to closed PQ30 with PU9  
 PRT6 place to closed PQ33 with PU13

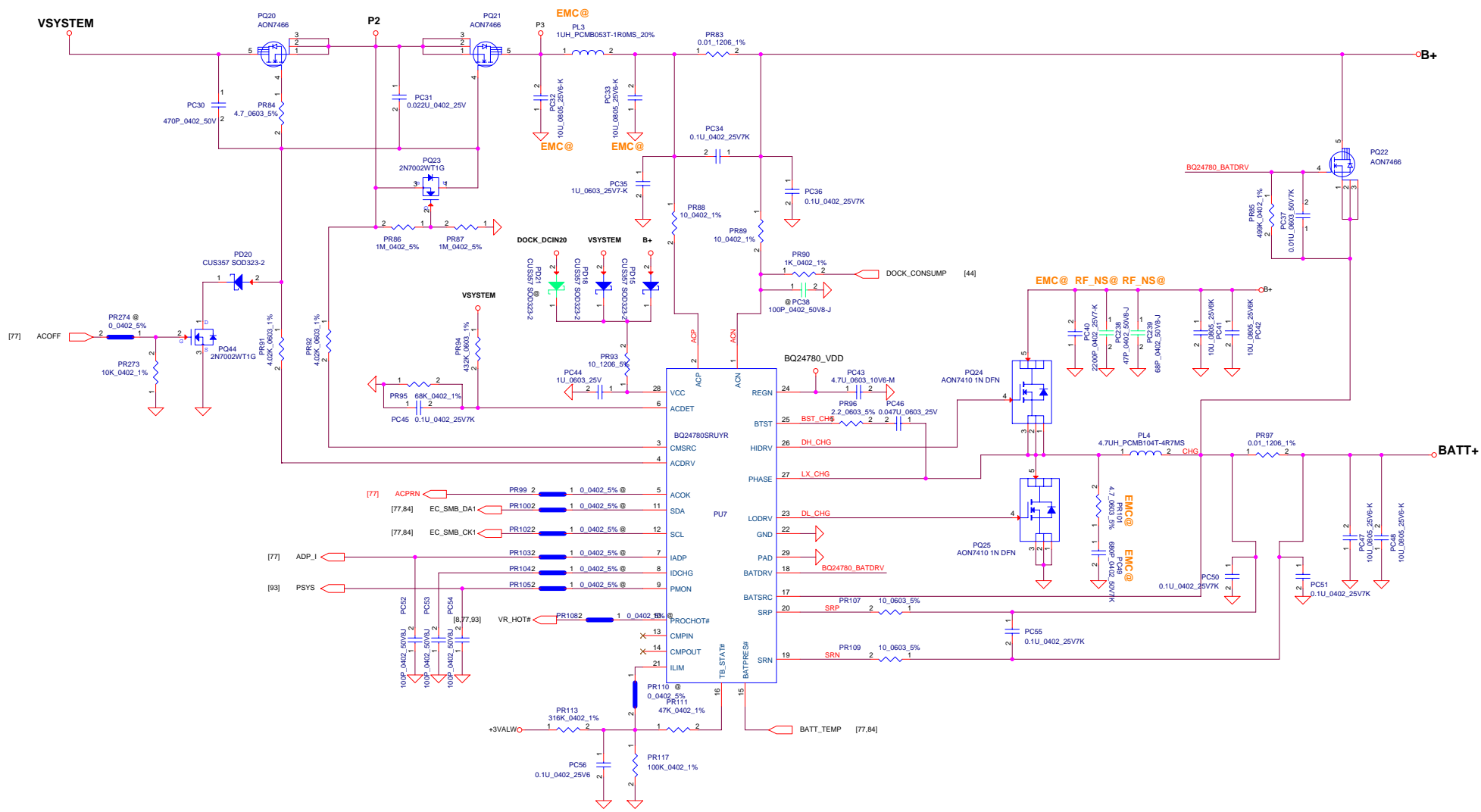
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				Rev 0.1




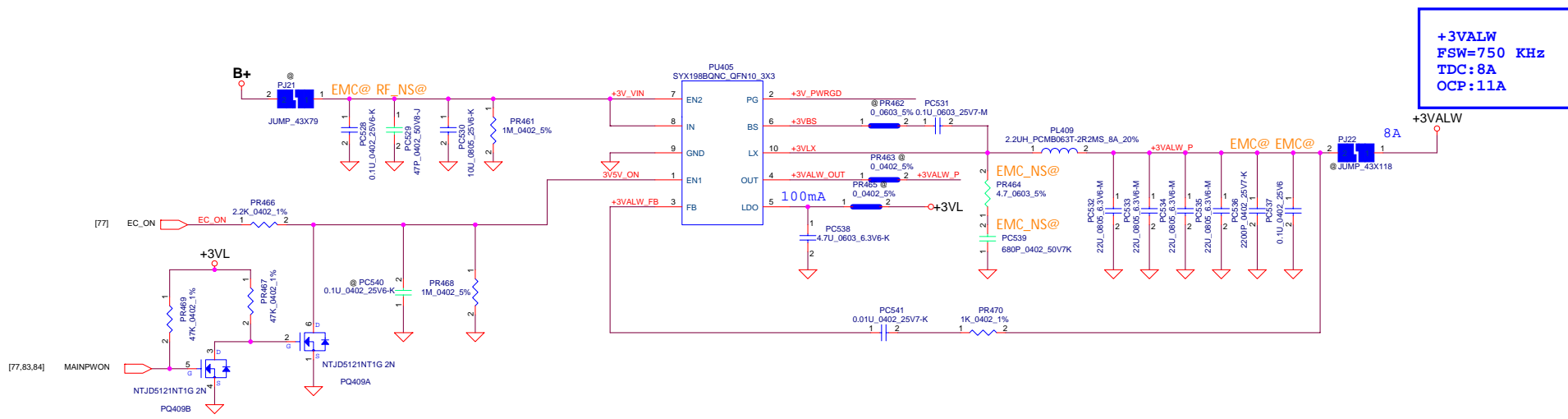
**PRT8 under CPU bottom side :**  
**CPU thermal protection at 92 +/-3 degree C**  
**Recovery at 60 +/-3 degree C**



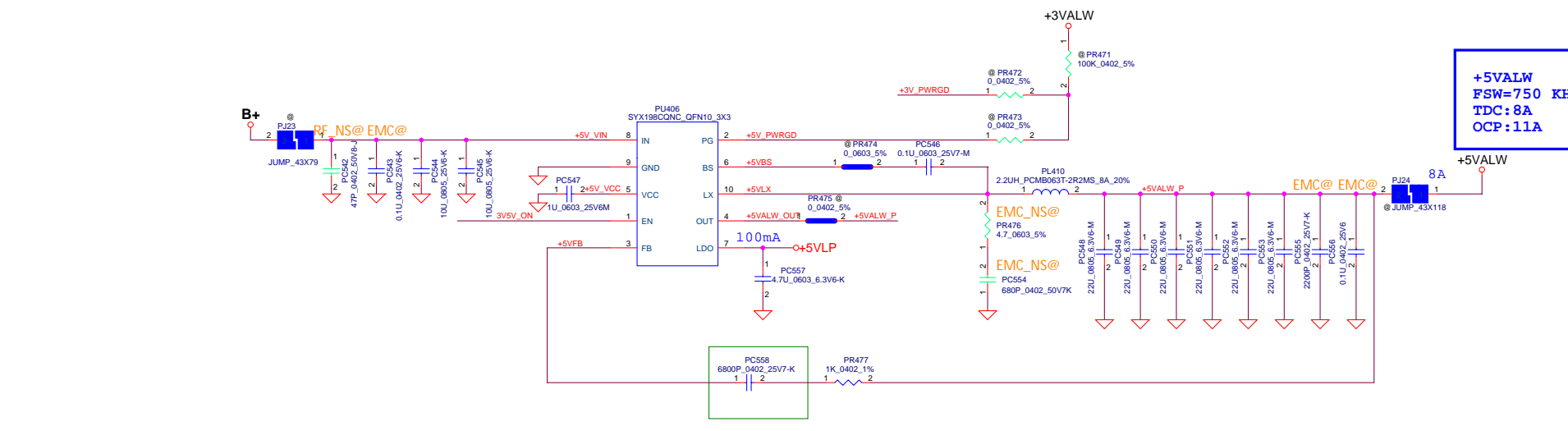
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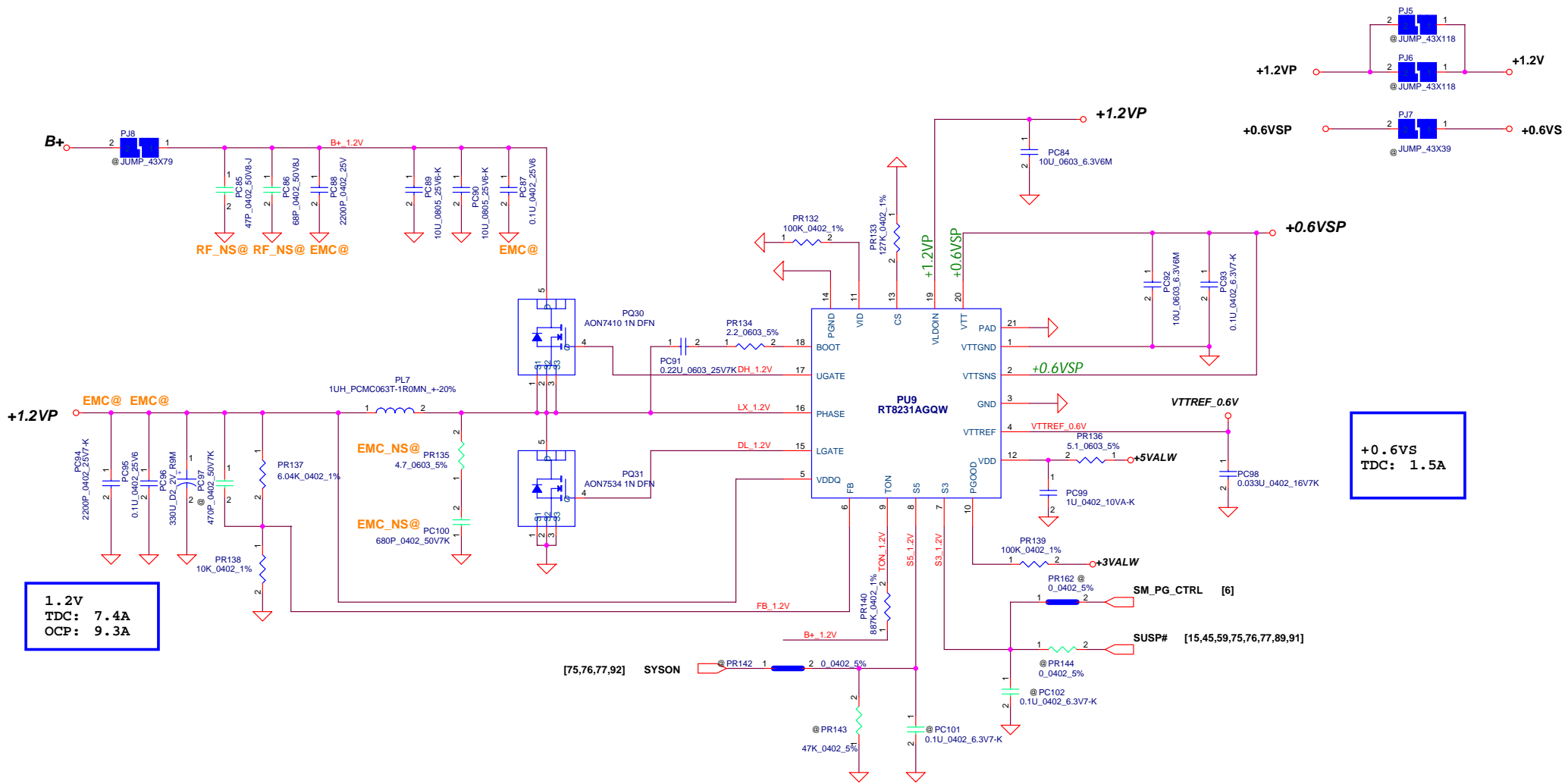
**+3VALW**  
**FSW=750 KHz**  
**TDC:8A**  
**OCF:11A**



**+5VALW**  
**FSW=750 KHz**  
**TDC:8A**  
**OCF:11A**

6800pF soft start 2ms  
 47nF soft start 7ms

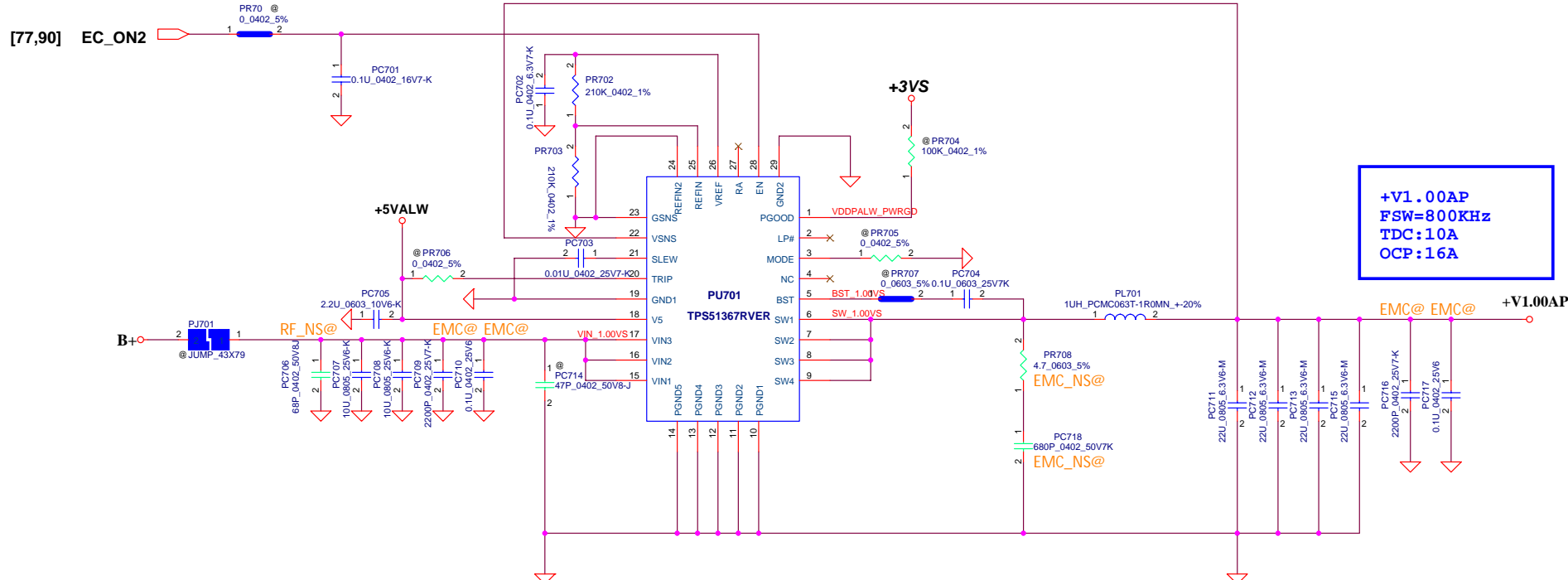
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1.2V  
TDC: 7.4A  
OCP: 9.3A

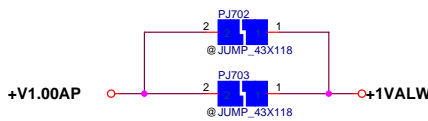
+0.6V  
TDC: 1.5A

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**+V1.00AP**  
**FSW=800KHz**  
**TDC:10A**  
**OCP:16A**

Mode	Frequency
GND	400KHz
Float	800KHz

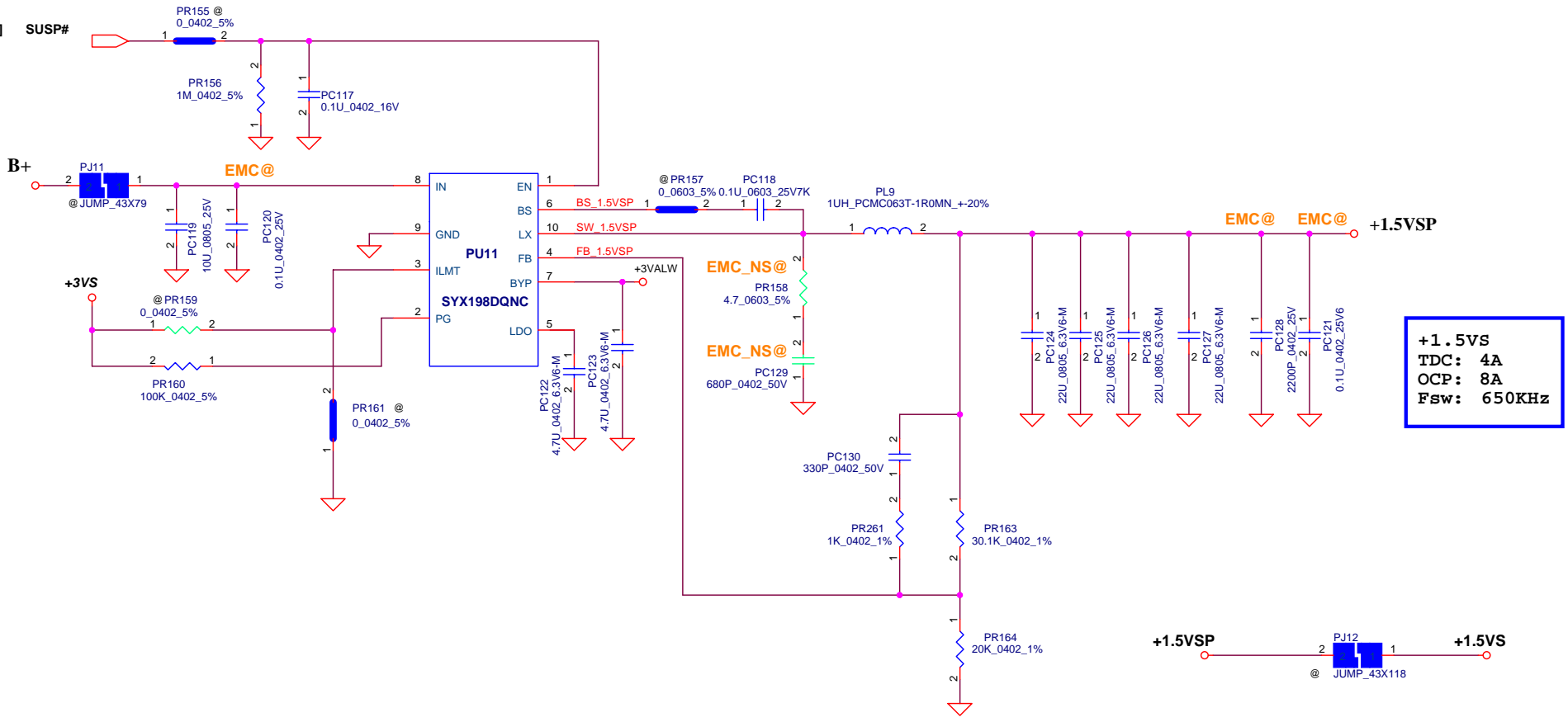


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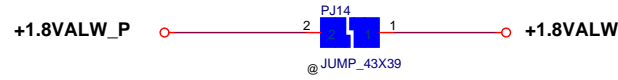
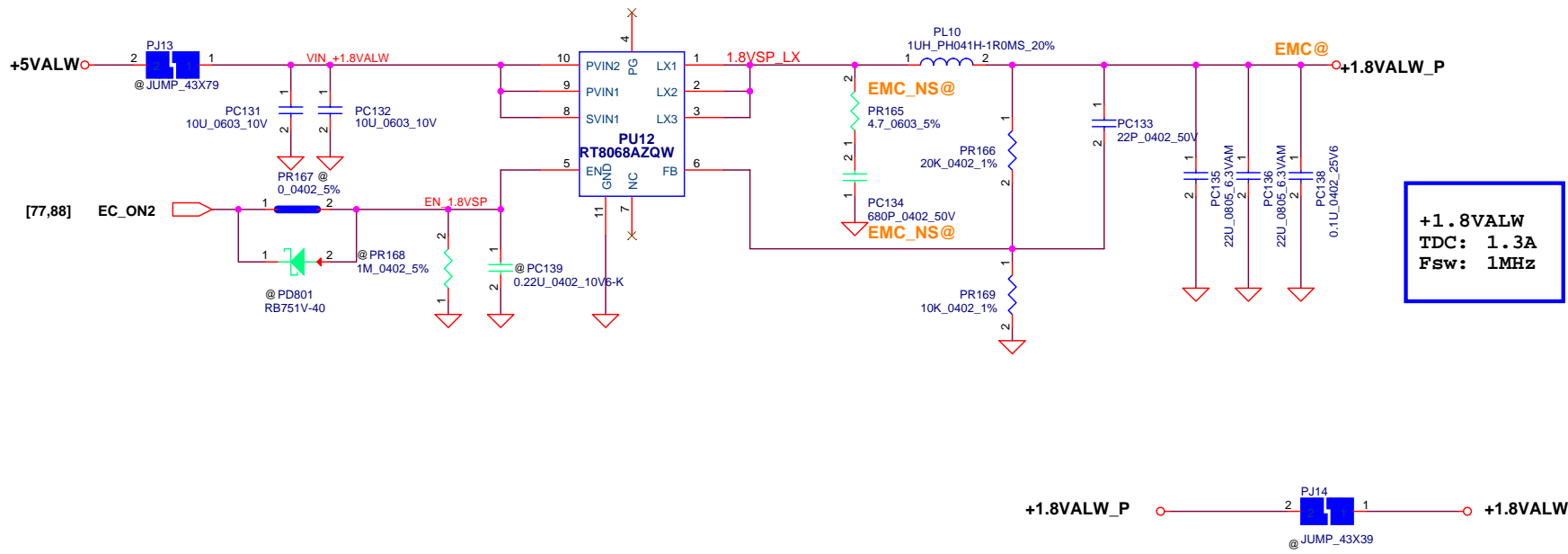


[15,45,59,75,76,77,87,91]



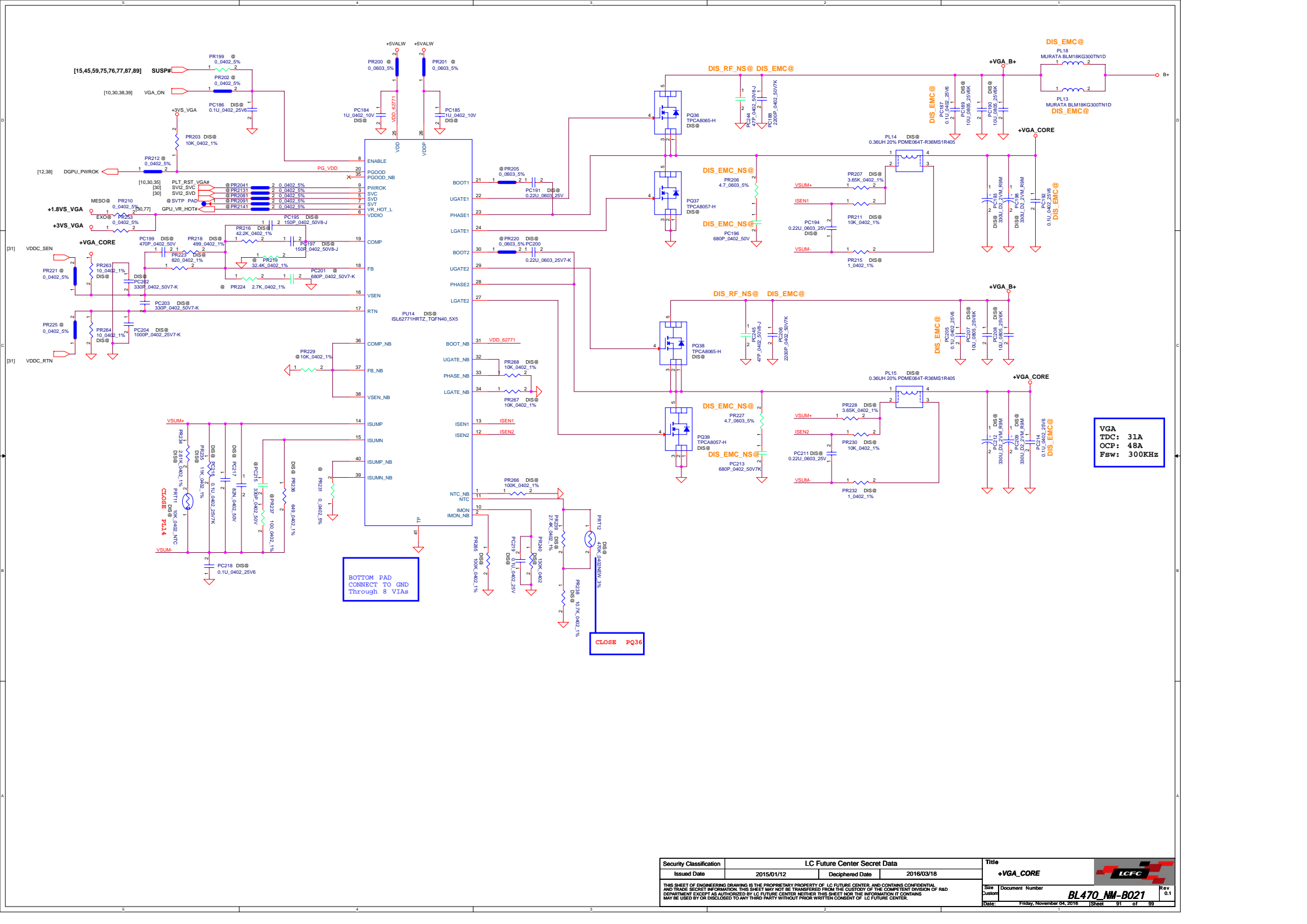
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+1.5VSP		
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VGA  
TDC: 31A  
OCP: 48A  
Fsw: 300KHz

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		2016/03/18

Title	+VGA_CORE
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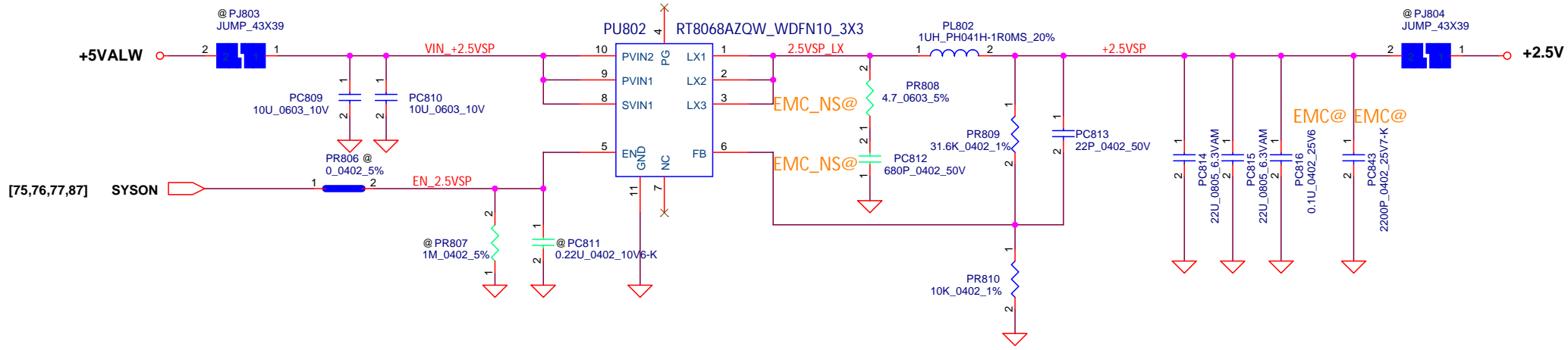
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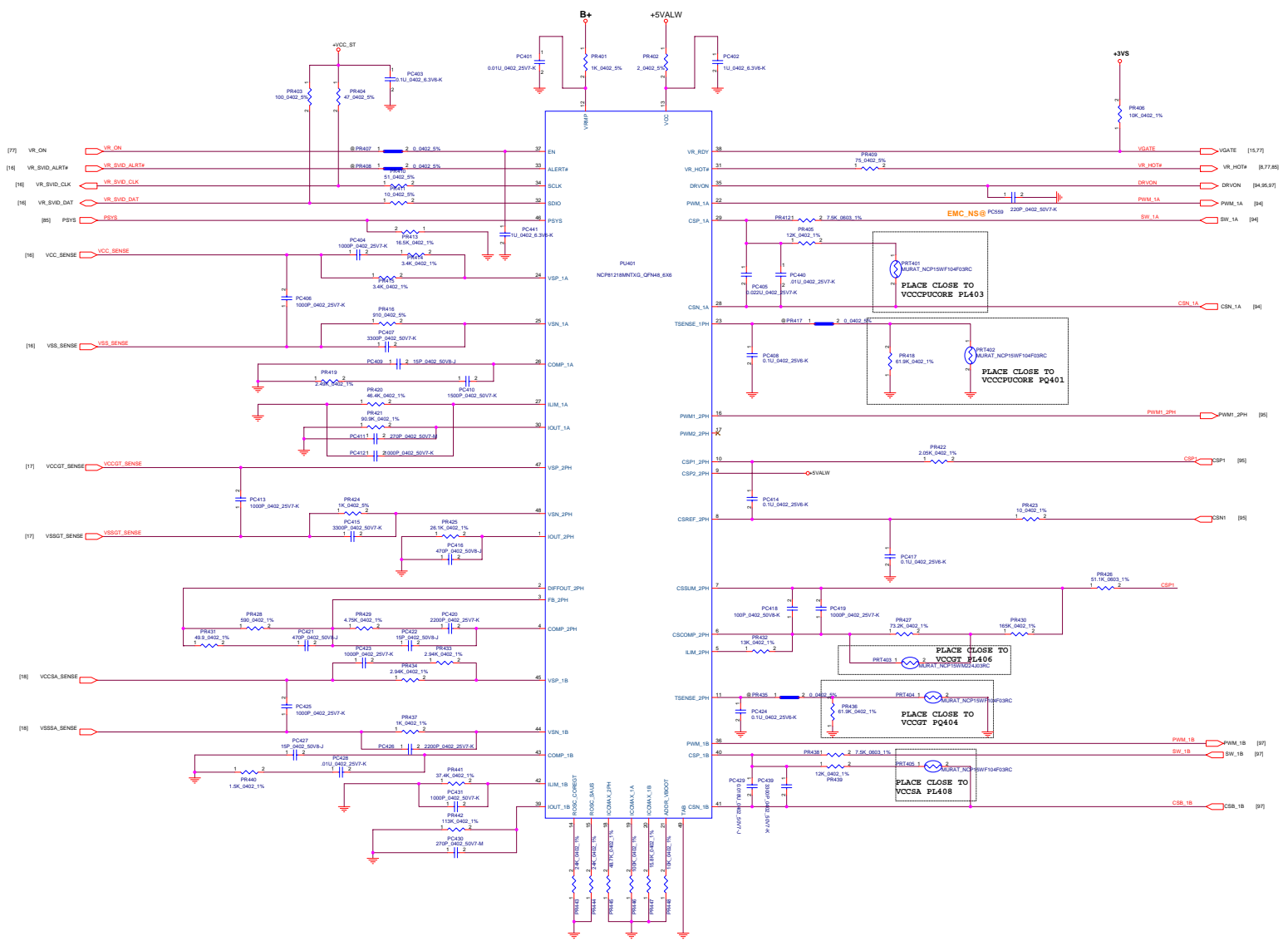
**+2.5V**  
**TDC: 2A**  
**Fsw: 1MHz**



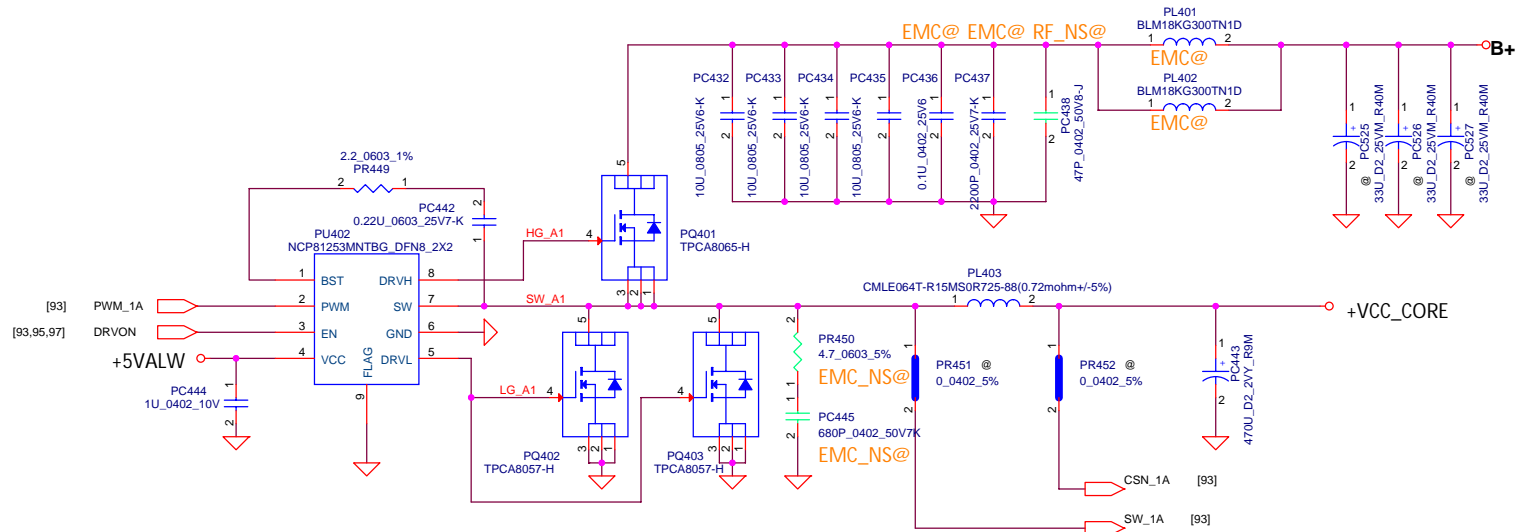
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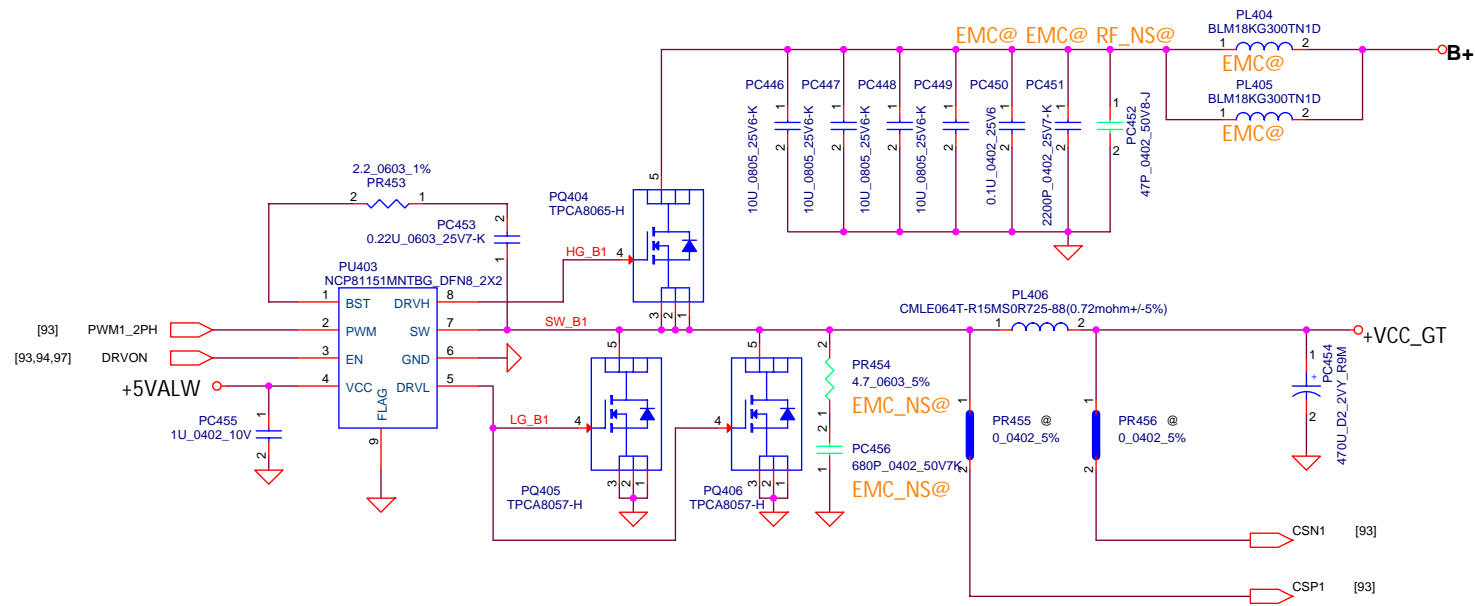


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Issue#	Issue#	Issue#	Issue#
001	001	001	001



+VCC\_CORE  
TDC= 24A  
IccMAX=32A  
OCP = 36A

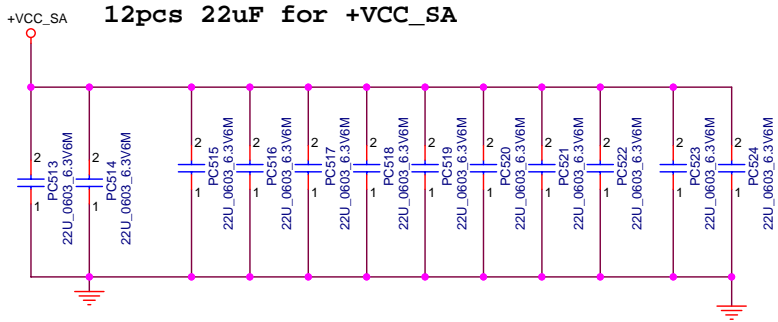
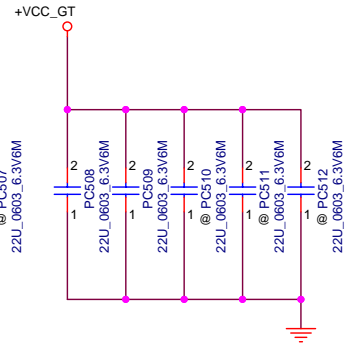
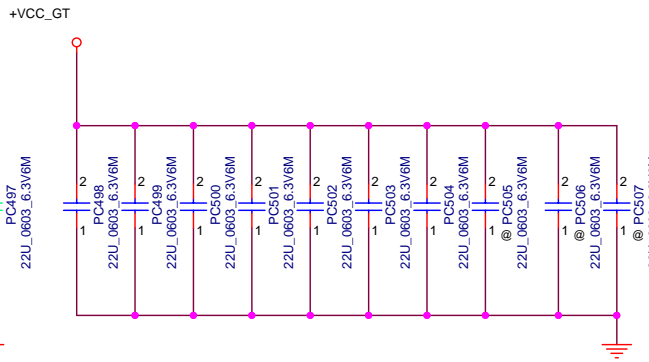
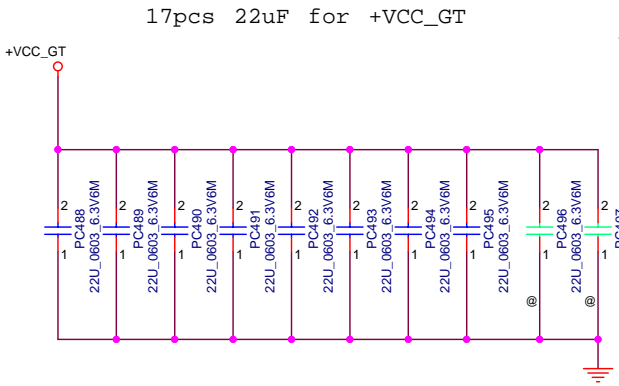
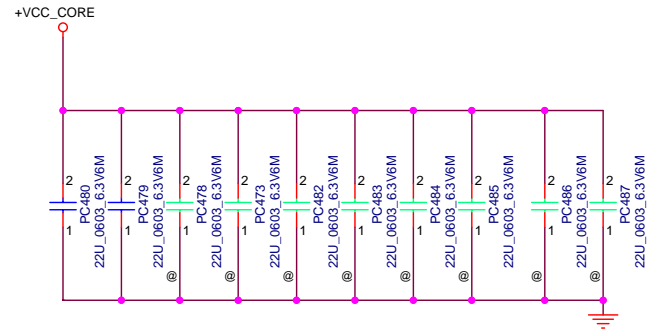
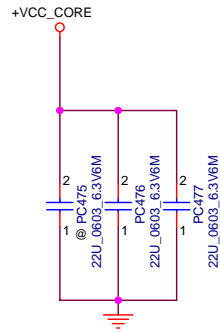
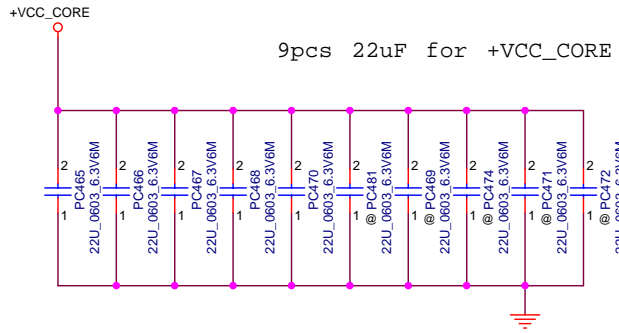
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+VCC\_GT  
 TDC= 18A  
 IccMAX=31A  
 OCP min = 40A

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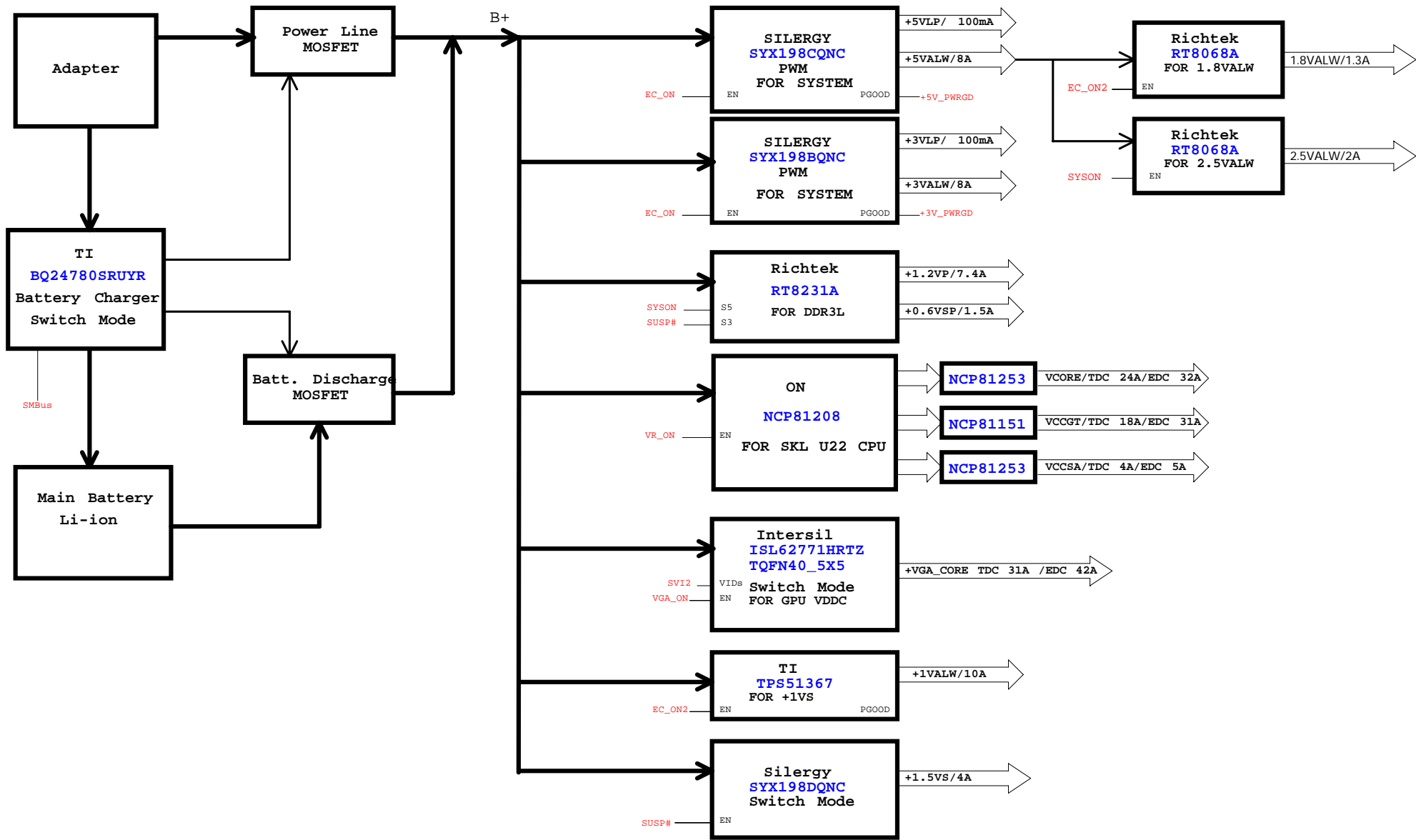



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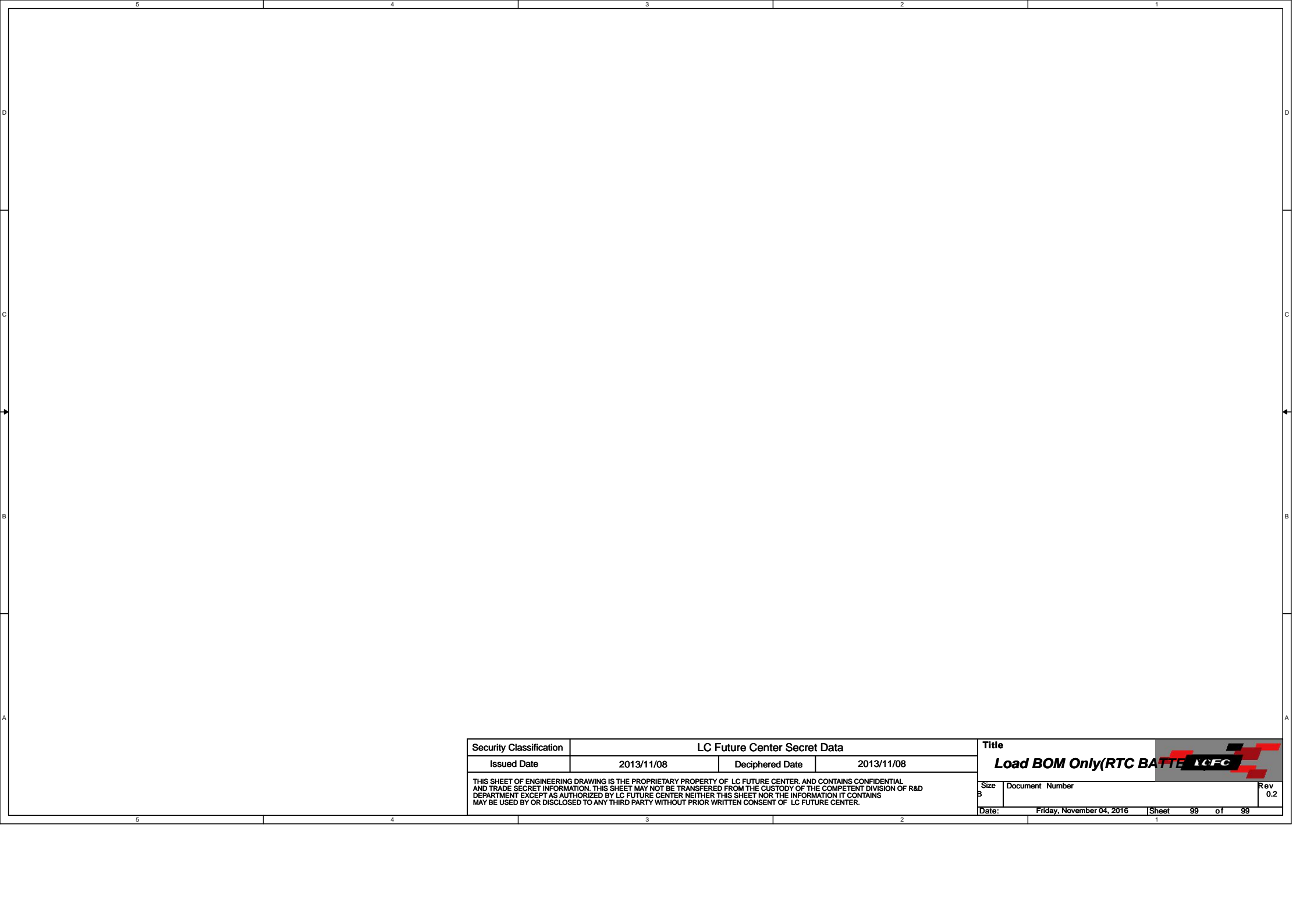
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