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AILZA/B/C (ZX10)

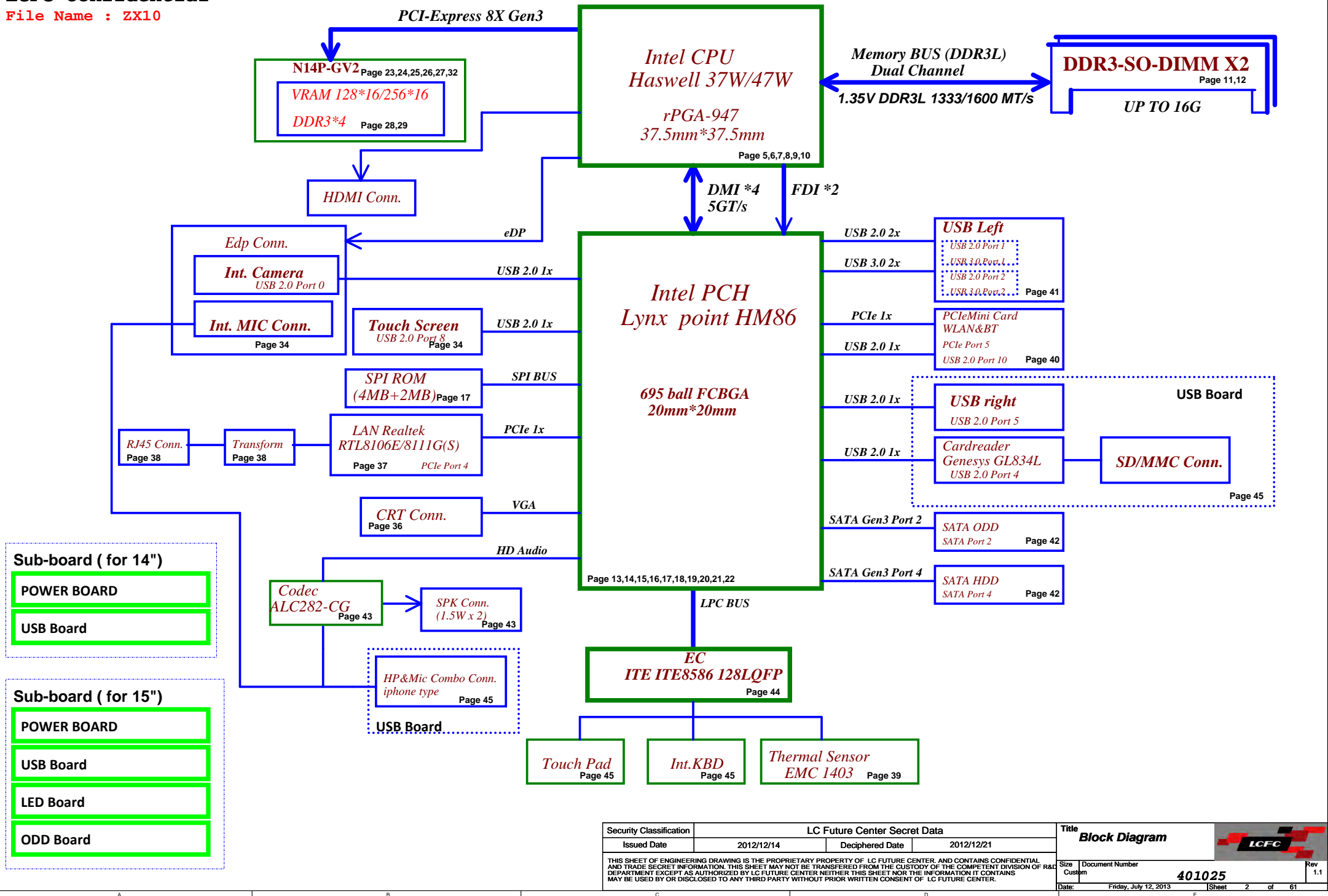
MB MA181 Schematics

**Intel Haswell Processor with DDRIIL + Lynx Point HM86
nVIDIA N14P-GV2**

2012-12-27

REV:1.1

| | | | | | | | |
|---|------------------------------|-----------------|------------|--------|-----------------------|-------|---|
| Security Classification | LC Future Center Secret Data | | | Title | Cover Page | |  |
| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | Size | Document Number | Rev | |
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| | | | | Date: | Friday, July 12, 2013 | Sheet | 1 of 61 |



| | | | | | |
|--|------------|------------------------------|------------|---------------|-----------------------|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | Block Diagram | |
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Voltage Rails (O --> Means ON , X --> Means OFF)

| Power Plane | State | B+ | +3VALW | +5VALW | +3V_PCH | +1.35V | +5VS | +3VS | +1.5VS | +1.05VS | +0.675VS | +CPU_CORE | +VGA_CORE | +3.3VS_VGA | +1.5VS_VGA | +1.05VS_VGA |
|--------------------------------------|-------|----|--------|--------|---------|--------|------|------|--------|---------|----------|-----------|-----------|------------|------------|-------------|
| S0 | | O | O | O | O | O | O | O | O | O | O | O | O | O | O | O |
| S3 | | O | O | O | O | O | O | O | O | O | O | O | O | O | O | X |
| S3 Battery only | | O | O | O | X | O | O | O | O | O | O | O | O | O | O | X |
| S5 S4/AC Only | | O | O | O | O | X | O | O | O | O | O | O | O | O | X | X |
| S5 S4 Battery only | | O | X | X | X | X | O | O | O | O | O | O | O | O | X | X |
| S5 S4 AC & Battery don't exist | | X | X | X | X | X | O | O | O | O | O | O | O | O | X | X |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VAL# | +V | +VS | Clock |
|----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3(Suspend to RAM) | | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4(Suspend to Disk) | | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5(Soft OFF) | | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

USB Port Table

| USB 2.0 | USB 3.0 | Port | 3 External USB Port |
|---------|---------|------|-----------------------|
| EHCI1 | XHCI 1 | 0 | Camera |
| | | 1 | USB Port (Left Side) |
| | | 2 | USB Port (Left Side) |
| | | 3 | |
| | | 4 | Cardreader |
| | | 5 | USB Port (Right Side) |
| | | 6 | |
| EHCI2 | | 7 | |
| | | 8 | TOUCH PANEL |
| | | 9 | |
| | | 10 | Mini Card(WLAN) |
| | | 11 | |
| | | 12 | |
| | | 13 | |

BOM Structure Table

| BOM Structure | BTO Item |
|---------------|--------------------------|
| AOAC@ | AOAC support part |
| OPT@ | External GPU SKU ID part |
| UMA@ | UMA SKU ID part |
| 14@ | For 2410 part |
| 15@ | For 2510 part |
| 8106@ | 8106E LAN part |
| 8111G@ | 8111G LAN Part |
| 8111GS@ | 8111GS LAN Part |
| N14PGV2@ | N14F GV2 stuff |
| GIGA@ | GIGA LAN Part |
| Gastube@ | Gastube Part |
| NOTS@ | No Touch screen part |
| GC6@ | GPU GC6 function part |
| TSE@ | Touch screen part |
| @ | Not stuff |
| ME@ | Connector |
| XDP@ | XDP part |
| 37@ | 37W CPU part |
| 47@ | 47W CPU part |
| H2@ | Hynix 2Gb Vram part |
| M2@ | Micron 2Gb Vram part |
| M4@ | Micron 4Gb Vram part |
| S2@ | Samsung 2Gb Vram part |
| S4@ | Samsung 4Gb Vram part |
| M1GB@ | Micron 1GB Vram BOM |
| M2GB@ | Micron 2GB Vram BOM |
| S1GB@ | samsung 1GB Vram BOM |
| S2GB@ | samsung 2GB Vram BOM |
| H1GB@ | hynix 1GB Vram BOM |

SMBUS Control Table

| | SOURCE | VGA | BATT | IT8586E | SODIMM | WLAN | WIMAX | Thermal Sensor | PCH | TP Module | Charger | XDP |
|-------------|---------|-----|------|---------|--------|------|-------|----------------|-----|-----------|---------|-----|
| EC_SMB_CK1 | IT8586E | | | | | | | | | | | |
| EC_SMB_DA1 | +3VALW | X | V | V | X | X | X | X | X | X | V | X |
| EC_SMB_CK2 | IT8586E | | | | | | | | | | | |
| EC_SMB_DA2 | +3VS | V | X | V | X | X | V | V | V | X | X | X |
| PCH_SMBCLK | PCH | X | X | X | V | V | X | V | V | V | X | V |
| PCH_SMBDATA | +3V_PCH | X | X | X | V | V | X | V | V | V | X | V |

PCIe PORT LIST

| Port | Device |
|------|--------|
| 1 | |
| 2 | |
| 3 | |
| 4 | LAN |
| 5 | WLAN |
| 6 | |
| 7 | |
| 8 | |

| | Fixed Signals | | | | Muxed Signals | | | | Fixed Signals | | | | Muxed Signals | | | | Fixed Signals | | | |
|-----------|---------------|--------|--------|--------|---------------|-------------|--------|--------|---------------|--------|--------|--------|-------------------|-------------------|--------------|--------------|---------------|--------------|--|--|
| HM86 | USB3 1 | USB3 2 | NA | NA | PCIE 1 (00) | PCIE 2 (00) | PCIE 3 | PCIE 4 | PCIE 5 | PCIE 6 | PCIE 7 | PCIE 8 | SATA 6Gb/s 4 (1b) | SATA 6Gb/s 5 (1b) | SATA 3Gb/s 0 | NA | SATA 3Gb/s 2 | NA | | |
| | | | | | USB3 3 (01) | USB3 4 (01) | | | | | | | PCIE 1 (0b) | PCIE 2 (0b) | | | | | | |
| HM87 QM87 | USB3 1 | USB3 2 | USB3 5 | USB3 6 | PCIE 1 | PCIE 2 | PCIE 3 | PCIE 4 | PCIE 5 | PCIE 6 | PCIE 7 | PCIE 8 | SATA 6Gb/s 4 | SATA 6Gb/s 5 | SATA 3Gb/s 0 | SATA 3Gb/s 1 | SATA 3Gb/s 2 | SATA 3Gb/s 3 | | |
| | | | | | USB3 4 | USB3 5 | | | | | | | PCIE 2 | PCIE 3 | | | | | | |

Soft Strap: (USB3P4_PCIEP2_MODE)
 00: PCIe Lane 2 is statically assigned to PCIe Express (or GbE)
 01: PCIe Lane 2 is statically assigned to USB3 Port 4

Soft Strap: (USB3P3_PCIEP1_MODE)
 00: PCIe Lane 1 is statically assigned to PCIe Express (or GbE)
 01: PCIe Lane 1 is statically assigned to USB3 Port 3

| Config | GPIO16,49 |
|-------------|-----------|
| SATA4,SATA5 | 11 |
| PCIE1,PCIE2 | 00 |

EC SM Bus1 address

EC SM Bus2 address

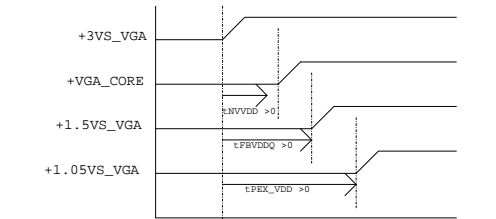
PCH SM Bus address

| Device | Address | Device | Address | Device | Address |
|---------------|-------------|--------------------------|------------|-----------|---|
| Smart Battery | 0001 011X b | Thermal Sensor EMC1403-2 | 1001_101xb | DDR DIMMA | 0xA0 |
| Charger | 0001 0010 b | VGA | 0x9E | DDR DIMMB | 0xA2 |
| | | PCH | 0x96 | Wlan | Rsvd |
| | | | | TP | 0x2C for Synopsys 0x15 for ELAN vendor |

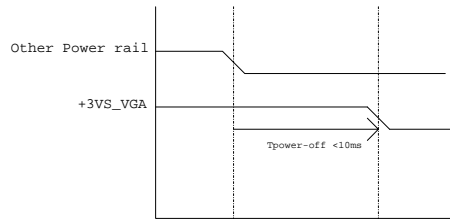
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VGA and GDDR3 Voltage Rails (N14P GPIO)

| GPIO | I/O | ACTIVE | Function Description |
|--------|-----|--------|---------------------------------------|
| GPIO0 | IN | - | FB Clamp monitor |
| GPIO1 | OUT | N/A | |
| GPIO2 | OUT | N/A | |
| GPIO3 | OUT | N/A | |
| GPIO4 | OUT | N/A | |
| GPIO5 | | N/A | |
| GPIO6 | OUT | - | Active low FB Clamp toggle request |
| GPIO7 | OUT | N/A | |
| GPIO8 | I/O | - | Thermal Catastrophic Over Temperature |
| GPIO9 | I/O | N/A | 2.2K Pull-up |
| GPIO10 | OUT | N/A | |
| GPIO11 | OUT | - | GPU Core VDD PWM control signal |
| GPIO12 | IN | | AC Power Detect Input (10K pull High) |
| GPIO13 | OUT | - | Phase Shedding |
| GPIO14 | IN | N/A | |
| GPIO15 | IN | N/A | |
| GPIO16 | OUT | N/A | |
| GPIO17 | IN | N/A | |
| GPIO18 | IN | N/A | |
| GPIO19 | IN | N/A | |



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (DDR3)


| Products | GPU (4) | Mem (1.5) | NVCLK /MCLK | NVVDD | | | FBVDD (1.5V) | | FBVDDQ (GPU+Mem) (1.5V) | | PCI Express (1.05V) (6) | | I/O and PLLVDD (1.8V) | | I/O and PLLVDD (1.05V) | | Other (3.3V) | |
|-------------------------|---------|-----------|-------------|-------|-----|-----|--------------|------|-------------------------|-----|-------------------------|-----|-----------------------|-----|------------------------|-----|--------------|-----|
| | (W) | (W) | (MHz) | (V) | (A) | (W) | (A) | (W) | (A) | (W) | (A) | (W) | (mA) | (W) | (mA) | (W) | (mA) | (W) |
| N14P 64bit 1GB/2GB DDR3 | 25W | TBD | 1000MHz | TBD | 32 | TBD | 1.7 | 2.55 | TBD | TBD | 1.98 | 2.1 | TBD | TBD | TBD | TBD | TBD | TBD |

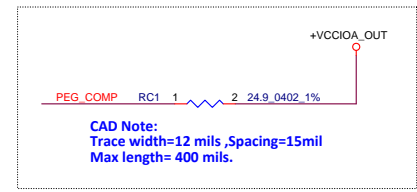
| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|------------------------|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VS_VGA | PCI_DEVID[4] | SUB_VENDOR | PCI_DEVID[5] | PEX_PLL_EN_TERM |
| ROM_SI | +3VS_VGA | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_VGA | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_VGA | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | +3VS_VGA | 3GIO_PAD_CFG_ADR[3] | 3GIO_PAD_CFG_ADR[2] | 3GIO_PAD_CFG_ADR[1] | 3GIO_PAD_CFG_ADR[0] |
| STRAP2 | +3VS_VGA | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | +3VS_VGA | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | +3VS_VGA | RESERVED | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V |

| GPU | Device ID | SMB_ALT_ADDR (ROM_SO Bit 1) | setting | I2C slave address ID |
|----------|-----------|-----------------------------|---------|----------------------|
| N14P-GV2 | 0x1292 | | 0 | 0x9E (Default) |
| | | | 1 | 0x9C |

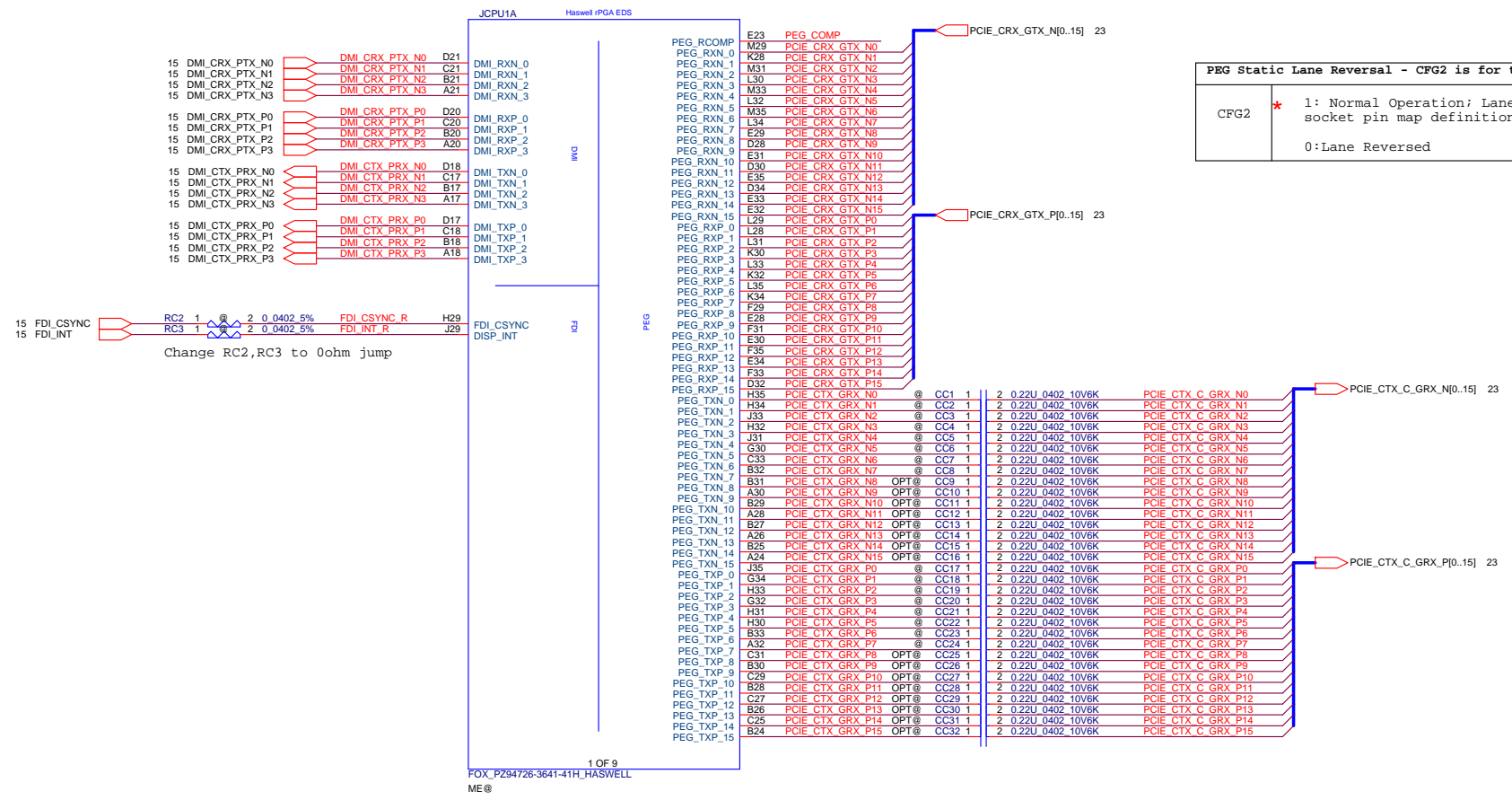
| GPU | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|----------|--------|----------|----------|----------|----------|--------|----------|----------|
| N14P-GV2 | TBD | PU 4.99K | PU 4.99K | PU 45.3K | PD 45.3K | PD 15K | PD 4.99K | PU 45.3K |

| GPU | N14P_GV2 | | |
|-------------------------|----------------------|----------|--|
| FB Memory (DDR3) | | | |
| Samsung 1GHz | K4W2G1646E-BC1A | 0x7 | |
| | 128M x 16 | PD 45.3K | |
| Micron 1GMHz | MT41J128M16JT-093G:K | 0x5 | |
| | 128M x 16 | PD 30.1K | |
| Hynix 1GMHz | H5TC2G63PFR-11C | 0x4 | |
| | 128M x 16 | PD 24.9K | |
| Samsung 900MHz | K4W4G1646B-HC11 | 0x3 | |
| | 256M x 16 | PD 20K | |
| Micron 900MHz | MT41K256M16HA-107G:E | 0x1 | |
| | 256M x 16 | PD 10K | |

| | | | | |
|---|------------------------------|-----------------|-----------------------|---|
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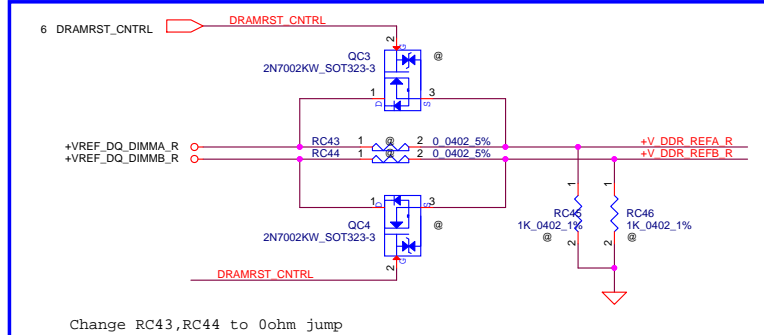
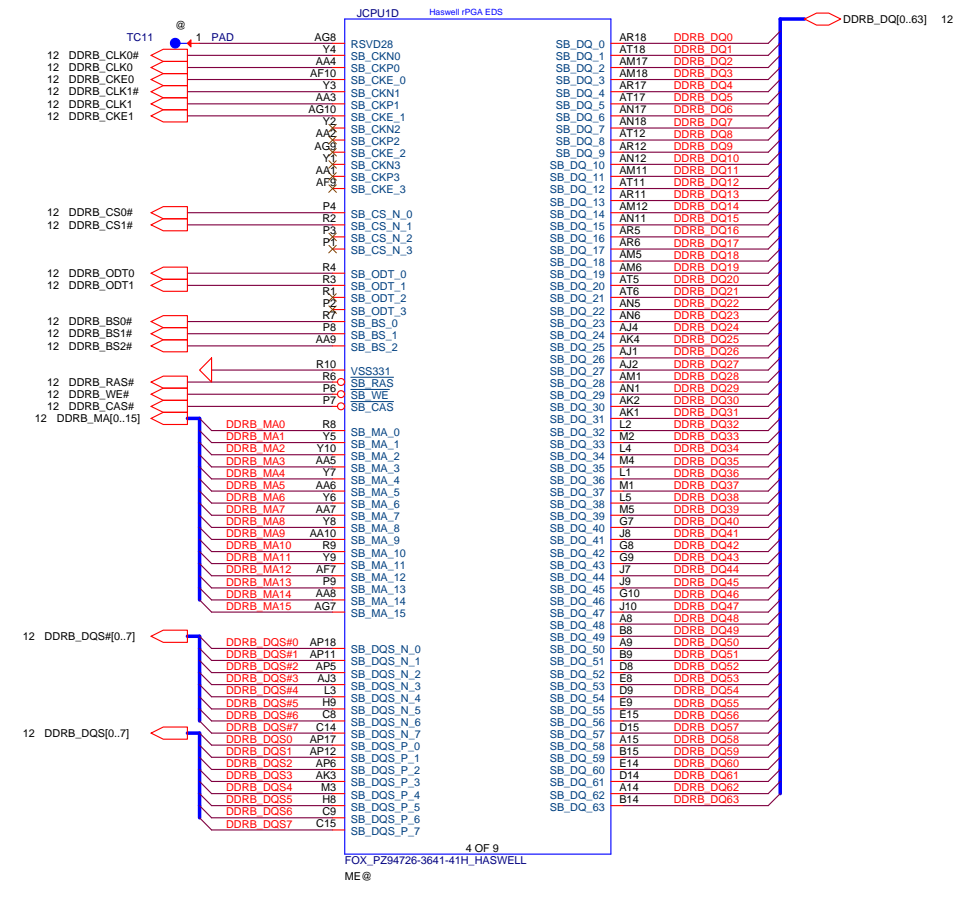
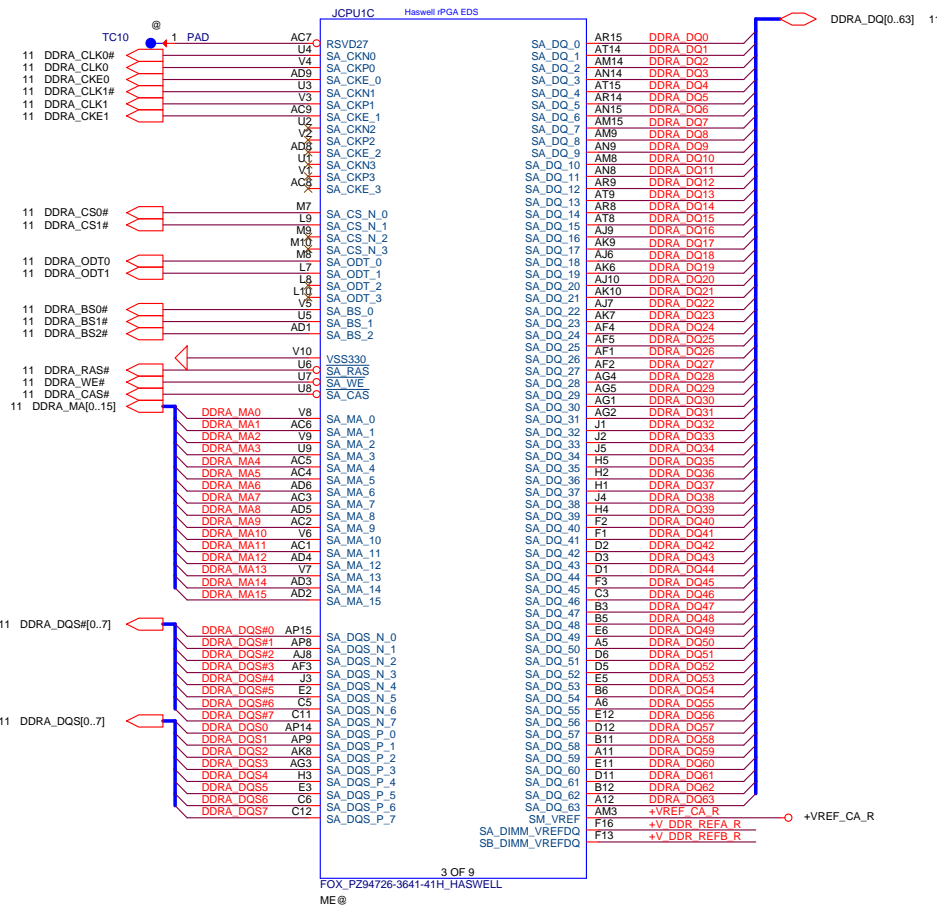
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | * 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed |



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| Title | Revision |
|-------------------------|-----------------------|
| CPU (1/7) DMI, FDI, PEG | 1.1 |
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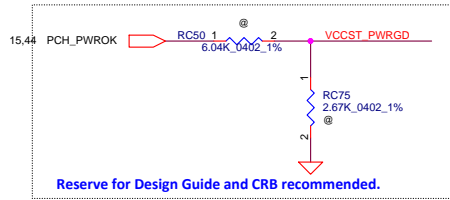
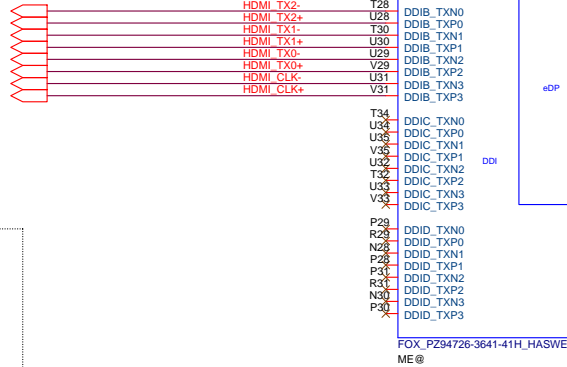




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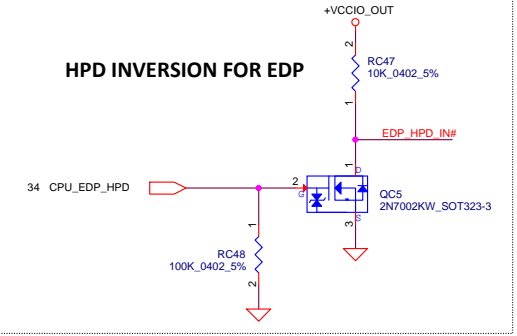
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

35 HDMI_TX2-
35 HDMI_TX2+
35 HDMI_TX1-
35 HDMI_TX1+
35 HDMI_TX0-
35 HDMI_TX0+
35 HDMI_CLK-
35 HDMI_CLK+

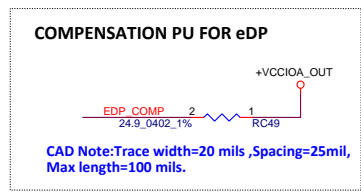


Reserve for Design Guide and CRB recommended.

HPD INVERSION FOR EDP

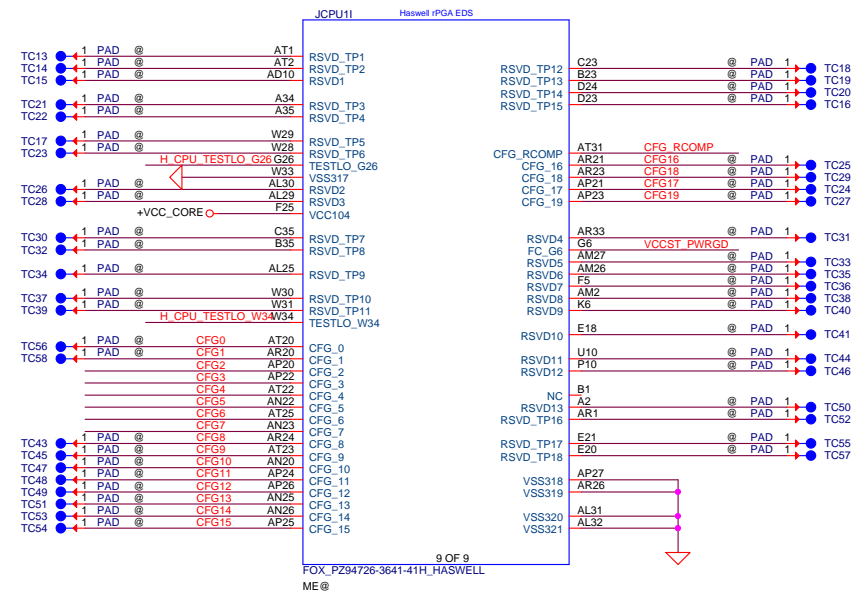


COMPENSATION PU FOR eDP

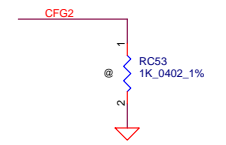


CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.

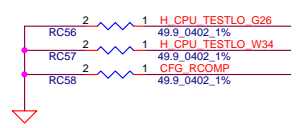
CFG STRAPS for CPU



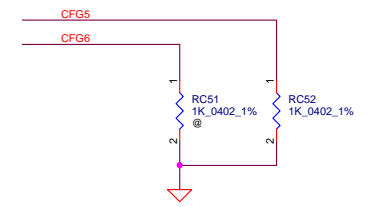
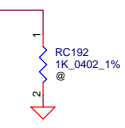
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | <ul style="list-style-type: none"> * 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed |



| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | <ul style="list-style-type: none"> 1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |



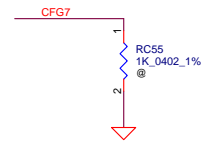
| PHYSICAL_DEBUG_ENABLED (DFX PRIVACY) | |
|--------------------------------------|--|
| CFG3 | <ul style="list-style-type: none"> 0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR * 1 : DISABLED |

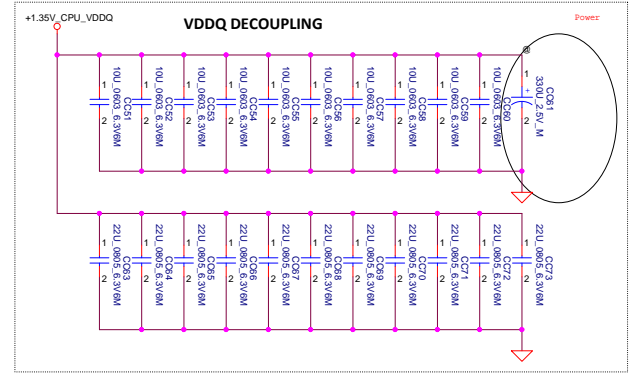
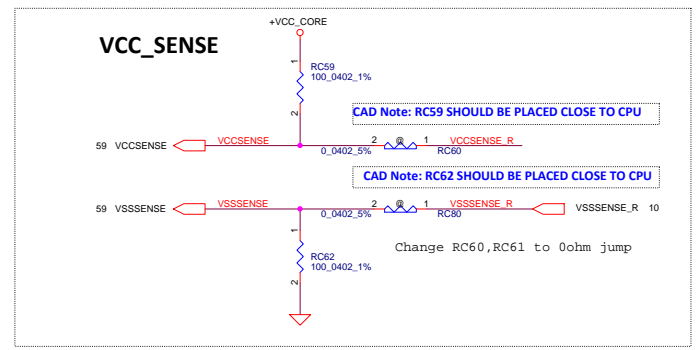
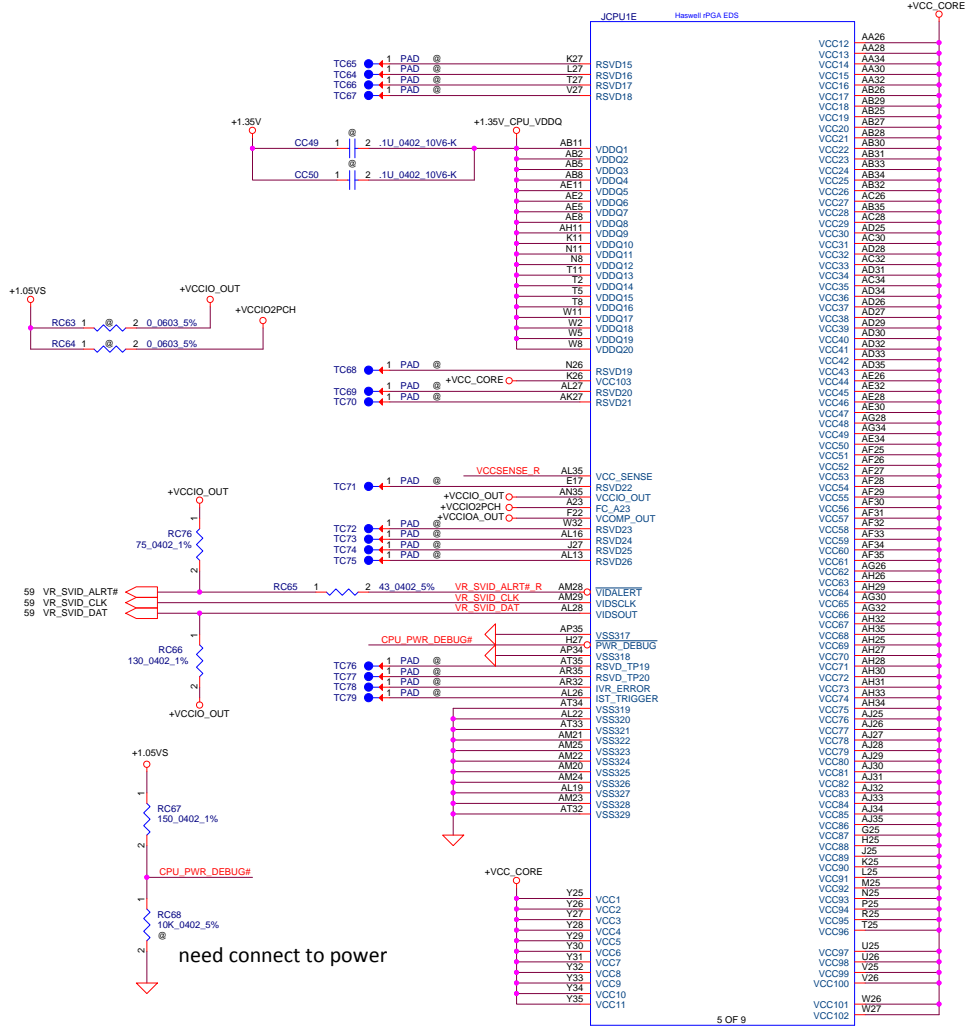


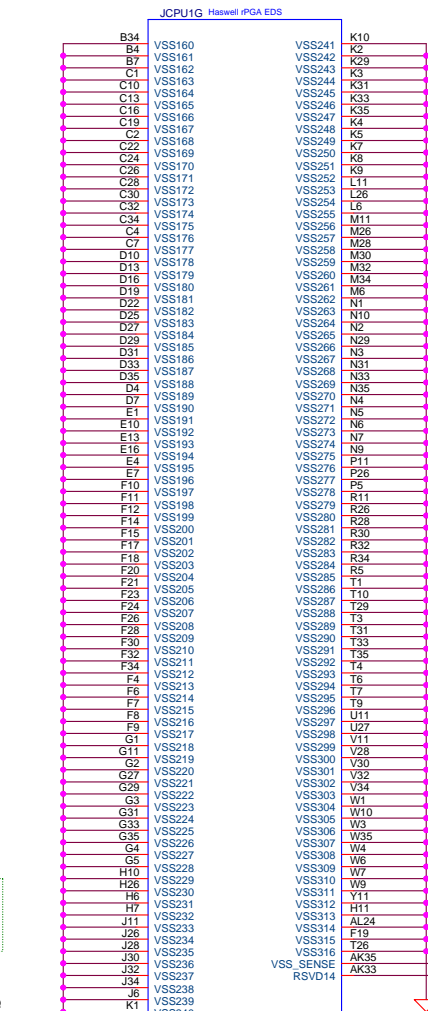
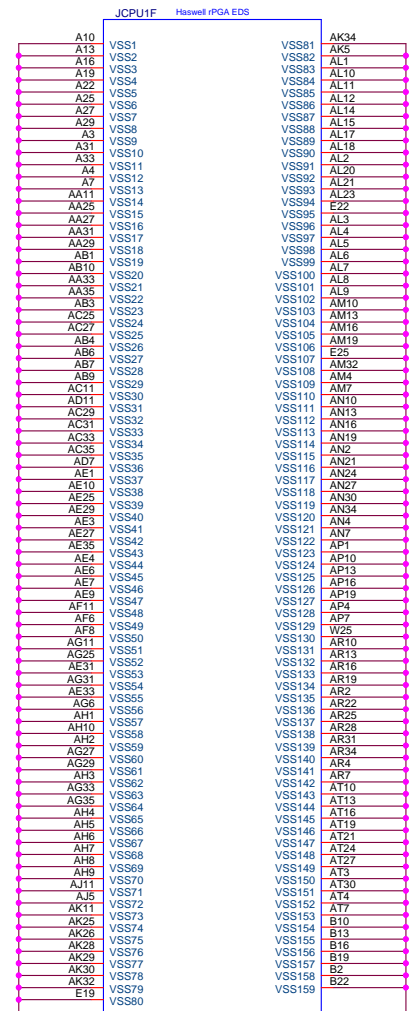
| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | <ul style="list-style-type: none"> 11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

| PEG DEFER TRAINING | |
|--------------------|--|
| CFG7 | <ul style="list-style-type: none"> * 1: (Default) PEG Train immediately following xxRESET de assertion 0: PEG Wait for BIOS for training |

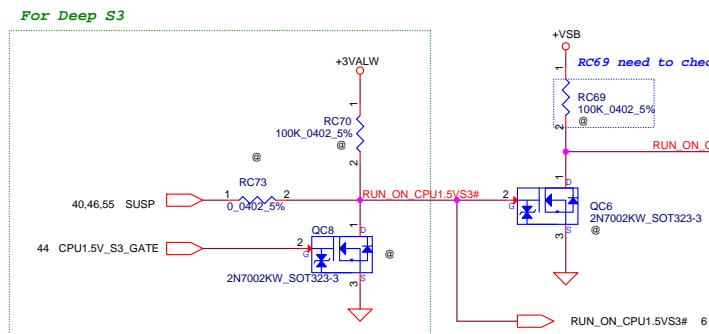
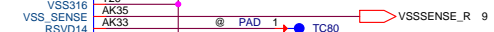
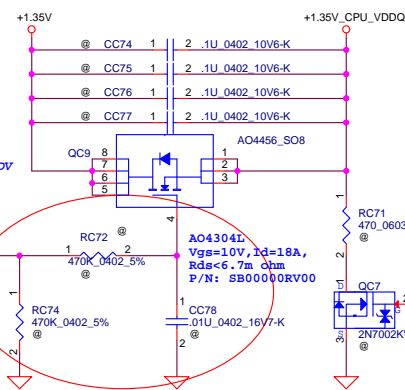
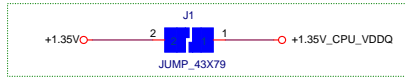
Need confirm with Intel if this reserved circuit can be deleted.







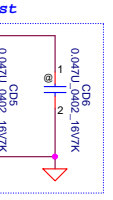
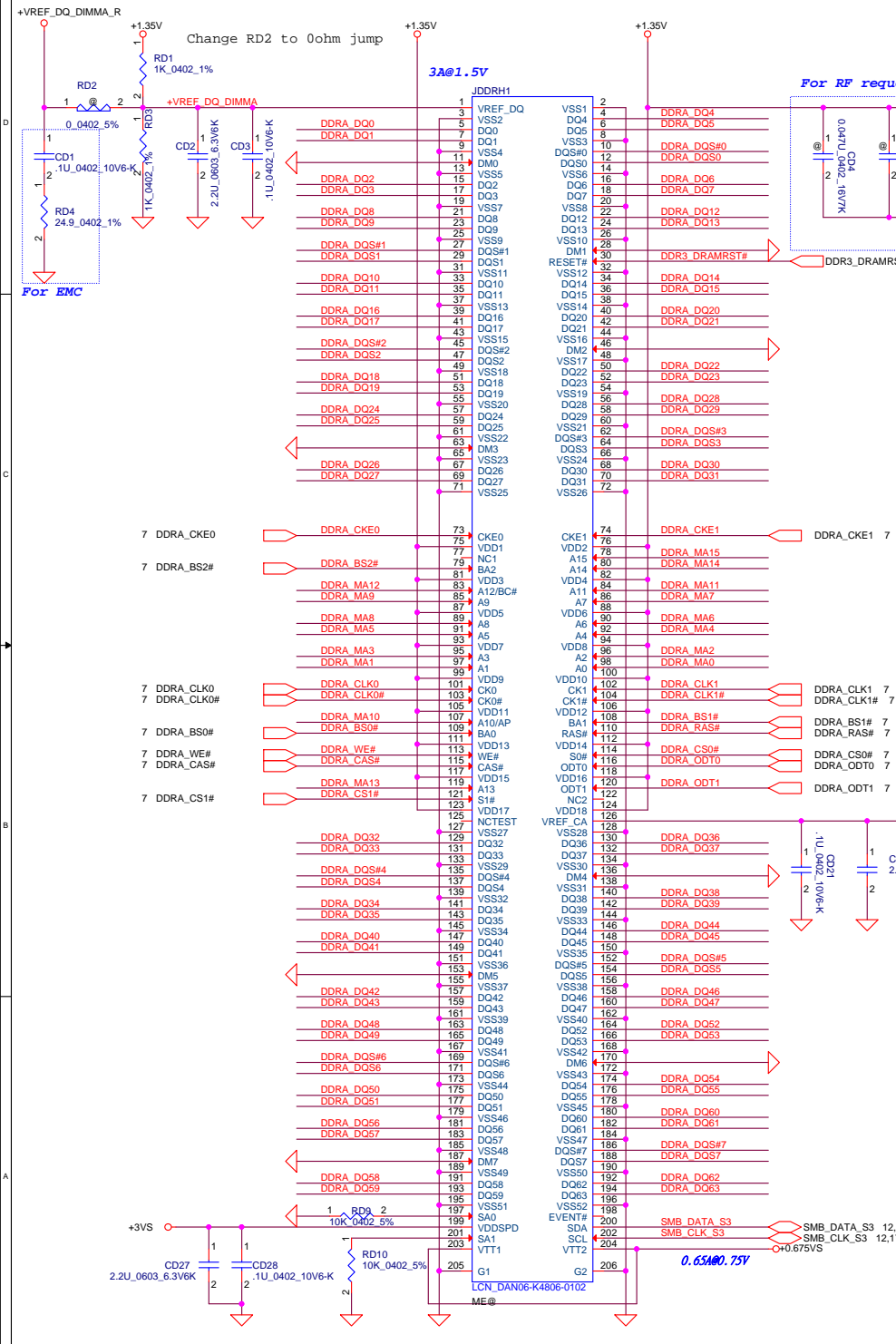
+1.35V_CPU_VDDQ



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| Title | | LCFC | |
|----------------------|-----------------------|-------|-----------------|
| CPU (6/7) PWR | | Size | Document Number |
| Customer | 401025 | Rev | 1.1 |
| Date: | Friday, July 12, 2013 | Sheet | 10 of 61 |

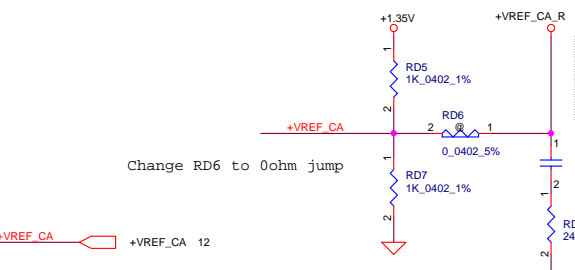
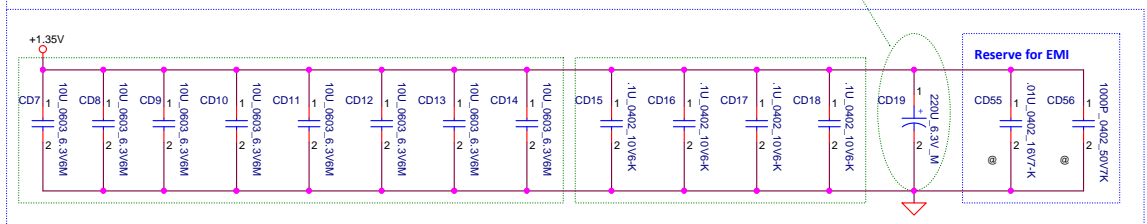
DDR3 SO-DIMM A



- DDR3 DQ[0..63] 7
- DDR3 DQS[0..7] 7
- DDR3 DQS#[0..7] 7
- DDR3 MA[0..15] 7

Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF00002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

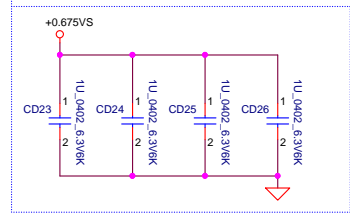


Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

DDR_A_DM[0:7] connect to GND

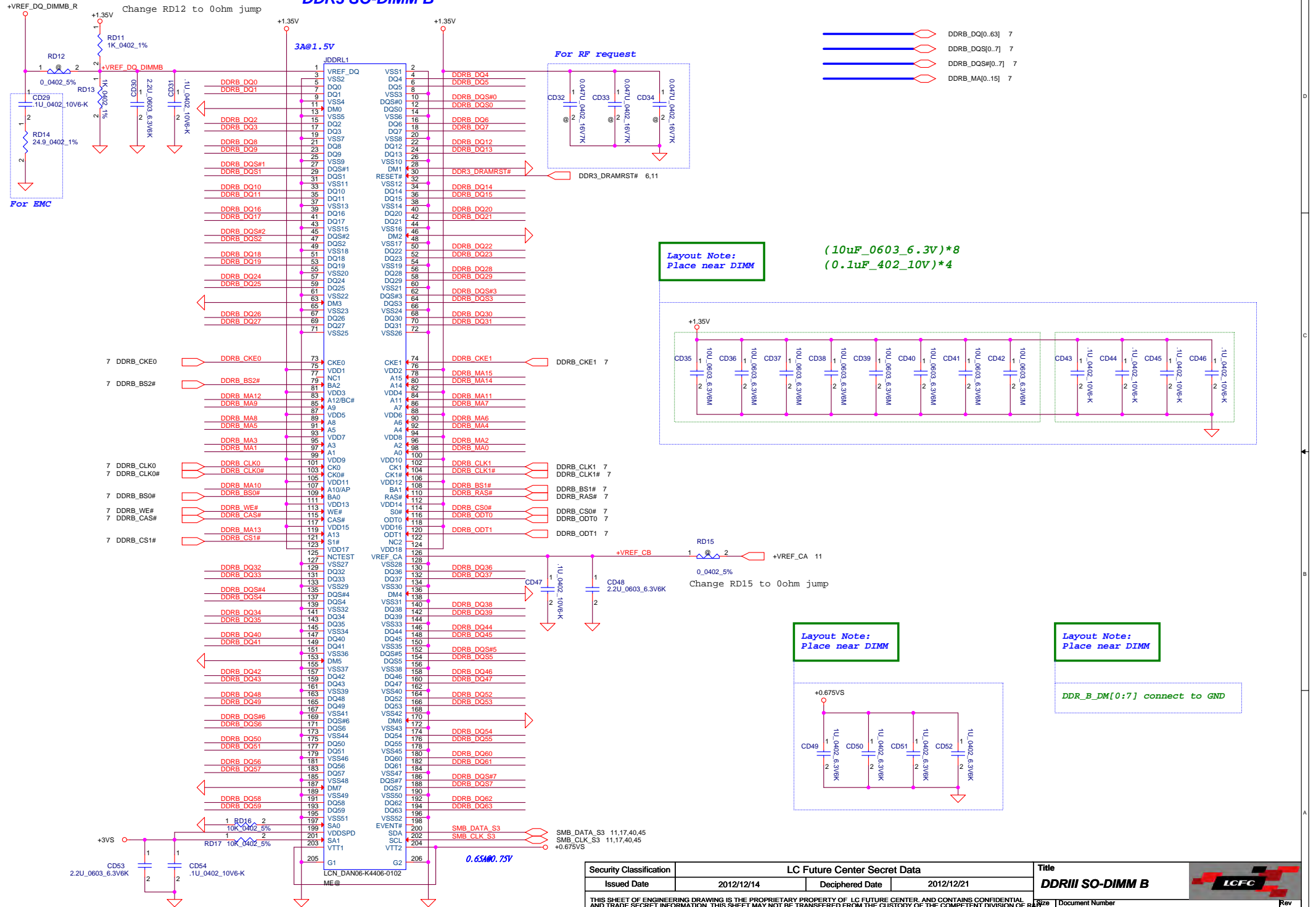


0.65A@0.75V

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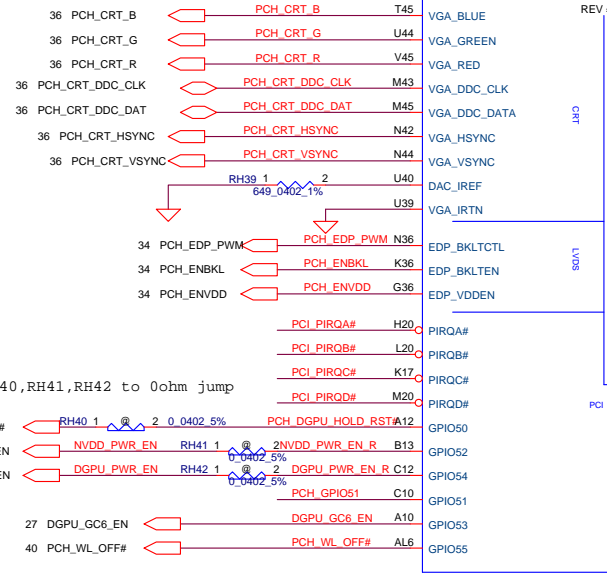
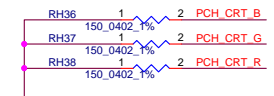
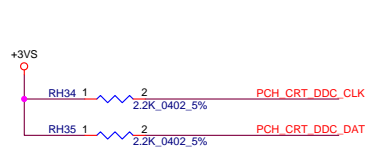
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|----------------|-----------------------|--------|----------|
| DDR3 SO-DIMM A | | LCFC | |
| Size | Document Number | 401025 | Rev |
| Custom | | | 1.1 |
| Date: | Friday, July 12, 2013 | Sheet | 11 of 61 |

DDR3 SO-DIMM B

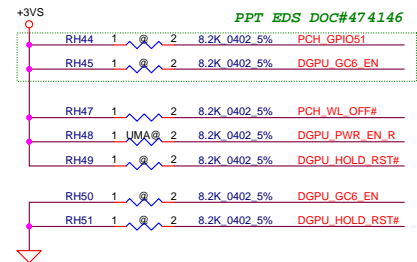


| LC Future Center Secret Data | | | |
|--|------------|-----------------|------------|
| Security Classification | 2012/12/14 | Deciphered Date | 2012/12/21 |
| Issued Date | 2012/12/14 | | |
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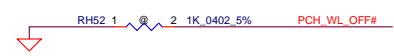
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|----------------|-----------------|--------|-----------------------|
| DDR3 SO-DIMM B | | 401025 | |
| Size | Document Number | Rev | 1.1 |
| Customer | 401025 | Date: | Friday, July 12, 2013 |
| Sheet 12 of 61 | | | |



Change RH40, RH41, RH42 to 0ohm jump



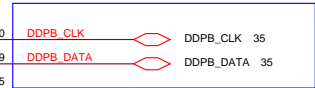
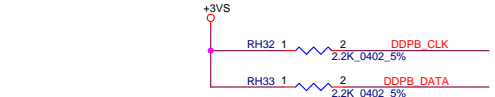
GPIO53 The signal has a weak internal pull-up.
 H DMI is in DC-coupling mode (desktop, mobile or server/workstation).
 L DMI is in AC-coupling mode (server/workstation only, not meant for desktop/mobile).



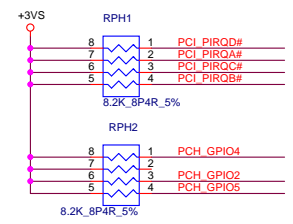
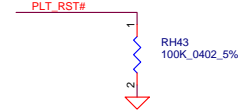
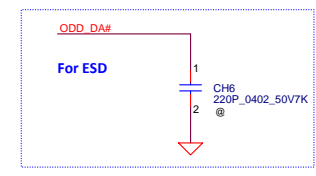
GPIO55 The signal has a weak internal pull-up.
 H Disable ' Top-Block Swap ' mode.
 L Enable ' Top-Block Swap ' mode.

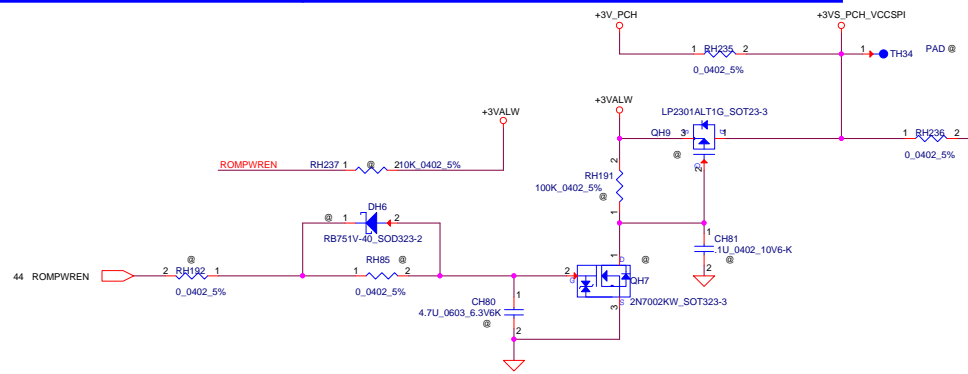
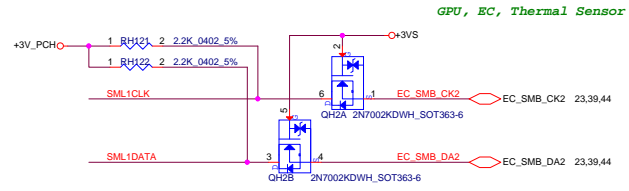
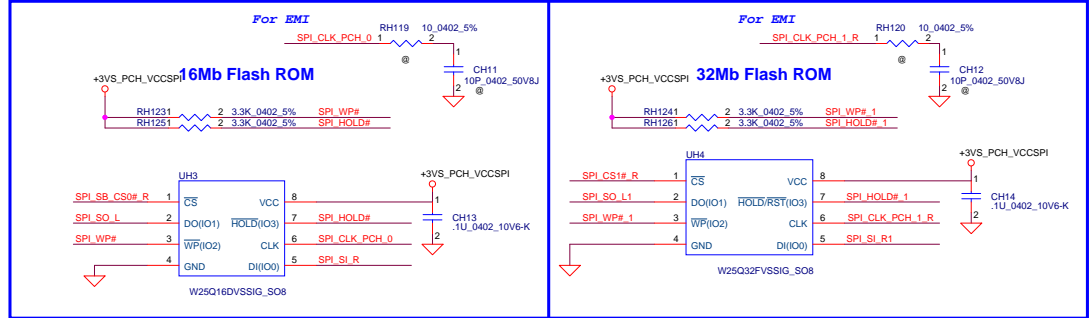
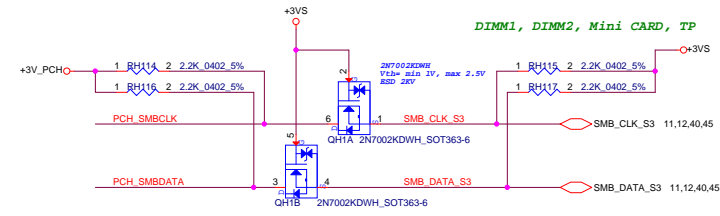
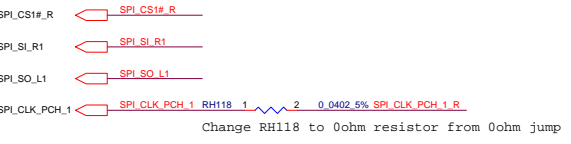
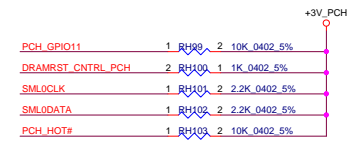
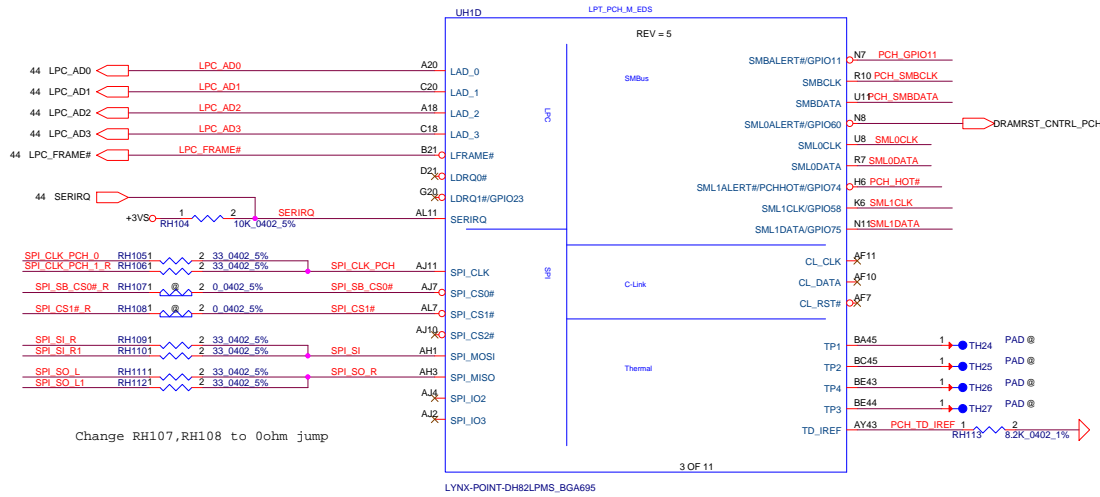
Boot BIOS Strap

| BBS_BIT1 (GPIO51) | SATA_SLPD (BBS_BIT0) | Boot BIOS Location |
|-------------------|----------------------|--------------------|
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

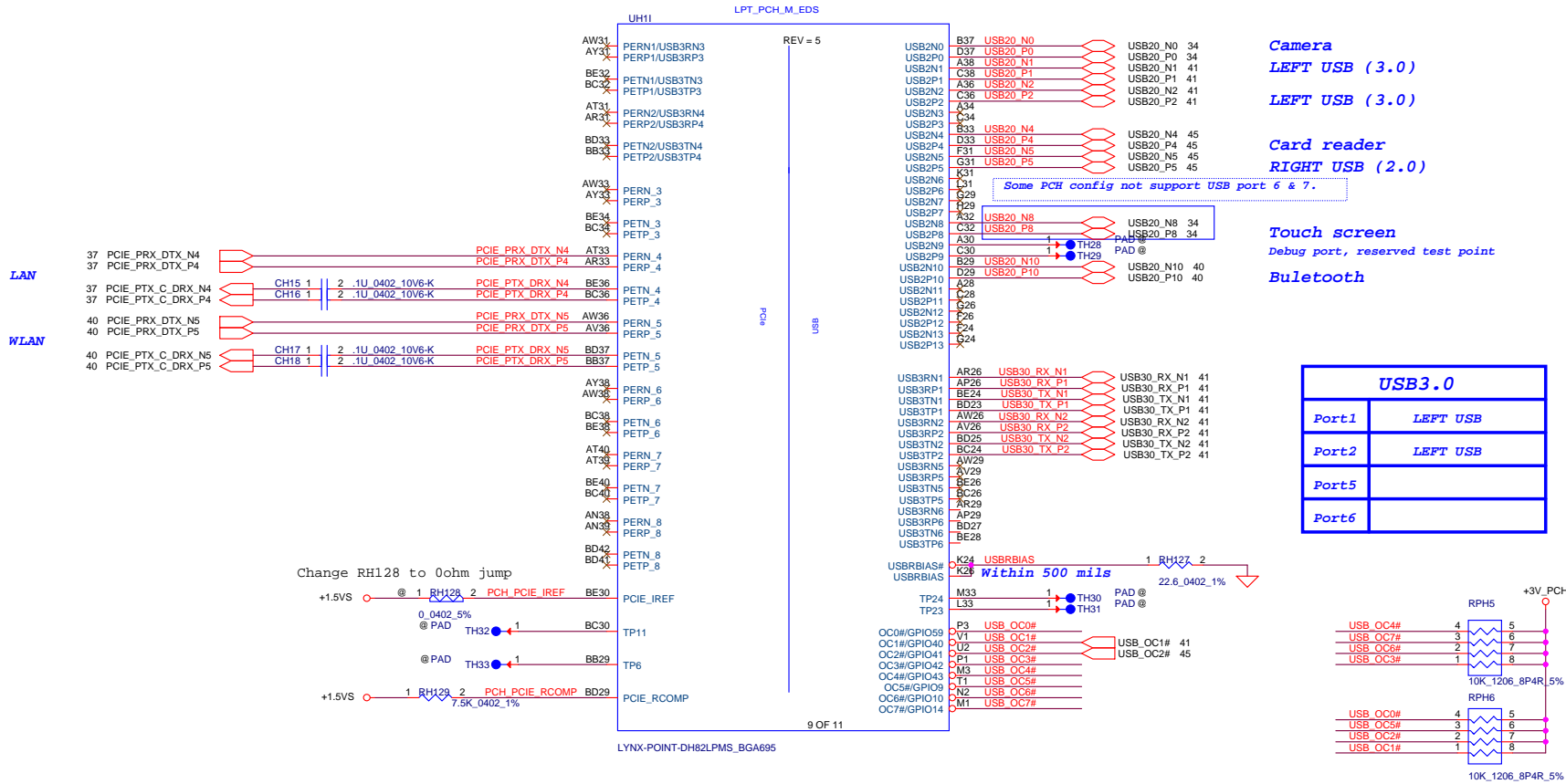


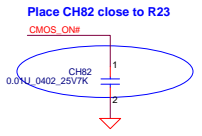
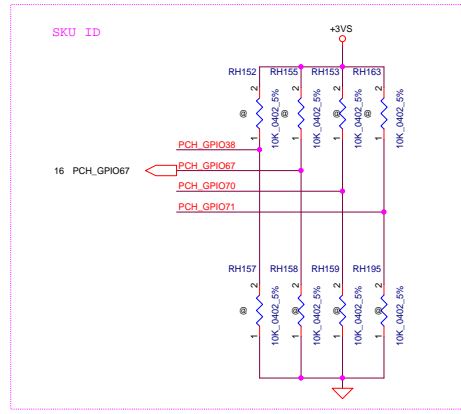
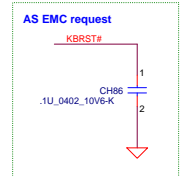
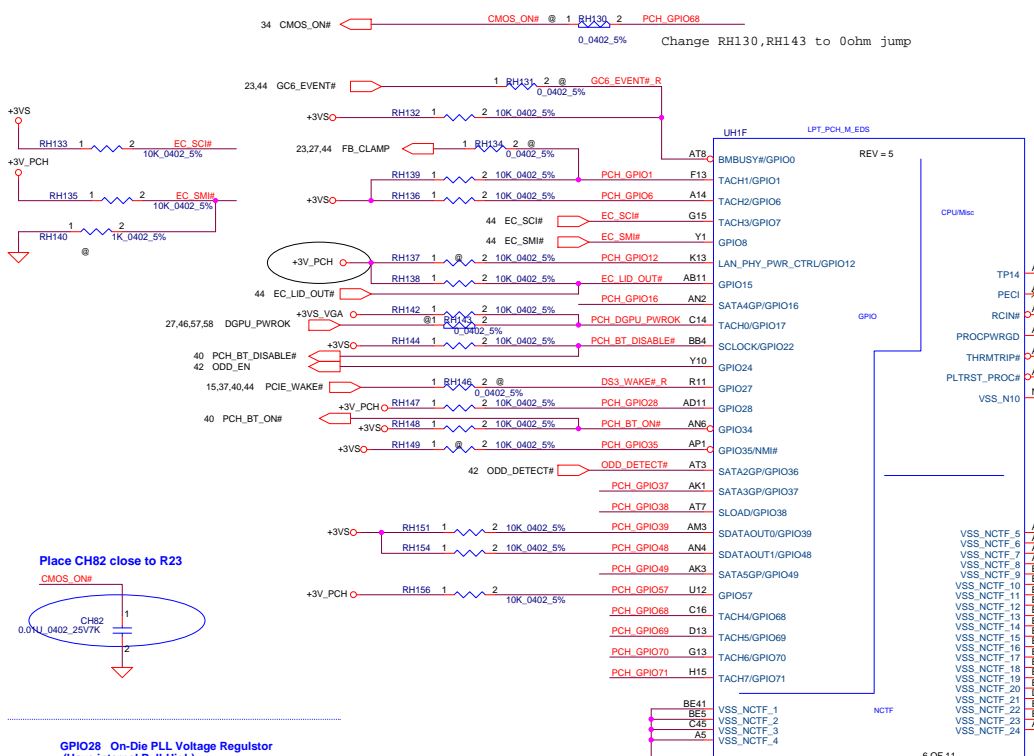
DDPB_CTRLDATA The signal has a weak internal pull-down.
 H Port B is detected.
 L Port B is not detected.



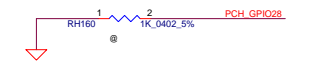


| | | | | |
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| Date: | Friday, July 12, 2013 | Sheet | 17 of 61 | Rev 1.1 |

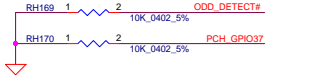
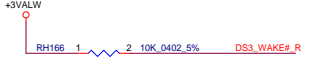




GPIO28 On-Die PLL Voltage Regulator
(Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



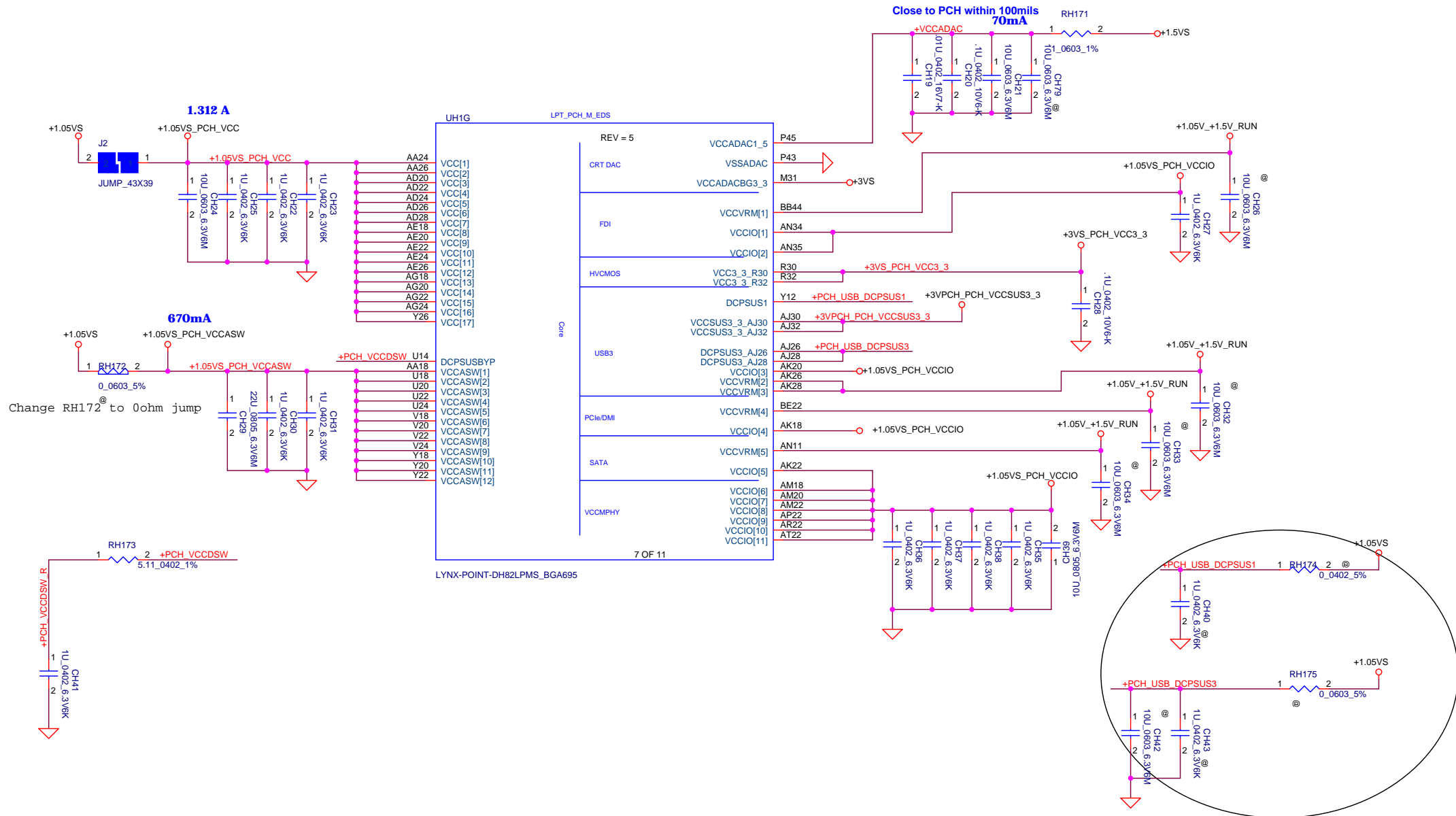
GPIO37
H Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)
L Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)


GPIO36
DMI RX termination Strap (Rising edge of PWROK)
If DMI is operating in DC-coupled mode (e.g. Client applications), then DMI RX is terminated to VSS and the value of this strap is ignored by the PCH and does not take effect.

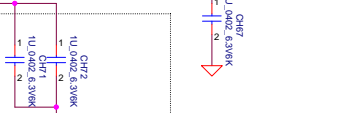
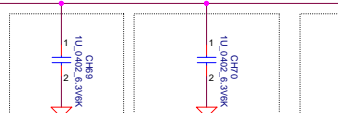
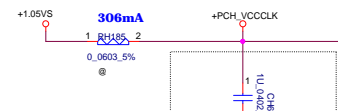
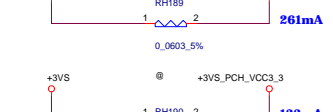
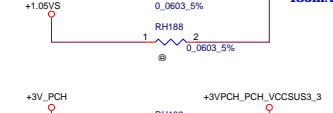
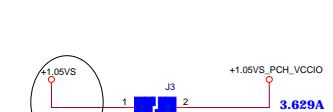
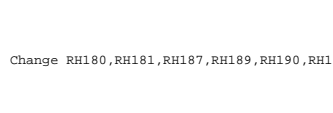
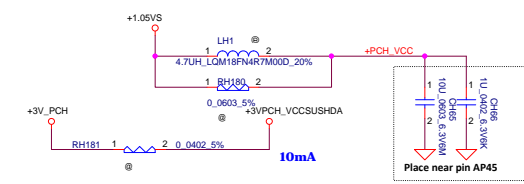
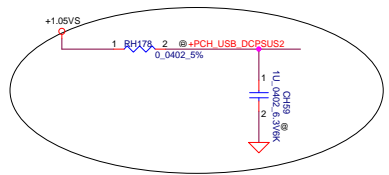
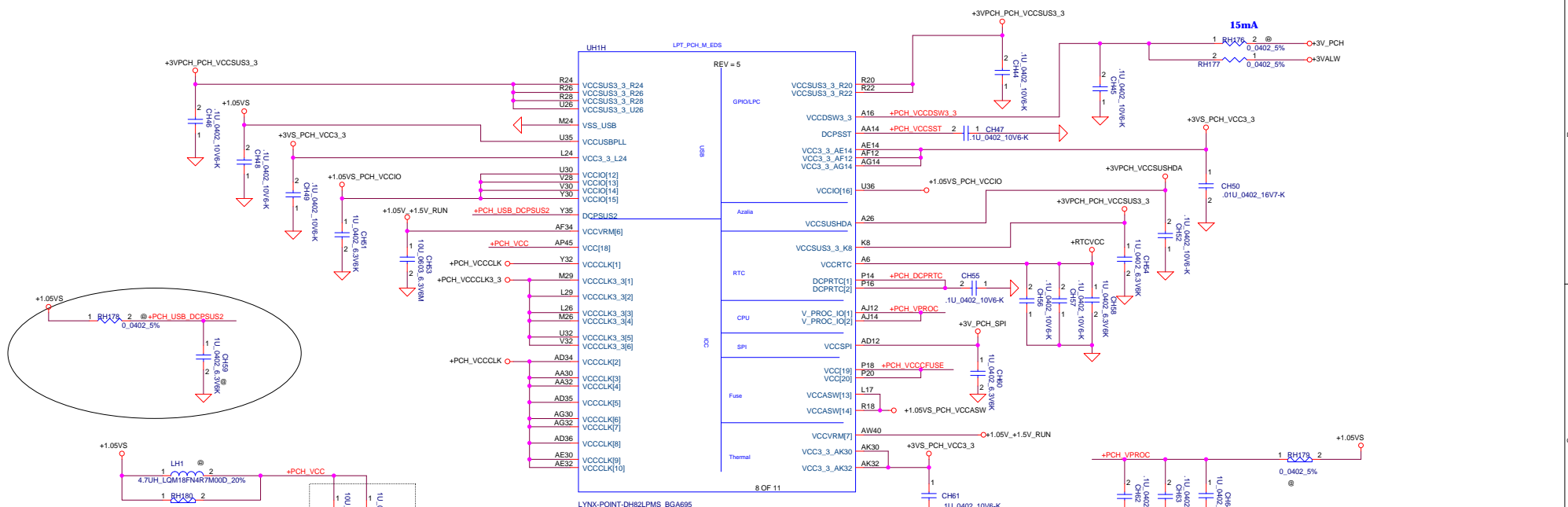
| Config | | GPIO16,49 | |
|-------------|----|-----------|--|
| SATA4,SATA5 | 11 | | |
| PCIE1,PECI2 | 00 | | |

| Fixed Signals | | | | Muxed Signals | | | | Fixed Signals | | | | Muxed Signals | | | | Fixed Signals | | | |
|---------------|------|------|------|---------------|------|------|------|---------------|------|------|------|---------------|------|------|------|---------------|------|------|------|
| USB3 | USB3 | USB3 | USB3 | PCIE | PCIE | PCIE | PCIE | PCIE | PCIE | PCIE | PCIE | SATA | SATA | SATA | SATA | SATA | SATA | SATA | SATA |
| 1 | 2 | 5 | 6 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 4 | 5 | 0 | 1 | 2 | 2 | 2 | 3 |
| | | | | (00) | (00) | | | | | | | (1b) | (1b) | | | | | | |
| | | | | USB3 | USB3 | | | | | | | PCIE | PCIE | | | | | | |
| | | | | (01) | (01) | | | | | | | (0b) | (0b) | | | | | | |

| Function | PCH_GPIO38 | PCH_GPIO67 | PCH_GPIO70 | PCH_GPIO71 |
|-----------------------|------------|------------|------------|------------|
| UMA 14" | 0 | 0 | 0 | 0 |
| UMA 15" | 0 | 1 | 0 | 0 |
| 14" VRAM 900MHz | 1 | 0 | 0 | 0 |
| 14" VRAM 1GHz | 1 | 0 | 1 | 0 |
| 15" VRAM 900MHz | 1 | 1 | 0 | 0 |
| 15" VRAM 1GHz | 1 | 1 | 1 | 0 |
| UMA 15" Touch | 0 | 1 | 0 | 1 |
| 15" VRAM 900MHz Touch | 1 | 1 | 0 | 1 |
| 15" VRAM 1GHz Touch | 1 | 1 | 1 | 1 |



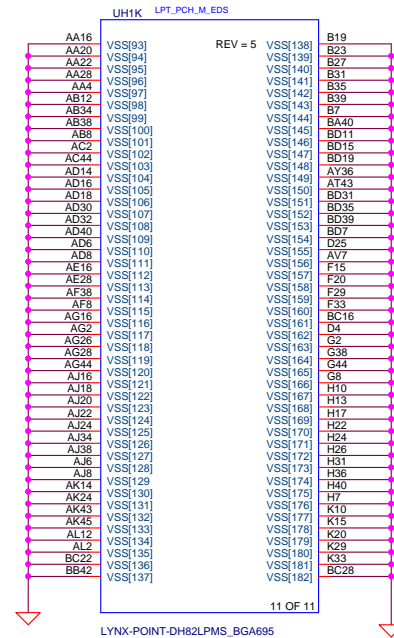
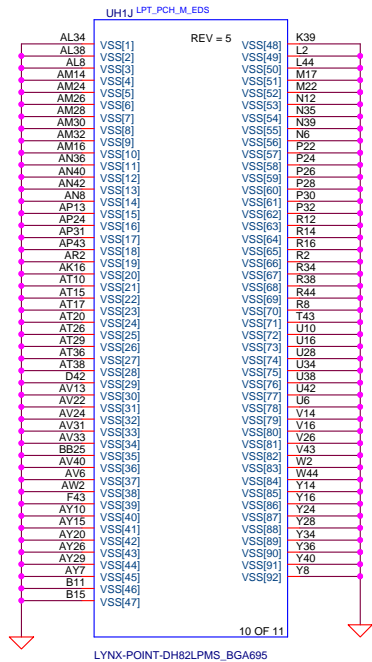
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| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | | Document Number |
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Change RH180, RH181, RH187, RH189, RH190, RH185, RH186 to 0ohm jump


Change RH183, RH179 to 0ohm jump

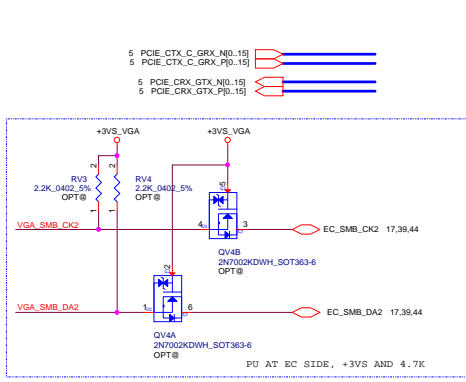
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| Title | Document Number | Rev |
|---------------|-----------------------|----------------|
| PCH (9/9) VSS | 401025 | 1.1 |
| Date: | Friday, July 12, 2013 | Sheet 22 of 61 |

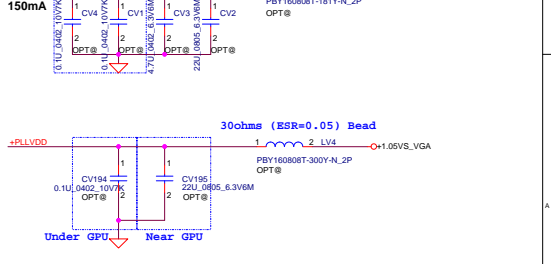
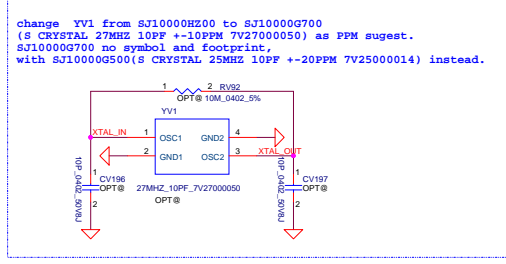
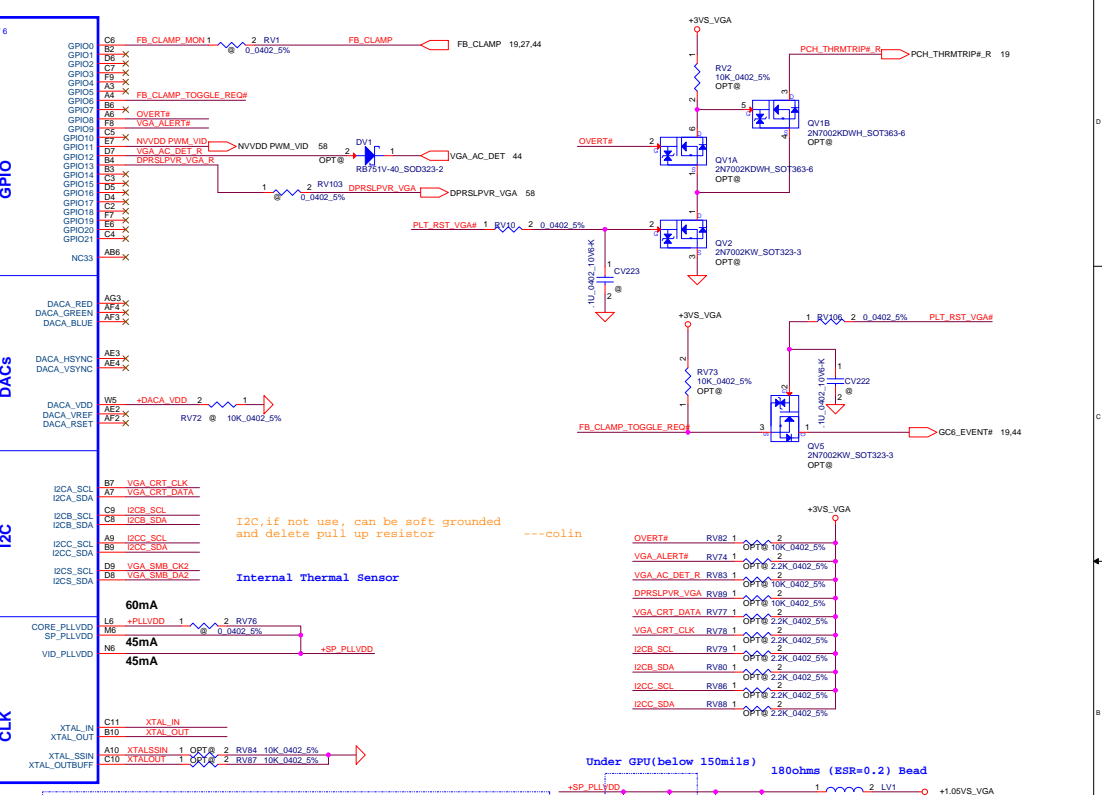
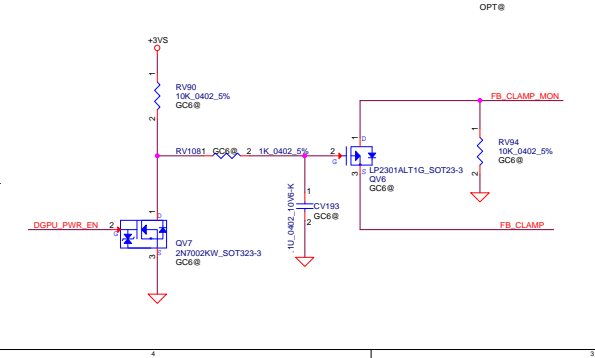
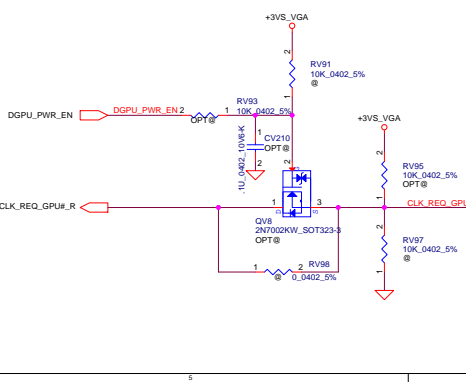
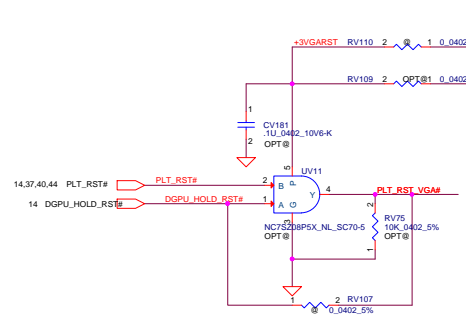
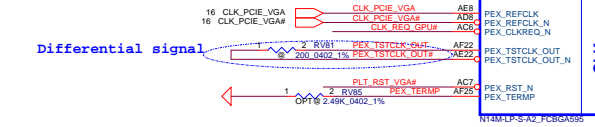




Part 1 of 6

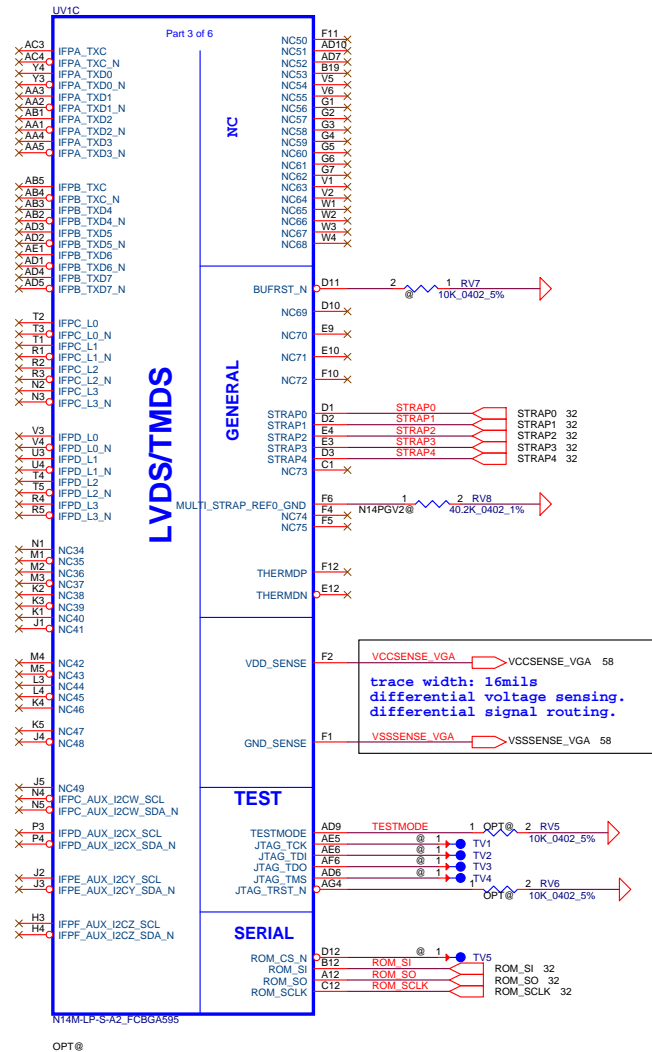
| PCIE CTX C GRX P15 AG6 | PEX_RX0_N |
|-------------------------|-----------|
| PCIE CTX C GRX N15 AG7 | PEX_RX0_N |
| PCIE CTX C GRX P15 AE7 | PEX_RX1_N |
| PCIE CTX C GRX N15 AE7 | PEX_RX1_N |
| PCIE CTX C GRX P15 AG9 | PEX_RX2_N |
| PCIE CTX C GRX N15 AG9 | PEX_RX2_N |
| PCIE CTX C GRX P15 AE9 | PEX_RX3_N |
| PCIE CTX C GRX N15 AE9 | PEX_RX3_N |
| PCIE CTX C GRX P15 AF10 | PEX_RX4_N |
| PCIE CTX C GRX N15 AF10 | PEX_RX4_N |
| PCIE CTX C GRX P15 AG11 | PEX_RX5_N |
| PCIE CTX C GRX N15 AG11 | PEX_RX5_N |
| PCIE CTX C GRX P15 AE11 | PEX_RX6_N |
| PCIE CTX C GRX N15 AE11 | PEX_RX6_N |
| PCIE CTX C GRX P15 AF12 | PEX_RX7_N |
| PCIE CTX C GRX N15 AF12 | PEX_RX7_N |
| PCIE CTX C GRX P5 AE13 | NC1 |
| PCIE CTX C GRX N5 AE13 | NC2 |
| PCIE CTX C GRX P5 AF14 | NC3 |
| PCIE CTX C GRX N5 AF14 | NC4 |
| PCIE CTX C GRX P5 AE15 | NC5 |
| PCIE CTX C GRX N5 AE15 | NC6 |
| PCIE CTX C GRX P5 AF16 | NC7 |
| PCIE CTX C GRX N5 AF16 | NC8 |
| PCIE CTX C GRX P5 AE18 | NC9 |
| PCIE CTX C GRX N5 AE18 | NC10 |
| PCIE CTX C GRX P5 AF19 | NC11 |
| PCIE CTX C GRX N5 AF19 | NC12 |
| PCIE CTX C GRX P5 AE21 | NC13 |
| PCIE CTX C GRX N5 AE21 | NC14 |
| PCIE CTX C GRX P5 AF21 | NC15 |
| PCIE CTX C GRX N5 AF21 | NC16 |

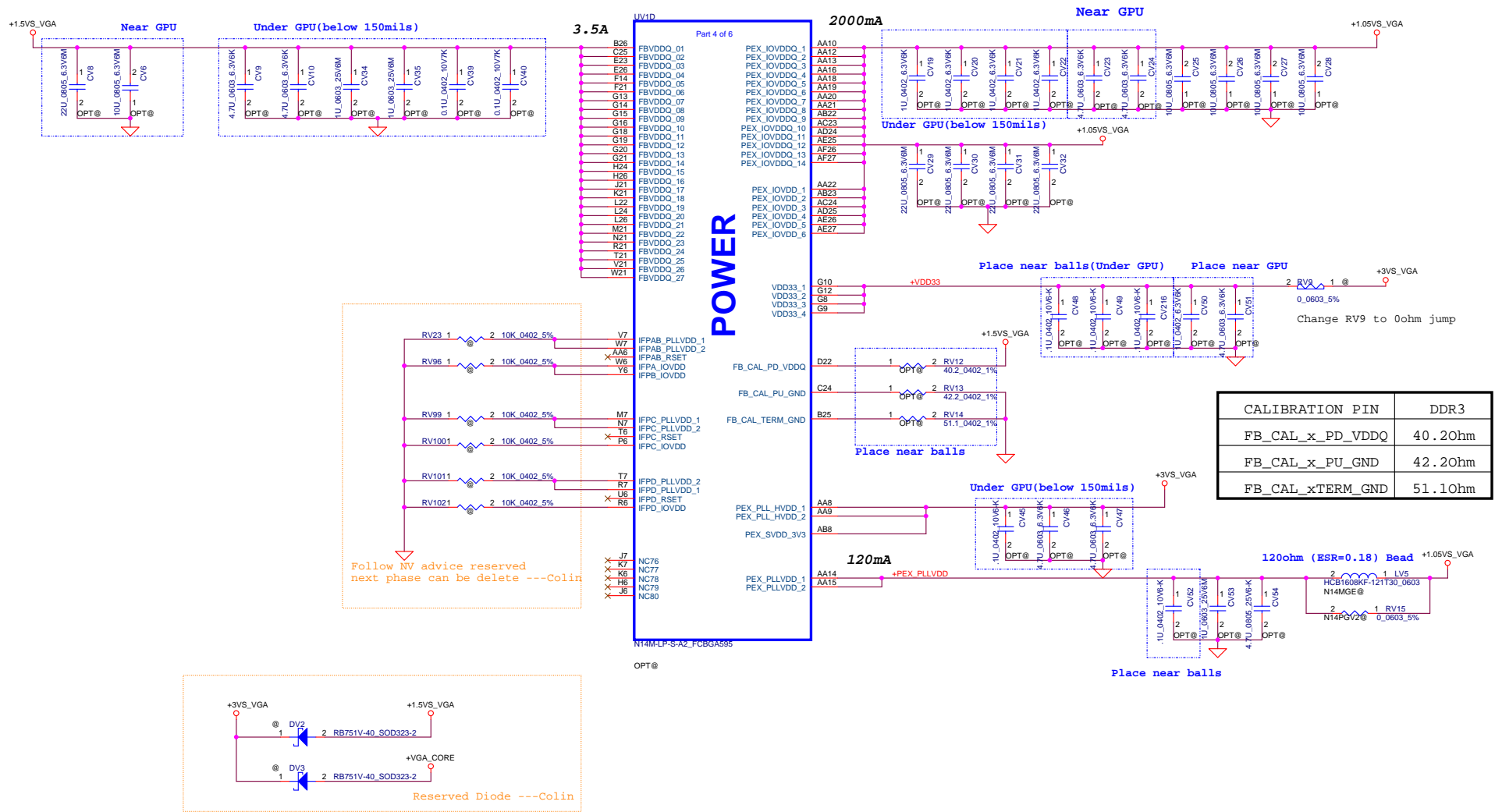
| PCIE CRX GTX P15 CV160 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC9 | PEX_TX0_N |
|------------------------------|------------------|-------------------------|-----------|
| PCIE CRX GTX N15 CV161 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB9 | PEX_TX0_N |
| PCIE CRX GTX P15 CV162 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB10 | PEX_TX1_N |
| PCIE CRX GTX N15 CV163 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB10 | PEX_TX1_N |
| PCIE CRX GTX P15 CV164 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB11 | PEX_TX2_N |
| PCIE CRX GTX N15 CV165 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB11 | PEX_TX2_N |
| PCIE CRX GTX P15 CV166 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB12 | PEX_TX3_N |
| PCIE CRX GTX N15 CV167 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB12 | PEX_TX3_N |
| PCIE CRX GTX P15 CV168 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB13 | PEX_TX4_N |
| PCIE CRX GTX N15 CV169 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB13 | PEX_TX4_N |
| PCIE CRX GTX P15 CV170 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB14 | PEX_TX5_N |
| PCIE CRX GTX N15 CV171 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB14 | PEX_TX5_N |
| PCIE CRX GTX P15 CV172 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC15 | PEX_TX6_N |
| PCIE CRX GTX N15 CV173 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC15 | PEX_TX6_N |
| PCIE CRX GTX P15 CV174 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB16 | PEX_TX7_N |
| PCIE CRX GTX N15 CV175 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB16 | PEX_TX7_N |
| PCIE CRX GTX P15 CV176 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC17 | NC17 |
| PCIE CRX GTX N15 CV177 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC17 | NC18 |
| PCIE CRX GTX P15 CV178 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB18 | NC19 |
| PCIE CRX GTX N15 CV179 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB18 | NC20 |
| PCIE CRX GTX P15 CV180 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB19 | NC21 |
| PCIE CRX GTX N15 CV181 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB19 | NC22 |
| PCIE CRX GTX P15 CV182 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC20 | NC23 |
| PCIE CRX GTX N15 CV183 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC20 | NC24 |
| PCIE CRX GTX P15 CV184 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB21 | NC25 |
| PCIE CRX GTX N15 CV185 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB21 | NC26 |
| PCIE CRX GTX P15 CV186 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC21 | NC27 |
| PCIE CRX GTX N15 CV187 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC21 | NC28 |
| PCIE CRX GTX P15 CV188 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AB22 | NC29 |
| PCIE CRX GTX N15 CV189 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AB22 | NC30 |
| PCIE CRX GTX P15 CV190 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC22 | NC31 |
| PCIE CRX GTX N15 CV191 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC22 | NC32 |
| PCIE CRX GTX P15 CV192 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX P15 AC23 | NC33 |
| PCIE CRX GTX N15 CV193 OPT@1 | 2 0.22u 0.402-5% | PCIE CRX C GTX N15 AC23 | NC33 |

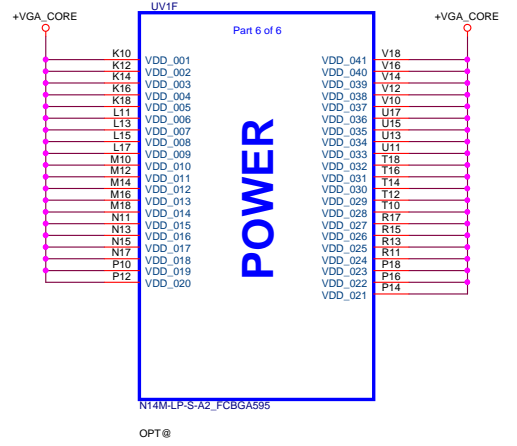
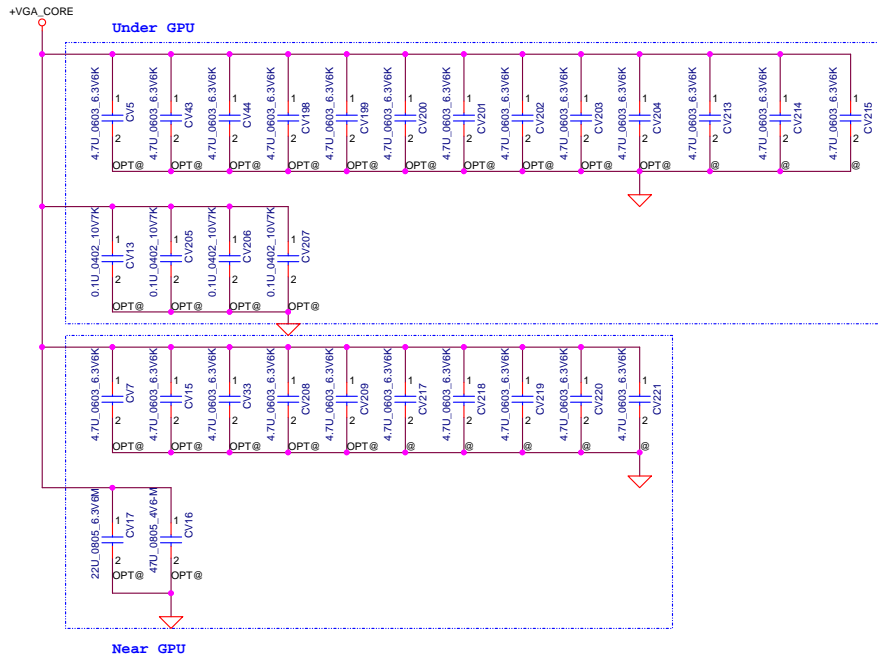
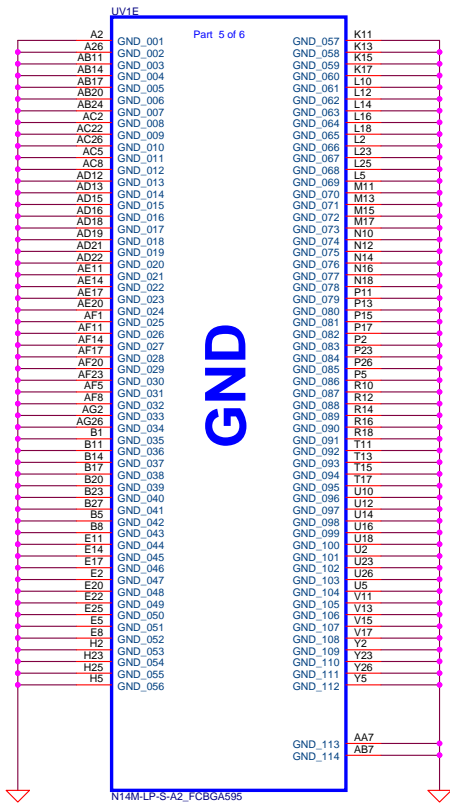


change Y1 from SJ10000H200 to SJ10000G700 (S CRYSTAL 27MHZ 10PF +-10PPM 7V27000050) as PPM suggest. SJ10000G700 no symbol and footprint, with SJ10000G500(S CRYSTAL 25MHZ 10PF +-20PPM 7V25000014) instead.

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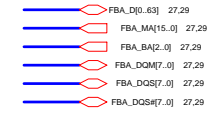
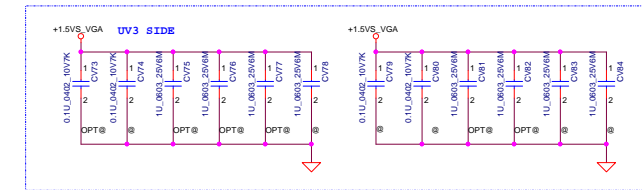
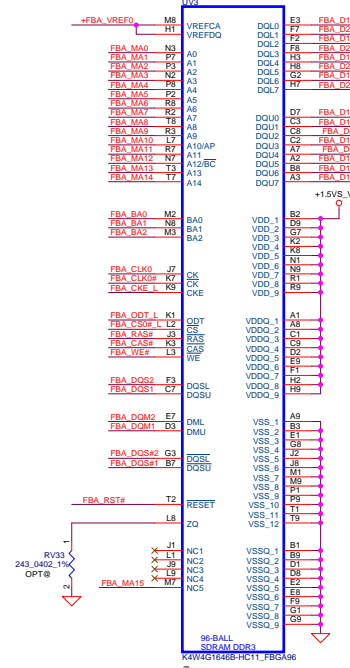
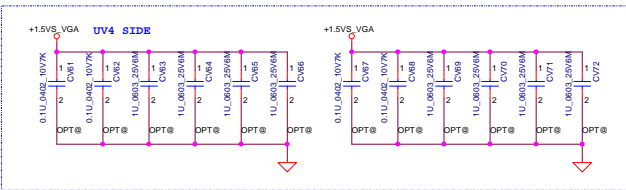
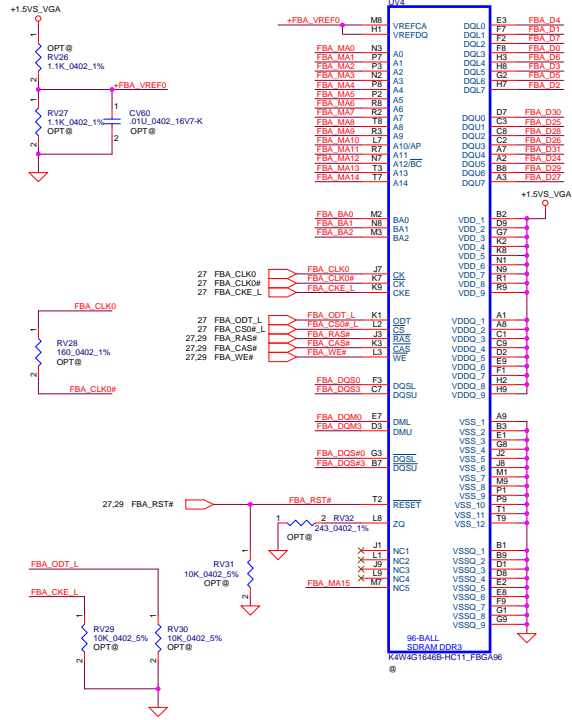






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at least 16 mils width(optimal)
20 mils spacing to other signals /planes

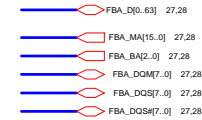
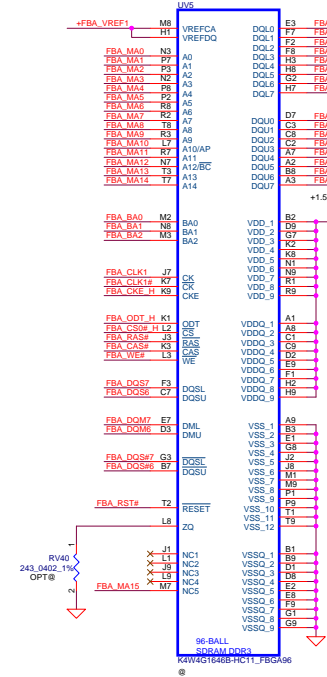
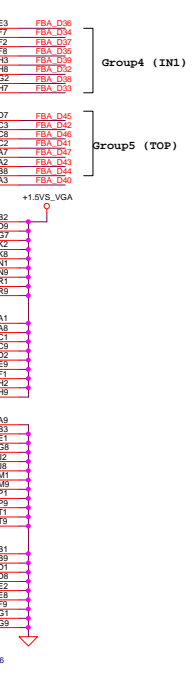
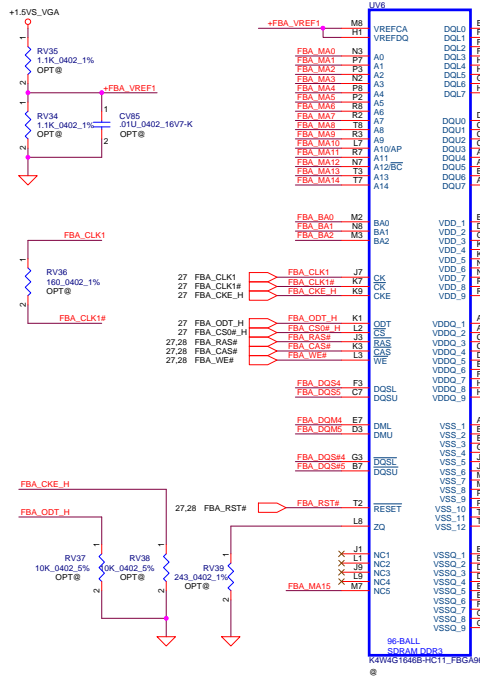


CMD mapping mod Mode D

| Address | DATA Bus |
|-----------|-----------|
| 0..31 | 32..63 |
| FbX_CMD0 | CS0#_L |
| FbX_CMD1 | |
| FbX_CMD2 | ODT_L |
| FbX_CMD3 | CKE_L |
| FbX_CMD4 | A14 A14 |
| FbX_CMD5 | RST RST |
| FbX_CMD6 | A9 A9 |
| FbX_CMD7 | A7 A7 |
| FbX_CMD8 | A2 A2 |
| FbX_CMD9 | A0 A0 |
| FbX_CMD10 | A4 A4 |
| FbX_CMD11 | A1 A1 |
| FbX_CMD12 | BA0 BA0 |
| FbX_CMD13 | WE# WE# |
| FbX_CMD14 | A15 A15 |
| FbX_CMD15 | CAS# CAS# |
| FbX_CMD16 | CS0#_H |
| FbX_CMD17 | |
| FbX_CMD18 | ODT_H |
| FbX_CMD19 | CKE_H |
| FbX_CMD20 | A13 A13 |
| FbX_CMD21 | A8 A8 |
| FbX_CMD22 | A6 A6 |
| FbX_CMD23 | A11 A11 |
| FbX_CMD24 | A5 A5 |
| FbX_CMD25 | A3 A3 |
| FbX_CMD26 | BA2 BA2 |
| FbX_CMD27 | BA1 BA1 |
| FbX_CMD28 | A12 A12 |
| FbX_CMD29 | A10 A10 |
| FbX_CMD30 | RAS# RAS# |

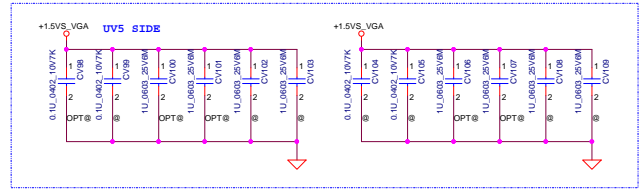
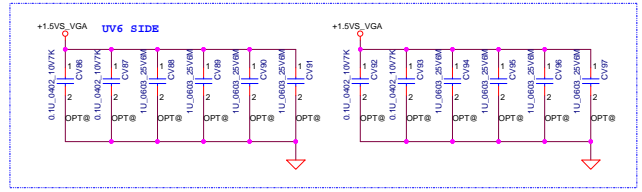
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at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode D

| Address | DATA | Bus |
|-----------|--------|------|
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT#_L | |
| FBx_CMD3 | CKE#_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | CS0#_H | |
| FBx_CMD17 | | |
| FBx_CMD18 | ODT#_H | |
| FBx_CMD19 | CKE#_H | |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |



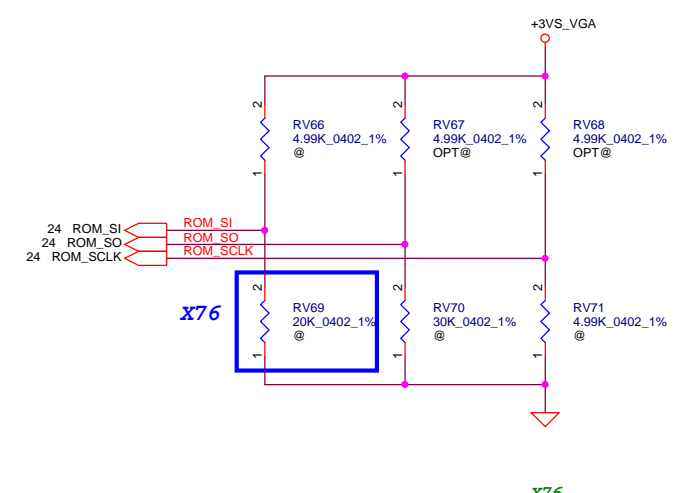
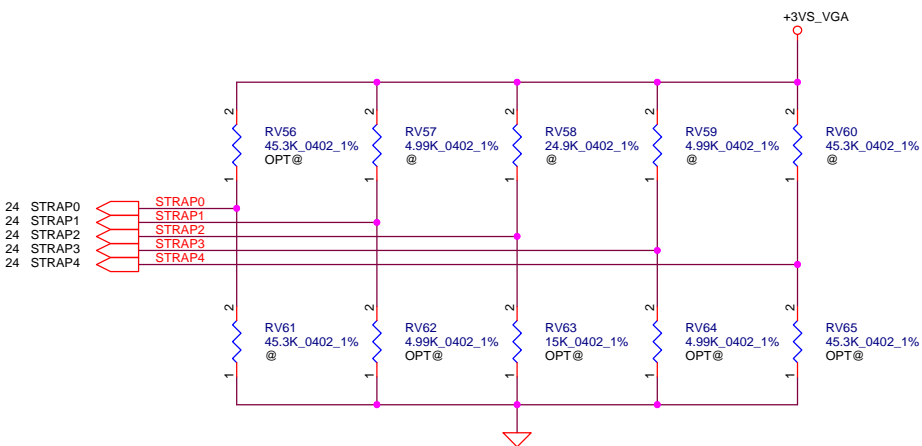
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| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|------------------------|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VS_VGA | PCI_DEVID[4] | SUB_VENDOR | PCI_DEVID5] | PEX_PLL_EN_TERM |
| ROM_SI | +3VS_VGA | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_VGA | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_VGA | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | +3VS_VGA | 3GIO_PAD_CFG_ADR[3] | 3GIO_PAD_CFG_ADR[2] | 3GIO_PAD_CFG_ADR[1] | 3GIO_PAD_CFG_ADR[0] |
| STRAP2 | +3VS_VGA | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | +3VS_VGA | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | +3VS_VGA | RESERVED | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V |

| Resistor Values | Pull-up to +3VS_VGA | Pull-down to Gnd |
|-----------------|---------------------|------------------|
| 4.99K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

| FB[1:0] | |
|---------|-----------------|
| 0 | Reserved |
| 1 | Reserved |
| 2 | 256MB (Default) |
| 3 | Reserved |

| PCIE_MAX_SPEED | |
|----------------|-------------------------------|
| 0 | Limit booting to PCIe Gen1 |
| 1 | Allow booting to PCIe Gen 2/3 |

| VGA_DEVICE | |
|------------|-----------------------------|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

| SMBUS_ALT_ADDR | |
|----------------|------------------------|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| SUB_VENDOR | |
|------------|-------------------------------|
| 0 | No VBIOS ROM |
| 1 | BIOS ROM is present (Default) |

| PEX_PLL_EN_TERM | |
|-----------------|-------------------|
| 0 | Disable (Default) |
| 1 | Enable |

| PCIE_SPEED_CHANGE_GEN3 | |
|------------------------|-----------------------------|
| 0 | Disable PCIe Gen3 operation |
| 1 | Enable PCIe Gen3 operation |

| USER Straps | |
|-------------|------------------|
| User[3:0] | |
| 1000-1100 | Customer defined |

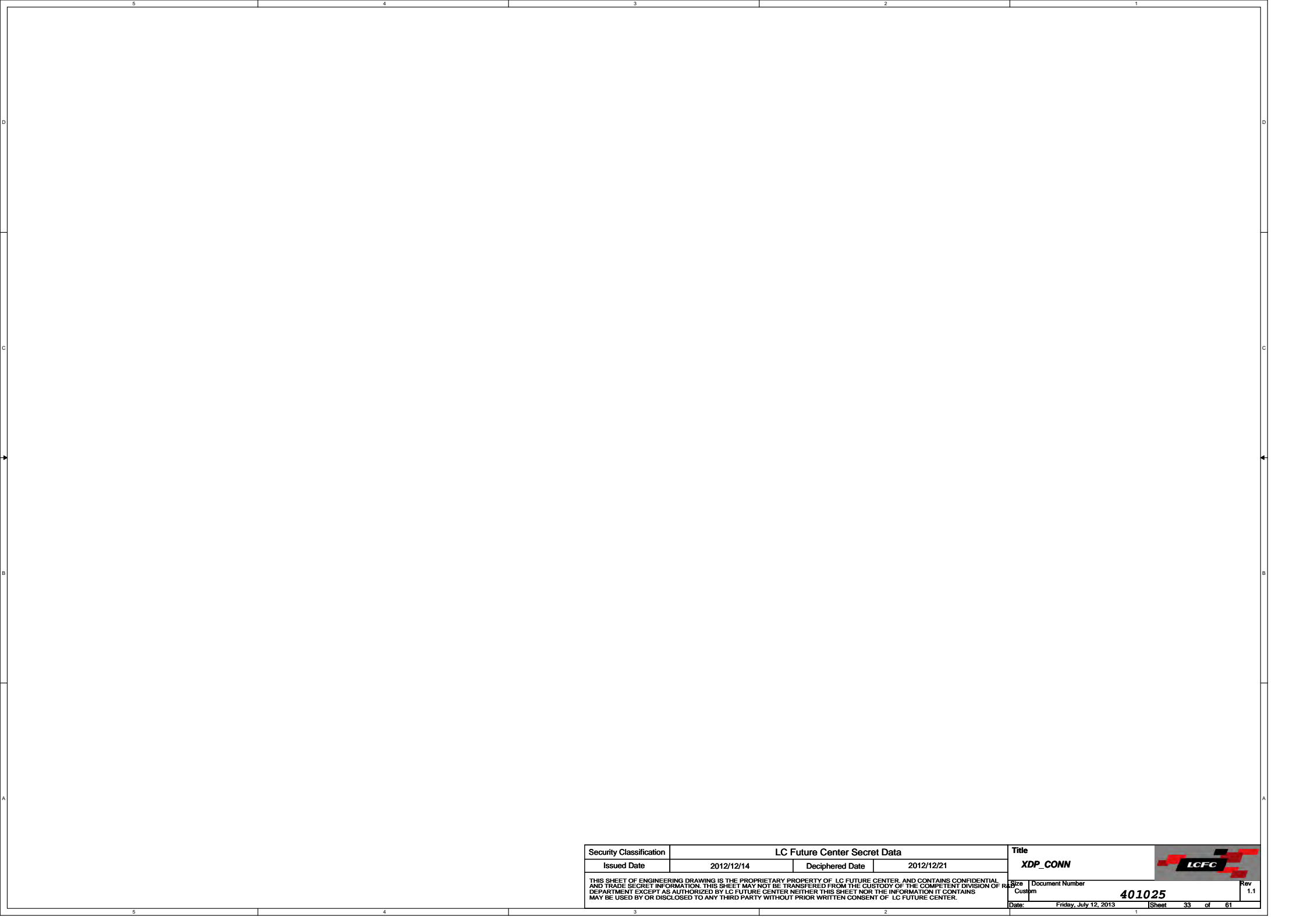
| DP_PLL_VDD33V | |
|---------------|----------|
| 0 | Reserved |
| 1 | Default |


| 3GIO_PADCFG[3:0] | |
|------------------|------------------------|
| 0110 | Gen1/Gen2 support only |
| 0000 | Gen3 support |

| GPU | FB Memory (DDR3) | ROM_SI | ROM_SO | ROM_SCLK | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|----------|--|-----------------|----------|----------|----------|----------|--------|----------|----------|
| N14P_GV2 | Samsung 1GHz K4W2G1646E-BC1A 128M x 16 | 0x7 PD 45.3K | PU 4.99K | PU 4.99K | PU 45.3K | PD 4.99K | PD 15K | PD 4.99K | PU 45.3K |
| | Micron 1GMHz MT41J128M16JT-093G:K 128M x 16 | 0x5 PD 30.1K | | | | | | | |
| | Hynix 1GMHz H5TC2G63FFR-11C 128M x 16 | 0x4 PD 24.9K | | | | | | | |
| | Samsung 900MHz K4W4G1646B-HC11 256M x 16 | 0x3 PD 20K | | | | | | | |
| | Micron 900MHz MT41K256M16HA-107G:E 256M x 16 | 0x1 PD 10K | | | | | | | |

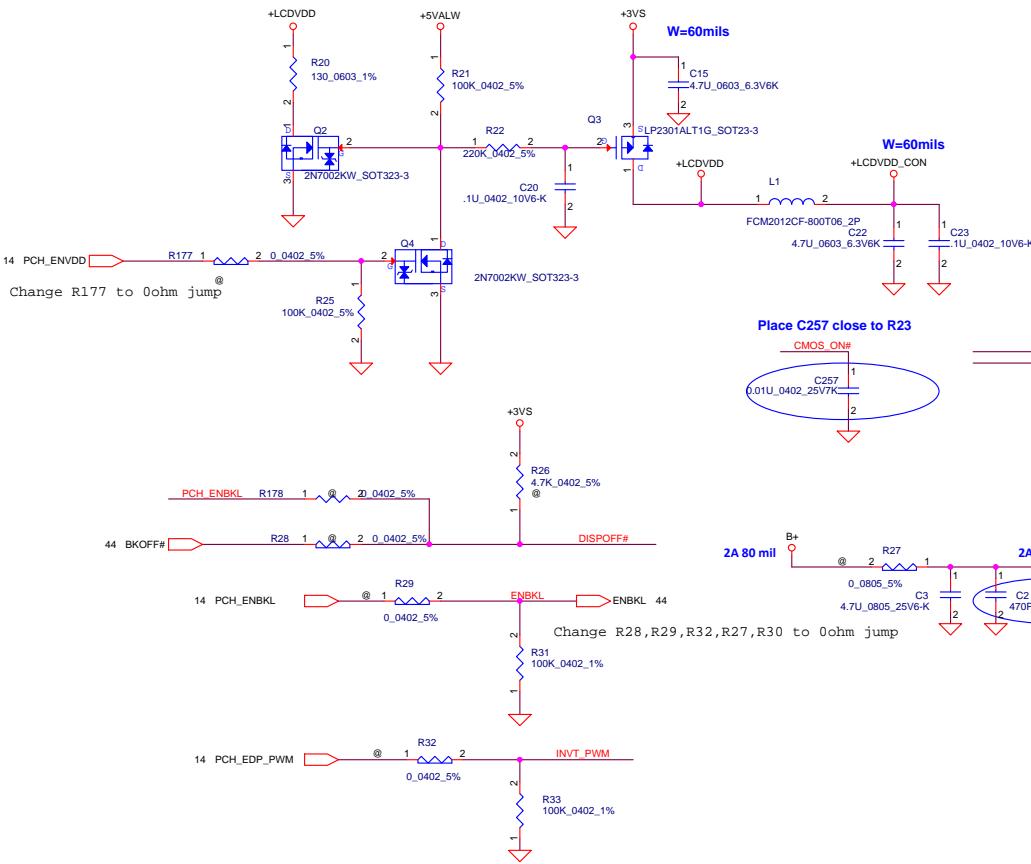
| VRAM | X76 | VRAM P/N |
|---------|-------------------------|-------------|
| Samsung | X76409JVL01 | SA00005SH10 |
| | X76409JVL51 (1G 32Mx16) | |
| Micron | X76409JVL02 | SA00005M100 |
| | X76409JVL02 (2G 64Mx32) | |
| Hynix | | |

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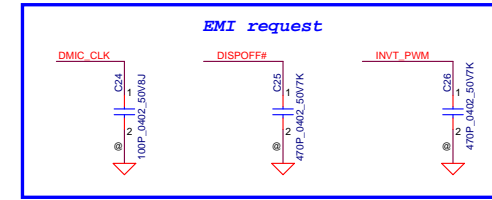
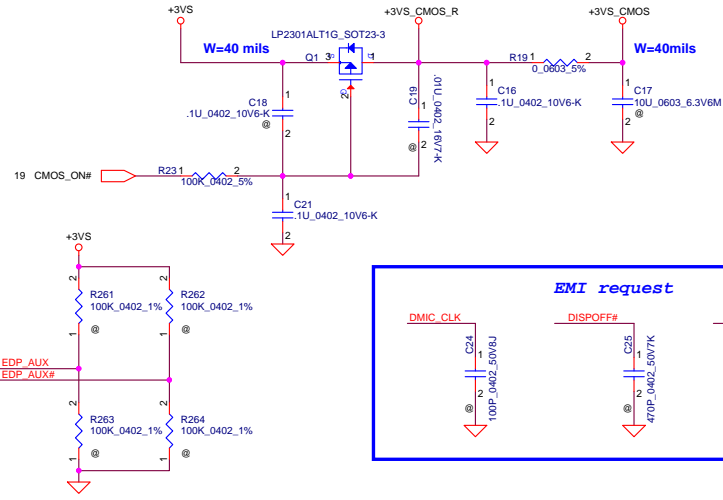


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|--|------------------------------|-----------------|------------|----------|---|
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| | | | | Custom | 401025 |
| | | | | Date: | Friday, July 12, 2013 |
| | | | | Rev | 1.1 |
| | | | | Sheet | 33 of 61 |

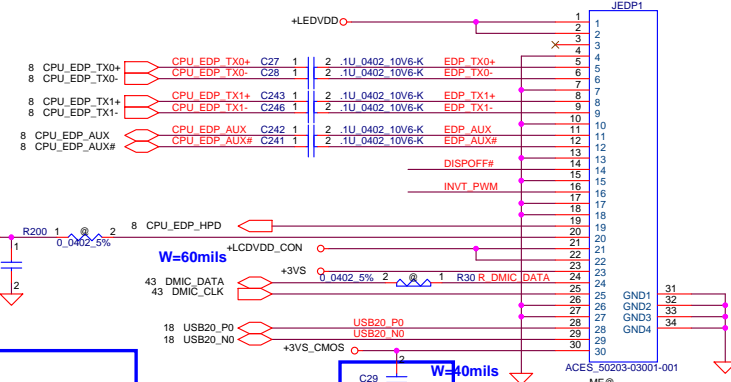
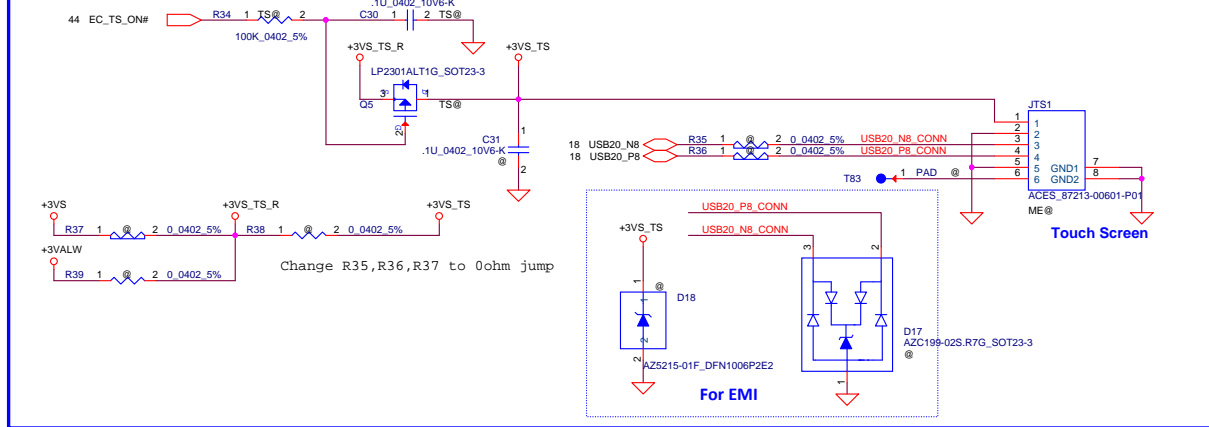
LCD POWER CIRCUIT

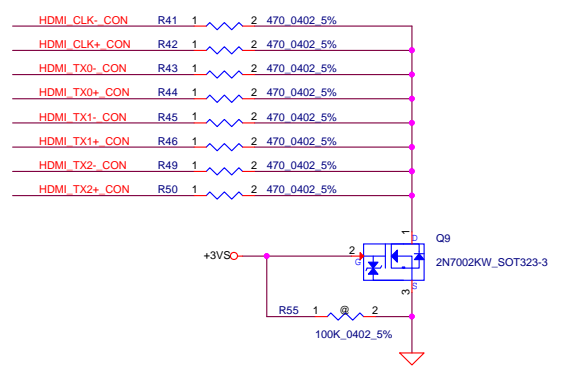
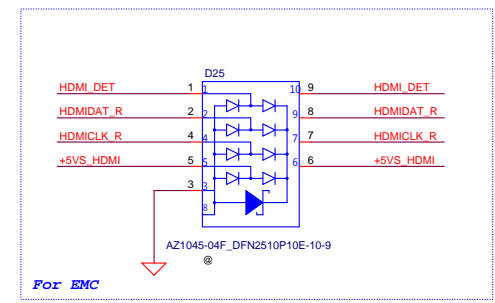
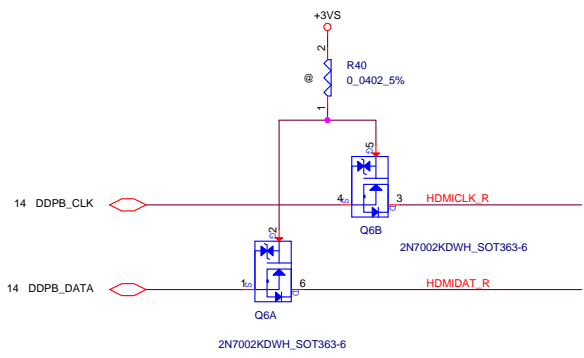
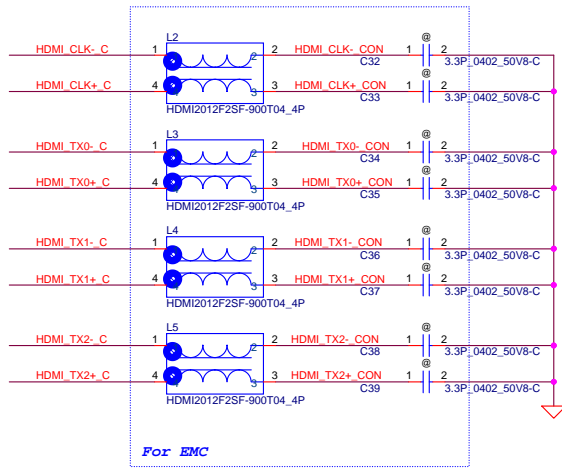


CMOS Camera

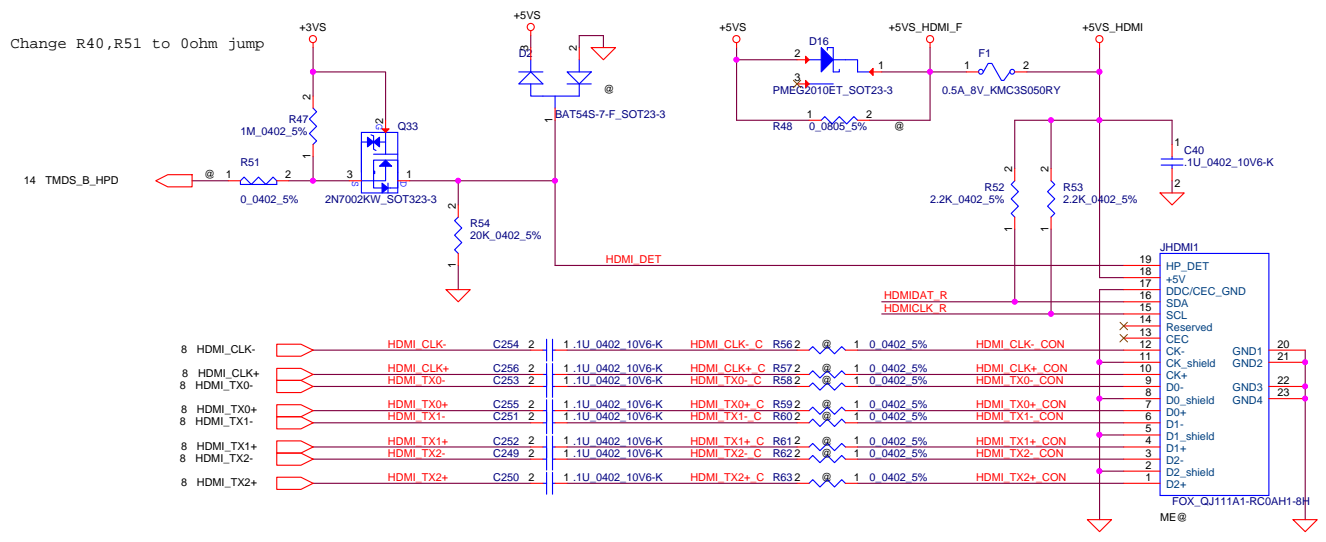


Touch Screen

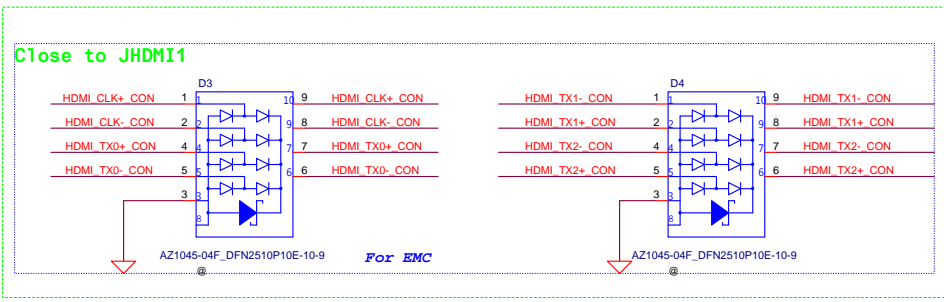




Change R40,R51 to 0ohm jump

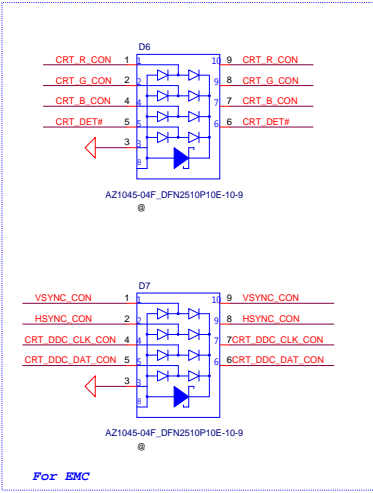
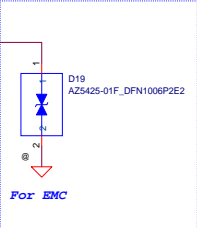
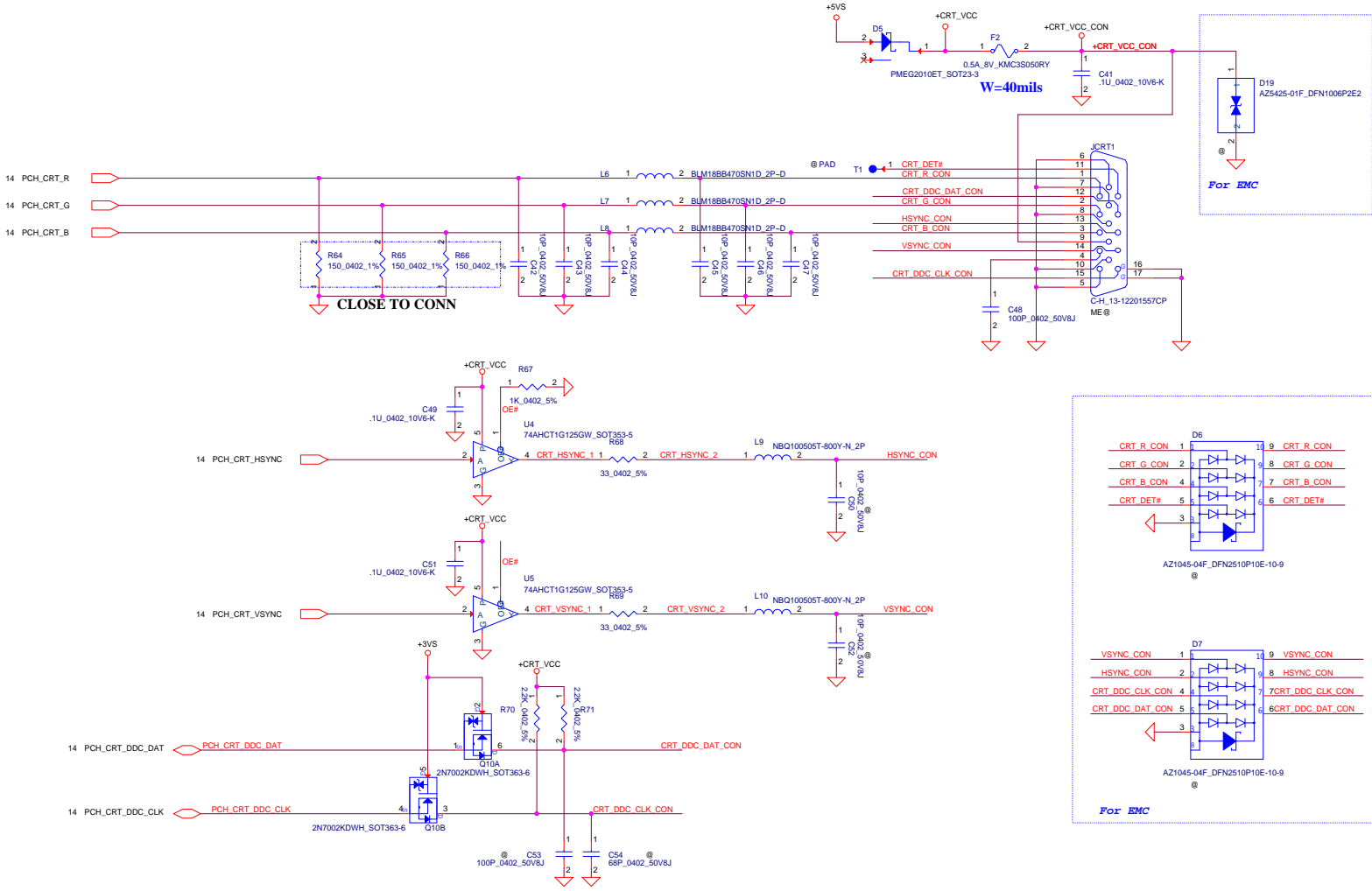



| | | | | | | | | | | | | |
|-------------|-----------|------|---|------------------|-------------|-----|---|---|---|---------|---------------|--|
| 8 HDMI_CLK- | HDMI_CLK- | C254 | 2 | 1.1U_0402_10V6-K | HDMI_CLK- C | R56 | 2 | 1 | 0 | 0402_5% | HDMI_CLK- CON | |
| 8 HDMI_CLK+ | HDMI_CLK+ | C256 | 2 | 1.1U_0402_10V6-K | HDMI_CLK+ C | R57 | 2 | 1 | 0 | 0402_5% | HDMI_CLK+ CON | |
| 8 HDMI_TX0- | HDMI_TX0- | C253 | 2 | 1.1U_0402_10V6-K | HDMI_TX0- C | R58 | 2 | 1 | 0 | 0402_5% | HDMI_TX0- CON | |
| 8 HDMI_TX0+ | HDMI_TX0+ | C255 | 2 | 1.1U_0402_10V6-K | HDMI_TX0+ C | R59 | 2 | 1 | 0 | 0402_5% | HDMI_TX0+ CON | |
| 8 HDMI_TX1- | HDMI_TX1- | C251 | 2 | 1.1U_0402_10V6-K | HDMI_TX1- C | R60 | 2 | 1 | 0 | 0402_5% | HDMI_TX1- CON | |
| 8 HDMI_TX1+ | HDMI_TX1+ | C252 | 2 | 1.1U_0402_10V6-K | HDMI_TX1+ C | R61 | 2 | 1 | 0 | 0402_5% | HDMI_TX1+ CON | |
| 8 HDMI_TX2- | HDMI_TX2- | C249 | 2 | 1.1U_0402_10V6-K | HDMI_TX2- C | R62 | 2 | 1 | 0 | 0402_5% | HDMI_TX2- CON | |
| 8 HDMI_TX2+ | HDMI_TX2+ | C250 | 2 | 1.1U_0402_10V6-K | HDMI_TX2+ C | R63 | 2 | 1 | 0 | 0402_5% | HDMI_TX2+ CON | |



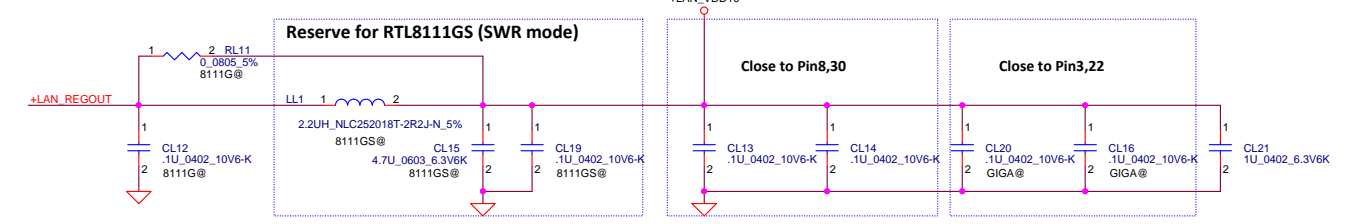
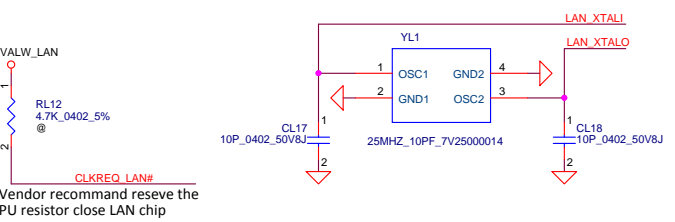
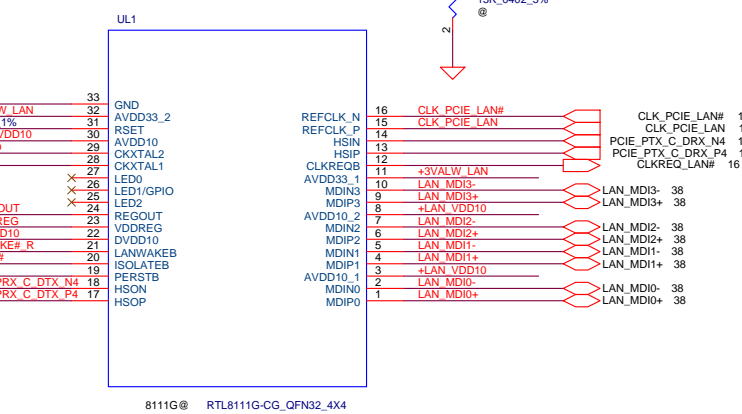
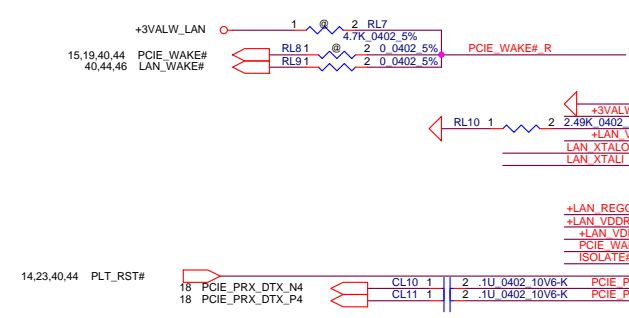
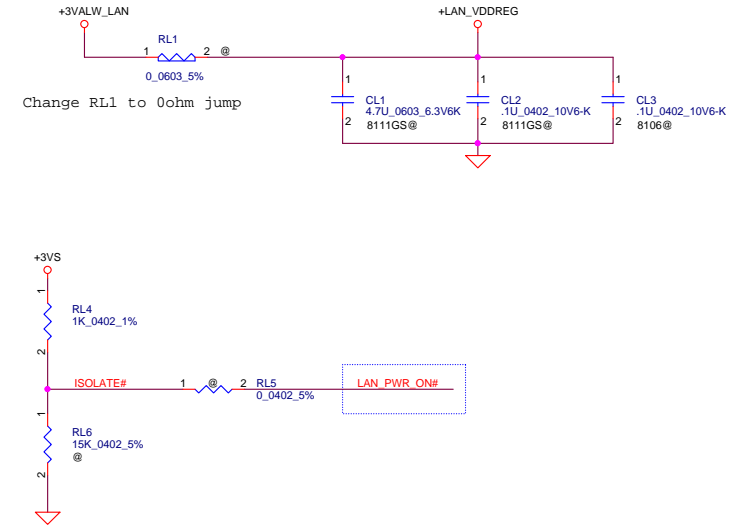
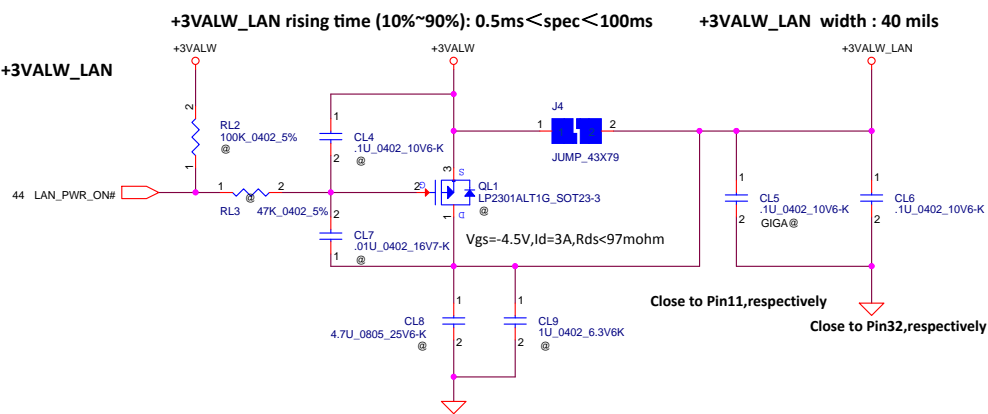
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| Security Classification | | | | LC Future Center Secret Data | | | | Title | | HDMI_CONN | |
| Issued Date | | 2012/12/14 | | Deciphered Date | | 2012/12/21 | | Size | | Document Number | |
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CRT Connector



| | | | | |
|--|------------------------------|-----------------|------------|---|
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| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | |
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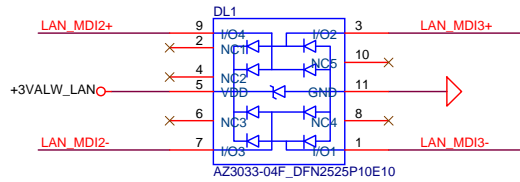
+3VALW TO +3VALW_LAN



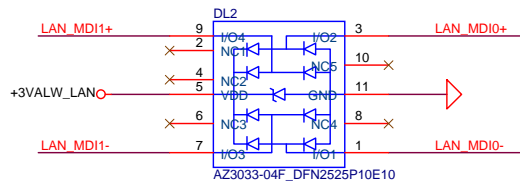
Layout Note: LL1 must be within 200mil to Pin36,
CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

| | | | | | |
|--|-----------------------|------------------------------|------------|--------------|-----|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | LAN_RTL8106E | |
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| Size Custom | Document Number | 401025 | | Rev | 1.1 |
| Date: | Friday, July 12, 2013 | Sheet | 37 | of | 61 |

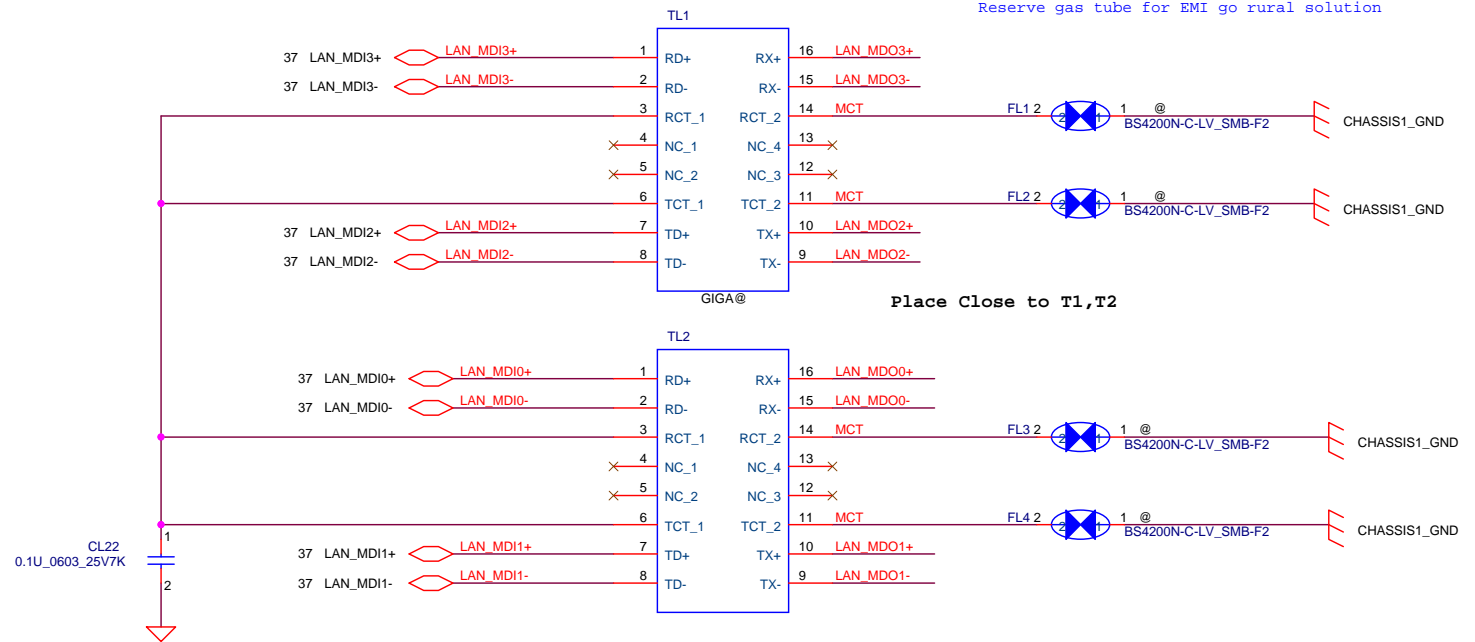
DL1/DL2
1'S PN:SC300003M00



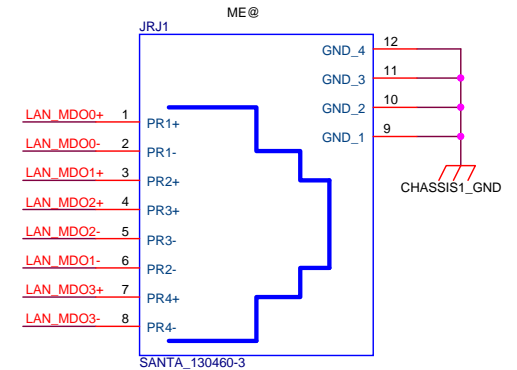
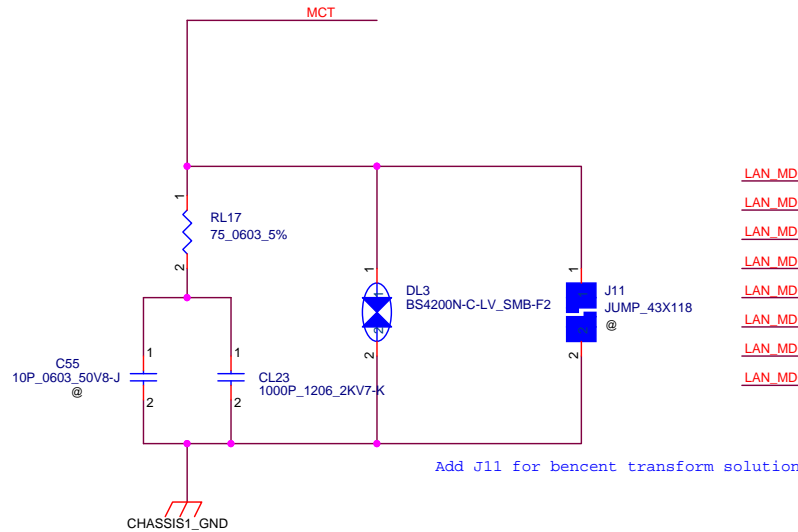
Place Close to TL1



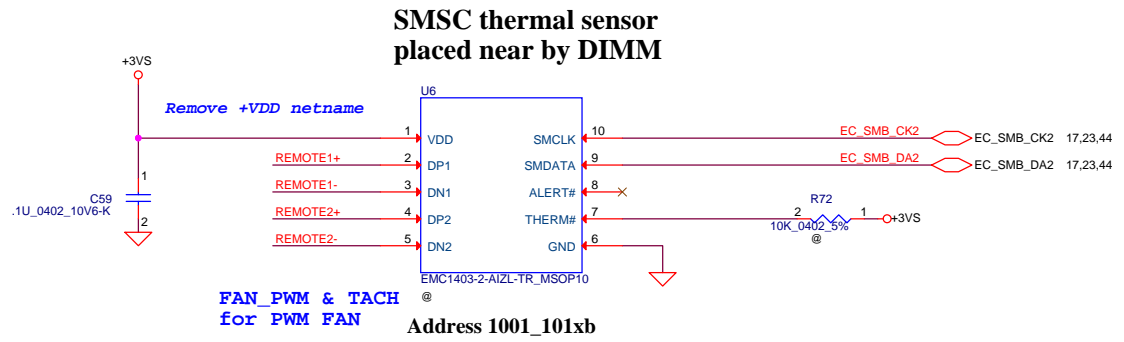
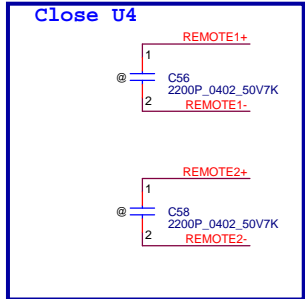
Place Close to TL2



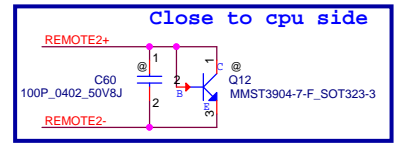
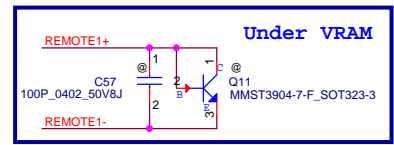
Place Close to T1,T2



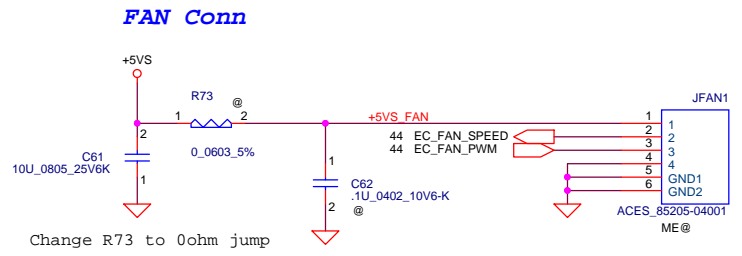
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| Security Classification | LC Future Center Secret Data | | Title | | | |
| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | | LAN_Transformer | |
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| | | | | Date: | Friday, July 12, 2013 | Sheet 38 of 61 |



internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

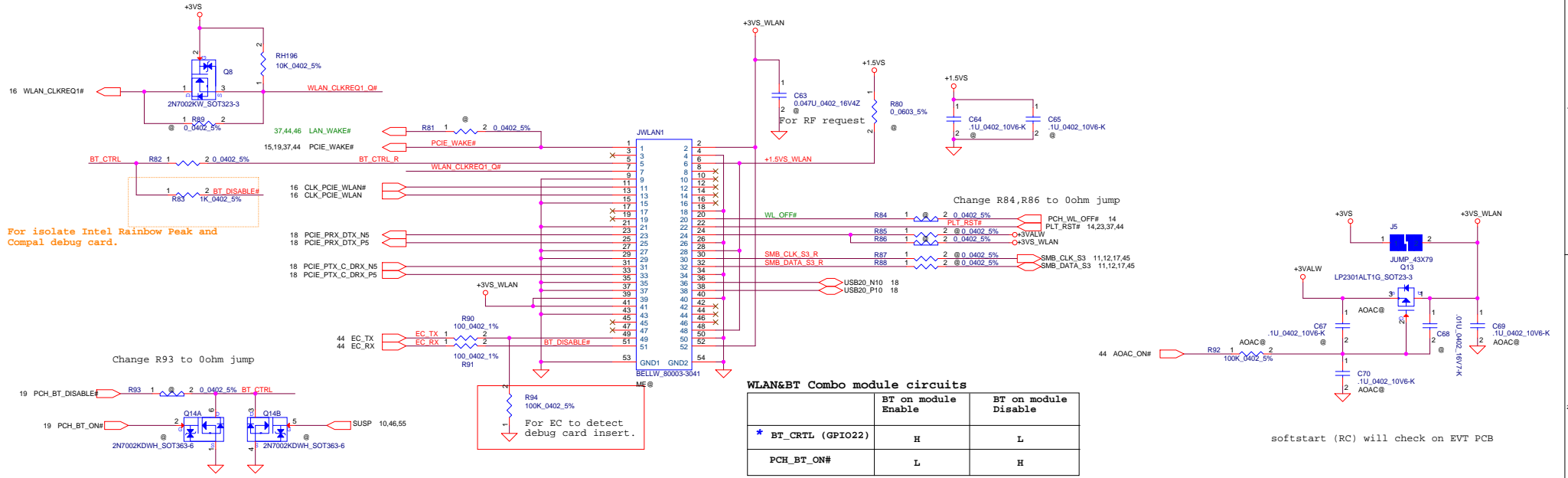


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



| | | | | |
|---|------------------------------|-----------------|------------|--------------------------------|
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| | | | | Document Number: 401025 |
| | | | | Rev: 1.1 |
| | | | | Date: Friday, July 12, 2013 |
| | | | | Sheet 39 of 61 |

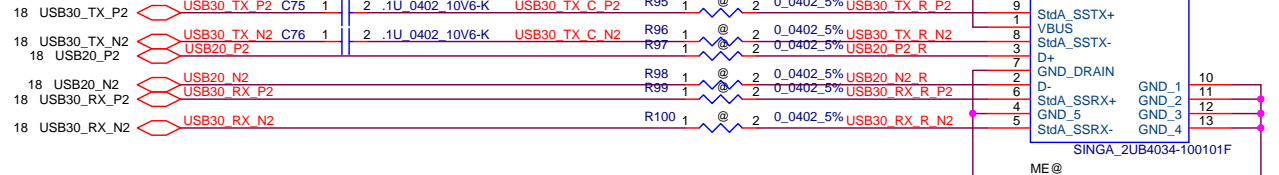
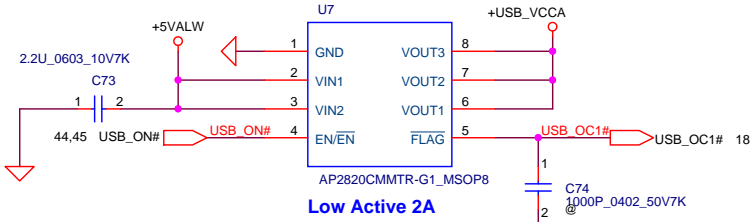
Mini-Express Card(WLAN/WiMAX)



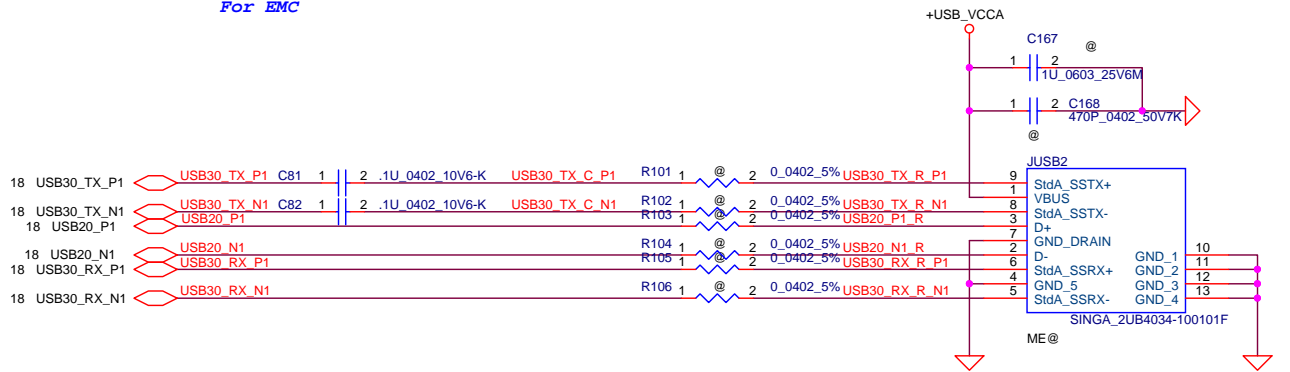
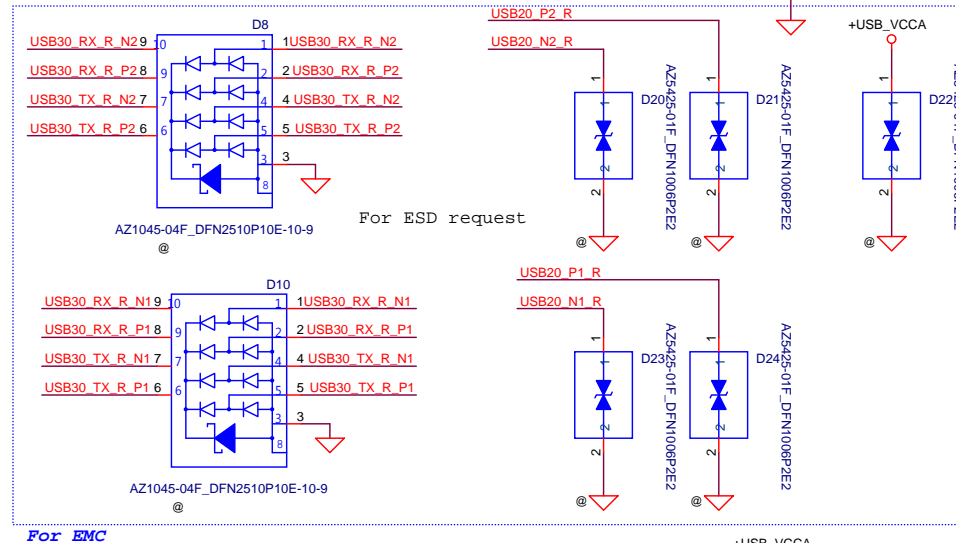
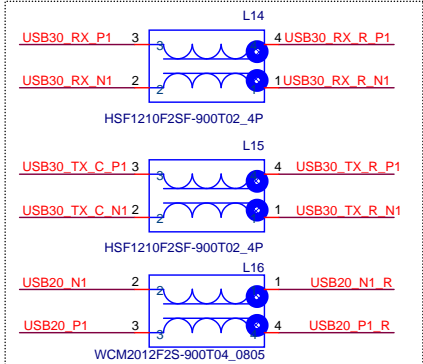
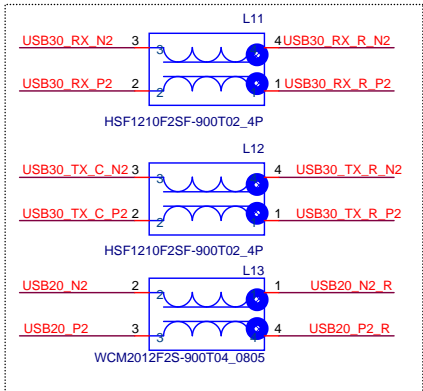
WLAN&BT Combo module circuits

| | BT on module Enable | BT on module Disable |
|--------------------|---------------------|----------------------|
| * BT_CTRL (GPIO22) | H | L |
| PCH_BT_ON# | L | H |

LEFT SIDE USB3.0 PORT X2



For EMI request
 USB2.0 choke ---> SM070001S0J
 USB3.0_Choke ---> SM070001S0J

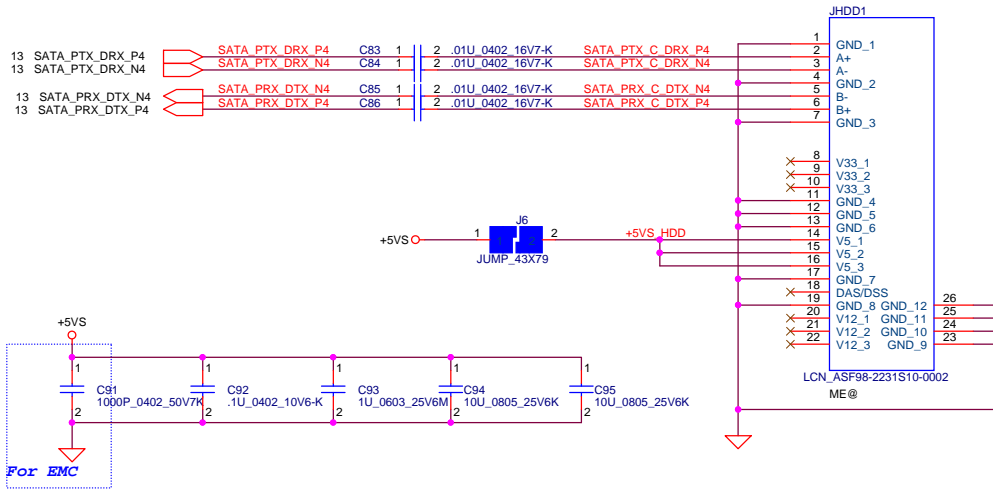


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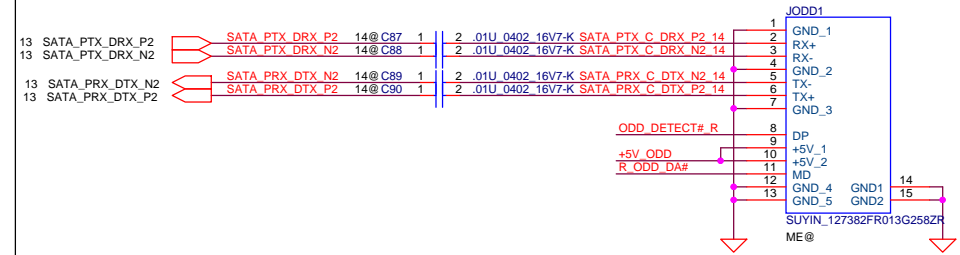
| | | |
|---------------------|-----------------------|----------------|
| Title | | |
| USB 3.0 PORT (LEFT) | | |
| Size | Document Number | 401025 |
| Custom | | |
| Date: | Friday, July 12, 2013 | Sheet 41 of 61 |

For EMC

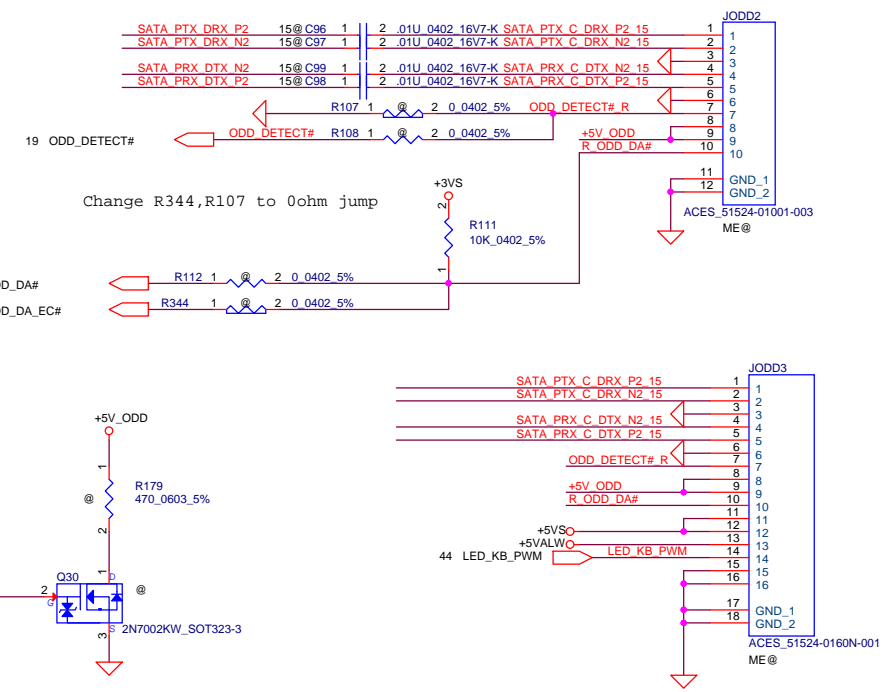
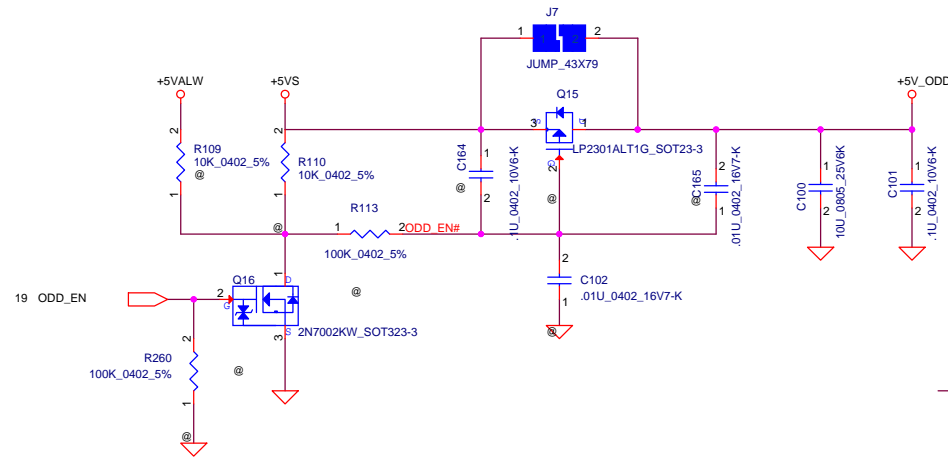
SATA HDD Conn.



FOR 14" SATA ODD Conn.

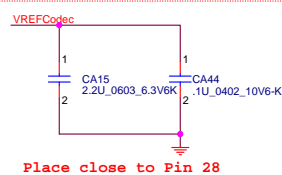
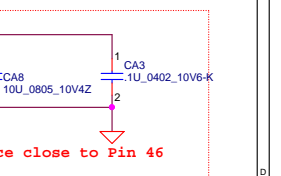
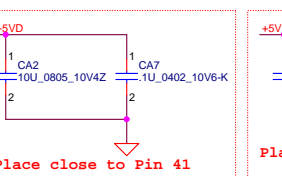
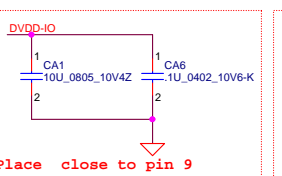
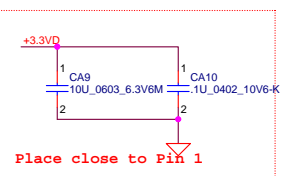
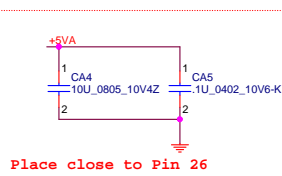
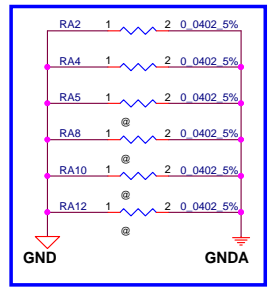
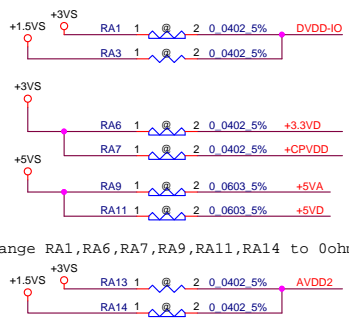


FOR 15" Co-lay SATA ODD FFC Conn JODD2& JODD3.



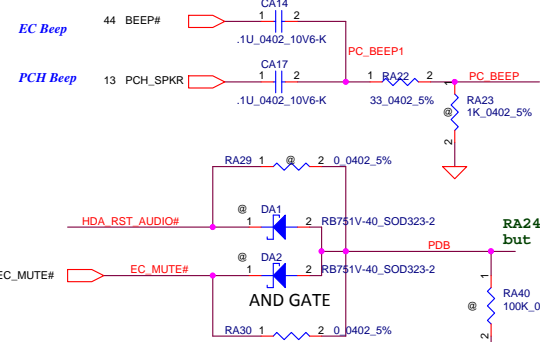
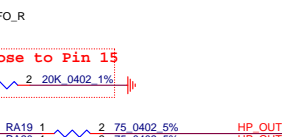
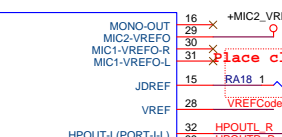
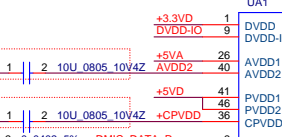
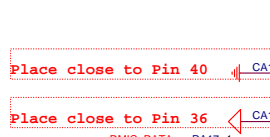
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| Issued Date | | | | 2012/12/14 | | Deciphered Date | | 2012/12/21 | |
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| Customer | | | | | | | 401025 | | 1.1 |
| Date: | | | | | | | Friday, July 12, 2013 | | Sheet 42 of 61 |



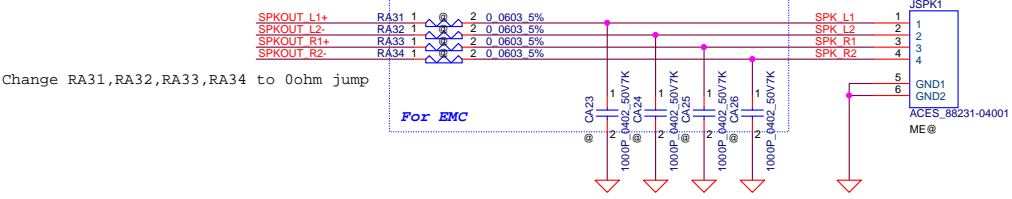
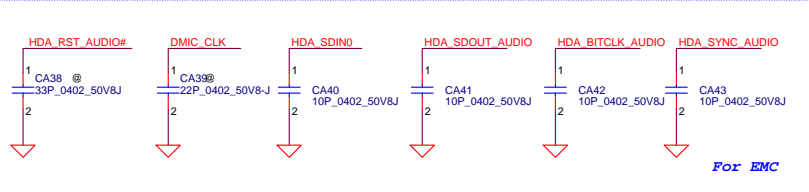
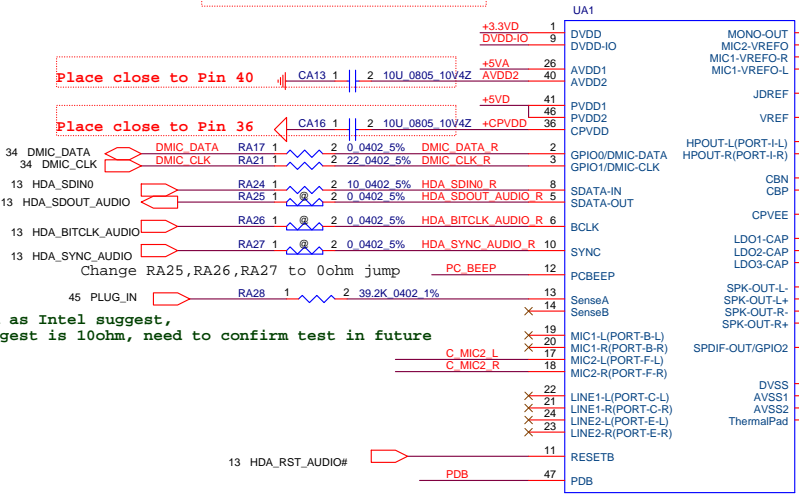


Change RA1, RA6, RA7, RA9, RA11, RA14 to 0ohm jump

If AVDD2 is design to 1.5V, you will get better power consumption.



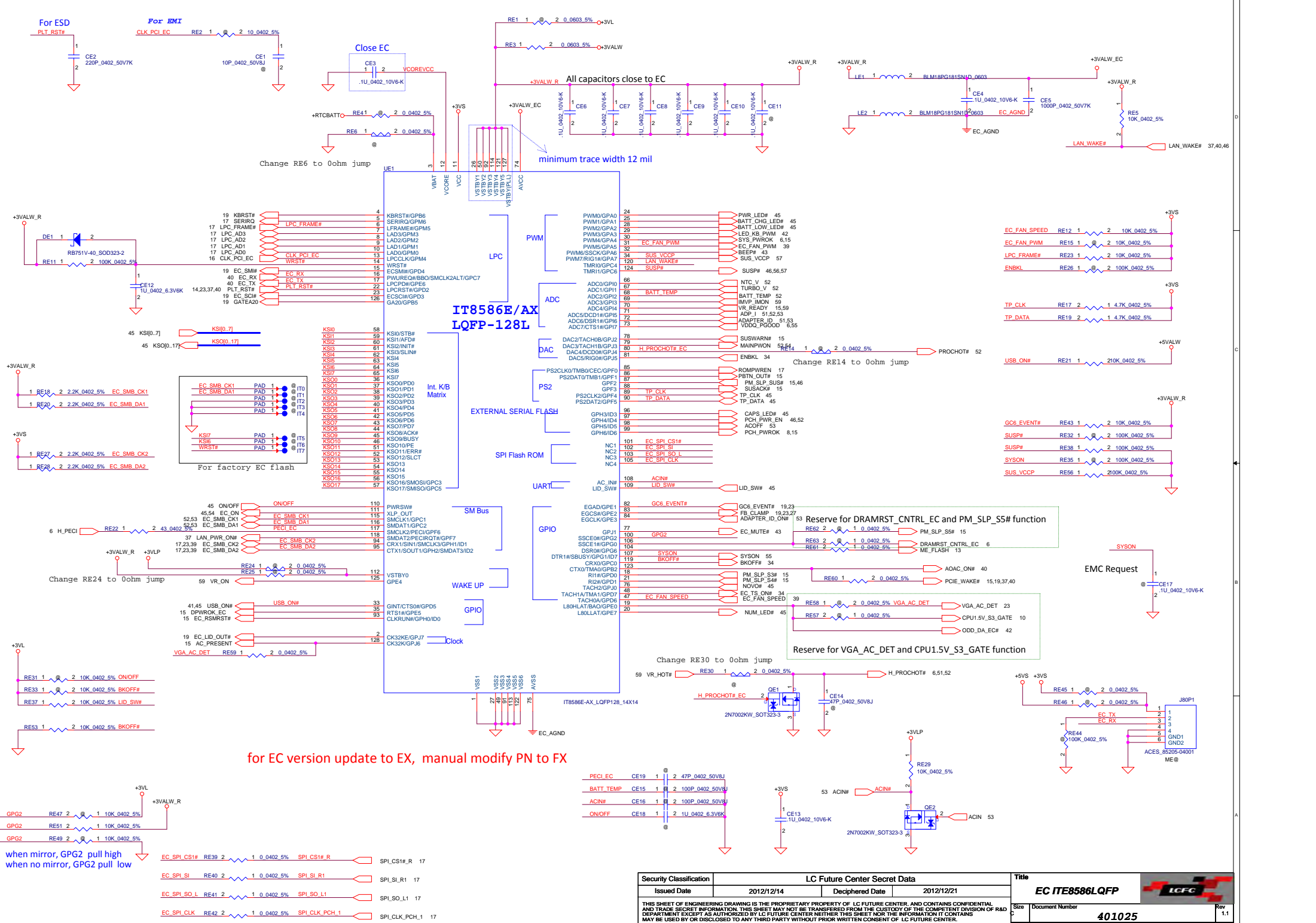
RA24 is 33ohm as Intel suggest, but codec suggest is 10ohm, need to confirm test in future



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Audio Codec_ALC282

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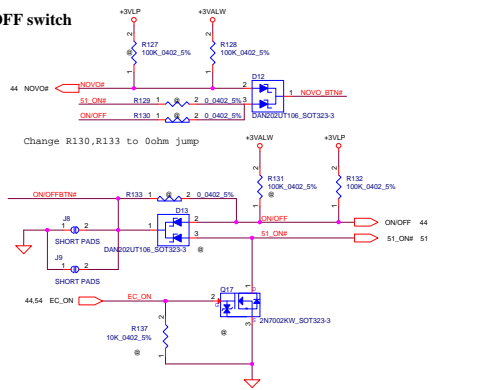
for EC version update to EX, manual modify PN to FX

- EC SPI_CS1# RE39 2 1 0.0402 5% SPI_CS1#_R
- EC SPI_SI RE40 2 1 0.0402 5% SPI_SI_R1
- EC SPI_SO_L RE41 2 1 0.0402 5% SPI_SO_L1
- EC SPI_CLK RE42 2 1 0.0402 5% SPI_CLK_PCH_1

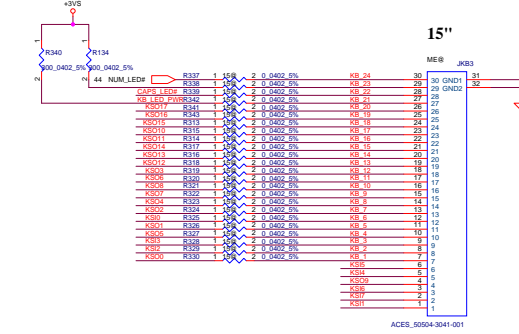
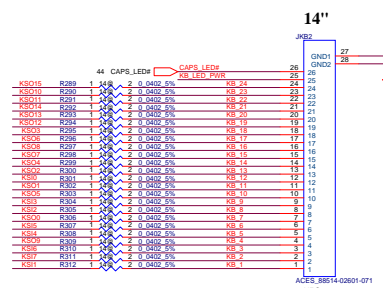
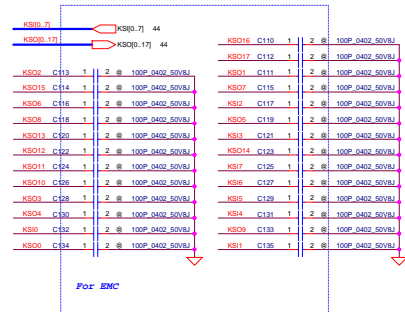
| Security Classification | LC Future Center Secret Data | |
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| Issued Date | 2012/12/14 | Deciphered Date |
| | | 2012/12/21 |
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| EC ITE8586LQFP | | |
| Size | Document Number | |
| | 401025 | |
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ON/OFF switch

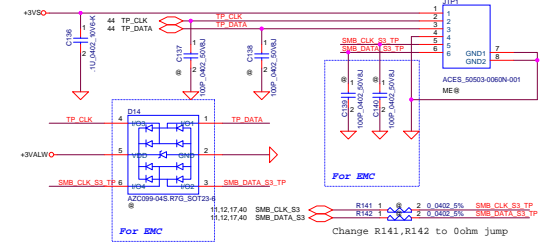


K/B Connector

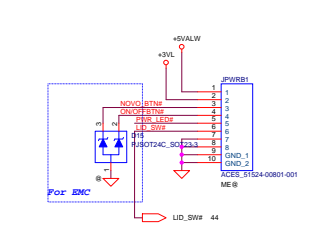


| | | |
|-------|---------|---------------|
| KB_1 | KS11_14 | KS00_15 |
| KB_2 | KS17_14 | KS12_15 |
| KB_3 | KS16_14 | KS13_15 |
| KB_4 | KS09_14 | KS05_15 |
| KB_5 | KS14_14 | KS10_15 |
| KB_6 | KS15_14 | KS10_15 |
| KB_7 | KS00_14 | KS02_15 |
| KB_8 | KS12_14 | KS07_15 |
| KB_9 | KS13_14 | KS07_15 |
| KB_10 | KS05_14 | KS08_15 |
| KB_11 | KS01_14 | KS06_15 |
| KB_12 | KS10_14 | KS03_15 |
| KB_13 | KS02_14 | KS02_15 |
| KB_14 | KS04_14 | KS03_15 |
| KB_15 | KS07_14 | KS04_15 |
| KB_16 | KS08_14 | KS01_15 |
| KB_17 | KS06_14 | KS01_15 |
| KB_18 | KS03_14 | KS05_15 |
| KB_19 | KS02_14 | KS06_15 |
| KB_20 | KS01_14 | KS07_15 |
| KB_21 | KS04_14 | KB_LED_PWR_15 |
| KB_22 | KS01_14 | CAPS_LED#_15 |
| KB_23 | KS01_14 | VDD_15 |
| KB_24 | KS01_14 | NUM_LED#_15 |

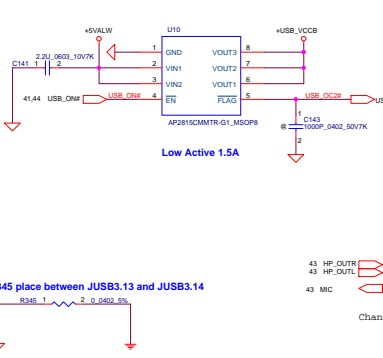
TP/B Connector



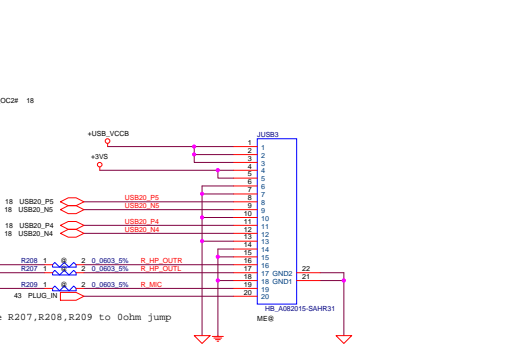
PWR/B Connector



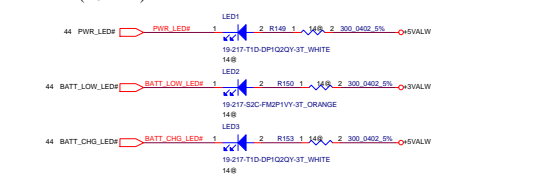
Right Side USB2.0 Port X 1 (USB/B)



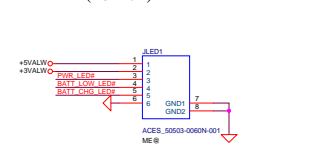
USB I/O Connector



LED (For 14")

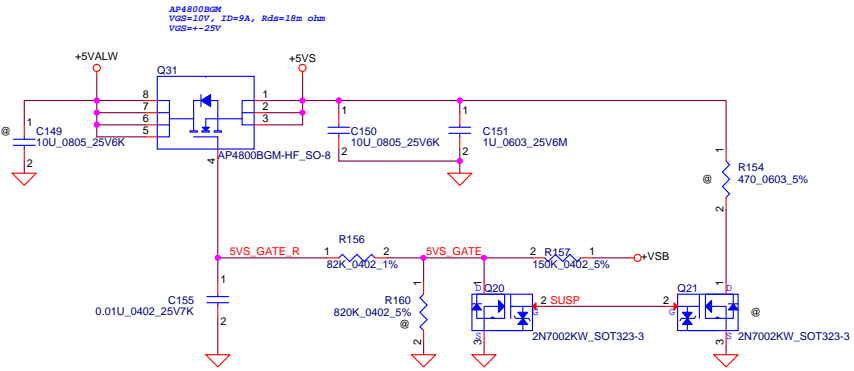


LED (For 15")

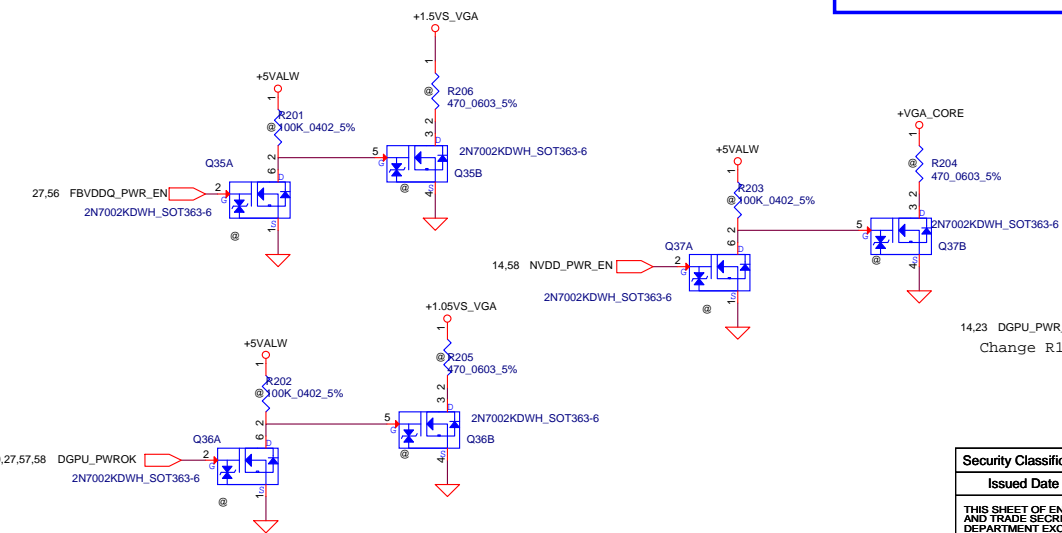
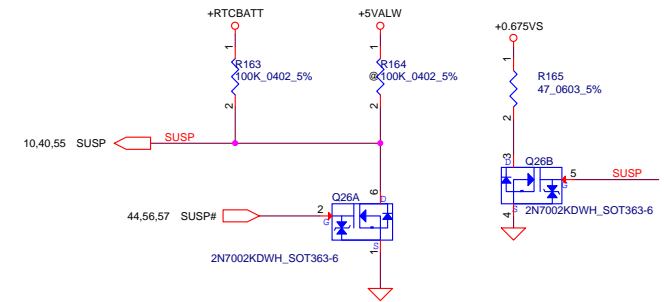
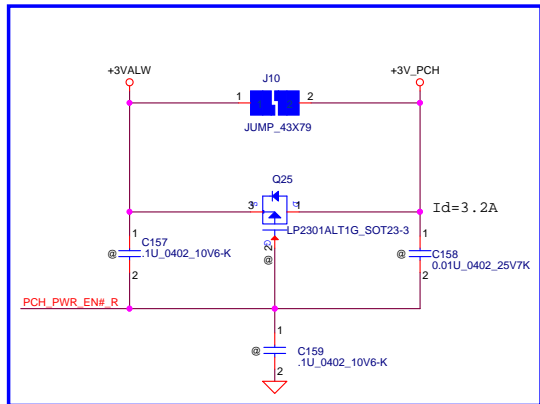
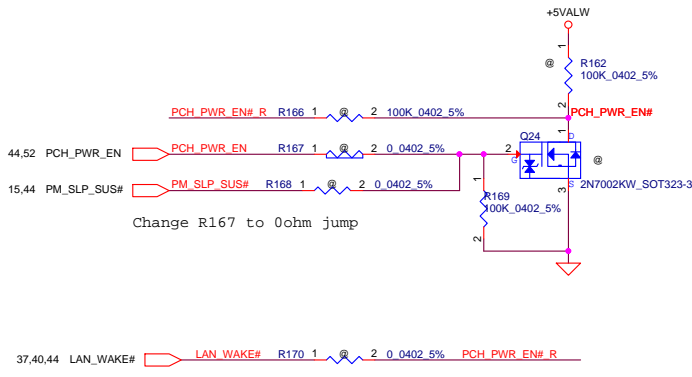
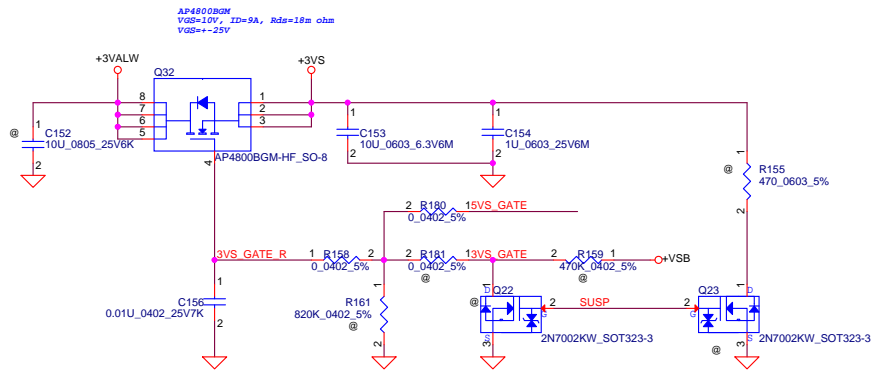


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| Size | Document Number | Rev | 1.1 |
| Count | 401025 | Date | Friday, 30/12/2012 |
| Sheet | 45 | of | 61 |

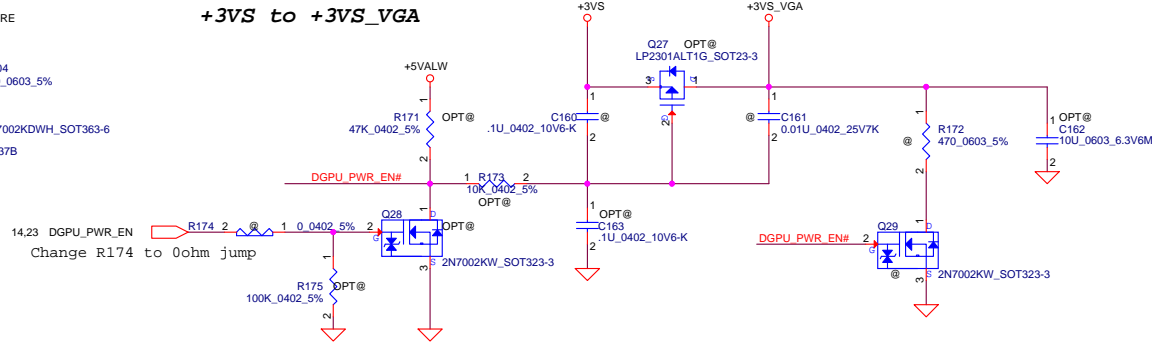
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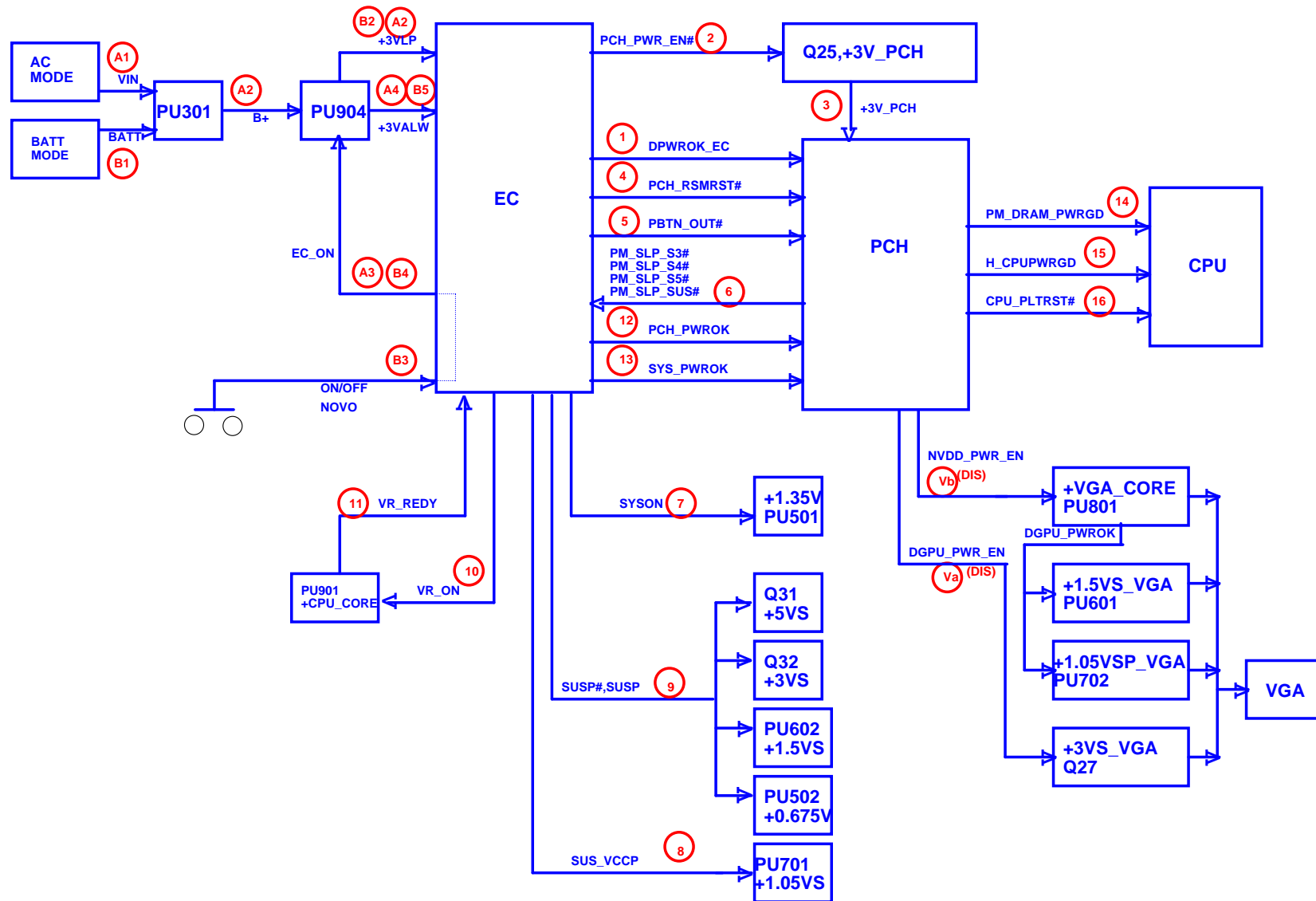
+3VALW to +3VS



+3VS to +3VS_VGA



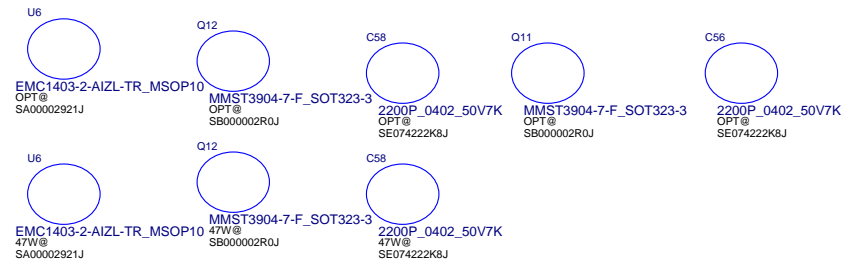
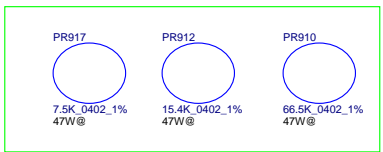
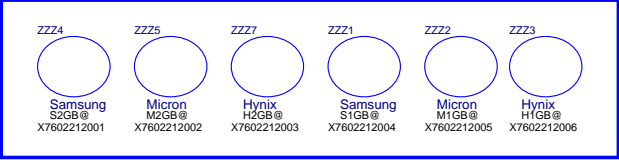
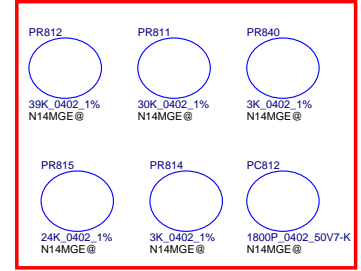
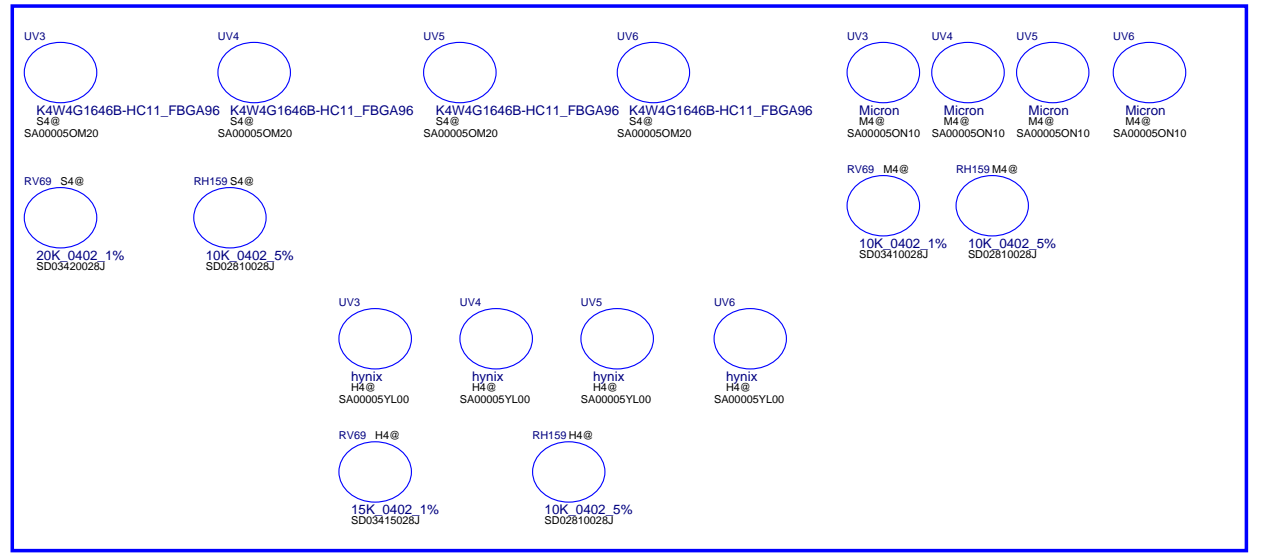
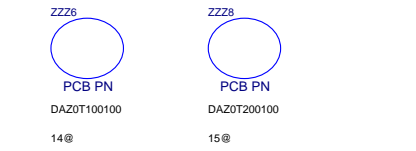
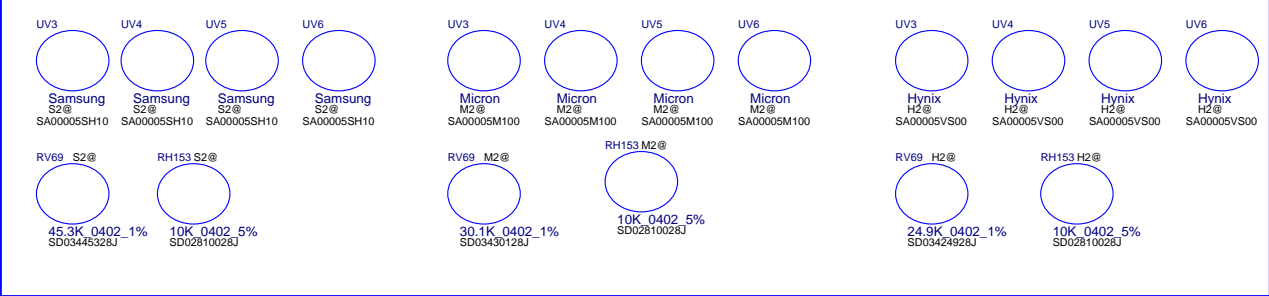
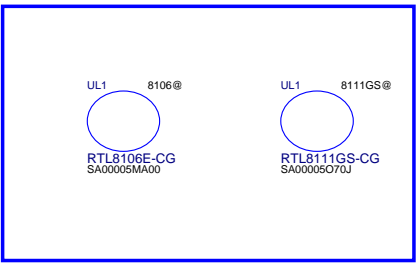
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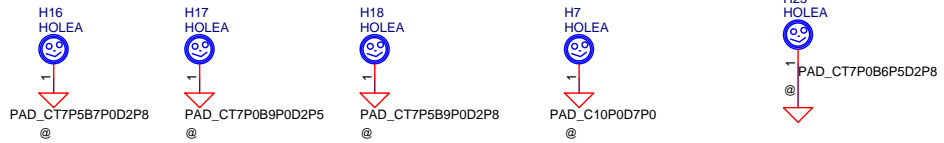
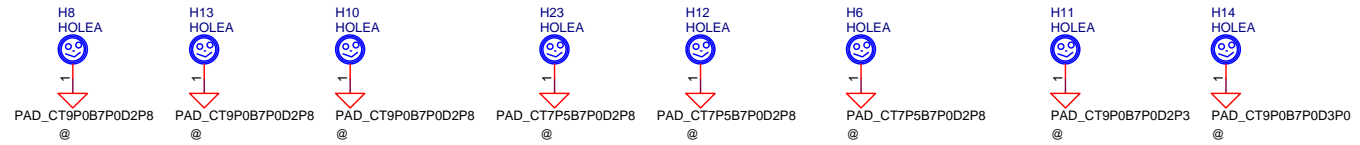
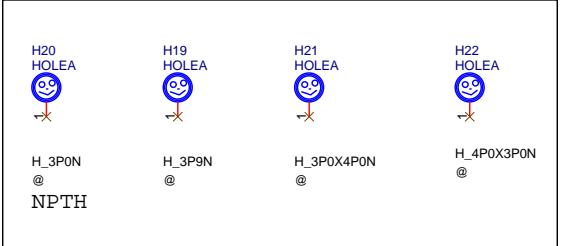
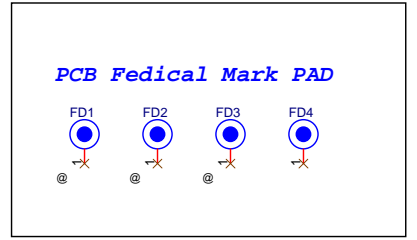
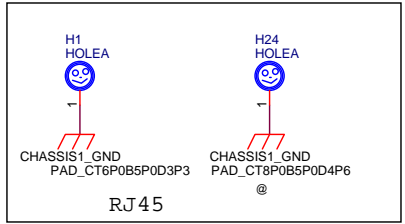
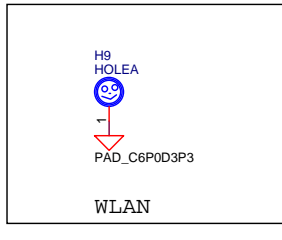
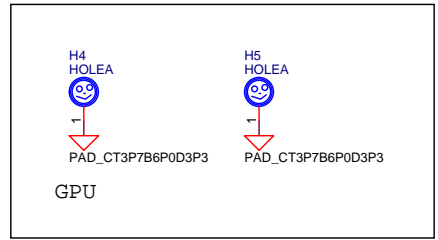
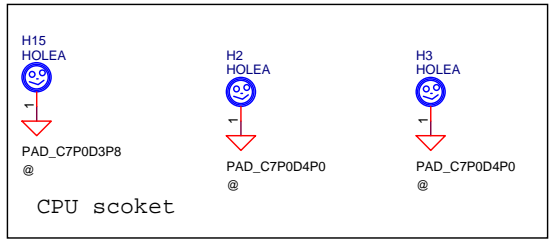
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| Title | Power sequence Block | |
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| Date: | Friday, July 12, 2013 | Sheet 47 of 61 |
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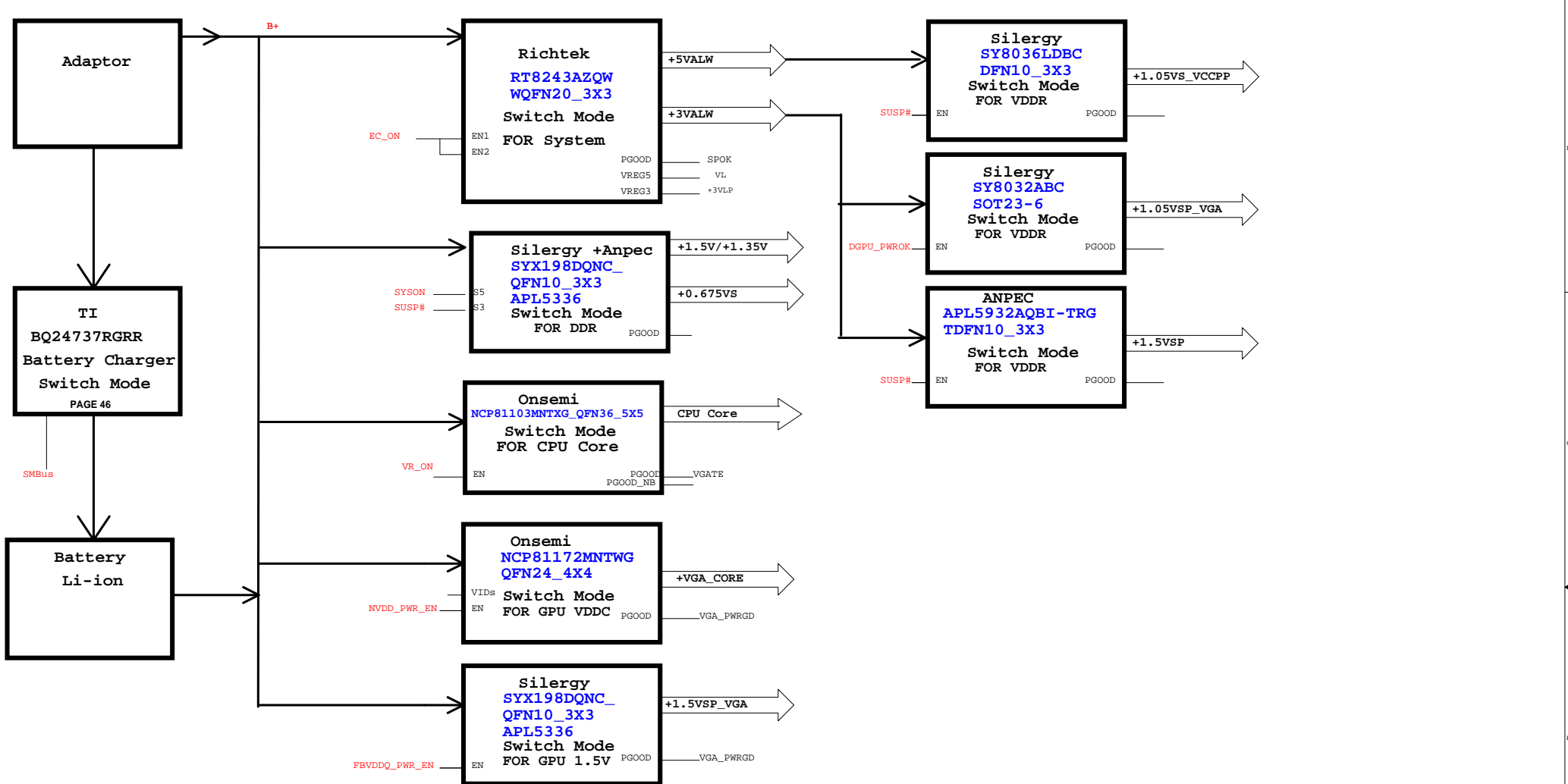





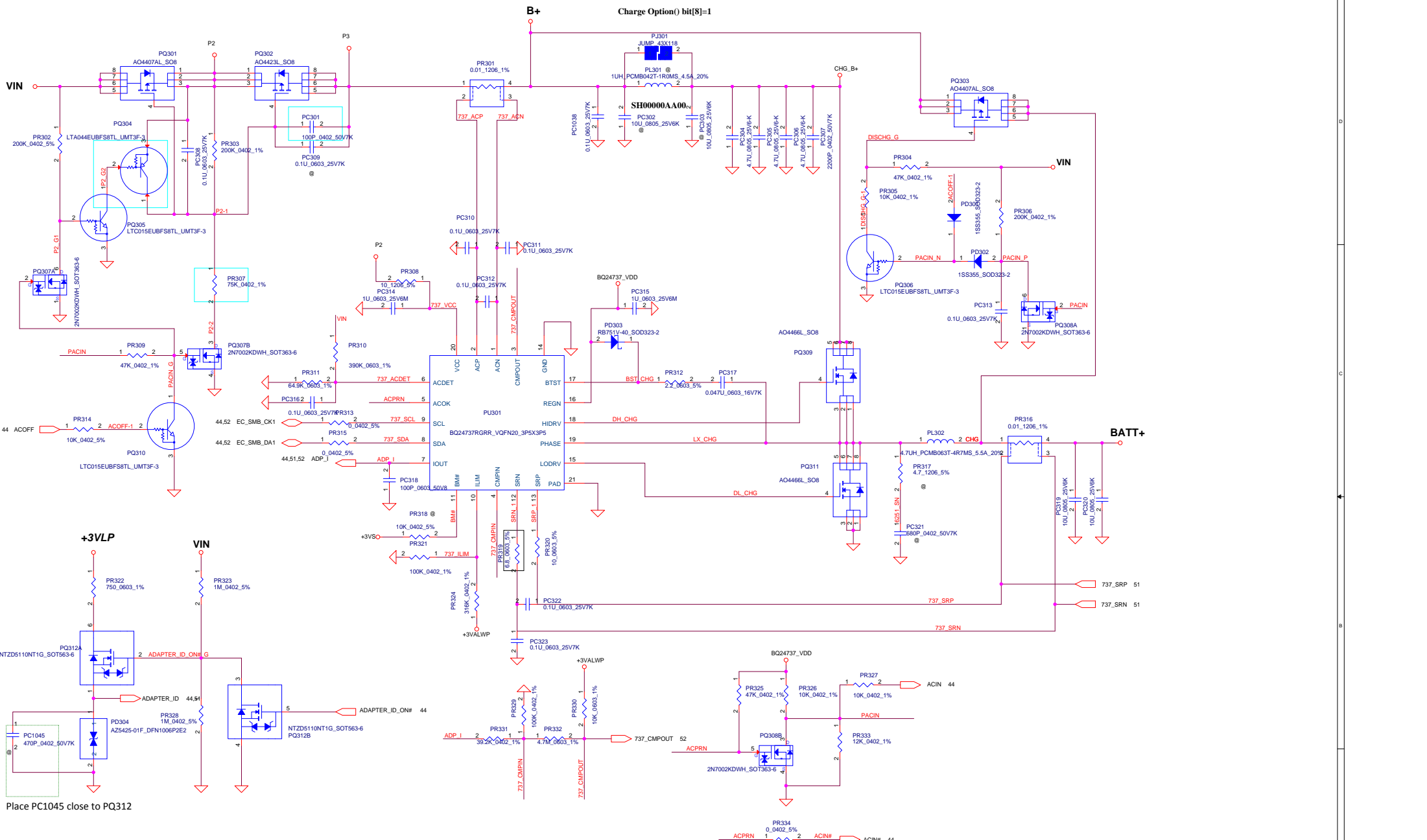
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| Issued Date | 2012/12/14 | Deciphered Date | 2012/12/21 | |
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| | | | | Rev: 0.3 Sheet: 48 of 61 |



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| | | | | Date: | Friday, July 12, 2013 |
| | | | | Sheet | 49 of 61 |
| | | | | Rev | 1.1 |
| | | | | Document Number | 401025 |

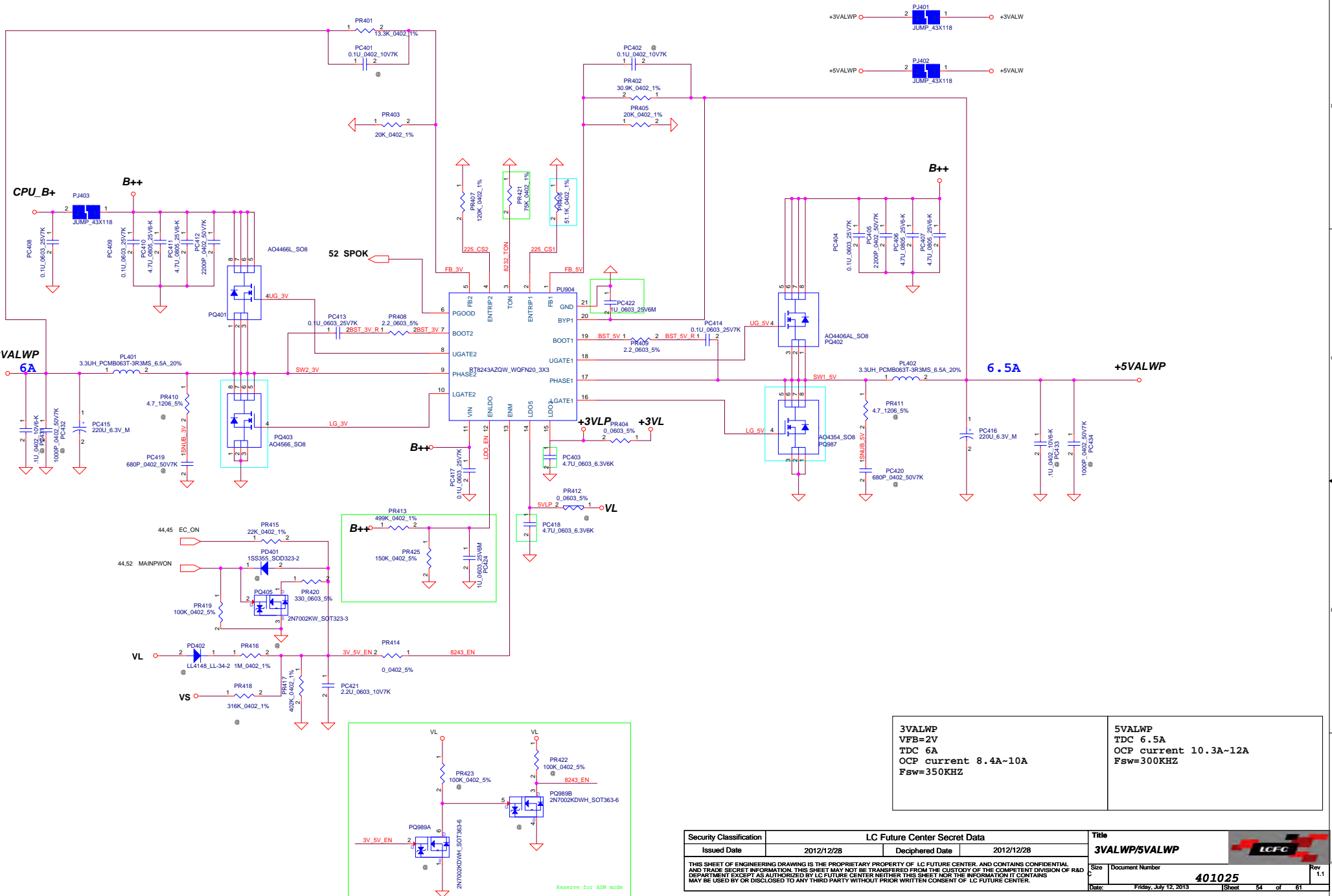


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| | | | | 4 | 401025 | 1.1 |
| | | | | Date: | Friday, July 12, 2013 | Sheet 50 of 61 |



Place PC1045 close to PQ312

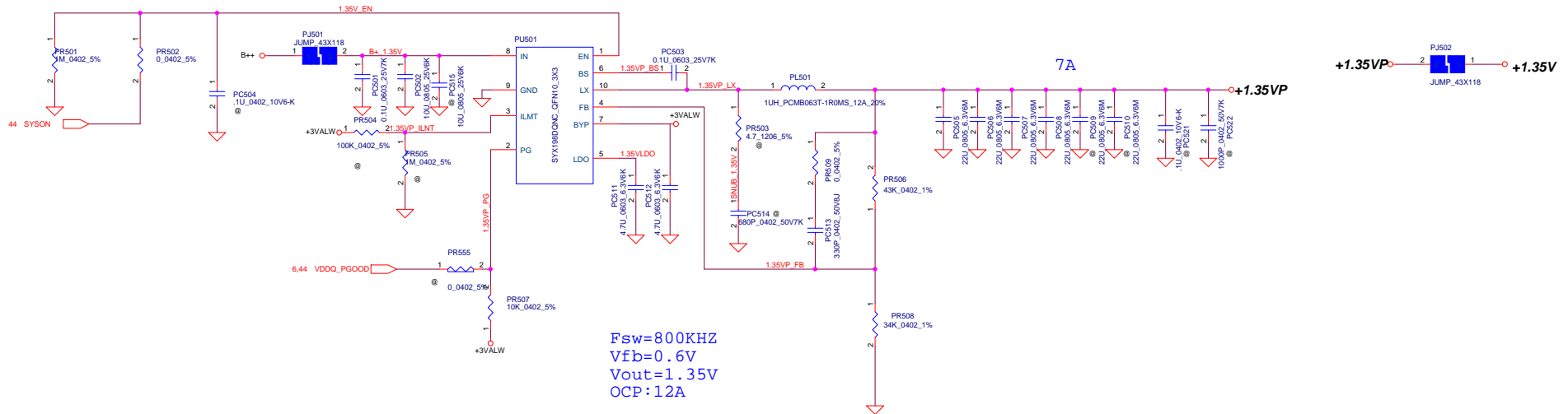
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| Size | Document Number | 401025 | | 1-1 |
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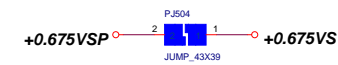
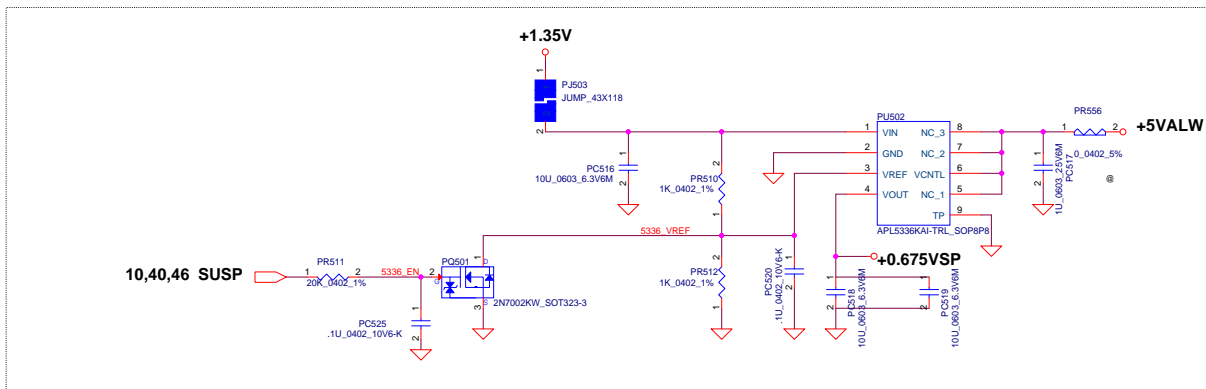
| | |
|---|--|
| 3VALWP VFB=2V TDC 6A OCP current 8.4A-10A Fsw=350KHZ | 5VALWP TDC 6.5A OCP current 10.3A-12A Fsw=300KHZ |
|---|--|

| | | | | | |
|--|-----------------------|------------------------------|------------|----------------------|-----|
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| Issued Date | 2012/12/28 | Deciphered Date | 2012/12/28 | 3VALWP/5VALWP | |
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| Date: | Friday, July 12, 2013 | Sheet | 54 | of | 61 |

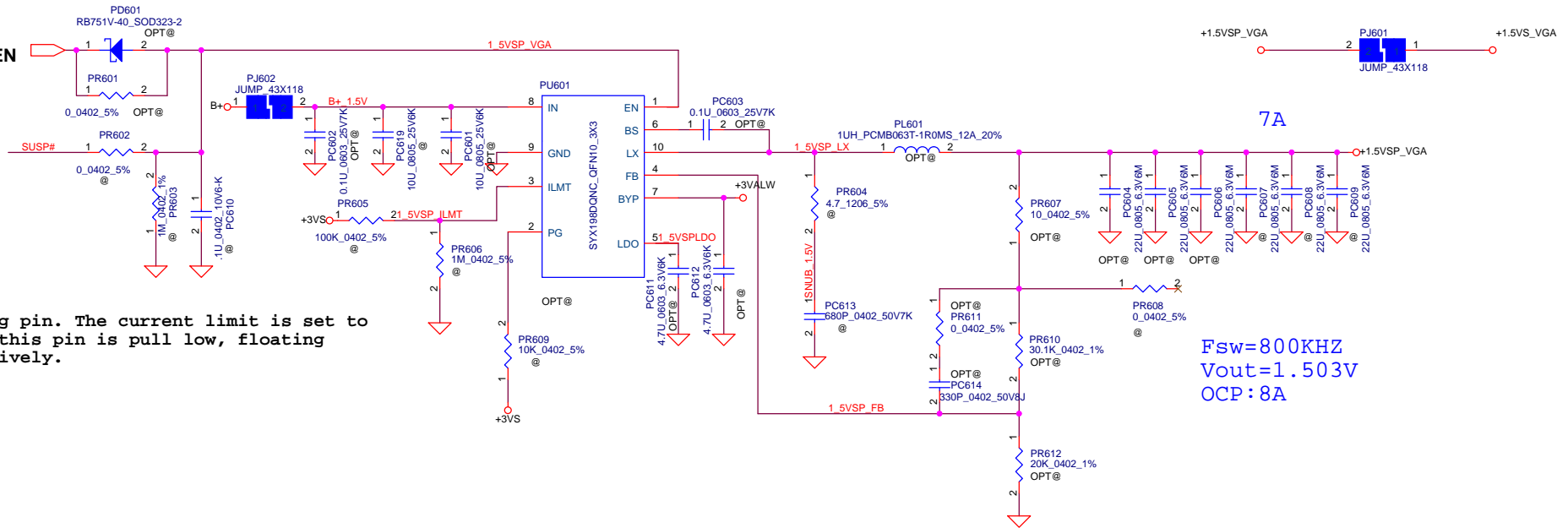




Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.



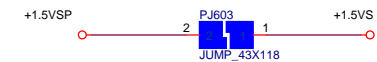
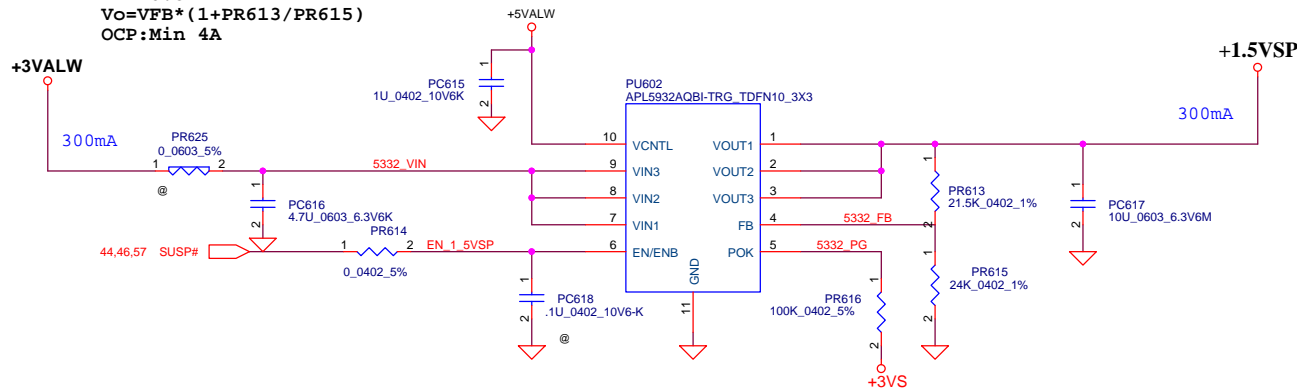
27,46 FBVDDQ_PWR_EN



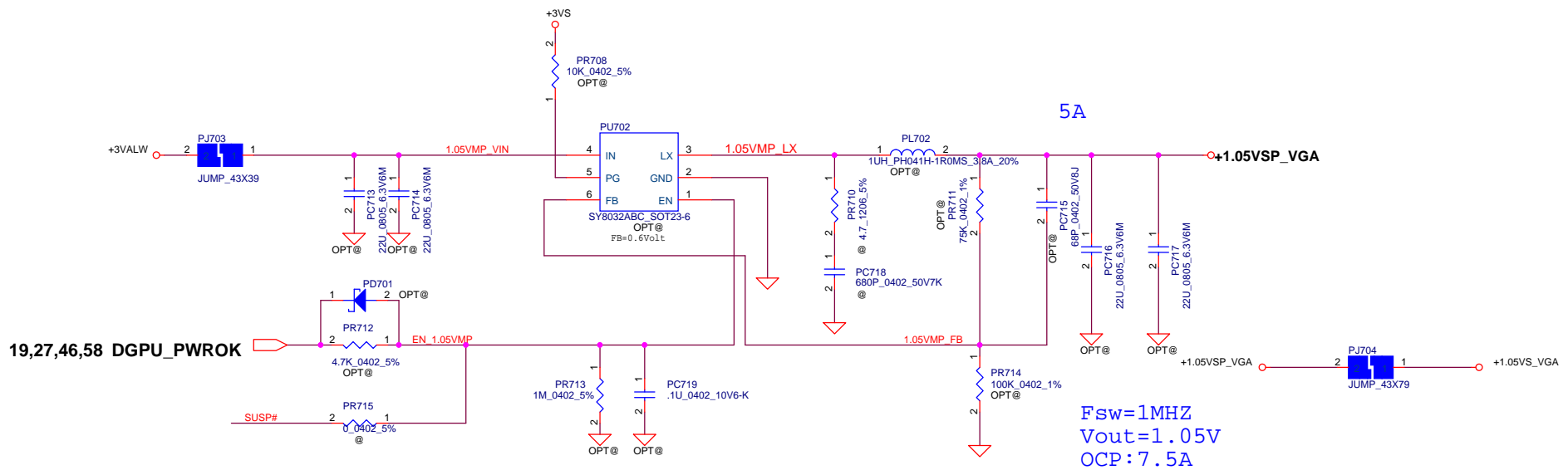
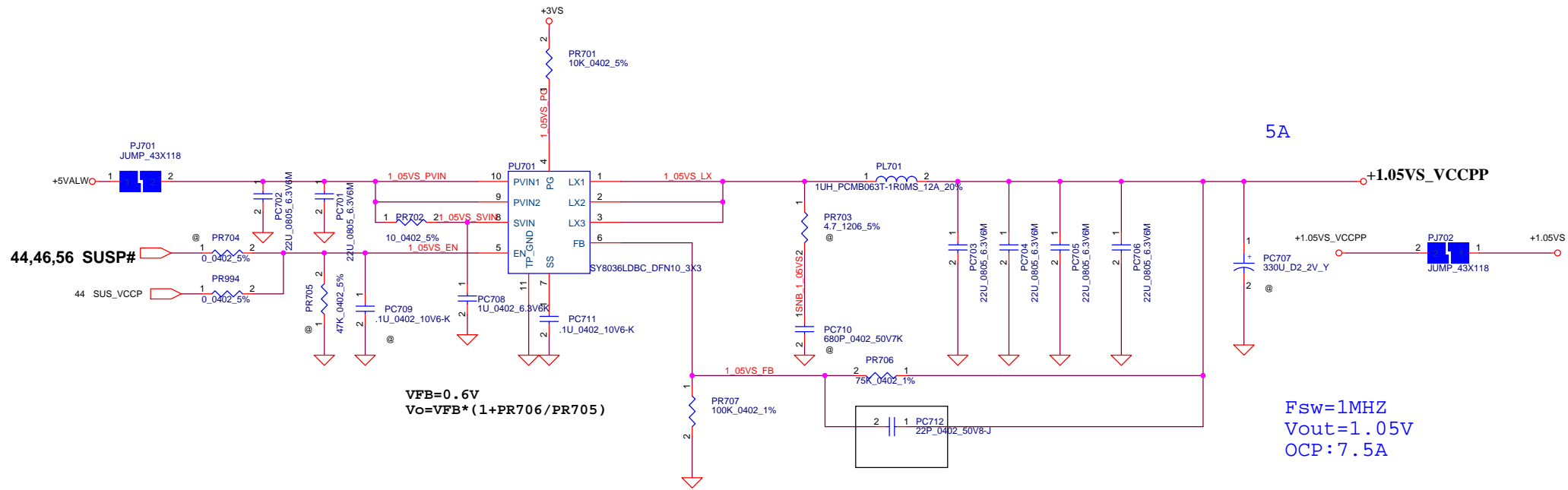
Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

Fsw=800KHZ
Vout=1.503V
OCP: 8A

VFB=0.8V
Vo=VFB*(1+PR613/PR615)
OCP:Min 4A



| | | | | | | |
|---|-----------------------|------------------------------|------------|--------------------|-----|-----|
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| Date: | Friday, July 12, 2013 | Sheet | 56 | of | 61 | |



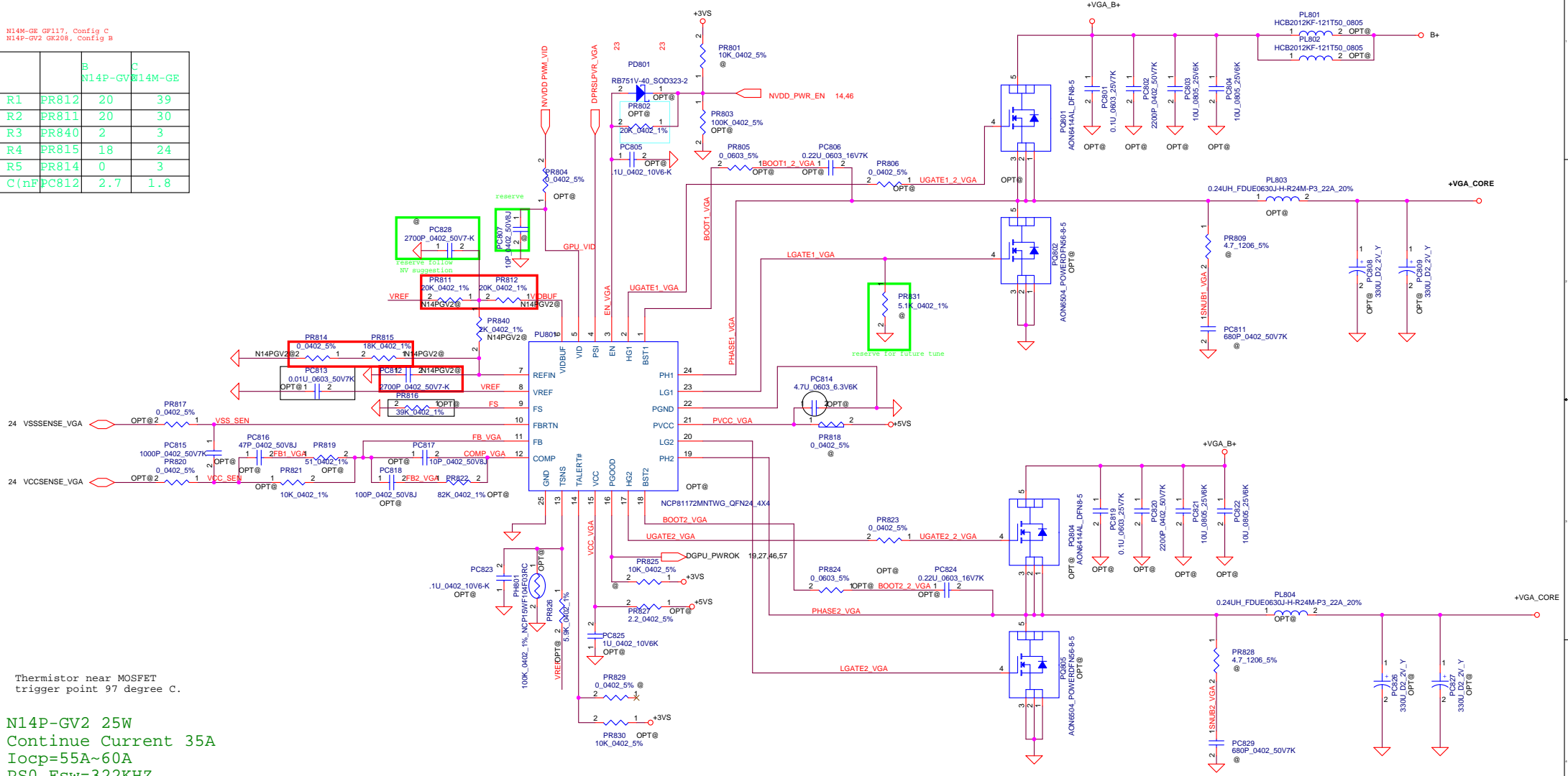
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N14M-GE GP117, Config C
 N14P-GV2 GR208, Config B

| | B | C |
|-------|-----------|-----|
| R1 | PR812 20 | 39 |
| R2 | PR811 20 | 30 |
| R3 | PR840 2 | 3 |
| R4 | PR815 18 | 24 |
| R5 | PR814 0 | 3 |
| C(nF) | PC812 2.7 | 1.8 |

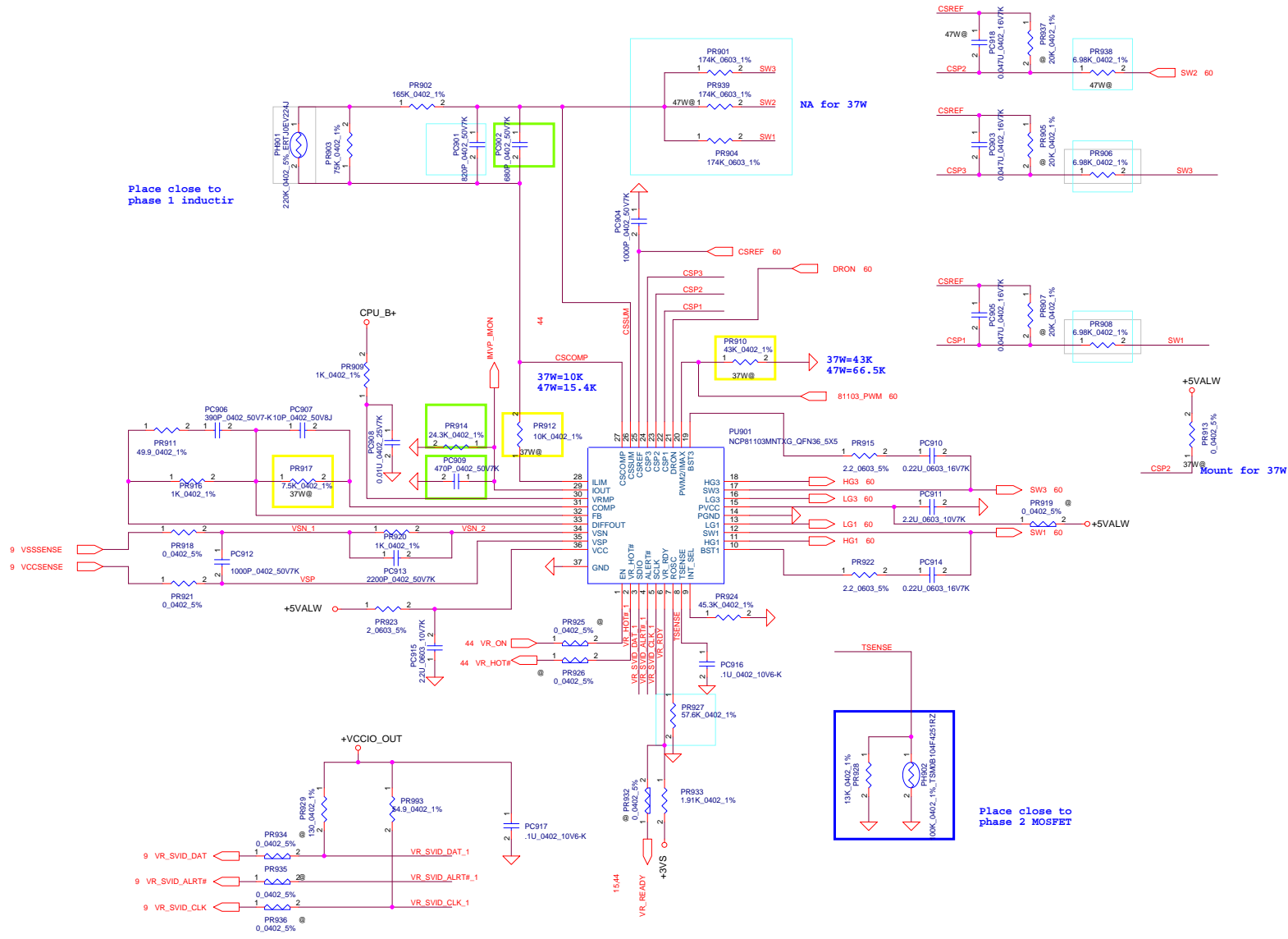
N14P-GV2 25W
 Continue Current 35A
 I_ocp=55A~60A
 PS0 F_{sw}=322KHZ
 PS1/PS2 F_{sw}=475KHZ
 V_{boot}=0.9V


Thermistor near MOSFET
 trigger point 97 degree C.




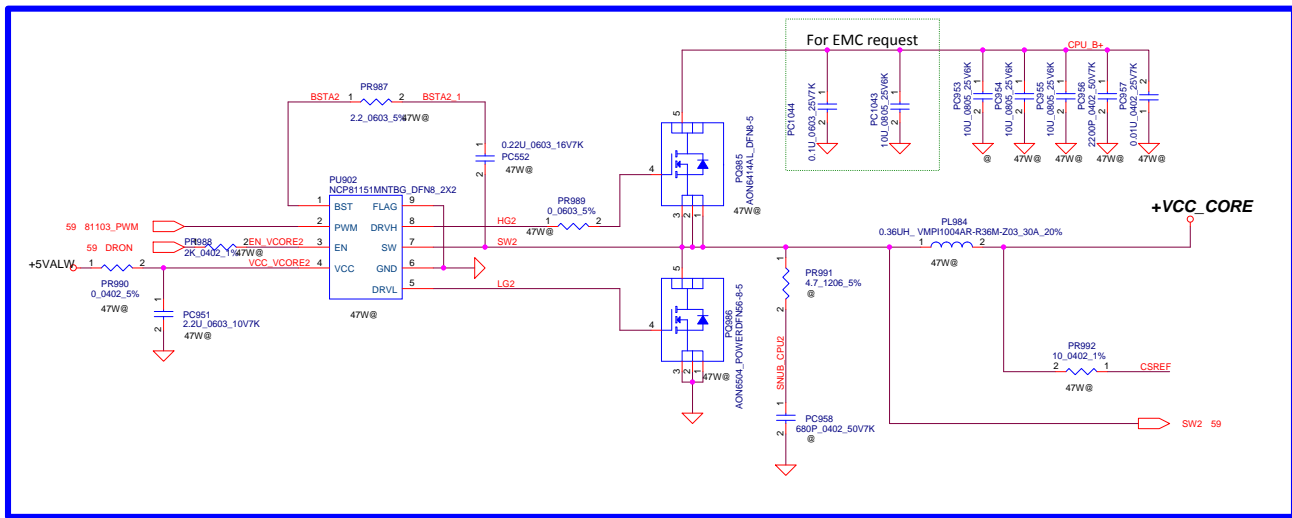
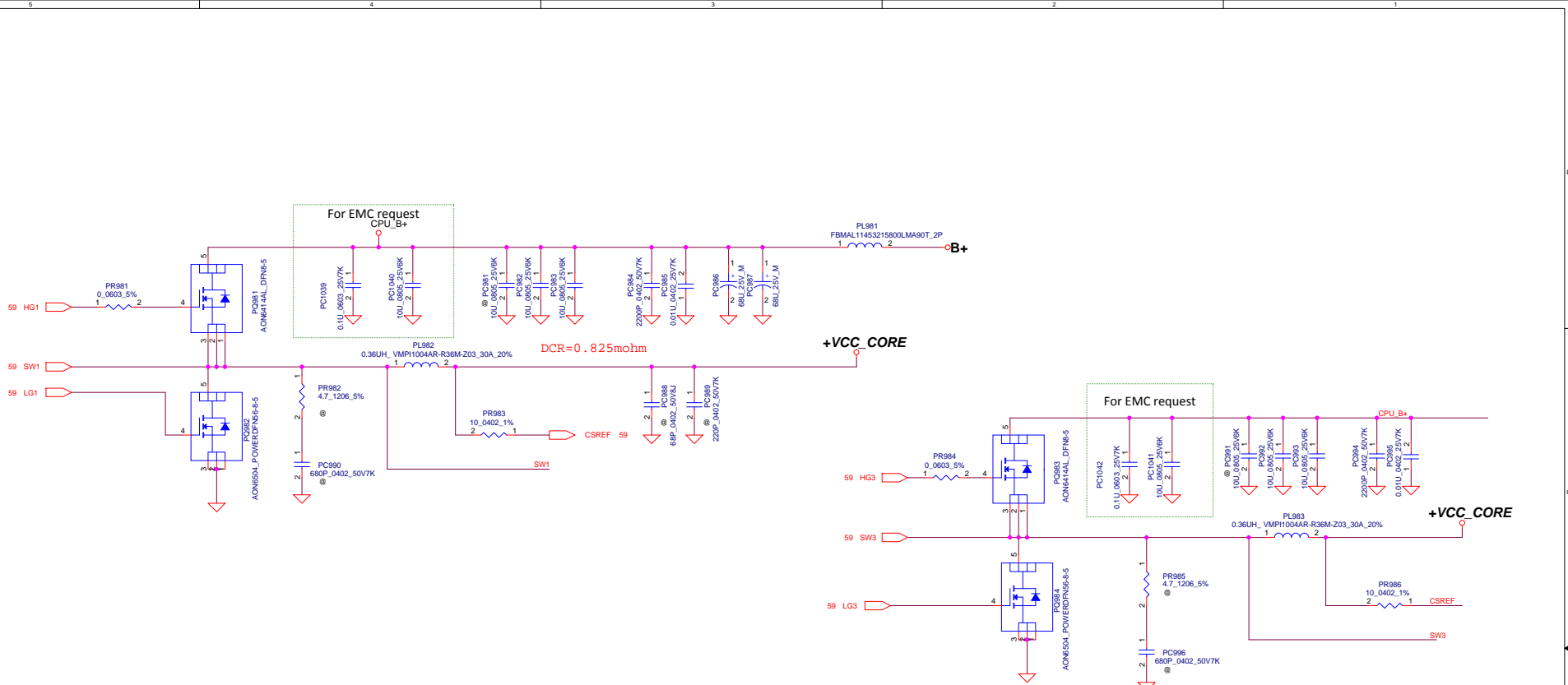
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| Custom | 401025 | 1.1 | |
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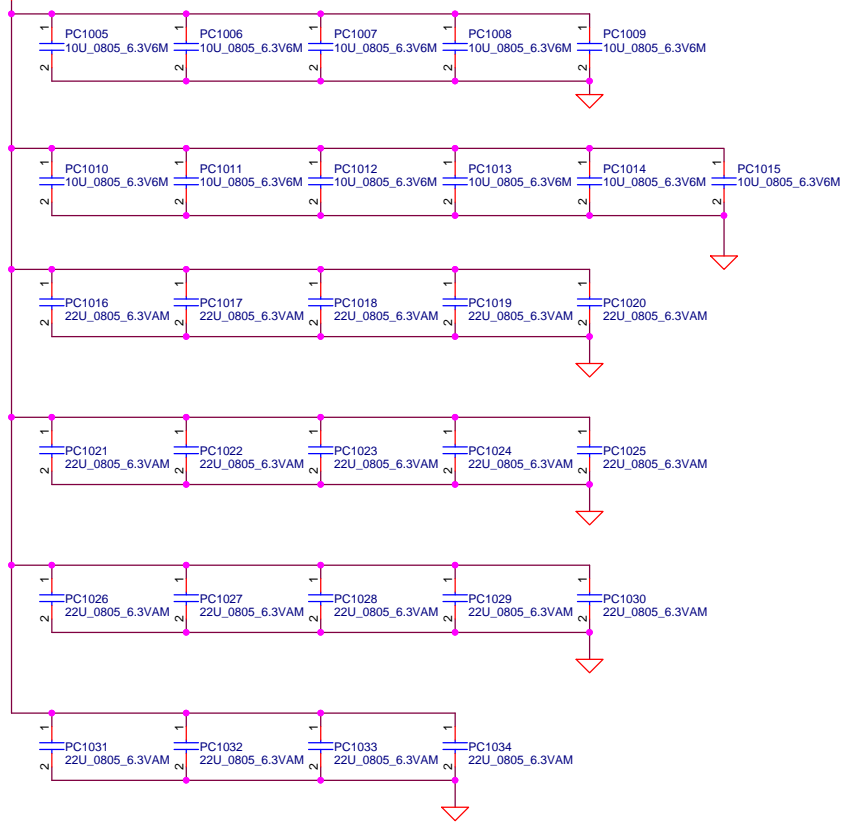
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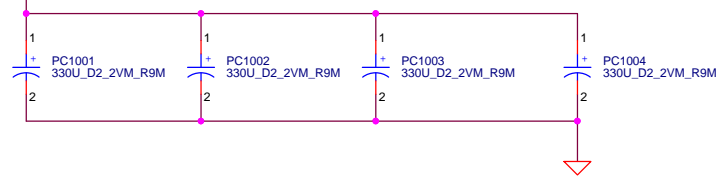



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