

P2132-A01

NVG GK208 DDR3 64BIT DVI-I/DVI-D + HDMI + VGA

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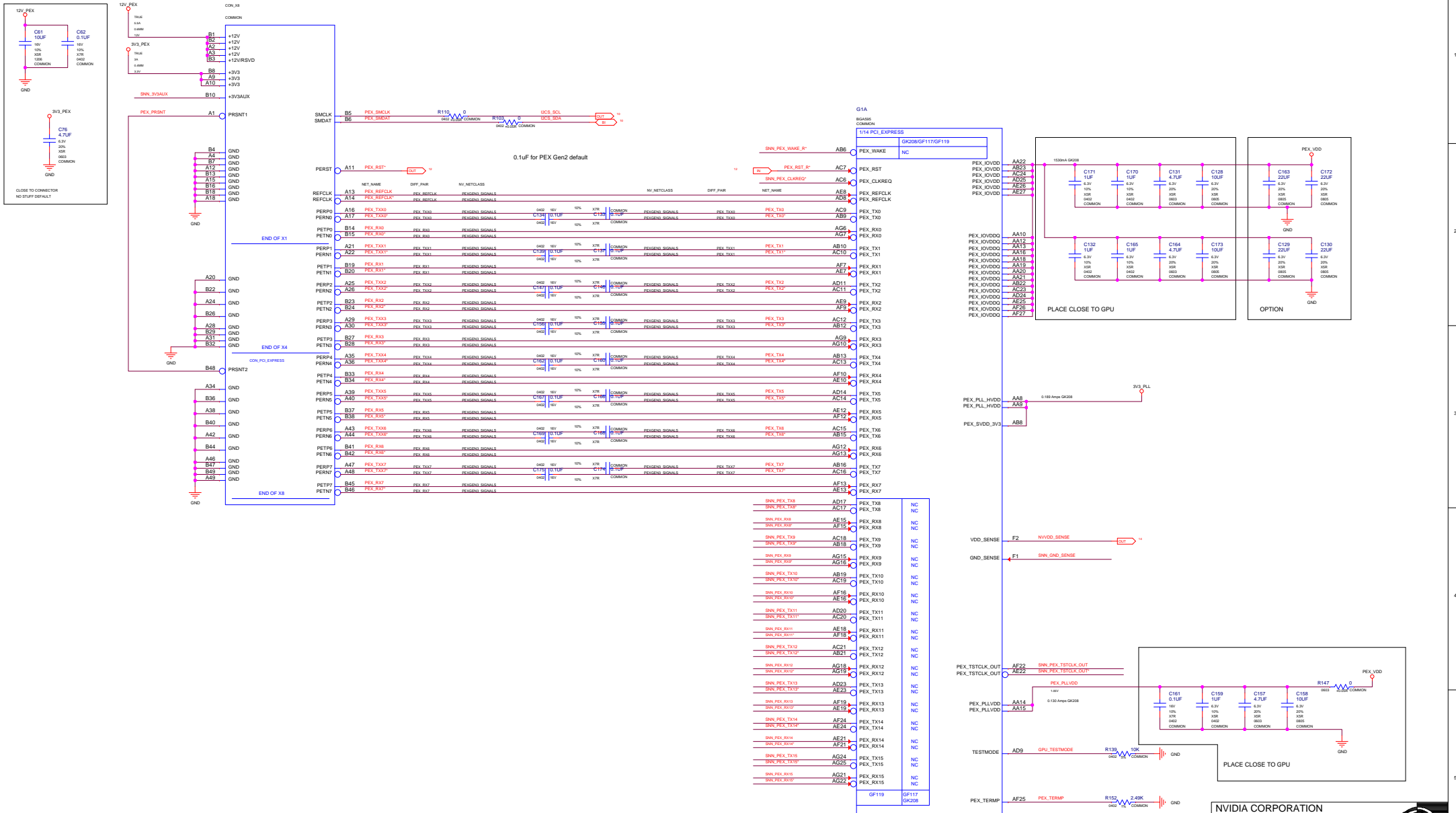
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PCI EXPRESS



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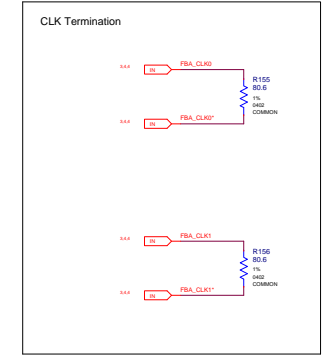
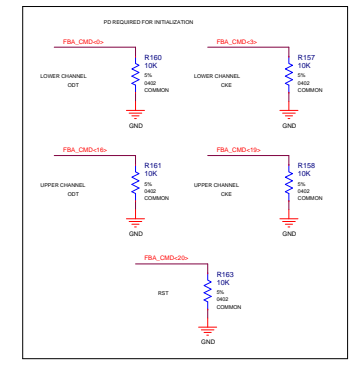
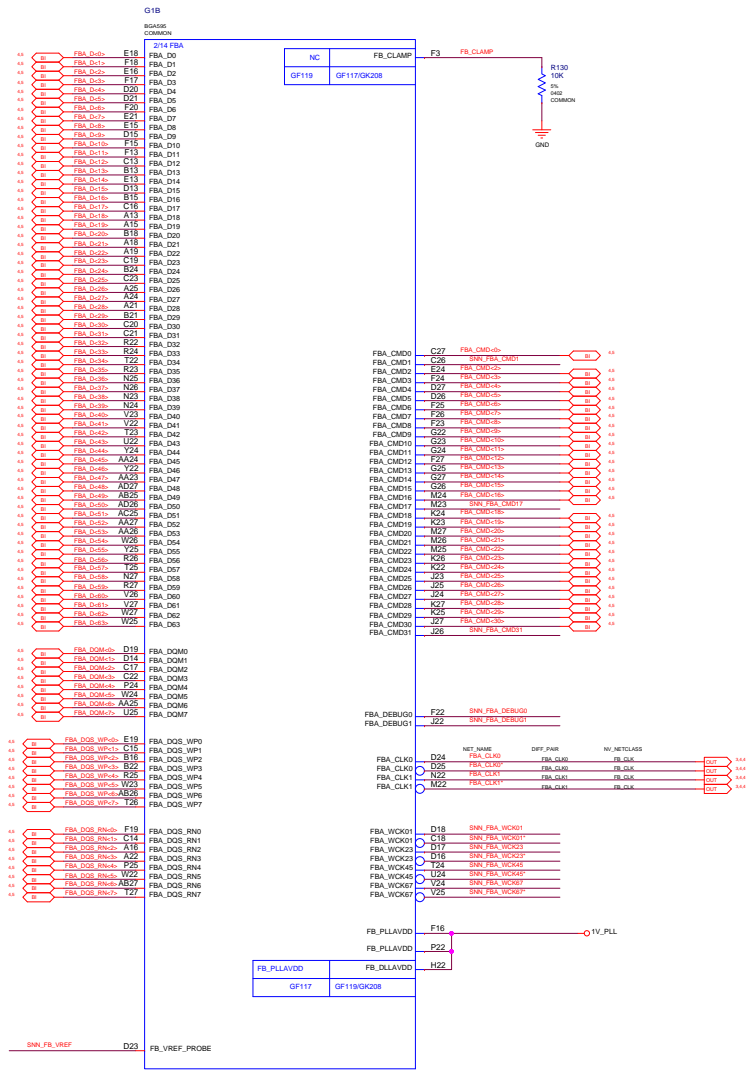
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GPU FRAME BUFFER: PARTITION A

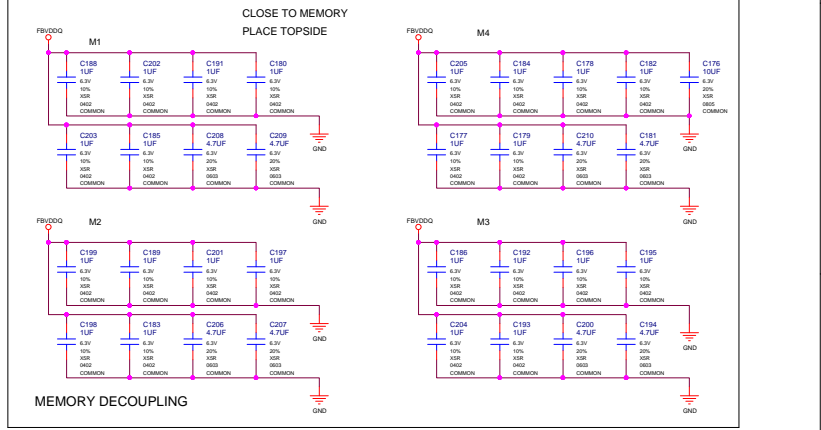
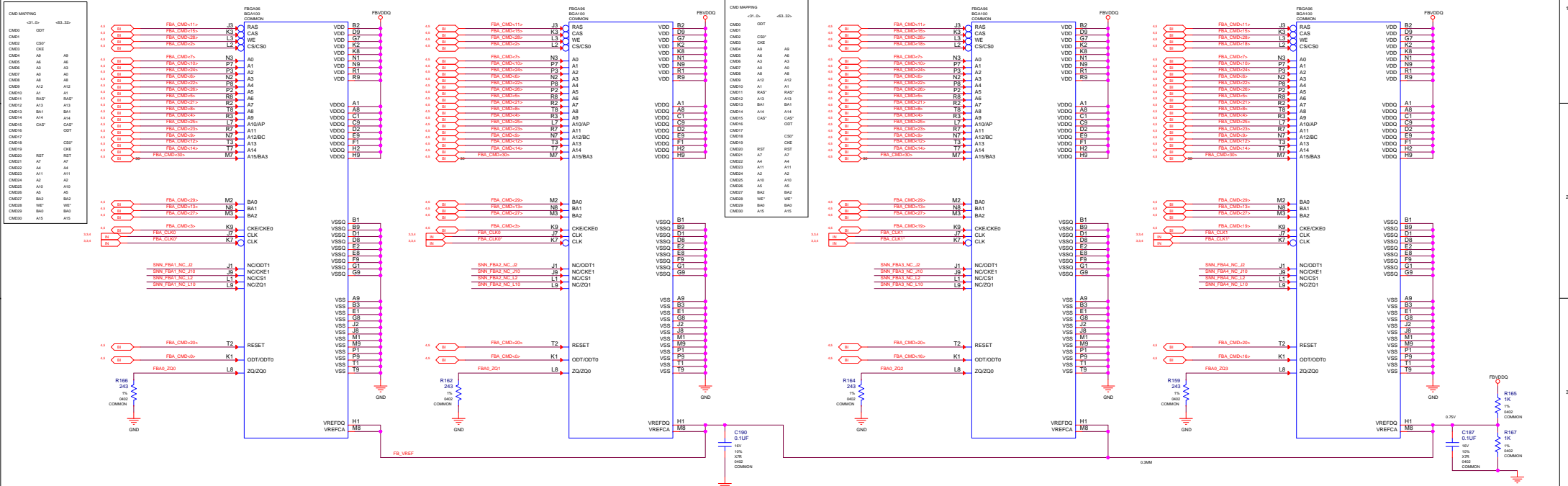


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DDR3 Memories



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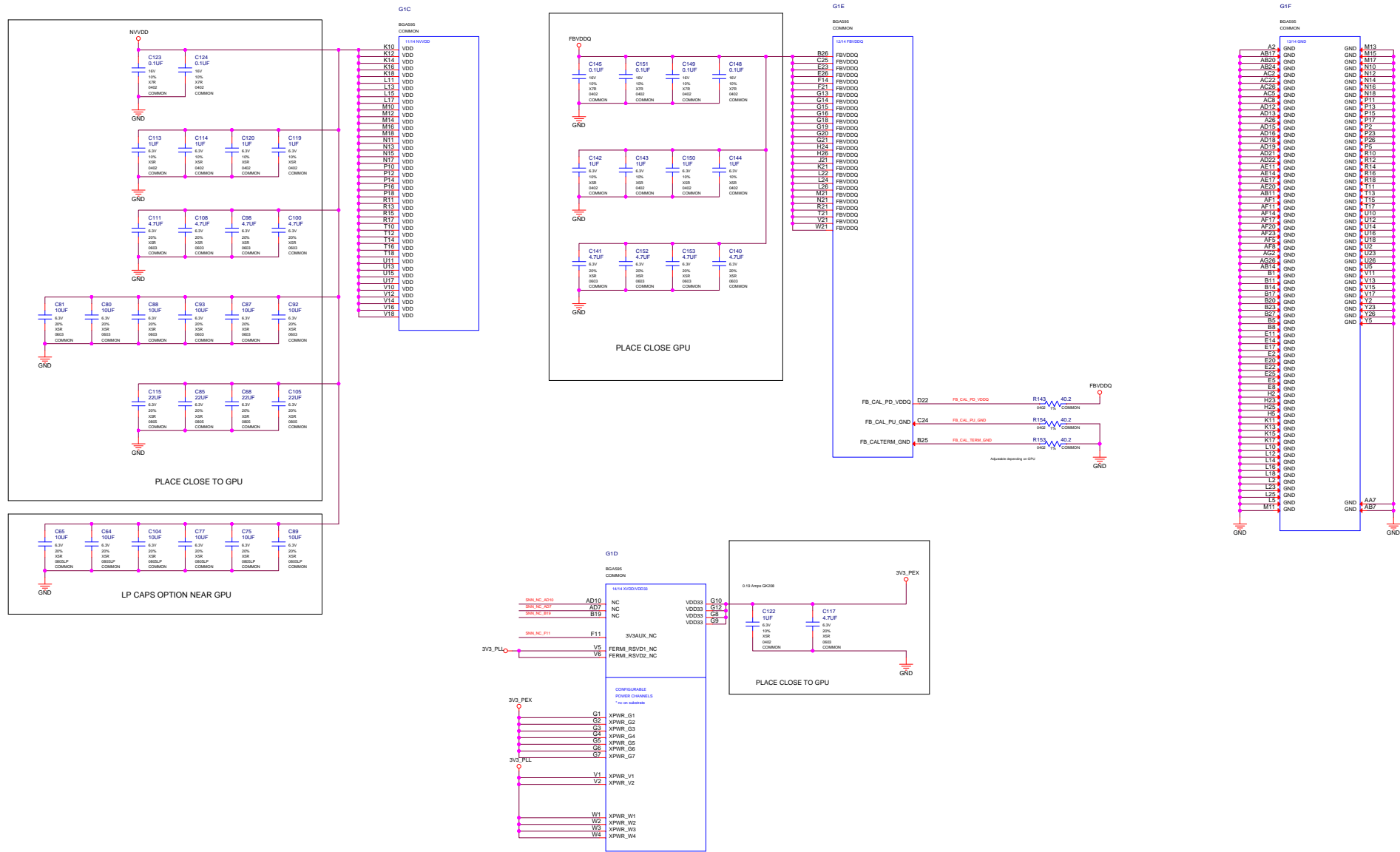
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 DDR3 Memories

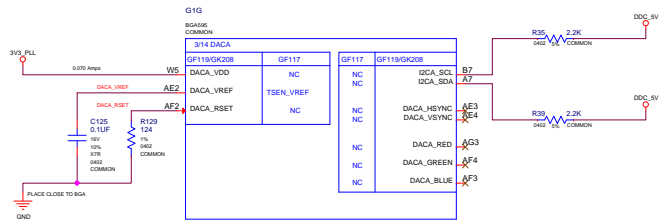
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DECOUPLING FOR CORE_POWER_TOP




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DACA VGA



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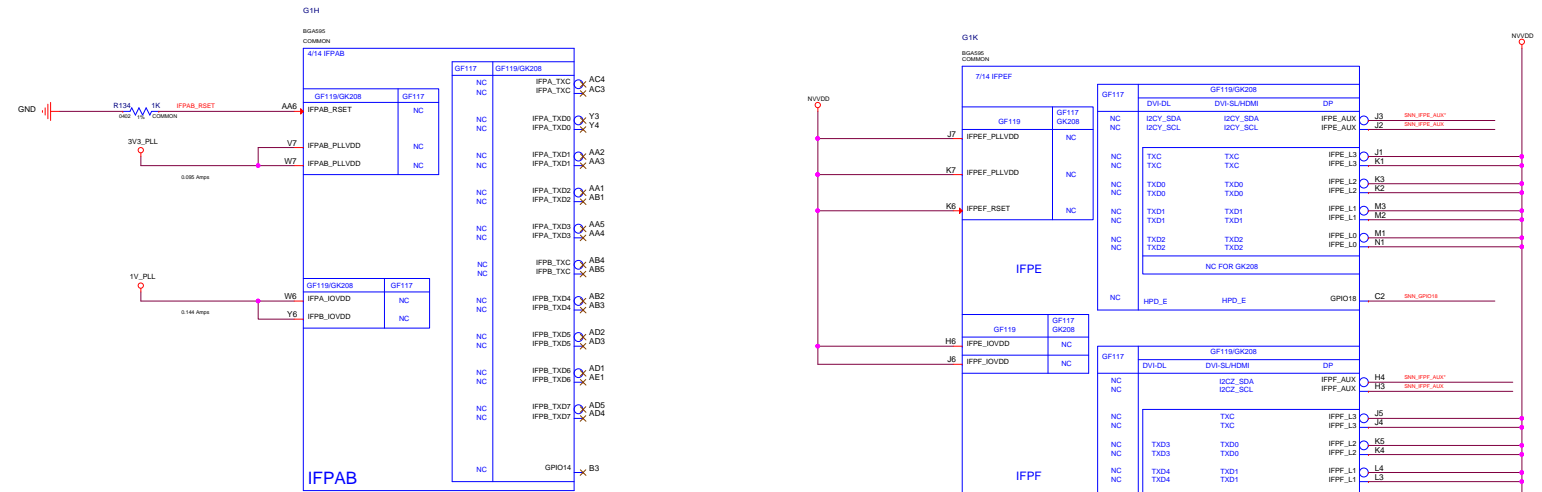
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IFPAB TMDs

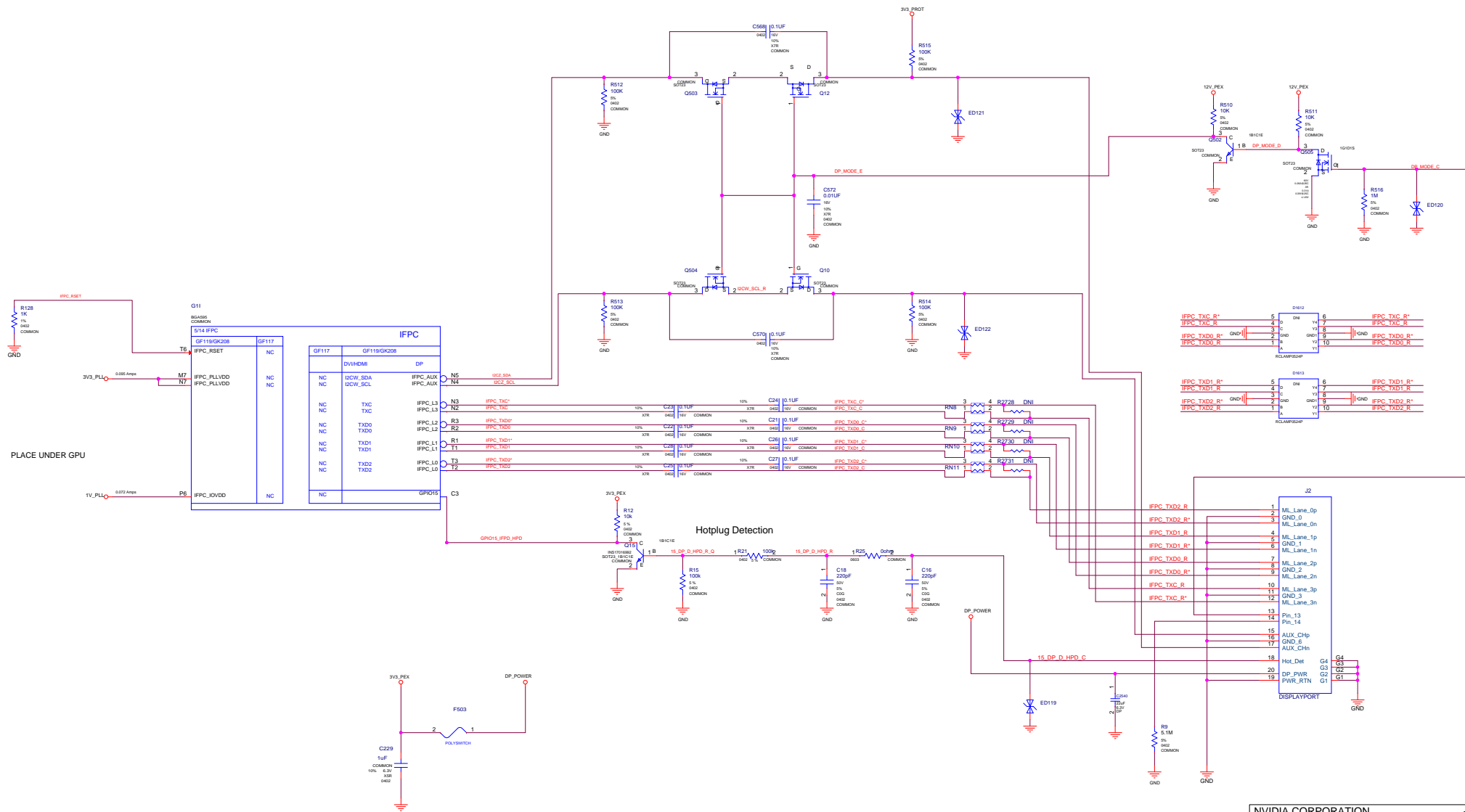


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IFPC HDMI




PLACE UNDER GPU

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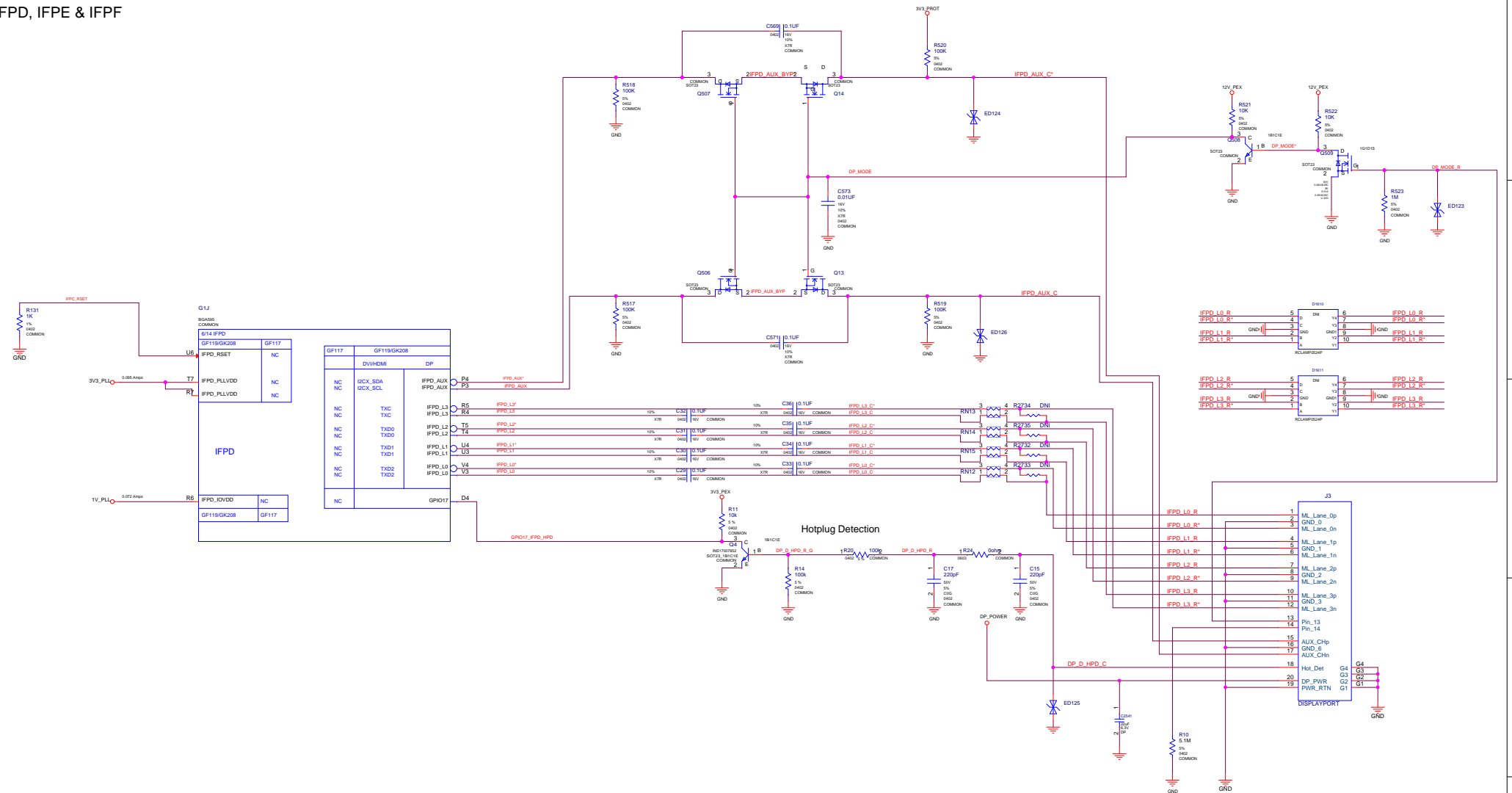
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UNUSED IFPD, IFPE & IFPF




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PAGE DETAIL	UNUSED IFPD, IFPE & IFPF

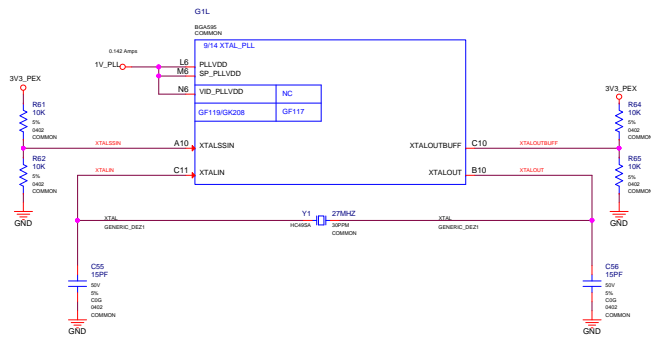
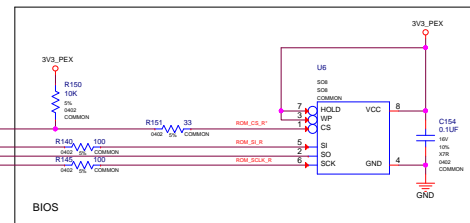
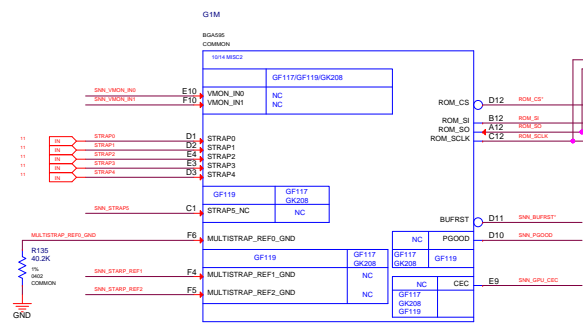
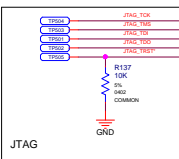
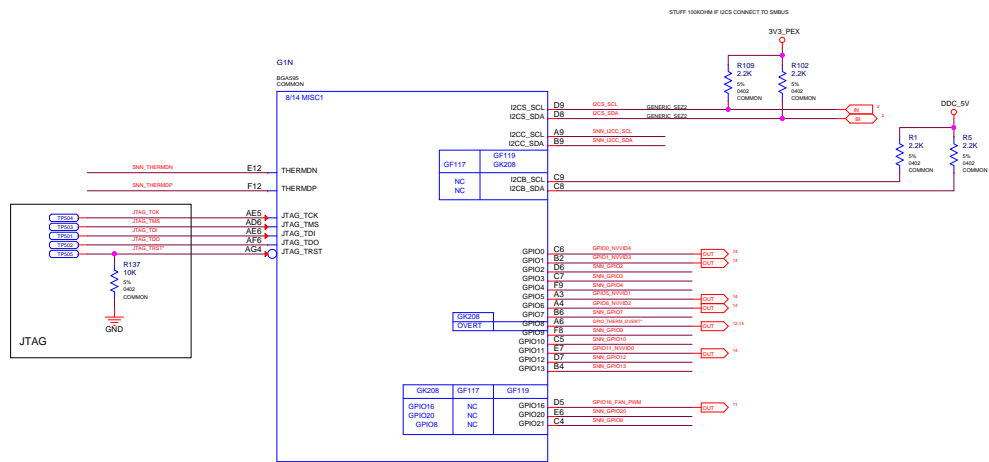
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MISC INTERFACES



SMART FAN STRAP		XTAL_OUTBUFF	
XTAL_SEN	XTAL_OUTBUFF	0	0
0	1	0	100% HIGH
1	0	1	33.3% HIGH
1	1	0	50.0% HIGH
1	1	1	67.0% HIGH

Inverted PWM!

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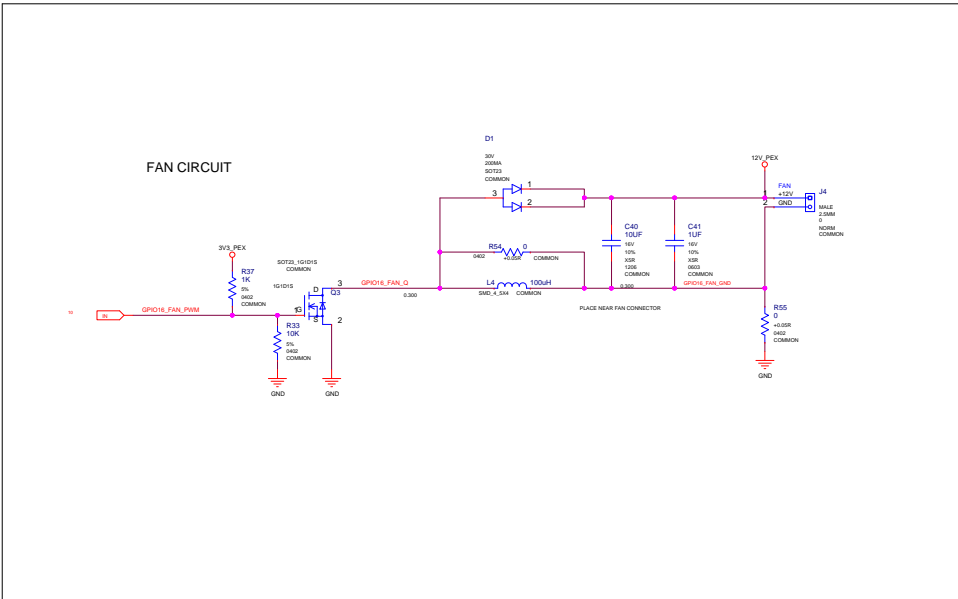
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Multilevel Straps			
0000	5.1K to GND	1000	5.1K to VCC
0001	10K to GND	1001	10K to VCC
0010	15K to GND	1010	15K to VCC
0011	20K to GND	1011	20K to VCC
0100	24.9K to GND	1100	24.9K to VCC
0101	30.1K to GND	1101	30.1K to VCC
0110	34.9K to GND	1110	34.9K to VCC
0111	40.1K to GND	1111	40.1K to VCC

GK208 Straps

Bit Signal	Values			
00: RAMCFG0	0000	Reserved		
01: RAMCFG0	0001	256Mx16 DDR3 X16 6480 Micron		
02: RAMCFG0	0010	256Mx16 DDR3 X16 6480 Hynix		
03: RAMCFG0	0011	256Mx16 DDR3 X16 6480 Samsung		
04: RAMCFG0	0101	128Mx16 DDR3 X16 6480 Micron		
05: RAMCFG0	0110	128Mx16 DDR3 X16 6480 Hynix		
06: RAMCFG0	0111	128Mx16 DDR3 X16 6480 Samsung		
07: FR0	00	128MB		
08: FR0	01	256MB		
09: SMB_ALT_ADDR	0	DISABLED	1	ENABLED
10: VGA_DEVICE	0	DISABLED	1	ENABLED
11: FDI_DEVICE_EXT	0x0	0	0x0	TRD
12: SUB_VENDOR	0	NO_BIOS	1	BIOS
13: FDI_DEVICE_BITS	0x0	0	0x0	TRD
14: FEK_FLT_EN_TERM10	0	DISABLED	1	ENABLED
15: USER0	0000	BIT		
16: USER0				
17: USER0				
18: SGIO_PACCFG0_LUT_ADDR0	0000	DKRTP_DEFAULT	1000	DKRTP_NTRES
19: SGIO_PACCFG0_LUT_ADDR0	0001	MOBILE_DEFAULT	1001	MOBILE_NTRES_LAMP
20: SGIO_PACCFG0_LUT_ADDR0	0010	MOBILE_NTRES_LLAMP	1010	MOBILE_NTRES_LLAMP
21: SGIO_PACCFG0_LUT_ADDR0	0011	MOBILE_NTRES_LAMP	1011	MOBILE_NTRES_LAMP
22: SGIO_PACCFG0_LUT_ADDR0	0100	MOBILE_NTRES_HAMP	1100	MOBILE_NTRES_HAMP
23: SGIO_PACCFG0_LUT_ADDR0	0101	MOBILE_NTRES_HAMP	1101	MOBILE_NTRES_HAMP
24: SGIO_PACCFG0_LUT_ADDR0	0110	MOBILE_NTRES_H99AMP	1110	MOBILE_NTRES_H99AMP
25: SGIO_PACCFG0_LUT_ADDR0	0111	MOBILE_NTRES_H99AMP	1111	MOBILE_NTRES_H99AMP
26: FDI_DEVICE0	0x0	0x0		
27: FDI_DEVICE0				
28: FDI_DEVICE0				
29: FDI_DEVICE0				
30: SOR0_EXPOSED	0	DISABLED	1	ENABLED
31: SOR0_EXPOSED	0	DISABLED	1	ENABLED
32: SOR1_EXPOSED	0	DISABLED	1	ENABLED
33: SOR1_EXPOSED	0	DISABLED	1	ENABLED
34: SOR2_EXPOSED	0	DISABLED	1	ENABLED
35: SOR2_EXPOSED	0	DISABLED	1	ENABLED
36: FDI_MAX_SPEED	0	GEN1	1	GEN3
37: FDI_MAX_SPEED	0	GEN1	1	GEN3
38: FDI_FULL_VDD_PVS	0	USER0	1	USER0

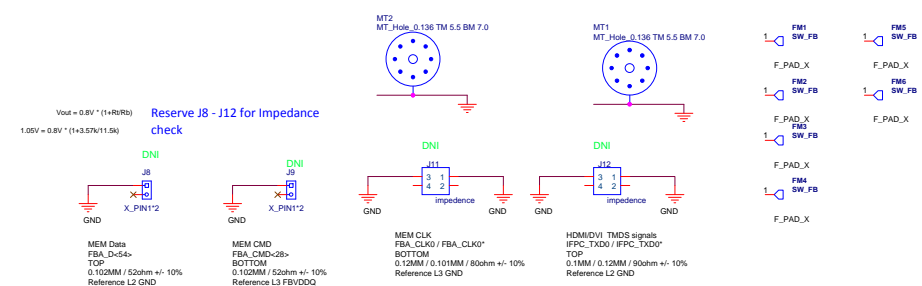
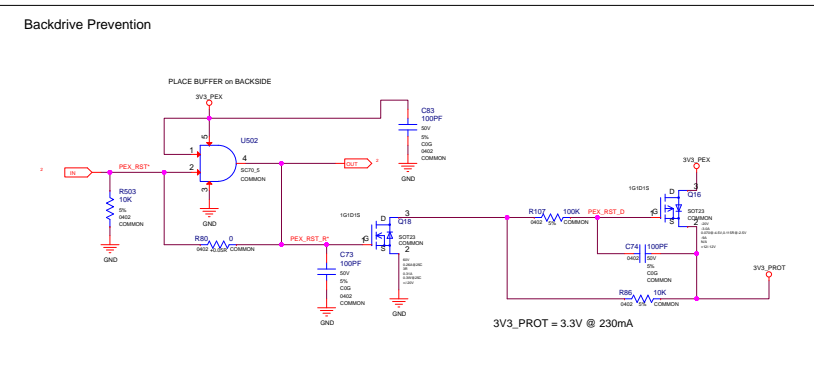
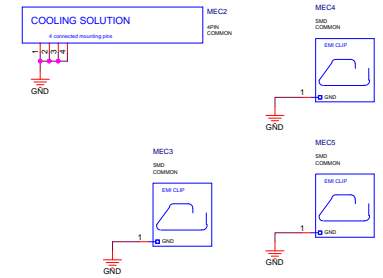
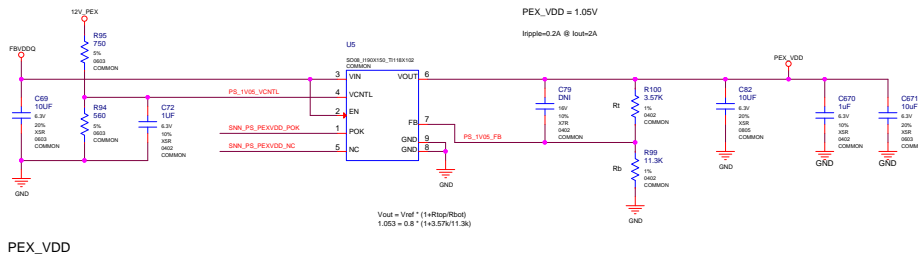
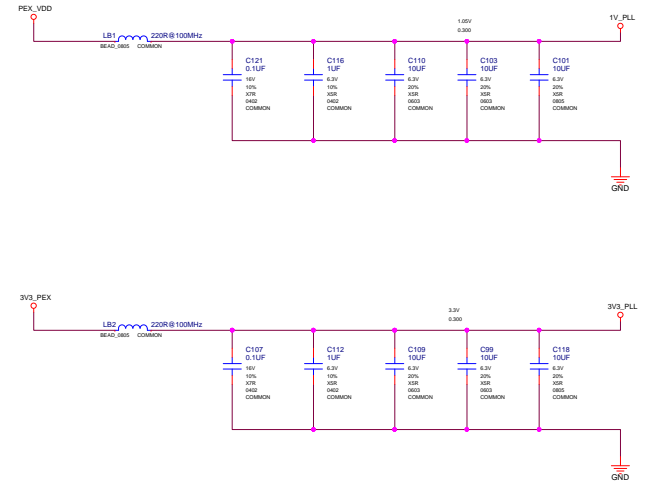
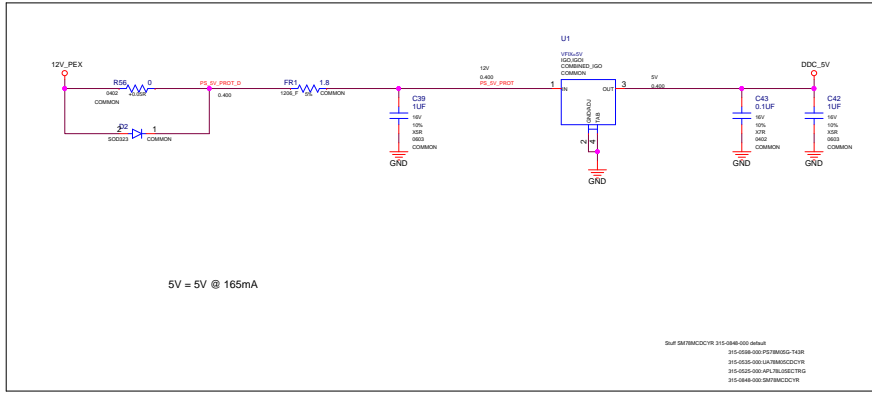


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POWER SUPPLY I: PEXVDD, 5V

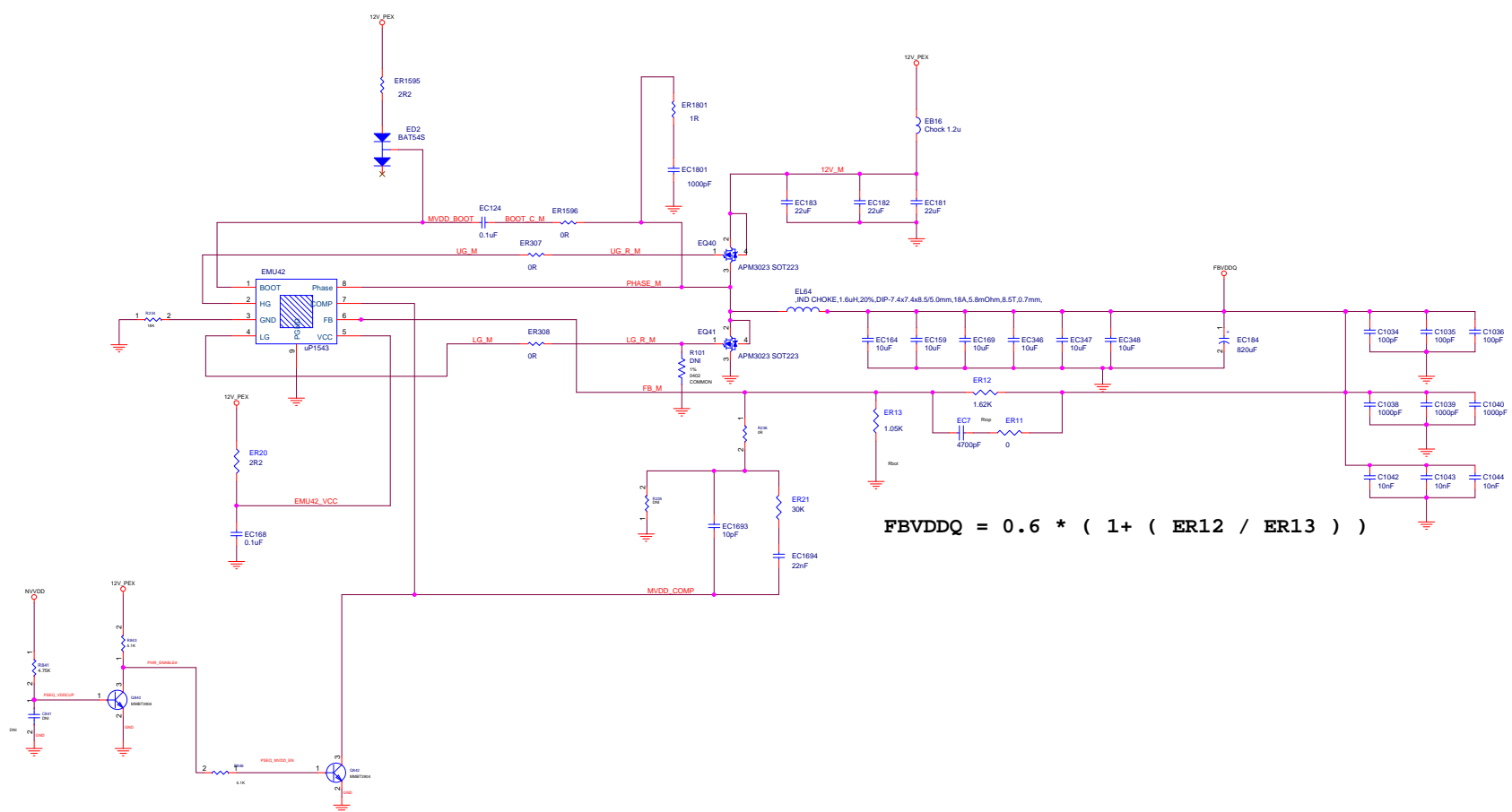


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POWER SUPPLY II: FBVDDQ



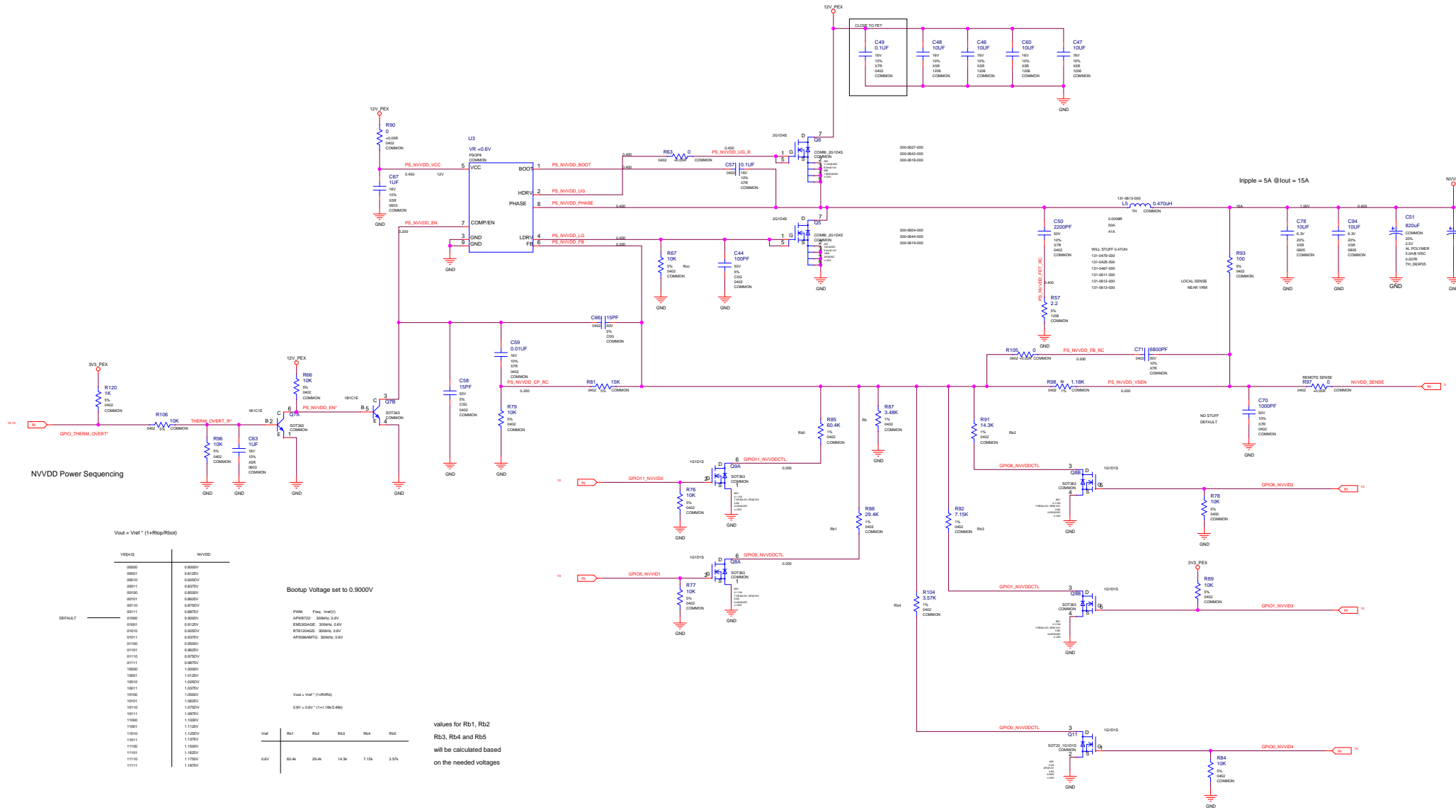
$$FBVDDQ = 0.6 * (1 + (ER12 / ER13))$$

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POWER SUPPLY III: NVDD



Ripple = 5A @Iout = 15A

NVDD Power Sequencing

$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$

VDDEN	NVDD
0000	0.8000V
0001	0.8125V
0010	0.8250V
0011	0.8375V
0100	0.8500V
0101	0.8625V
0110	0.8750V
0111	0.8875V
1000	0.9000V
1001	0.9125V
1010	0.9250V
1011	0.9375V
1100	0.9500V
1101	0.9625V
1110	0.9750V
1111	0.9875V
1000	1.0000V
1001	1.0125V
1010	1.0250V
1011	1.0375V
1100	1.0500V
1101	1.0625V
1110	1.0750V
1111	1.0875V
1000	1.1000V
1001	1.1125V
1010	1.1250V
1011	1.1375V
1100	1.1500V
1101	1.1625V
1110	1.1750V
1111	1.1875V

Bootup Voltage set to 0.9000V

FROM File: NVDD1
 FWREV22: 300W_0.6V
 EMBEDDAGE: 300W_0.6V
 STRUCRAGE: 300W_0.6V
 APFSGMAMTG: 300W_0.6V


$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$

$0.8V * 0.6V * (1 + 1.58K/4.8K)$

values for Rb1, Rb2, Rb3, Rb4 and Rb5 will be calculated based on the needed voltages

Vref	Rb1	Rb2	Rb3	Rb4	Rb5
0.6V	60.4K	29.4K	14.3K	7.15K	3.57K

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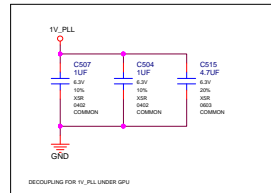
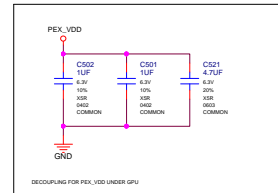
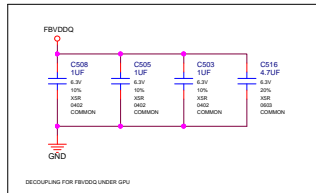
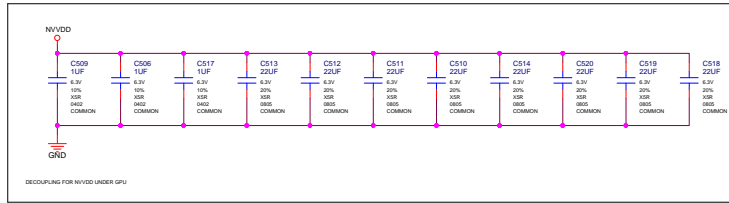


NV_P/N	600-12132-BASE-QS1
PCB REV	P2132-A01
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 PAGE DETAIL: POWER SUPPLY III: NVDD

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DECOUPLING FOR CORE POWER_BOTTOM



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